S75WS-N Based MCPs

Stacked Multi-Chip Product (MCP)
256 Megabit (16M x 16-bit) CMOS 1.8 Volt-only Simultaneous Read/Write, Burst-mode Flash Memory with 128 Mb (8M x 16-Bit) RAM Type 4 and 512 Mb (32M x 16-bit) Data Flash or 1 Gb ORNAND Flash

Data Sheet

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Publication Number S75WS-N_02 **Revision** A **Amendment** 2 **Issue Date** October 6, 2005

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256 Megabit (16M x 16-bit) CMOS 1.8 Volt-only Simultaneous Read/Write, Burst-mode Flash Memory with 128 Mb (8M x 16-Bit) RAM Type 4 and 512 Mb (32M x 16-bit) Data Flash or 1Gb ORNAND Flash

Data Sheet

PRELIMINARY

General Description

The S75WS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more S29WS-N code Flash
- RAM Type 4
- One or more S29WS-N data Flash, or one or more S30MS-P ORNAND Flash

The products covered by this document are listed in the table below:

Device	Code Flash Density	RAM Density		NOR Data Flash Density	ORNAND Data Flash Density
	256 Mb	128 Mb	256 Mb	512 Mb	1024 Mb
S75WS256NDF	■	■		■	
S75WS256NEG	■		■		■

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **High Performance**
  - — 54 MHz, 66 Mhz, 80 MHz
- **Packages**
  - — 9 x 12 mm 84 ball FBGA
  - — 11 x 13 mm 115 ball FBGA
- Operating Temperature
  - — Wireless, –25°C to +85°C

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1 Product Selector Guide

Device	Model Numbers	MCP Configuration			Code Density (Mb)	RAM Density (Mb)	Data Flash Density (Mb)	Flash Speed (MHz)	pSRAM Speed (MHz)	DYB Power-Up State (See Note)	pSRAM (RAM Type 4) Supplier	Package 84 ball FBGA (mm)
		Code Flash	RAM (Mb)	Data Storage Flash								
S75WS256NDF	LK	WS256N	128	2xWS256N	256	128	512	54	54	0	4	9x12
	NK									1		
	LJ							66	66	0		
	NJ									1		
	LH							80	80	0		
	NH									1		

Note: 0 (Protected), 1 (Unprotected [Default State])

1.1 NOR Flash + pSRAM + ORNAND Flash MCPs

Device	Model Numbers	NOR Flash Density	ORNAND Flash Density	pSRAM Density	MCP Speed	Supplier	ORNAND Bus Width	Package
S75WS256NEG	UK	512 Mb	1024 Mb	256 Mb	54 MHz	1.8 V pSRAM Type 4	x16	11 x 13 x 1.4 mm
	UJ				66 MHz			
	UH				80 MHz			
	SK				54 MHz		x8	
	SJ				66 MHz			
	SH				80 MHz			

2 Ordering Information

The ordering part number is formed by a valid combination of the following:

S75WS 256 N D F BA W L K 0

Packing Type
0 = Tray
2 = 7” Tape and Reel
3 = 13” Tape and Reel

RAM Supplier; Speed Combination
K = RAM Type 4, 54 MHz
J = RAM Type 4, 66 MHz
H = RAM Type 4, 80 MHz

Package Dimensions and Ball Count; DYB Power Up; Flash Device Family (Data Storage)
L = 1.4 mm, 9 x 12, 84 ball; 0, WS as Data Flash
N = 1.4 mm, 9 x 12, 84 ball; 1, WS as Data Flash
U = 1.4mm, 11x13, 115-ball, x16 ORNAND Data Flash
S = 1.4mm, 11x13, 115-ball, x8 ORNAND Data Flash

Temperature Range
W = Wireless (–25°C to +85°C)

Package Type And Material
BA = Very Thin Fine-Pitch Ball Grid Array (BGA), Lead (Pb)-free Compliant Package
BF = Very Thin Fine-Pitch Ball Grid Array (BGA), Lead (Pb)-free Package

Data Flash Density
F = 512 Mb
G = 1024 Mb

RAM Density
D = 128 Mb
E = 256 Mb

Process Technology
N = 110 nm, Mirror Bit Technology

Code Flash Density
256 = 256 Mb

Device Family
S75WS = Multi-chip Product (MCP)
1.8-volt Burst Mode Flash Memory, RAM, and data flash

Table 2.1 MCP Configurations and Valid Combinations

Valid Combination						
S75WS256N	D	F	BA, BF	W	L, N	K, H

Table 2.2 ORNAND Configurations and Valid Combinations

Valid Combination						
S75WS256N	E	G	BA, BF	W	U, S	K, J, H

Package Marking Note:

The BGA package marking omits the leading S75 and packing type designator from the ordering part number.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

3 Input/Output Descriptions

Table 3.1 identifies the input and output package connections provided on the device.

Table 3.1 NOR Flash and RAM Input/Output Descriptions

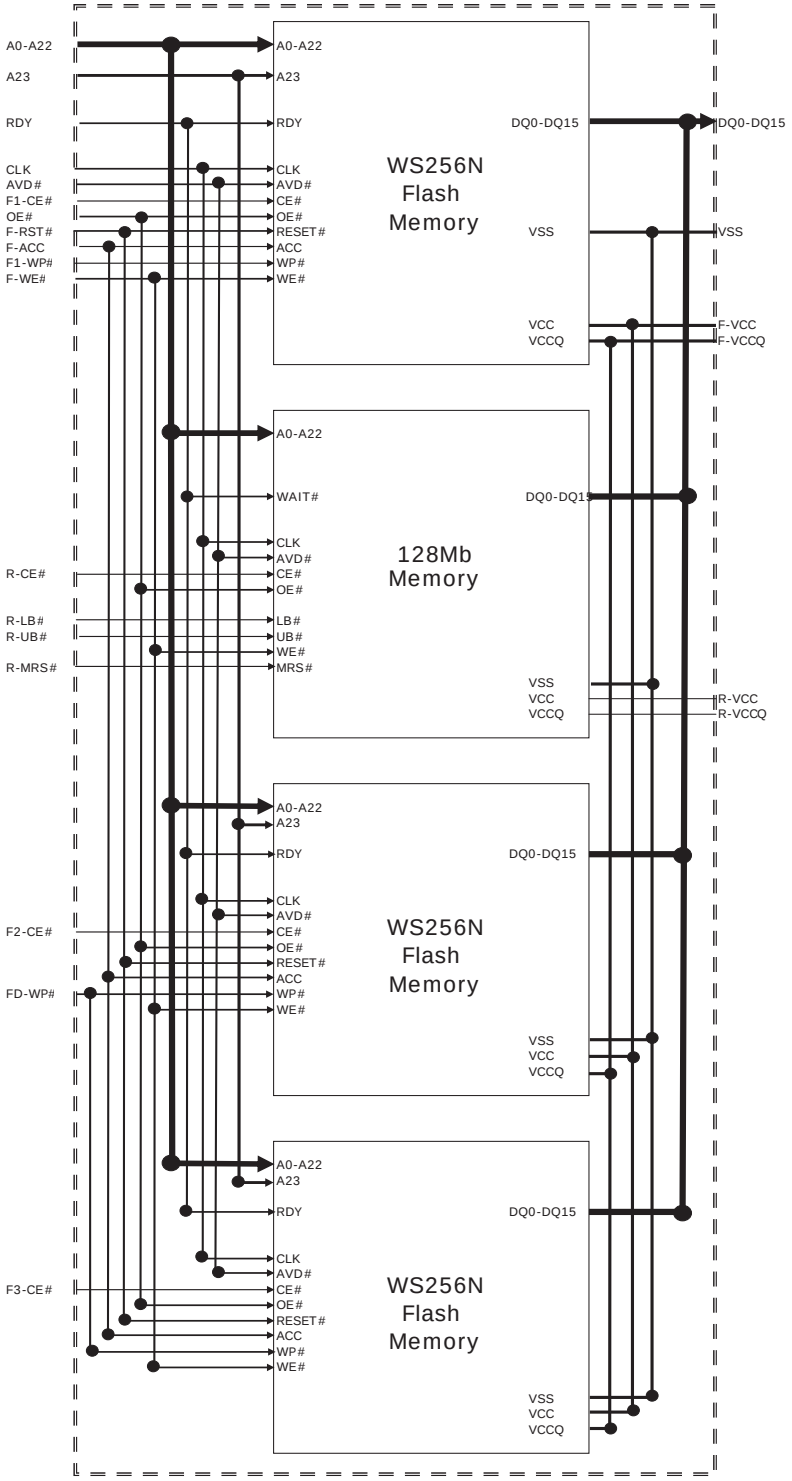
Symbol	Description	
A_{max} – A0	Address Inputs	(Common)
DQ15 - DQ0	Data Inputs/Outputs	
OE#	Output Enable input	
WE#	Write Enable input	
V_{SS}	Ground	
NC	No Connect; not connected internally.	
RDY	Ready output. Indicates the status of the Burst read.	(Flash)
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode.	(Common)
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs.	(Flash)
F-RST#	Hardware reset input.	
F-WP#	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.	
F-ACC	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	
R-CE#	Chip-enable input for pSRAM	
F1-CE#	Chip-enable input for Code Flash.	Asynchronous relative to CLK for Burst Mode.
F2-CE#	Chip-enable input for Data Flash 1.	
F2-CE#	Chip-enable input for Data Flash 2.	
R-MRS#	Control Register Enable.	(pSRAM – RAM Type 4 only)
F-V_{CC}	Flash 1.8 Volt-only single power supply.	
R-V_{CC}	pSRAM Power Supply.	
R-UB#	Upper Byte Control.	(pSRAM)
R-LB#	Lower Byte Control .	

Table 3.2 identifies the ORNAND input and output connections provided on the device.

Table 3.2 ORNAND Flash Input/Output Descriptions

Symbol	Description
N-PRE	ORNAND Power-On Read Enable. Tie to V_{SS} on customer board if not used.
N-ALE	ORNAND Address Latch Enable
N-CLE	ORNAND Command Latch Enable
N-CE#	ORNAND Chip-enable
N-WP#	ORNAND Write-protect
N-WE#	ORNAND Write-enable
N-RE#	ORNAND Read-enable
N-RY/BY#	ORNAND Ready-Busy—this is shared with NOR RDY
N-I/O0-N-I/O15	ORNAND I/O signals (I/O0-I/O7 for x8 bus width)
N-V_{CC}	ORNAND Power supply

4 MCP Block Diagram



Notes:

1. *MRS is only present in RAM Type 4.*
2. *CE#f1, CE#f2, and CE#f3 are the chip enable pins for the first, second and third Flash devices, respectively.*

Figure 4.1 MCP Block Diagram 1

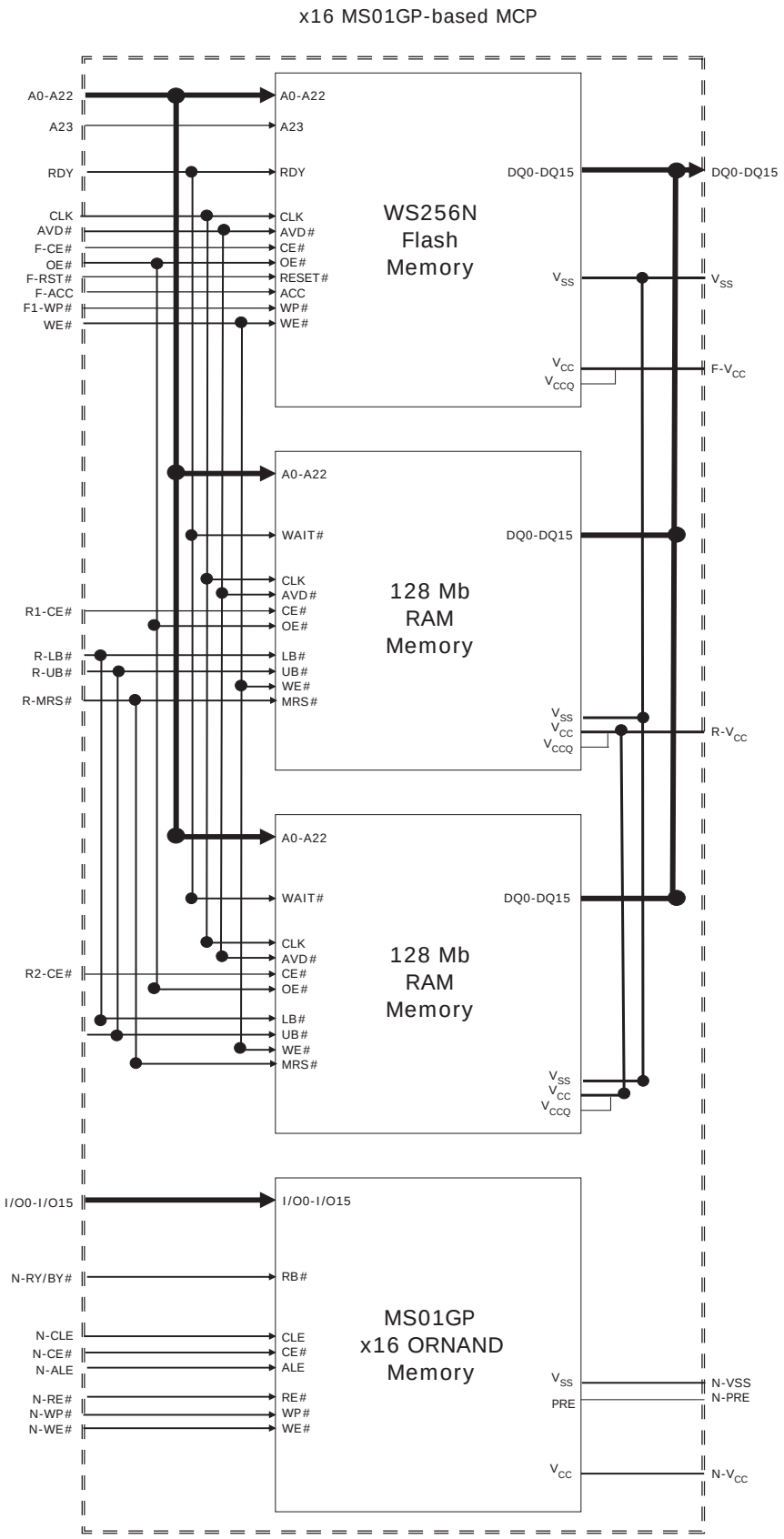


Figure 4.2 ORNAND Block Diagram

5 Connection Diagrams/Physical Dimensions

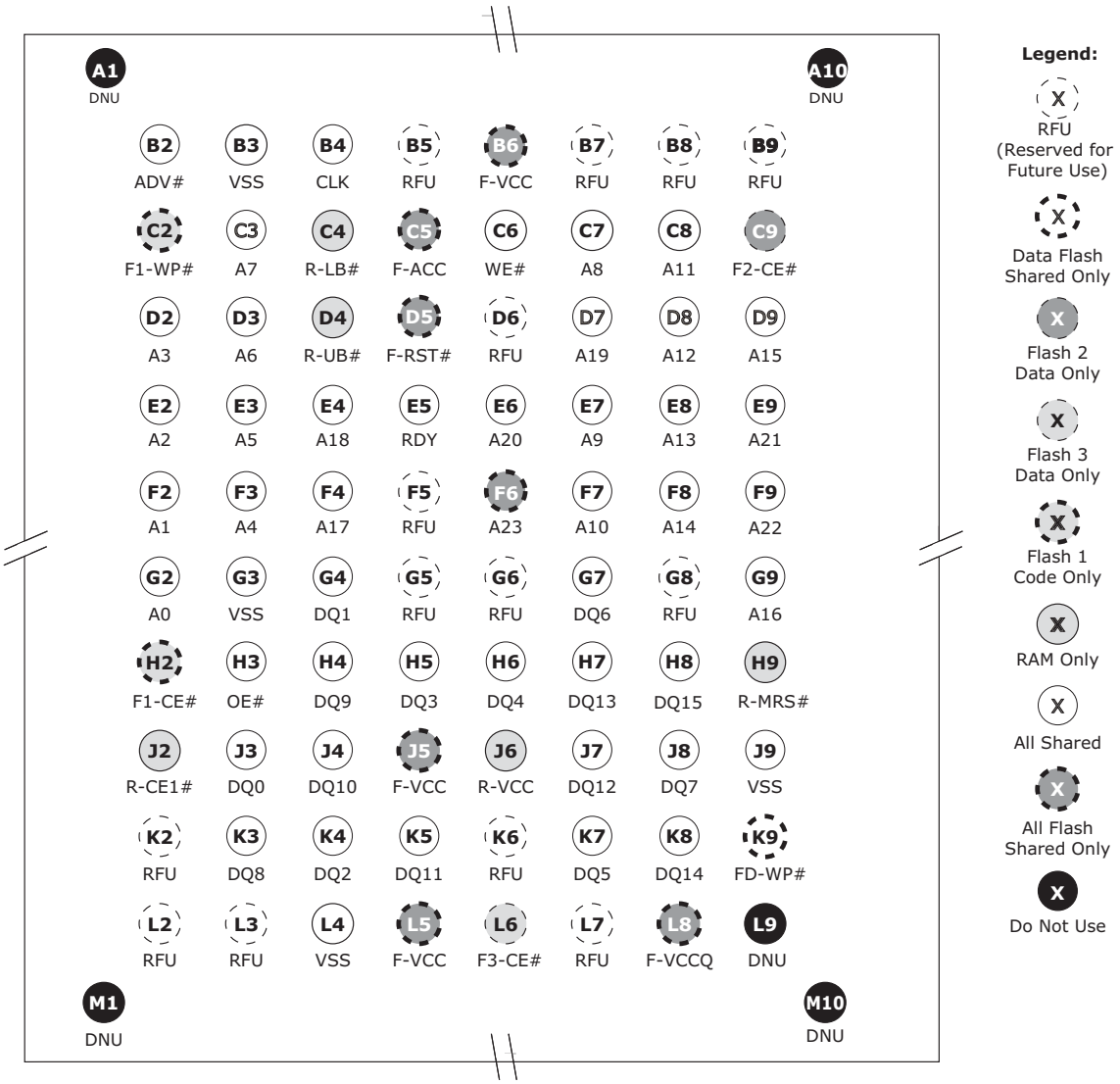
This section contains the I/O designations and package specifications for the S75WS.

5.1 Special Handling Instructions for FBGA Package

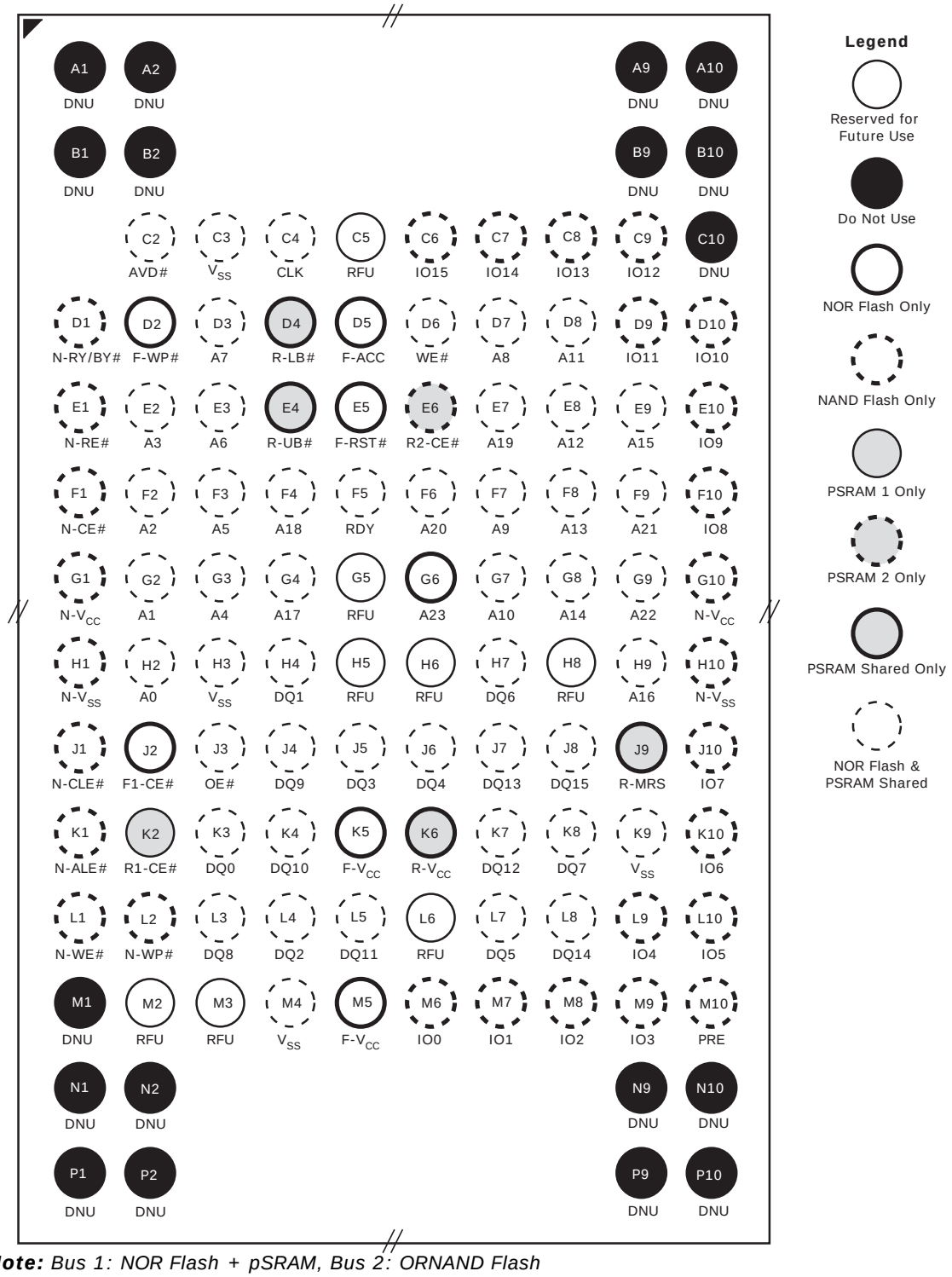
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.2 Connection Diagram – NOR Flash & 1.8 V RAM Type 4 Based Pinout, 9 x 12 mm

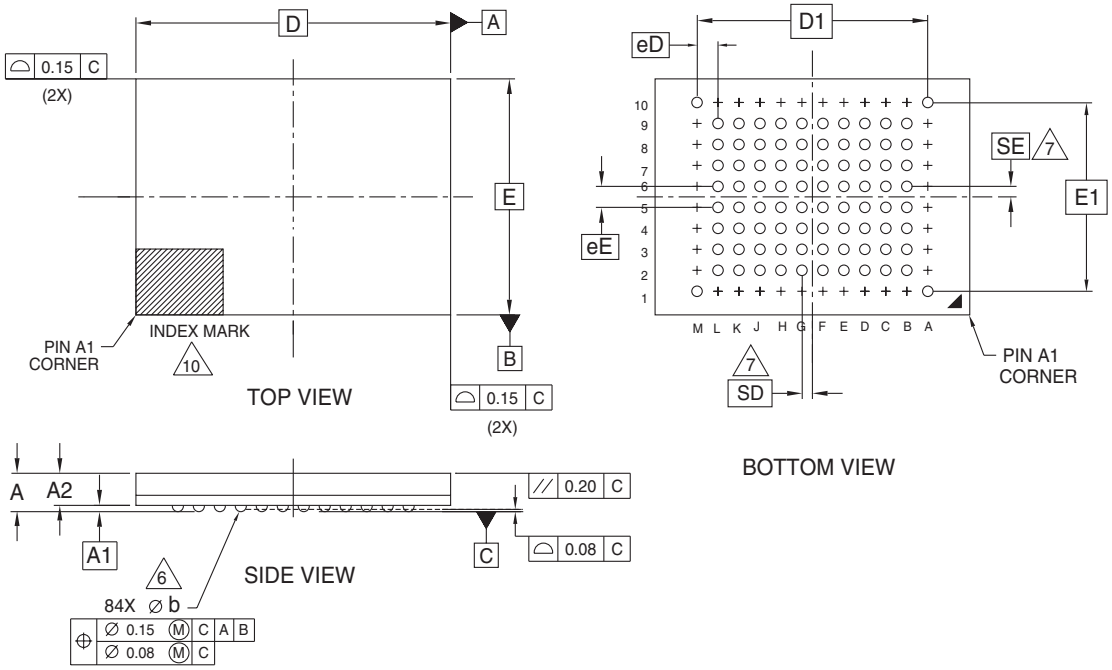


5.3 Connection Diagram – ORNAND-Based Pinout, 11 x 13 mm



Note: *Bus 1: NOR Flash + pSRAM, Bus 2: ORNAND Flash*

5.4 Physical Dimensions – FEA084 – Fine Pitch Ball Grid Array 9 x 12 mm



PACKAGE	FEA 084			NOTE
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.10	---	---	BALL HEIGHT
A2	1.11	---	1.26	BODY THICKNESS
D	12.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10 E1,E10,F1,F10,G1,G10 H1,H10,J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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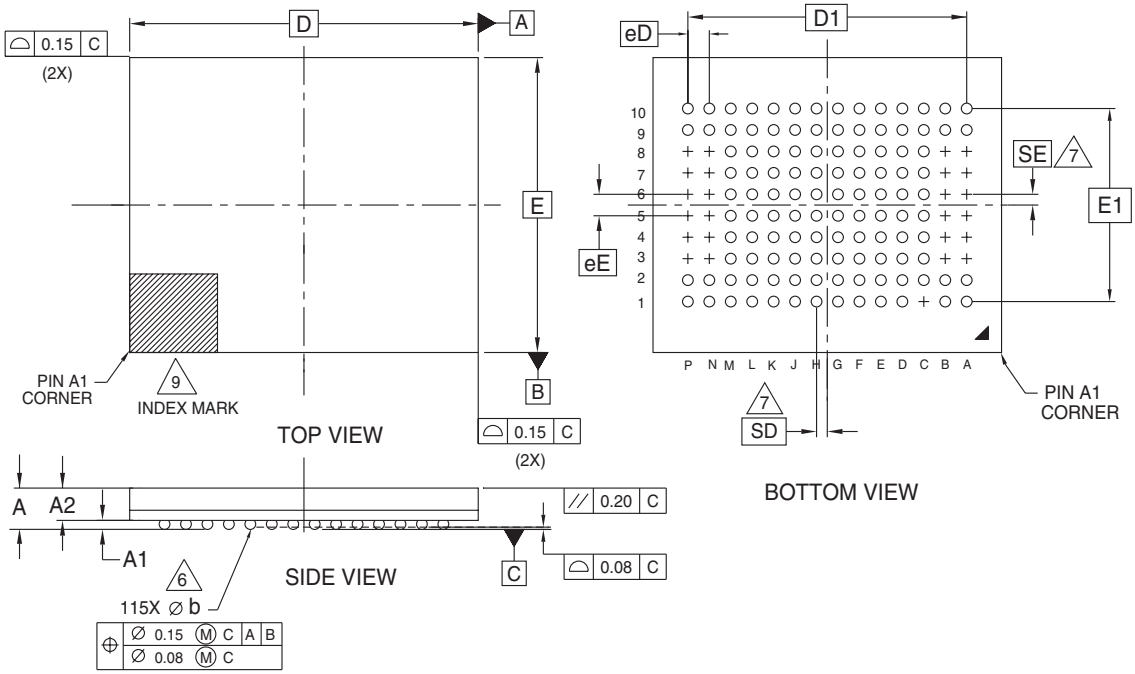
5.5 Physical Dimensions – FND115 – Fine Pitch Ball Grid Array 11 x 13 mm



PACKAGE	FND 115			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.98	---	1.15	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	10.40 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	115			BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A3-A8,B3-B8,C1,N3-N8,P3-P8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6 MCP Revisions

Revision A0 (February 17, 2005)

Initial Release

Revision A1 (September 8, 2005)

Global

Removed references to the S29RS-N data sheet

Product Selector Guide

Updated table and added 80 MHz options

Ordering Information

Updated table with new options

MCP Configurations and Valid Combinations

Updated table to reflect new options

Input/Output Descriptions

Updated table and changed some pin names

MCP Block Diagram

Updated the illustration

Connection Diagram

Updated the pinout diagram

Physical Dimensions

Added the FEA084 package diagram

Look-Ahead Connection Diagram

Removed from data sheet

S29WS-N Flash Module

Updated to the latest revision

Revision A2 (October 6, 2005)

Global

Added ORNAND Flash information

Product Selector Guide

Added ORNAND options

Ordering Information

Updated table with new options

MCP Block Diagram

Added the ORNAND illustration

Connection Diagram

Added the pinout diagram for the ORNAND device

Physical Dimensions

Added the FND115 package diagram

S29WS-N Flash Module

Removed from MCP. Available as a standalone document.

1.8 V Type 4 pSRAM Module

Removed from MCP. Available as a standalone document.

Colophon

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