EVB7122

27 to 930MHz Transceiver Evaluation Board Description

Features

- ❒ Single chip solution with only a few external components
- ❒ Stand-alone fixed-frequency user mode
- ❒ Programmable multi-channel user mode
- ❒ Low current consumption in active mode and very low standby current
- ❒ PLL-stabilized RF VCO (LO) with internal varactor diode
- ❒ Lock detect output in programmable user mode
- ❒ On-chip AFC for extended input frequency acceptance range
- ❒ FSK for digital data or FM for analog signal reception
- ❒ FSK/ASK mode selection
- ❒ RSSI output for signal strength indication and ASK reception
- ❒ ASK detection normal or with peak detector
- ❒ Switchable LNA gain for improved dynamic range
- ❒ Automatic PA turn-on after PLL lock
- ❒ ASK modulation achieved by PA on/off keying
- ❒ 3wire bus serial control interface
- ❒ EVB comes with a cable to connect to a PC's LPT port
- ❒ EVB programming software is available on Melexis web site

Ordering Information

Part No. (see paragraph 6)

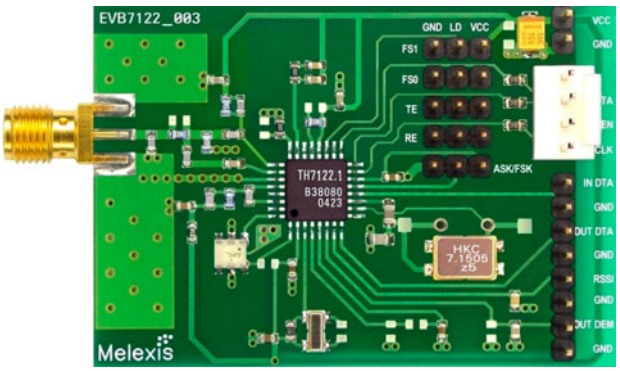
EVB7122-315-FSK-C
EVB7122-433-FSK-C
EVB7122-868-FSK-C
EVB7122-915-FSK-C

Note 1: EVB default population is FSK, ASK modifications according to section 4.2 and 4.3.
Note 2: EVB7122 is applicable for devices TH7122 and TH71221.

Application Examples

- ❒ General bi-directional half duplex digital data RF signaling or analog signal communication
- ❒ Tire Pressure Monitoring Systems (TPMS)
- ❒ Remote Keyless Entry (RKE)
- ❒ Low-power telemetry systems
- ❒ Alarm and security systems
- ❒ Wireless access control
- ❒ Garage door openers
- ❒ Networking solutions
- ❒ Active RFID tags
- ❒ Remote controls
- ❒ Home and building automation

Evaluation Board Example



General Description

The TH7122 is a single chip FSK/FM/ASK transceiver IC. It is designed to operate in low-power multi-channel programmable or single-channel stand-alone, half-duplex data transmission systems. It can be used for applications in automotive, industrial-scientific-medical (ISM), short range devices (SRD) or similar applications operating in the frequency range of 300 MHz to 930 MHz. In programmable user mode, the transceiver can operate down to 27 MHz by employing an external VCO varactor diode.

Document Content

1 Theory of Operation

1.1 General

The main building block of the transceiver is a programmable PLL frequency synthesizer that is based on an integer-N topology. The PLL is used for generating the carrier frequency during transmission and for generating the LO signal during reception. The carrier frequency can be FSK-modulated by pulling the crystal and ASK-modulated by on/off keying of the power amplifier. The receiver is based on the principle of a single conversion superhet. Therefore the VCO frequency has to be changed between transmit and receive mode. In receive mode, the preferred LO injection type is low-side injection.

The TH7122 transceiver IC consists of the following building blocks:

- Low-noise amplifier (LNA) for high-sensitivity RF signal reception with switchable gain
- Mixer (MIX) for RF-to-IF down-conversion
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase-coincidence demodulator with external ceramic discriminator (FSK Demodulator)
- Operational amplifier (OA1), connected to demodulator output
- Operational amplifier (OA2), for geral use
- Peak detector (PKDET) for ASK detection
- Control logic with 3wire bus serial control interface (SCI)
- Reference oscillator (RO) with external crystal
- Reference divider (R counter)
- Programmable divider (N/A counter)
- Phase-frequency detector (PFD)
- Charge pump (CP)
- Voltage controlled oscillator (VCO) with internal varactor
- Power amplifier (PA) with adjustable output power

1.2 Technical Data Overview

- ❒ Frequency range: 300 MHz to 930 MHz in programmable user mode
- ❒ Extended frequency range with external VCO varactor diode: 27 MHz to 930 MHz
- ❒ 315 MHz, 433 MHz, 868 MHz or 915 MHz fixed-frequency settings in stand-alone mode
- ❒ Power supply range: 2.2 V to 5.5 V
- ❒ Temperature range: -40 °C to +85 °C
- ❒ Standby current: 50 nA
- ❒ Operating current in receive: 6.5 mA (low gain)
- ❒ Operating current in transmit: 12 mA (at -2 dBm)
- ❒ Adjustable RF power range: -20 dBm to +10dBm
- ❒ Sensitivity: -105 dBm at FSK with 180 kHz IF filter BW
- ❒ Sensitivity: -107 dBm at ASK with 180 kHz IF filter BW
- ❒ Max. data rate with crystal pulling: 20 kbps NRZ
- ❒ Max. data rate with direct VCO modulation: 115 kbps NRZ
- ❒ Max. input level: -10 dBm at FSK and -20 dBm at ASK
- ❒ Input frequency acceptance: ± 10 to ± 150 kHz (depending on FSK deviation)
- ❒ FM/FSK deviation range: ±2.5 to ±80 kHz
- ❒ Analog modulation frequency: max. 10 kHz
- ❒ Crystal reference frequency: 3 MHz to 12 MHz
- ❒ External reference frequency: 1 MHz to 16 MHz

1.3 Note on ASK Operation

Optimum ASK performance can be achieved by using an 8-MHz crystal for operation at 315 MHz, 434 MHz and 915 MHz. For details please refer to the software settings shown in sections 4.2 and 4.3. FSK operation is the preferred choice for applications in the European 868MHz band.

For more detailed information, please refer to the latest TH7122 data sheet revision

1.4 Block Diagram

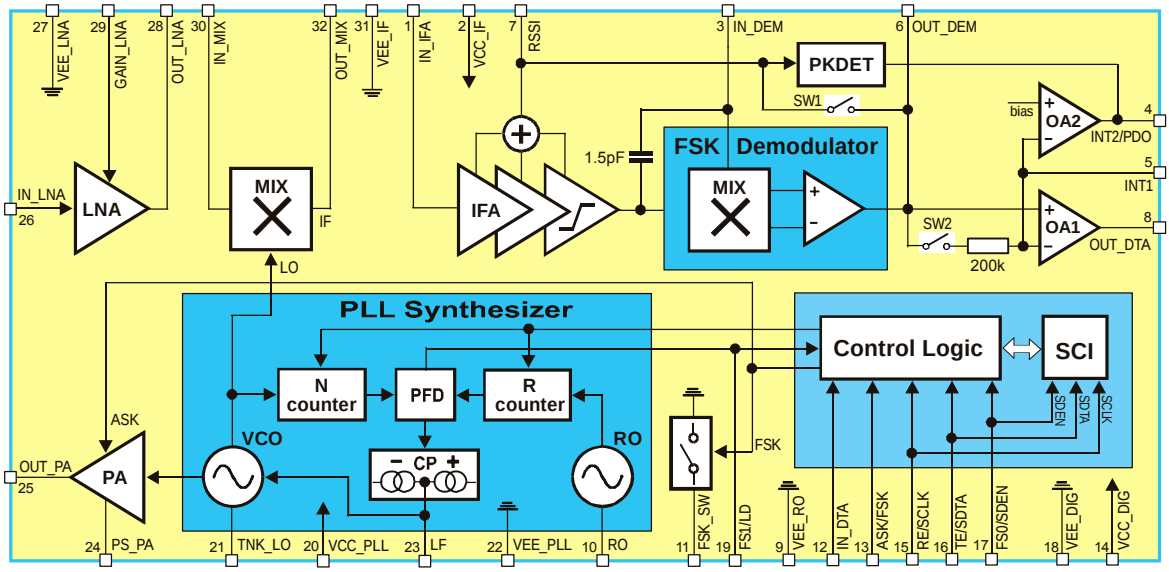


Fig. 1: TH7122 block diagram

1.5 User Mode Features

The transceiver can operate in two different user modes. It can be used either as a 3wire-bus-controlled programmable or as a stand-alone fixed-frequency device. After power up, the transceiver is set to Stand-alone User Mode (SUM). In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} in order to set the desired frequency of operation. There are 4 pre-defined frequency settings: 315MHz, 433.92MHz, 868.3MHz and 915MHz. The logic level at pin FS0/SDEN must not be changed after power up in order to remain in fixed-frequency mode.

After the first logic level change at pin FS0/SDEN, the transceiver enters into Programmable User Mode (PUM). In this mode, the user can set any PLL frequency or mode of operation by the SCI. In SUM pins FS0/SDEN and FS1/LD are used to set the desired frequency, while in PUM pin FS0/SDEN is part of the 3-wire serial control interface (SCI) and pin FS1/LD is the look detector output signal of the PLL synthesizer.

A mode control logic allows several operating modes. In addition to standby, transmit and receive mode, two idle modes can be selected to run either the reference oscillator only or the whole PLL synthesizer. The PLL settings for the PLL idle mode are taken over from the last operating mode which can be either receive or transmit mode.

The different operating modes can be set in SUM and PUM as well. In SUM the user can program the transceiver via control pins RE/SCLK and TE/SDTA. In PUM the register bits OPMODE are used to select the modes of operation while pins RE/SCLK and TE/SDTA are part of the SCI.

2 Description of User Modes

2.1 Stand-alone User Mode Operation

After power up the transceiver is set to stand-alone user mode. In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} to set the desired frequency of operation. The logic level at pin FS0/SDEN must not be changed after power up in order to remain in stand-alone user mode. The default settings of the control word bits in stand-alone user mode are described in the frequency selection table. Detailed information about the default settings can be found in the tables of section 5.

2.1.1 Frequency Selection

Channel frequency	433.92 MHz	868.3 MHz	315 MHz	915 MHz
FS0/SDEN	**1**	**0**	**1**	**0**
FS1/LD	**0**	**0**	**1**	**1**
Reference oscillator frequency	**7.1505 MHz**			
R counter ratio in RX mode (RR)	**32**	**16**	**18**	**32**
PFD frequency in RX mode	**223.45 kHz**	**446.91 kHz**	**397.25 kHz**	**223.45 kHz**
N counter ratio in RX mode (NR)	**1894**	**1919**	**766**	**4047**
VCO frequency in RX mode	**423.22 MHz**	**857.60 MHz**	**304.30 MHz**	**904.30 MHz**
RX frequency	**433.92 MHz**	**868.30 MHz**	**315.00 MHz**	**915.00 MHz**
R counter ratio in TX mode (RT)	**32**	**16**	**18**	**32**
PFD frequency in TX mode	**223.45 kHz**	**446.91 kHz**	**397.25 kHz**	**223.45 kHz**
N counter ratio in TX mode (NT)	**1942**	**1943**	**793**	**4095**
VCO frequency in TX mode	**433.92 MHz**	**868.30 MHz**	**315.00 MHz**	**915.00 MHz**
TX frequency	**433.92 MHz**	**868.30 MHz**	**315.00 MHz**	**915.00 MHz**
IF in RX mode	**10.7 MHz**	**10.7 MHz**	**10.7 MHz**	**10.7 MHz**

In stand-alone user mode, the transceiver can be set to Standby, Receive, Transmit or Idle mode (only PLL synthesizer active) via control pins RE/SCLK and TE/SDTA. The modulation scheme and the LNA gain are set by pins ASK/FSK and GAIN_LNA, respectively.

2.1.2 Operation Mode

Operation mode	Standby	Receive	Transmit	Idle
RE/SCLK	**0**	**1**	**0**	**1**
TE/SDTA	**0**	**0**	**1**	**1**

Note: Pins with internal pull-down

2.1.3 Modulation Type

Modulation type	ASK	FSK
ASK / FSK	**0**	**1**

2.1.4 LNA Gain Mode

LNA gain	high	low
GAIN_LNA	**0**	**1**

2.2 Programmable User Mode Operation

The transceiver can also be used in programmable user mode. After power-up the first logic change at pin FS0/SDEN enters into this mode. Now full programmability can be achieved via the Serial Control Interface (SCI).

2.2.1 Serial Control Interface Description

A 3-wire (SCLK, SDTA, SDEN) Serial Control Interface (SCI) is used to program the transceiver in programmable user mode. At each rising edge of the SCLK signal, the logic value on the SDTA pin is written into a 24-bit shift register. The data stored in the shift register are loaded into one of the 4 appropriate latches on the rising edge of SDEN. The control words are 24 bits lengths: 2 address bits and 22 data bits. The first two bits (bit 23 and 22) are latch address bits. As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. The first incoming bit is the most significant bit (MSB). To program the transceiver in multi-channel application, four 24-bit words may be sent: A-word, B-word, C-word and D-word. If individual bits within a word have to be changed, then it is sufficient to program only the appropriate 24-bit word. The serial data input timing and the structure of the control words are illustrated in Fig. 2 and 3.

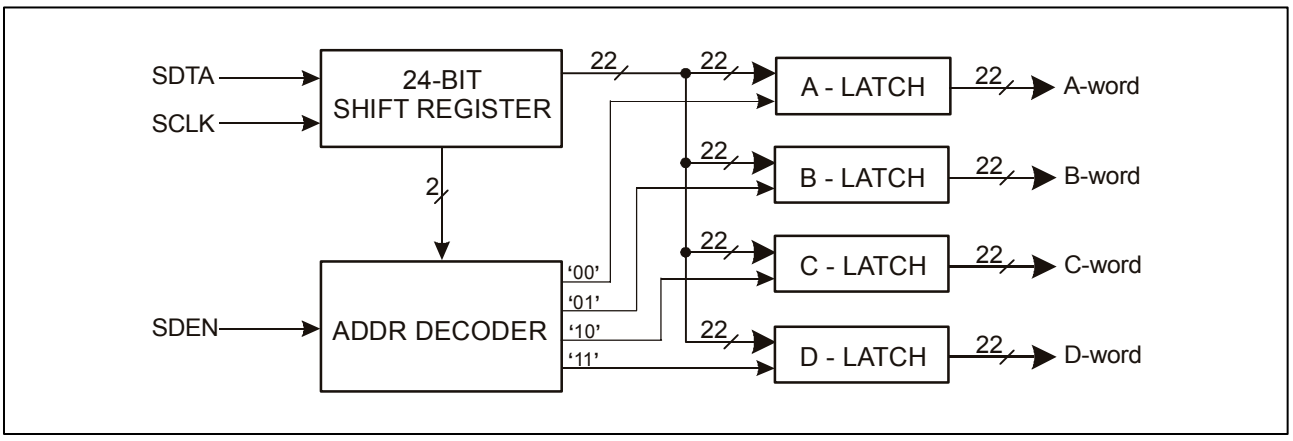


Fig. 2: SCI Block Diagram

Due to the static CMOS design, the SCI consumes virtually no current and it can be programmed in active as well as in standby mode.
If the transceiver is set from standby mode to any of the active modes (idle, receive, transmit), the SCI settings remain the same as previously set in one of the active modes, unless new settings are done on the SCI while entering into an active mode.

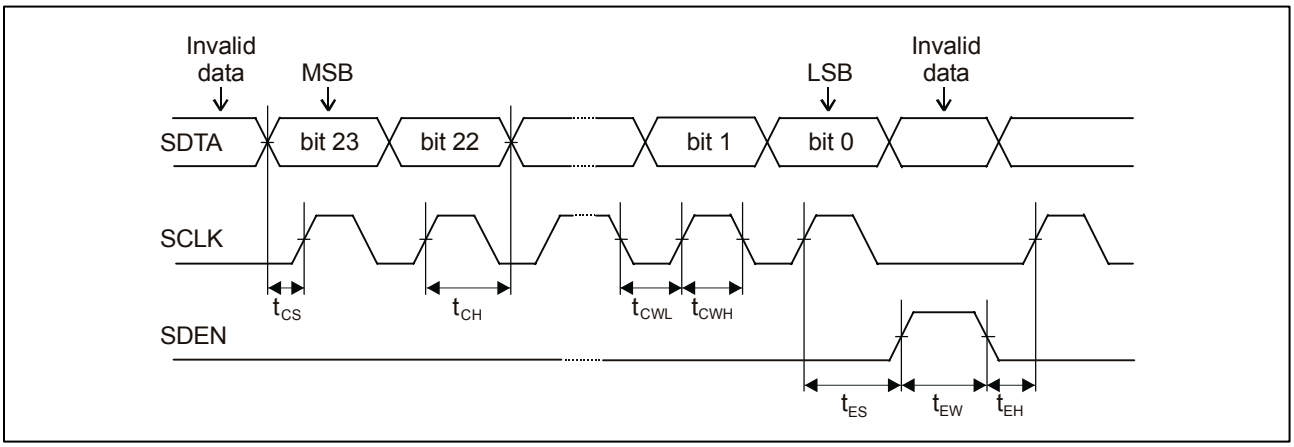


Fig. 3: Serial Data Input Timing

3 Register Description

As shown in the previous section there are four control words which stipulate the operation of the whole chip. In Stand-alone User Mode SUM the intrinsic default values with respect to the applied levels at pins FS0 and FS1 lay down the configuration of the transceiver. In Programmable User Mode (PUM) the register settings can be changed via 3-wire interface SCI. The default settings which vary with the desired operating frequency depend on the voltage levels at the frequency selection pins FS0 and FS1 before entering the PUM. Table 5.1.1 shows the default register settings of different frequency selections. It should be noted that the channel frequency listed below will be achieved with a crystal frequency of 7.1505 MHz. The following table depicts an overview of the register configuration of the TH7122.

3.1 Register Overview

WORD MSB		DATA																						LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Bit No.
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	Depends on FS0/FS1 voltage level after power up											**default**
A		IDLE	DATAPOL	MODSEL	CPCUR	LOCKMODE	PACTRL	TXPOWER [1 : 0]		*Set to 1*	LNAGAIN	OPMODE [1 : 0]		RR [9 : 0]											
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Bit No.
0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	Depends on FS0/FS1 voltage level after power up											**default**
B		PKDET	*Set to 1*	DELPLL	LNAHYST	AFC	OA2	ROMAX [2 : 0]			ROMIN [2 : 0]			RT [9 : 0]											
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Bit No.
1	**0**	**0**	**0**	Depends on FS0/FS1 voltage level after power up																					**default**
C		LNACTRL	PFDPOL	VCOCUR [1 :0]		BAND	NR [16 : 0]																		
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Bit No.
1	**1**	**0**	**0**	**1**	**0**	**0**	Depends on FS0/FS1 voltage level after power up																		**default**
D		MODCTRL	LDTM [1 :0]		ERTM [1 :0]		NT [16 : 0]																		

3.1.1 Default Register Settings for FS0, FS1

FS1	FS0	Channel frequency	BAND	VCOCUR [1 : 0]	RR [9 : 0]	NR [16 :0]	RT [9 :0]	NT [16 : 0]
0	0	**868.30 MHz**	1	11	16d	1919d	16d	1943d
0	1	**433.92 MHz**	0	01	32d	1894d	32d	1942d
1	0	**915.00 MHz**	1	11	32d	4047d	32d	4095d
1	1	**315.00 MHz**	0	00	18d	766d	18d	793d

Note: d – decimal code

A detailed description of the registers function and their configuration can be found in the following sections.

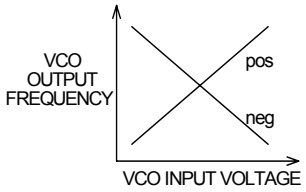
3.1.2 A – word

Name	Bits	Description
RR	[9:0]	Reference divider ratio in RX operation mode **4d .. 1023d**
OPMODE	[11:10]	Operation mode **00** **Standby mode** #default **01** **Receive mode** **10** **Transmit mode** **11** **Idle mode**
LNAGAIN	[12]	LNA gain **0** **low LNA gain** **1** **high LNA gain** #default This selection is valid if bit LNACTR (bit 21 in C-word) is set to internal LNA gain control.
not used	[13]	set to '1' for correct function
TXPOWER	[15:14]	Output power steps **00** **P1** **01** **P2** **10** **P3** **11** **P4** #default
PACTRL	[16]	Set the PA-on condition **0** **PA is switched on if the PLL locks** **1** **PA is always on in TX mode** #default
LOCKMODE	[17]	Set the PLL locked state observation mode **0** **before lock only** #default Locked state condition will be ascertained only one time afterwards the LD signal remains in high state. **1** **before and after lock** locked state will be observed permanently
CPCUR	[18]	Charge Pump output current **0** **260 µA** #default **1** **1300 µA**
MODSEL	[19]	Modulation mode **0** **ASK** #default **1** **FSK** This selection is valid if bit MODCTRL (bit 21 in D-word) is set to internal modulation control.
DTAPOL	[20]	Input data polarity **0** **normal** #default '0' for space at ASK or f_{min} at FSK, '1' for mark at ASK or f_{max} at FSK **1** **inverse** '1' for space at ASK or f_{min} at FSK, '0' for mark at ASK or f_{max} at FSK
IDLESEL	[21]	Active blocks in IDLE mode **0** **only RO active** #default **1** **whole PLL active**

3.1.3 B – word

Name	Bits	Description
RT	[9:0]	Reference divider ratio in TX operation mode **4d .. 1023d**
ROMIN	[12:10]	Set the desired steady state current of the reference oscillator **000** **0 µA** **001** **75 µA** **010** **150 µA** #default **011** **225 µA** **100** **300 µA** **101** **375 µA** **110** **450 µA** **111** **525 µA** The control circuitry regulates the current of the oscillator core between the values ROMAX and ROMIN. As the regulation input signal the amplitude on pin RO is used. If the ROMIN value is sufficient to achieve an amplitude of about 400mV on pin RO the current of the reference oscillator core will be set to ROMIN. Otherwise the current will be permanently regulated between ROMAX and ROMIN. If ROMIN and ROMAX are equal no regulation of the oscillator current occurs. Please also note the block description of the reference oscillator in para. 3.1.1
ROMAX	[15:13]	Set the start-up current of the reference oscillator **000** **0 µA** **001** **75 µA** **010** **150 µA** **011** **225 µA** **100** **300 µA** **101** **375 µA** **110** **450 µA** **111** **525 µA** #default Set the start-up current of the reference oscillator core. Please also note the description of the ROMIN register and the block description of the reference oscillator which can be seen above.
OA2	[16]	OA2 operation **0** **disabled** #default **1** **enabled** OA2 can be enabled in FSK receive mode. OA2 is disabled in ASK mode receive.
AFC	[17]	Internal AFC feature **0** **disabled** #default **1** **enabled**
LNAHYST	[18]	Hysteresis on pin GAIN_LNA **0** **disabled** **1** **enabled** - typical 340 mV ($V_{0\rightarrow1}$ = 1.56V, $V_{1\rightarrow0}$ = 1.22V) #default
DELPLL	[19]	Delayed start of the PLL **0** **undelayed start** PLL starts at the reference oscillator start-up **1** **starts after 8 valid RO-cycles** #default PLL starts after 8 valid RO-cycles before entering an active mode to ensure reliable oscillation of the reference oscillator.
not used	[20]	set to ‘1’ for correct function
PKDET	[21]	RSSI Peak Detector **0** **disabled** #default The RSSI output signal directly feeds the data slicer setup by means of OA1. **1** **enabled** In ASK receive mode the RSSI Peak Detector output is multiplexed to pin INT2/PDO.

3.1.4 C – word

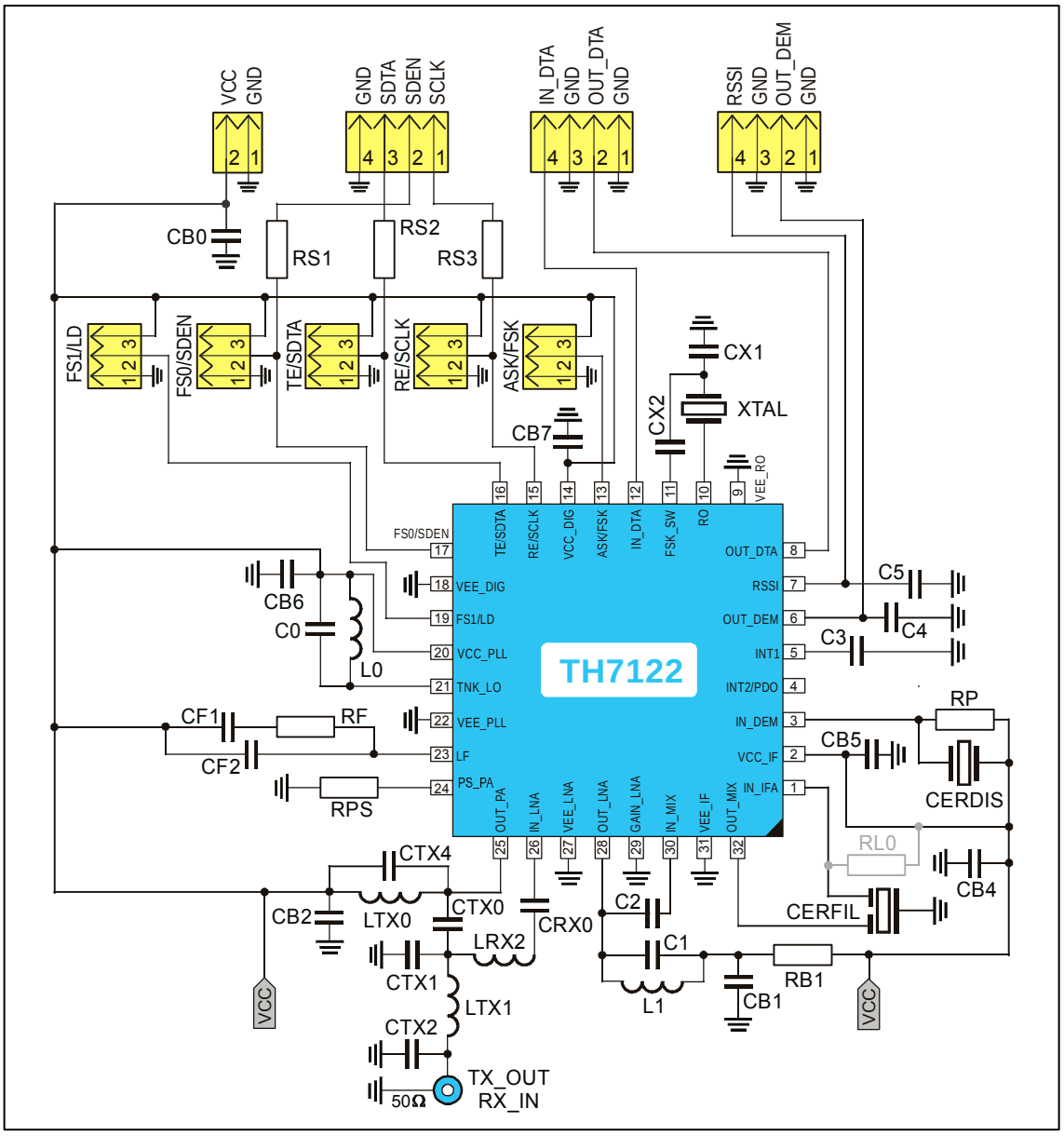
Name	Bits	Description
NR	[16:0]	Feedback divider ratio in RX operation mode **64d .. 131071d**
BAND	[17]	Set the desired frequency range **0** **recommended at f_{RF} < 500 MHz** **1** **recommended at f_{RF} > 500MHz** Some tail current sources are linked to this bit in order to save current for low frequency operations.
VCOCUR	[19:18]	VCO active current **00** **low current (300 µA)** **01** **standard current (500 µA)** **10** **high1 current (700 µA)** **11** **high2 current (900 µA)**
PFDPOL	[20]	Phase Detector polarity **0** **negative** #default **1** **positive** 
LNACTRL	[21]	LNA gain control mode **0** **external LNA gain control** #default LNA gain will be set via pin GAIN_LNA. **1** **internal LNA gain control** LNA gain will be set via bit LNAGAIN (bit 12 in A-word). Nevertheless pin GAIN_LNA must be connected to either VCC or VEE.

3.1.5 D – word

Name	Bits	Description			
NT	[16:0]	Feedback divider ratio in TX operation mode			
		64d .. 131071d			
ERTM	[18:17]	Set the unlock condition of the PLL			
		00 **01** **10** **11**	**2 clocks** **4 clocks** **8 clocks** **16 clocks**	#default	Set the maximum allowed number of reference clocks ($1/f_{RO}$) during the phase detector output signals (UP & DOWN) can be in-consecutive.
LDTM	[20:19]	Set the lock condition of the PLL			
		00 **01** **10** **11**	**4 clocks** **16 clocks** **64 clocks** **256 clocks**	#default	Set the minimum number of consecutive edges of phase detector output cycles, without appearance of any unlock condition.
MODCTRL	[21]	Set mode of modulation control:			
		0	**external modulation control**		#default
			Modulation will be set via pin ASK/FSK.		
		1	**internal modulation control**		
			Modulation will be set via bit MODSEL (bit 19 in A-word). Nevertheless pin ASK/FSK must be connected to either VCC or VEE.		

4 Application Circuits

4.1 FSK Application Circuit Programmable User Mode (internal AFC option)

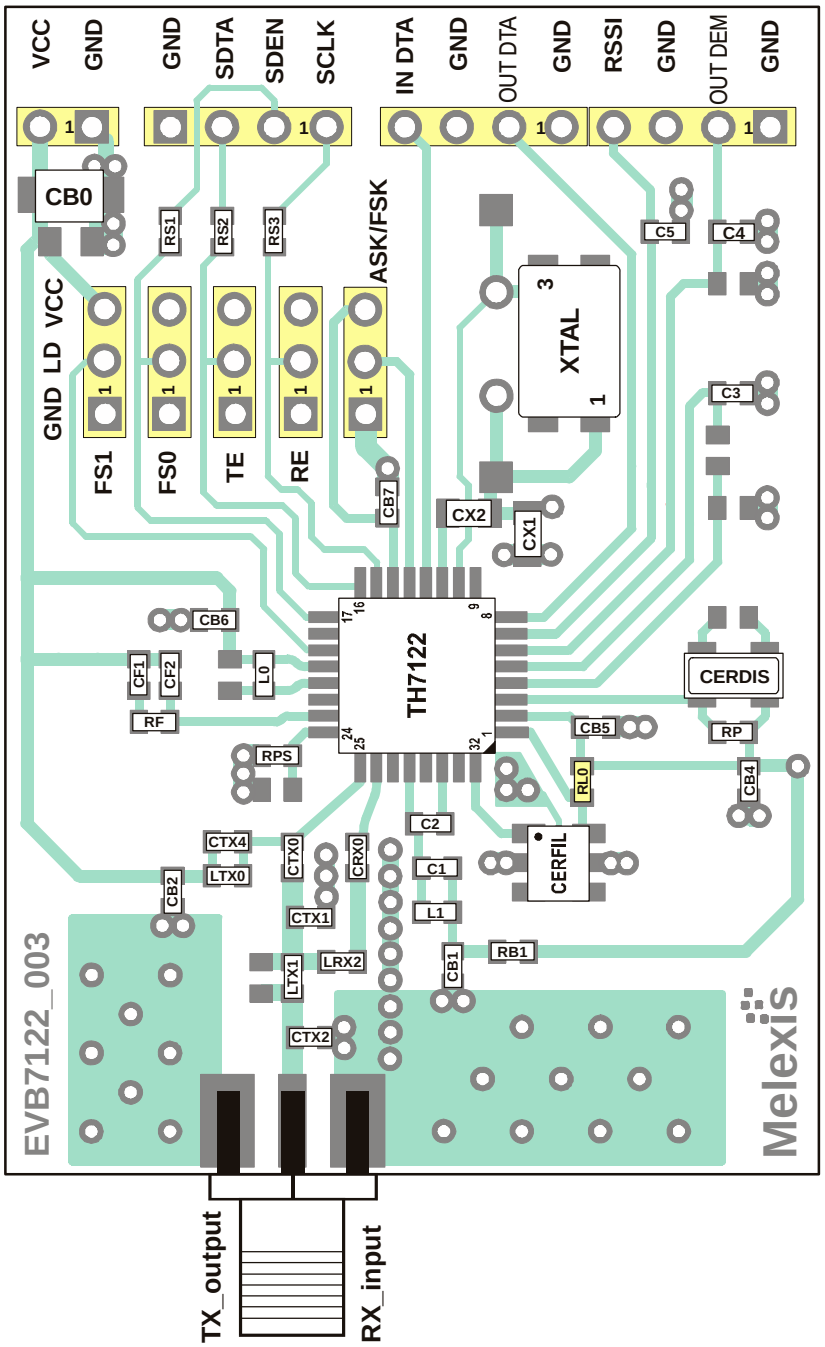


4.1.1 Board Component Values for FSK Reception

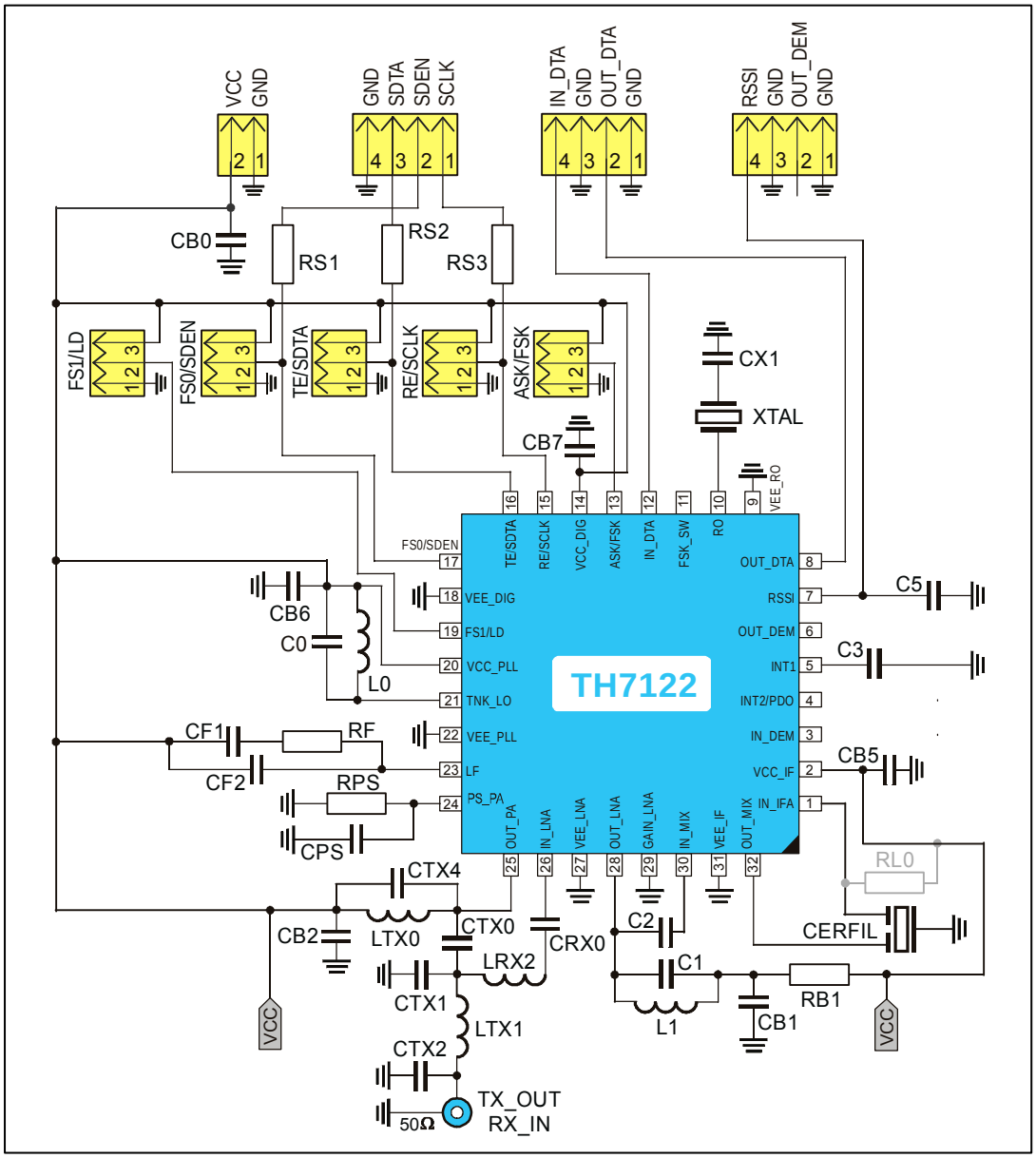
Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	0.47 pF	NIP	1.8 pF	1.5 pF	±5%	VCO tank capacitor
C1	0603	3.9 pF	4.7 pF	1.8 pF	1 pF	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.5 pF	1.5 pF	1.5 pF	±5%	MIX input matching capacitor
C3	0603	10 nF	10 nF	10 nF	10 nF	±10%	data slicer capacitor
C4	0603	330 pF	330 pF	330 pF	330 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C5	0603	1.5 nF	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
CB0	1210	10 µF	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	10 nF	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB2	0603	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB4	0603	10 nF	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	1 nF	1 nF	1 nF	1 nF	±10%	loop filter capacitor
CF2	0603	100 pF	68 pF	150 pF	82 pF	±5%	loop filter capacitor
CX1	0805	8.2 pF	10 pF	12 pF	12 pF	±5%	RO capacitor for FSK (Δf = ±20 kHz)
CX2	0805	150 pF	56 pF	18 pF	15 pF	±5%	RO capacitor for FSK (Δf = ±20 kHz)
CRX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	RX coupling capacitor
CTX0	0603	10 pF	10 pF	10 pF	10 pF	±5%	TX coupling capacitor
CTX1	0603	10 pF	6.8 pF	5.6 pF	4.7 pF	±5%	TX impedance matching capacitor
CTX2	0603	10 pF	6.8 pF	3.9 pF	3.9 pF	±5%	TX impedance matching capacitor
CTX4	0603	12 pF	4.7 pF	2.2 pF	1.8 pF	±5%	TX impedance matching capacitor
RB1	0603	100 Ω	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RP	0603	3.3 KΩ	3.3 KΩ	3.3 KΩ	3.3 KΩ	±5%	CERDIS loading resistor
RL0	0603	390 Ω	390 Ω	390 Ω	390 Ω	±5%	CERFIL loading, optionally
RPS	0603	18 kΩ	33 kΩ	43 kΩ	43 kΩ	±5%	power-select resistor
RS1...RS3	0603	10 kΩ	10 kΩ	10 kΩ	10 kΩ	±5%	protection resistor
L0	0603	56 nH	33 nH	4.7 nH	3.9 nH	±5%	VCO tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L1	0603	33 nH	15 nH	4.7 nH	4.7 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
LRX2	0603	82 nH	56 nH	15 nH	15 nH	±5%	impedance matching inductor from Würth-Elektronik (WE-KI series) or equivalent part
LTX0	0603	15 nH	15 nH	3.9 nH	3.9 nH	±5%	
LTX1	0603	33 nH	33 nH	10 nH	10 nH	±5%	
XTAL	HC49 SMD 7x5	7.1505 MHz ±20ppm cal., ±20ppm temp.					fundamental-mode crystal from: Telcona/Hong Kong X'tals C5L7150500D10F3EHK02
CERFIL	SMD 3.45x3.1	SFECF10M7HA00 B_{3dB} = 180 kHz					ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA136					ceramic Discriminator from Murata, or equivalent part

Note: - NIP – not in place, may be used optionally

4.1.2 Component Arrangement Top Side for FSK Reception



4.2 ASK Application Circuit Programmable User Mode (normal data slicer option)



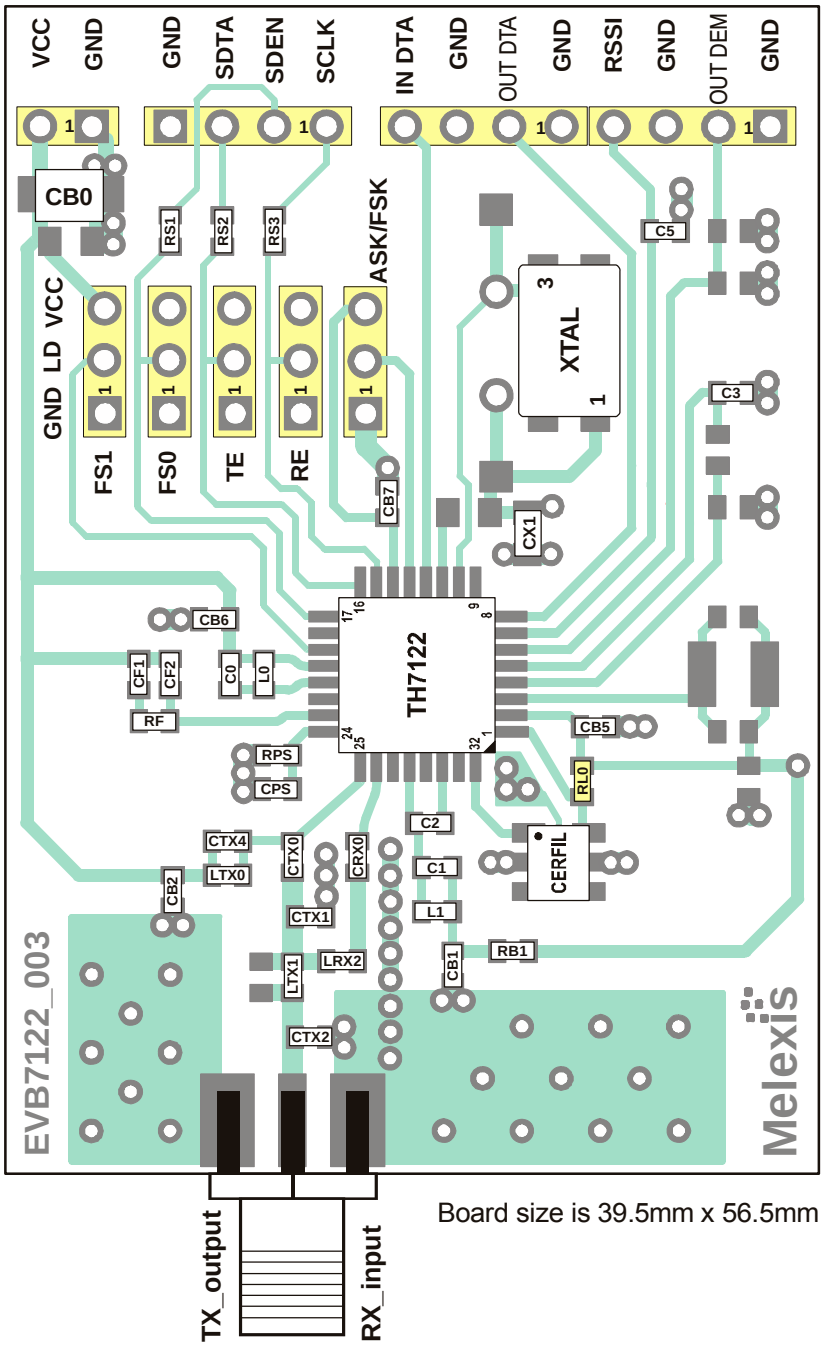
Software Settings for ASK

Channel frequency	f_{RO} = 8.0000MHz				CPCUR		VCOCUR	
	RR	NR	RT	NT	RX	TX	RX	TX
315.00 MHz	80	3043	8	315	260µA	1300µA	300µA	900µA
434.00 MHz	80	4233	8	434	260µA	1300µA	300µA	900µA
915.00 MHz	80	9043	8	915	260µA	1300µA	300µA	900µA

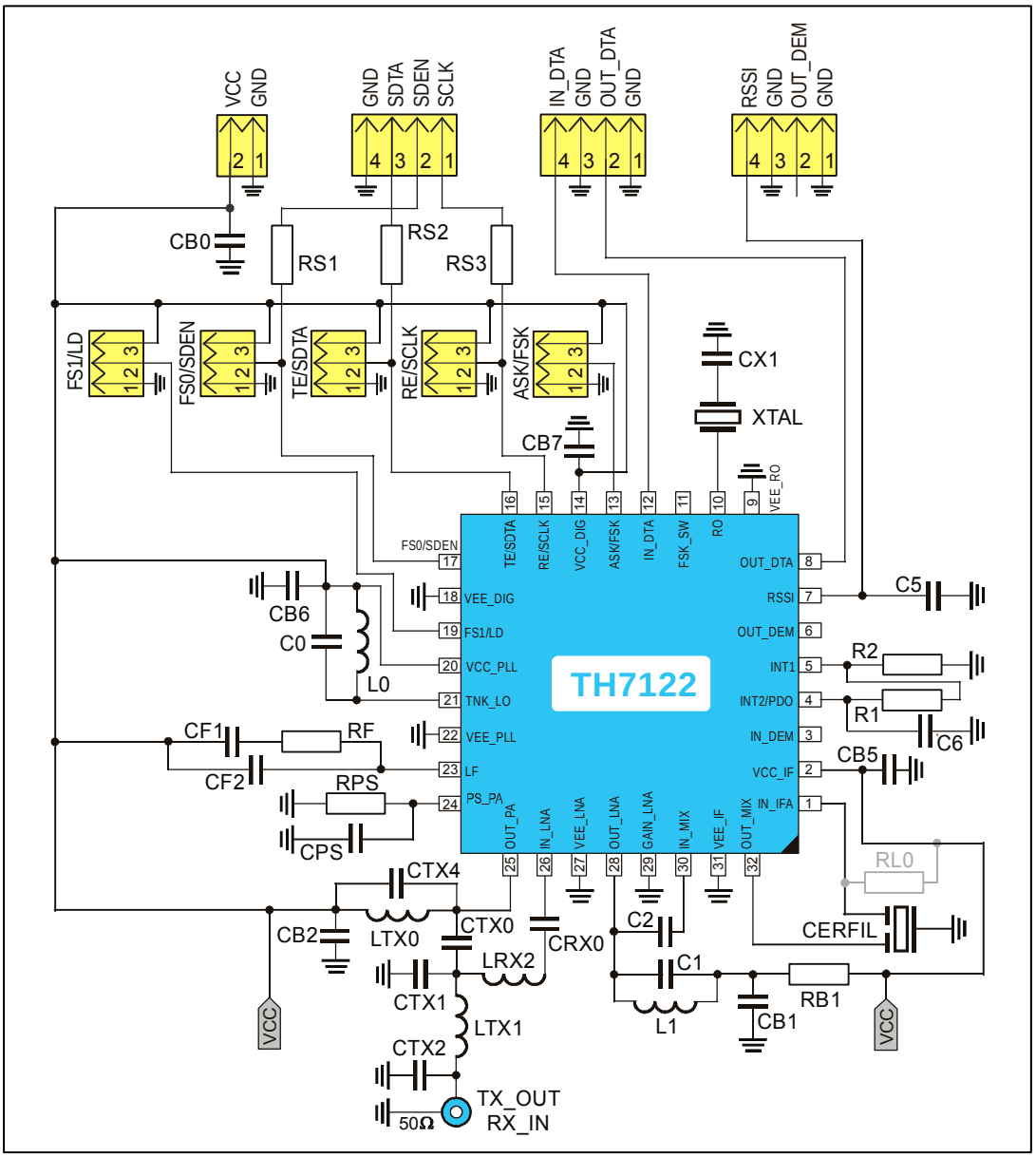
4.2.1 Board Component Values for ASK (normal data slicer option)

Part	Size	Value @ 315 MHz	Value @ 434 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	1.8 pF	2.2 pF	1.8 pF	±5%	VCO tank capacitor
C1	0603	3.9 pF	4.7 pF	1 pF	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	±5%	MIX input matching capacitor
C3	0603	10 nF	10 nF	10 nF	±10%	data slicer capacitor
C5	0603	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
CB0	1210	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB2	0603	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	100 pF	100 pF	100 pF	±10%	loop filter capacitor
CF2	0603	39 pF	39 pF	39 pF	±5%	loop filter capacitor
CPS	0603	1 nF	1 nF	1 nF	±10%	power-select capacitor
CX1	0805	18 pF	18 pF	18 pF	±5%	RO capacitor
CRX0	0603	100 pF	100 pF	10 pF	±5%	RX coupling capacitor
CTX0	0603	10 pF	10 pF	10 pF	±5%	TX coupling capacitor
CTX1	0603	10 pF	6.8 pF	4.7 pF	±5%	TX impedance matching capacitor
CTX2	0603	10 pF	6.8 pF	3.9 pF	±5%	TX impedance matching capacitor
CTX4	0603	12 pF	4.7 pF	1.8 pF	±5%	TX impedance matching capacitor
RB1	0603	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RP	0603	3.3 KΩ	3.3 KΩ	3.3 KΩ	±5%	CERDIS loading resistor
RL0	0603	390 Ω	390 Ω	390 Ω	±5%	CERFIL loading, optionally
RPS	0603	18 kΩ	33 kΩ	43 kΩ	±5%	power-select resistor
RS1...RS3	0603	10 kΩ	10 kΩ	10 kΩ	±5%	protection resistor
L0	0603	47 nH	27 nH	3.9 nH	±5%	VCO tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L1	0603	33 nH	15 nH	4.7 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
LRX2	0603	82 nH	56 nH	15 nH	±5%	impedance matching inductor from Würth-Elektronik (WE-KI series) or equivalent part
LTX0	0603	15 nH	15 nH	3.9 nH	±5%	
LTX1	0603	33 nH	33 nH	10 nH	±5%	
XTAL	HC49 SMD 7x5	8.0000 MHz ±20ppm cal., ±20ppm temp.				fundamental-mode crystal from: Telcona/Hong Kong X'tals C5L8000000D10F3EHK01
CERFIL	SMD 3.45x3.1	SFECF10M7HA00 B_{3dB} = 180 kHz				ceramic filter from Murata, or equivalent part

4.2.2 Component Arrangement Top Side for ASK Reception (normal data slicer option)



4.3 ASK Application Circuit with Peak Detector Option



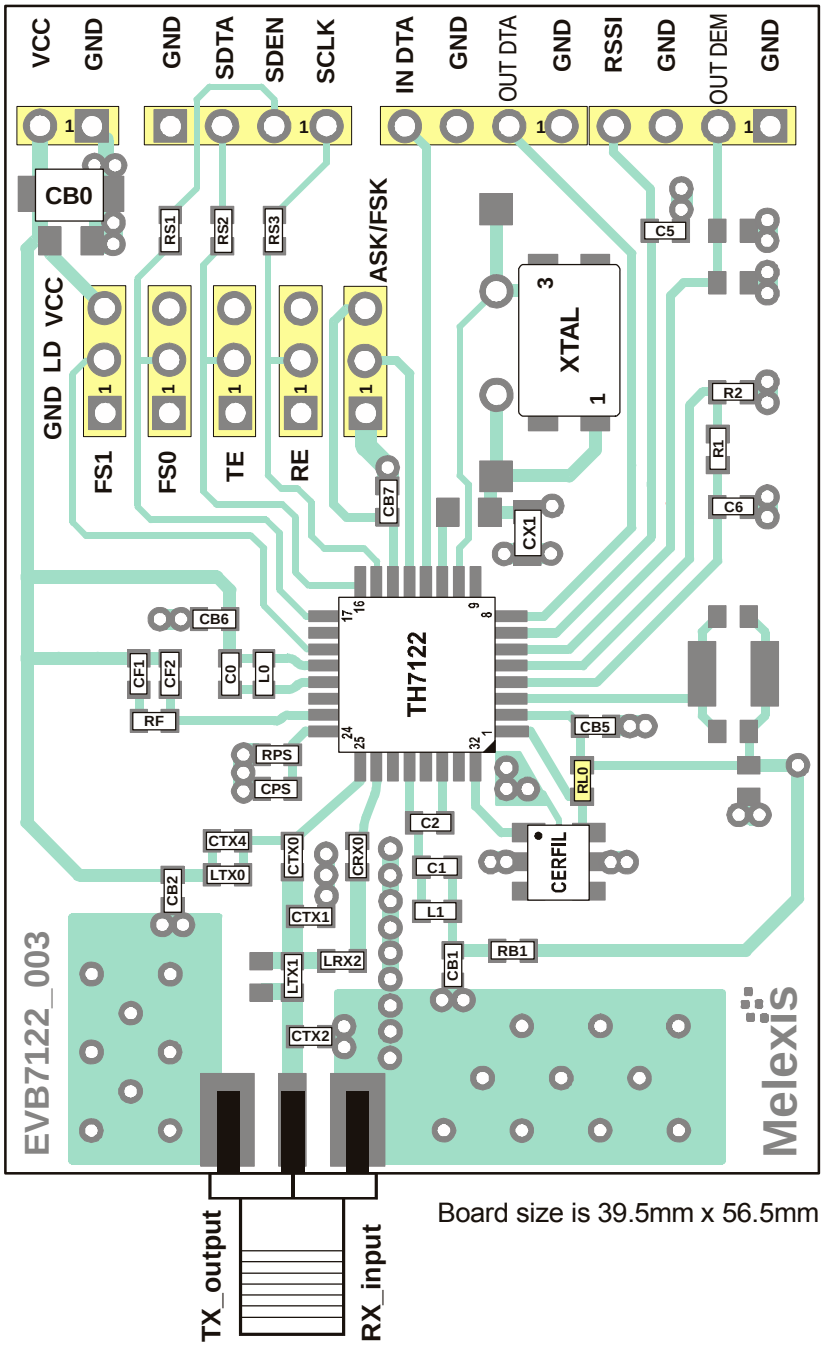
Software Settings for ASK

Channel frequency	f_{RO} = 8.0000MHz				CPCUR		VCOCUR	
	RR	NR	RT	NT	RX	TX	RX	TX
315.00 MHz	80	3043	8	315	260µA	1300µA	300 µA	900µA
434.00 MHz	80	4233	8	434	260µA	1300µA	300 µA	900µA
915.00 MHz	80	9043	8	915	260µA	1300µA	300 µA	900µA

4.3.1 Board Component Values for ASK (peak detector option)

Part	Size	Value @ 315 MHz	Value @ 434 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	1.8 pF	2.2 pF	1.8 pF	±5%	VCO tank capacitor
C1	0603	3.9 pF	4.7 pF	1 pF	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	±5%	MIX input matching capacitor
C5	0603	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
C6	0603	100 nF	100 nF	100 nF	±10%	PKDET capacitor
CB0	1210	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB2	0603	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	100 pF	100 pF	100 pF	±10%	loop filter capacitor
CF2	0603	39 pF	39 pF	39 pF	±5%	loop filter capacitor
CPS	0603	1 nF	1 nF	1 nF	±10%	power-select capacitor
CX1	0805	18 pF	18 pF	18 pF	±5%	RO capacitor
CRX0	0603	100 pF	100 pF	10 pF	±5%	RX coupling capacitor
CTX0	0603	10 pF	10 pF	10 pF	±5%	TX coupling capacitor
CTX1	0603	10 pF	6.8 pF	4.7 pF	±5%	TX impedance matching capacitor
CTX2	0603	10 pF	6.8 pF	3.9 pF	±5%	TX impedance matching capacitor
CTX4	0603	12 pF	4.7 pF	1.8 pF	±5%	TX impedance matching capacitor
R1	0603	100 kΩ	100 kΩ	100 kΩ	±5%	PKDET resistor
R2	0603	680 kΩ	680 kΩ	680 kΩ	±5%	PKDET resistor
RB1	0603	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RP	0603	3.3 KΩ	3.3 KΩ	3.3 KΩ	±5%	CERDIS loading resistor
RL0	0603	390 Ω	390 Ω	390 Ω	±5%	CERFIL loading, optionally
RPS	0603	18 kΩ	33 kΩ	43 kΩ	±5%	power-select resistor
RS1...RS3	0603	10 kΩ	10 kΩ	10 kΩ	±5%	protection resistor
L0	0603	47 nH	27 nH	3.9 nH	±5%	VCO tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L1	0603	33 nH	15 nH	4.7 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
LRX2	0603	82 nH	56 nH	15 nH	±5%	impedance matching inductor from Würth-Elektronik (WE-KI series) or equivalent part
LTX0	0603	15 nH	15 nH	3.9 nH	±5%	
LTX1	0603	33 nH	33 nH	10 nH	±5%	
XTAL	HC49 SMD 7x5	8.0000 MHz ±20ppm cal., ±20ppm temp.				fundamental-mode crystal from: Telcona/Hong Kong X'tals C5L8000000D10F3EHK01
CERFIL	SMD 3.45x3.1	SFECF10M7HA00 B_{3dB} = 180 kHz				ceramic filter from Murata, or equivalent part

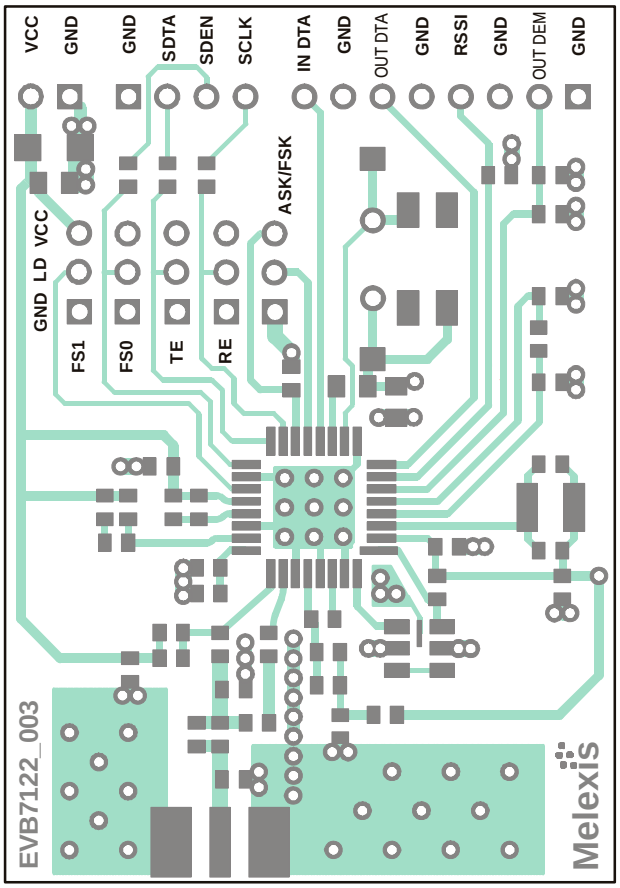
4.3.2 Component Arrangement Top Side for ASK Reception (peak detector option)



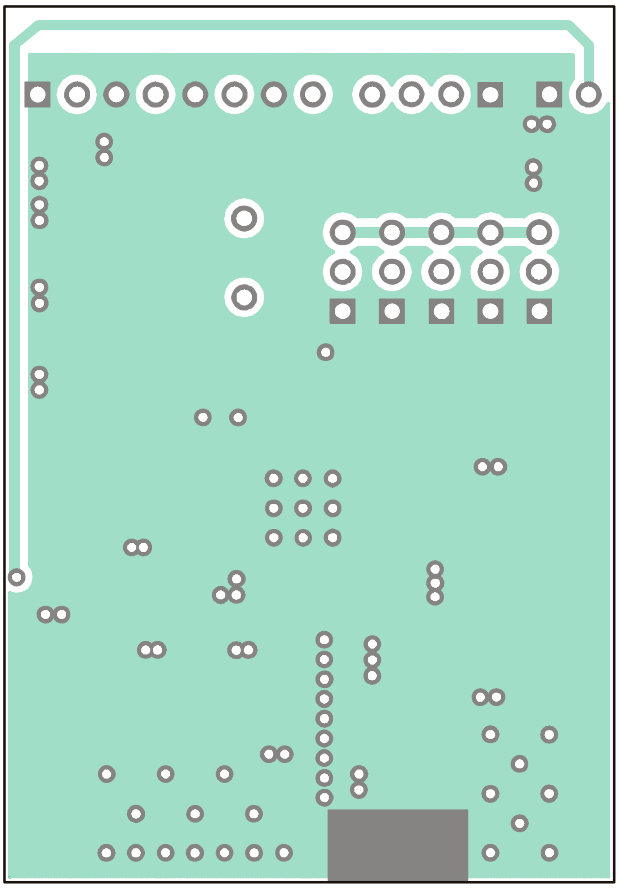
Board size is 39.5mm x 56.5mm

5 Evaluation Board Layouts

- Board layout data in Gerber format is available, board size is 39.5mm x 56.5mm.



PCB top view



PCB bottom view

6 Board Variants

Type	Frequency/MHz	Modulation	Board Execution
EVB7122	**–315**	**–FSK**	**–A** antenna version
	–433	**–ASK** according to section 4.2 / 4.3	**–C** connector version
	–868	**–FM**	
	–915		

Note: **available EVB setups**

7 Package Description

The device TH7122 is RoHS compliant.

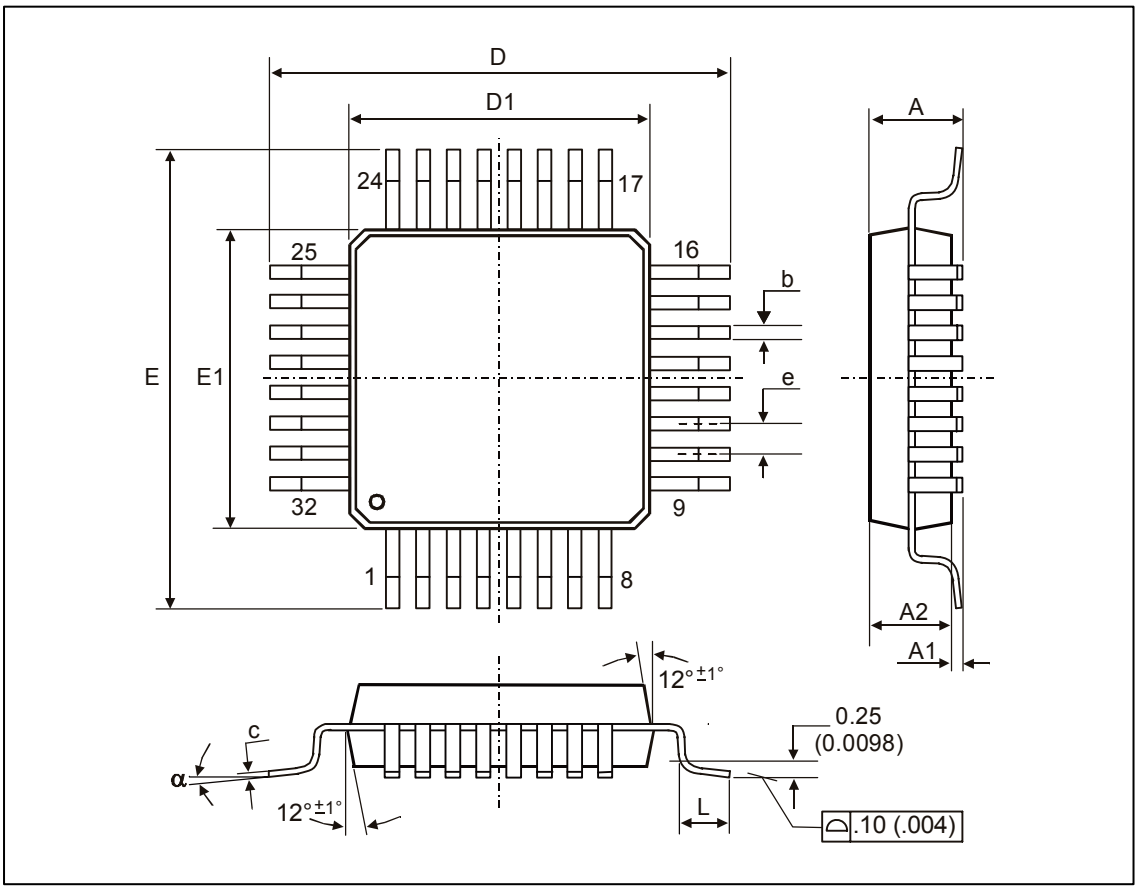


Fig. 4: LQFP32 (Low profile Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm										
	E1, D1	**E, D**	**A**	**A1**	**A2**	**e**	**b**	**c**	**L**	**α**
min	7.00	9.00	1.40	0.05	1.35	0.8	0.30	0.09	0.45	0°
max			1.60	0.15	1.45		0.45	0.20	0.75	7°
All Dimension in inch, coplanarity < 0.004”										
min	0.276	0.354	0.055	0.002	0.053	0.031	0.012	0.0035	0.018	0°
max			0.063	0.006	0.057		0.018	0.0079	0.030	7°

7.1 Soldering Information

- The device TH7122 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

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