	<b>SRAM MODULE 512KByte (128K x 32-Bit)</b> <b>Part No. HMS12832M4</b>
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**GENERAL DESCRIPTION**

The HMS12832M4 is a high-speed static random access memory (SRAM) module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

PD0 and PD1 identify the module’s density allowing interchangeable use of alternate density, industry- standard modules. Four chip enable inputs, (/CE1, /CE2, /CE3 and /CE4) are used to enable the module’s 4 bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW.

Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

**FEATURES**

- ◆ Access times : 12, 15 and 20ns
- ◆ High-density 512KByte design
- ◆ High-reliability, high-speed design
- ◆ Single + 5V ±0.5V power supply
- ◆ Easy memory expansion with /CE and /OE functions
- ◆ All inputs and outputs are TTL-compatible
- ◆ Industry-standard pinout
- ◆ FR4-PCB design

**OPTIONS**

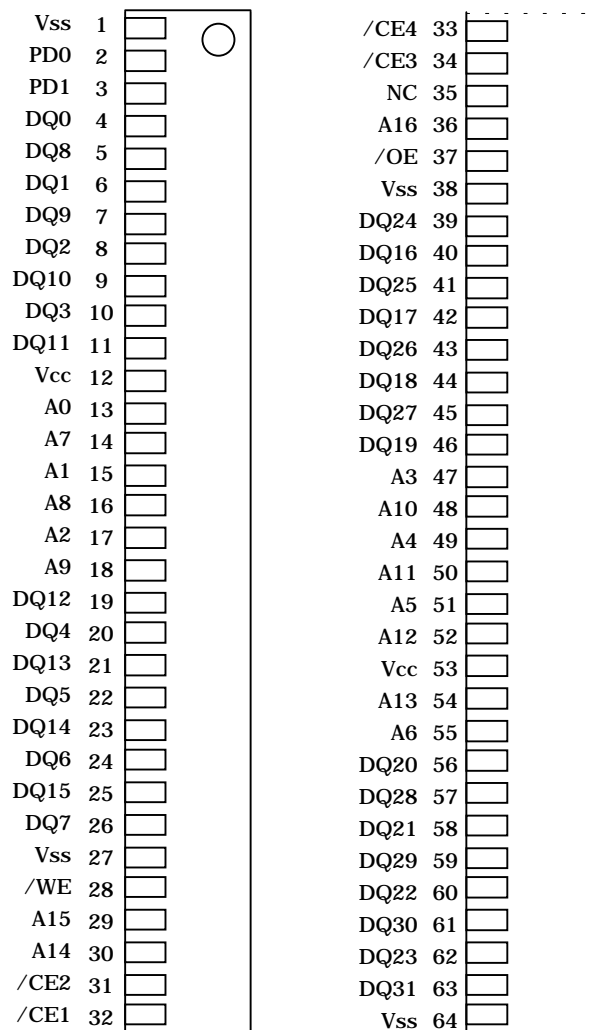
**MARKING**

- ◆ Timing
 

8ns access	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
- ◆ Packages
 

64-pin SIMM	M
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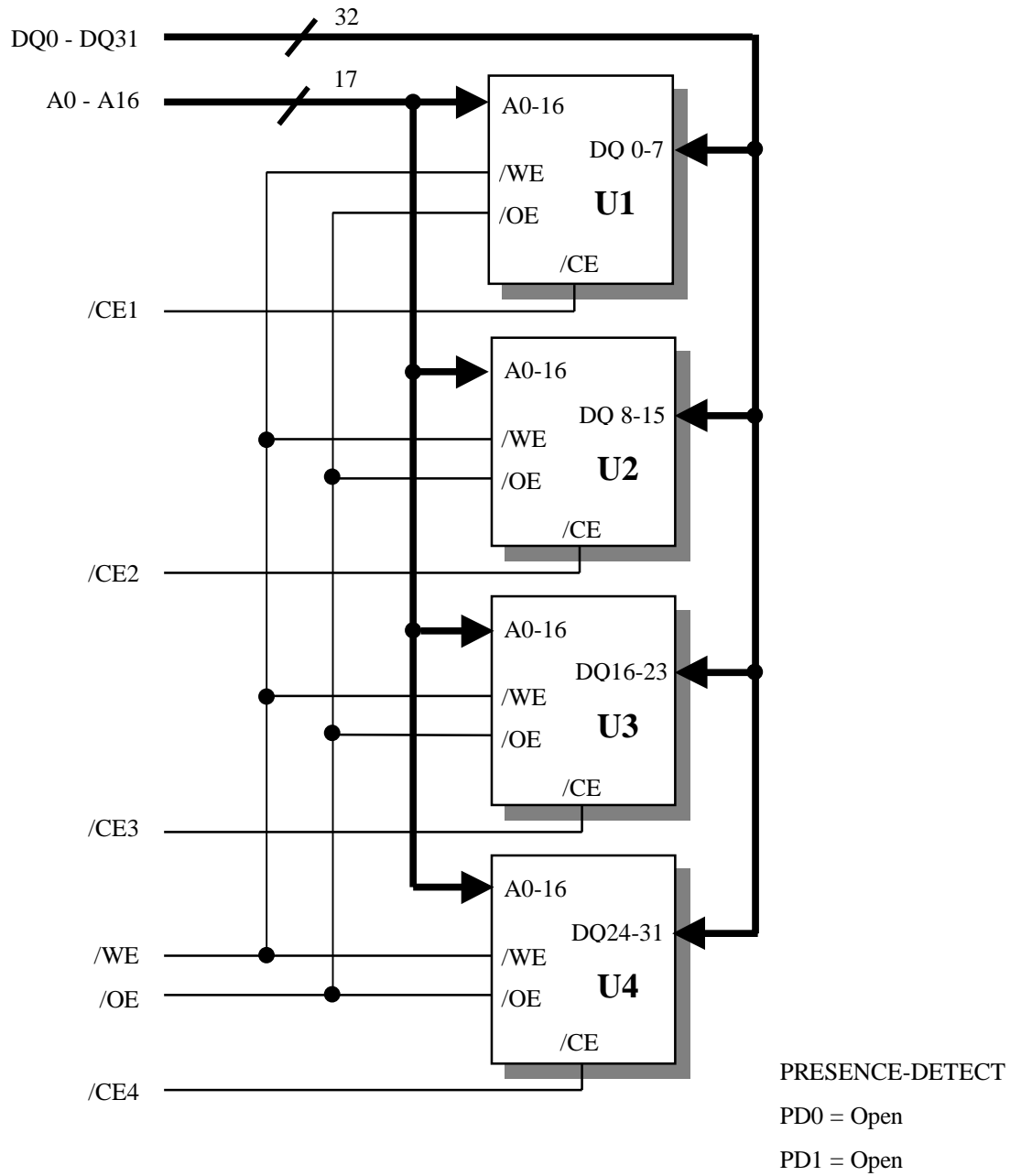
**PIN ASSIGNMENT**



**SIMM  
TOP VIEW**

PD0 = Open  
PD1 = Open

**FUNCTIONAL BLOCK DIAGRAM**



**TRUTH TABLE**

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE	X	L	L	Din	ACTIVE

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>IN,OUT</sub>	-0.5V to V <sub>CC</sub> +0.5V
Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5V to +7.0V
Power Dissipation	P <sub>D</sub>	4.0W
Storage Temperature	T <sub>STG</sub>	-65°C to +150°C
Operating Temperature	T <sub>A</sub>	0°C to +70°C

- ♦ Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** ( T<sub>A</sub>=0 to 70 °C )

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V <sub>CC</sub>	4.5V	5.0V	5.5V
Ground	V <sub>SS</sub>	0	0	0
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5V**
Input Low Voltage	V <sub>IL</sub>	-0.5*	-	0.8V

\* V<sub>IL</sub>(Min.) = -2.0V ac (Pulse Width ≤ 10ns) for I ≤ 20 mA

\*\* V<sub>IH</sub>(Min.) = V<sub>CC</sub>+2.0V ac (Pulse Width ≤ 10ns) for I ≤ 20 mA

**DC AND OPERATING CHARACTERISTICS (1)**(0°C ≤ T<sub>A</sub> ≤ 70 °C ; V<sub>CC</sub> = 5V ± 10% )

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	I <sub>L1</sub>	-2	2	μA
Output Leakage Current	/CE=V <sub>IH</sub> or /OE =V <sub>IH</sub> or /WE=V <sub>IL</sub> V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>	I <sub>L0</sub>	-2	2	μA
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V

\* V<sub>CC</sub>=5.0V, Temp=25 °C

**DC AND OPERATING CHARACTERISTICS (2)**

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX			UNIT
			-12	-15	-20	
Power Supply Current:Operating	Min. Cycle, 100% Duty /CE=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	I <sub>CC</sub>	75	73	70	mA
Power Supply Current:Standby	Min. Cycle, /CE=V <sub>IH</sub>	I <sub>SB</sub>	30	30	30	mA
	f=0MHZ, /CE≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	I <sub>SB1</sub>	5	5	5	mA

**CAPACITANCE** (T<sub>A</sub> =25 °C , f= 1.0Mhz)

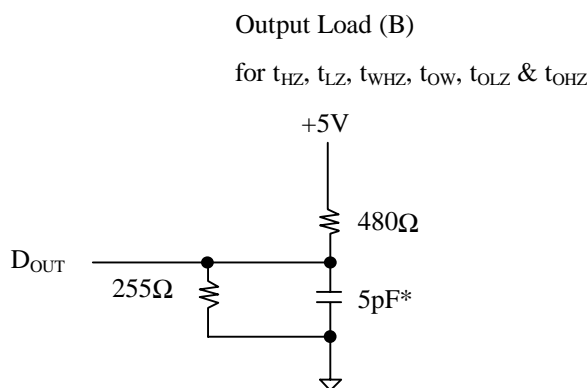
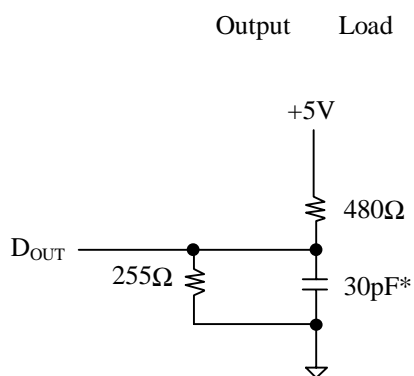
DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	V <sub>IO</sub> =0V	C <sub>IO</sub>	8	pF
Input Capacitance	V <sub>IN</sub> =0V	C <sub>IN</sub>	8	pF

\* NOTE : Capacitance is sampled and not 100% tested

**AC CHARACTERISTICS** (0°C ≤ T<sub>A</sub> ≤ 70 °C ; V<sub>CC</sub> = 5V ± 0.5V, unless otherwise specified)

**Test conditions**

PARAMETER	VALUE
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



**READ CYCLE**

PARAMETER	SYMBOL	-12		-15		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t <sub>RC</sub>	12		15		20		ns
Address Access Time	t <sub>AA</sub>		12		15		20	ns

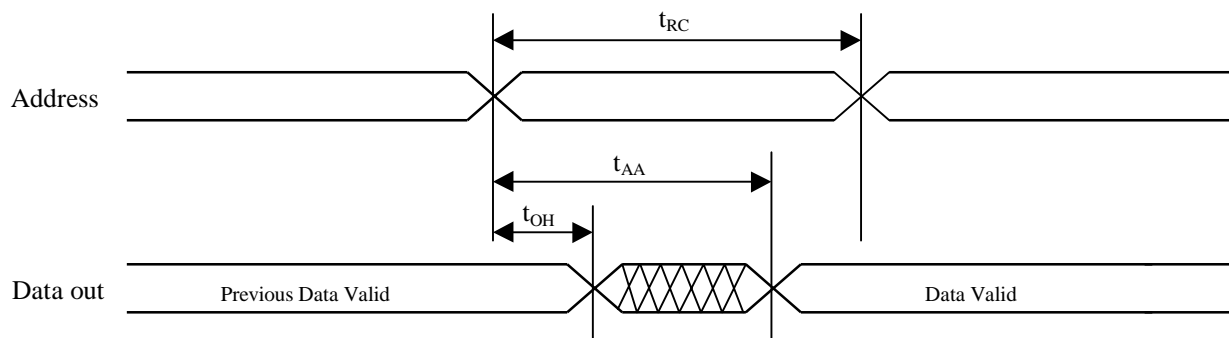
Chip Select to Output	$t_{CO}$		12		15		20	ns
Output Enable to Output	$t_{OE}$		6		7		9	ns
Output Enable to Low-Z Output	$t_{OLZ}$	0		0		0		ns
Chip Enable to Low-Z Output	$t_{LZ}$	3		3		3		ns
Output Disable to High-Z Output	$t_{OHZ}$	0	6	0	7	0	9	ns
Chip Disable to High-Z Output	$t_{HZ}$	0	6	0	7	0	9	ns
Output Hold from Address Change	$t_{OH}$	3		3		3		ns
Chip Select to Power Up Time	$t_{PU}$	0		0		0		ns
Chip Select to Power Down Time	$t_{PD}$	-	12		15		20	ns

**WRITE CYCLE**

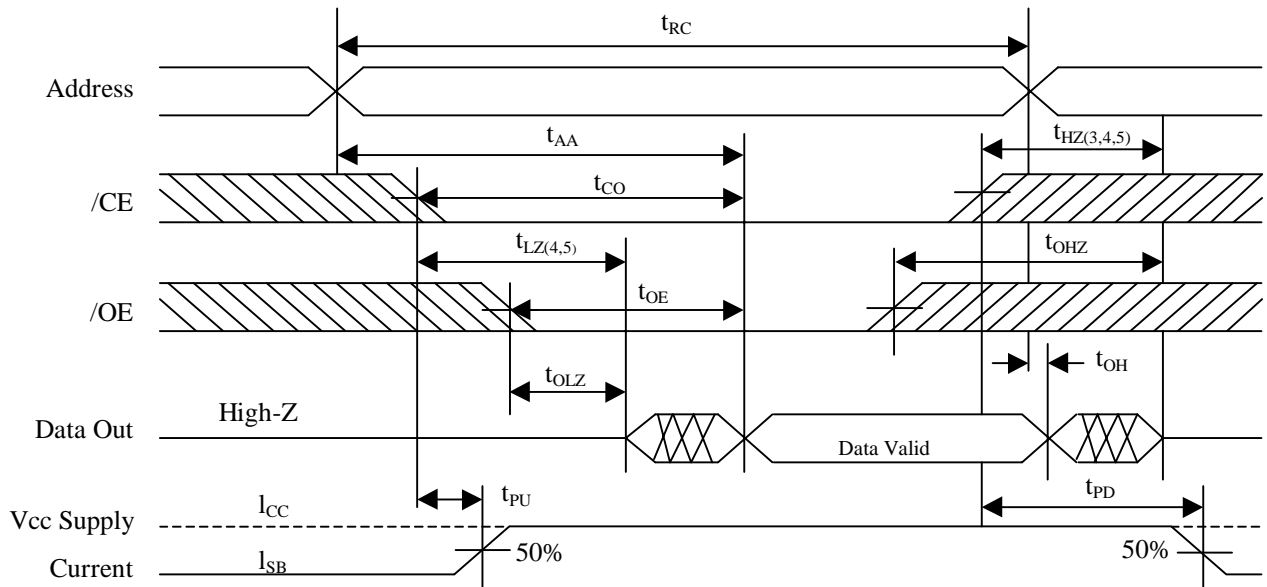
PARAMETER	SYMBOL	-12		-15		-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	$t_{WC}$	12		15		20		ns
Chip Select to End of Write	$t_{CW}$	8		10		12		ns
Address Set-up Time	$t_{AS}$	0		0		0		ns
Address Valid to End of Write	$t_{AW}$	8		9		10		ns
Write Pulse Width	$t_{WP}$	8		9		10		ns
Write Recovery Time	$t_{WR}$	0		0		0		ns
Write to Output High-Z	$t_{WHZ}$	0	6	0	7	0	9	ns
Data to Write Time Overlap	$t_{DW}$	6		7		8		ns
Data Hold from Write Time	$t_{DH}$	0		0		0		ns
End of Write to Output Low-Z	$t_{OW}$	3		3		3		ns

**TIMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE**(Address Controlled) (/CE =/ OE =  $V_{IL}$  , /WE =  $V_{IH}$ )



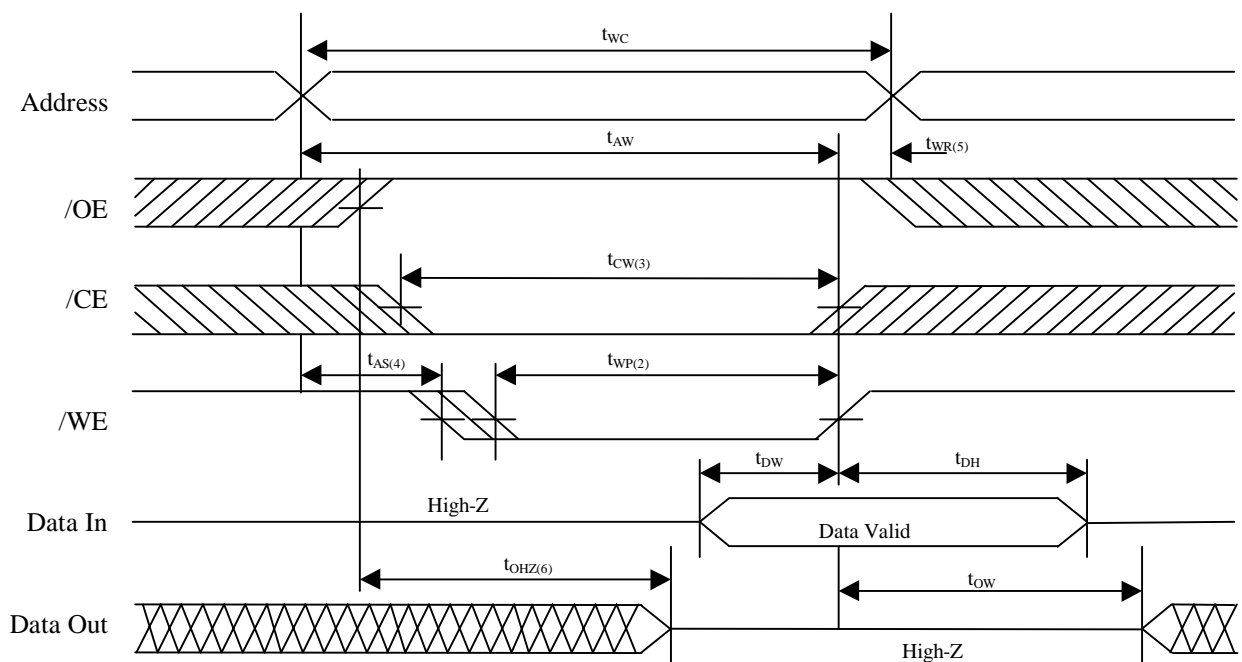
**TIMING WAVEFORM OF READ CYCLE ( /CE Controlled )**



**Notes (Read Cycle)**

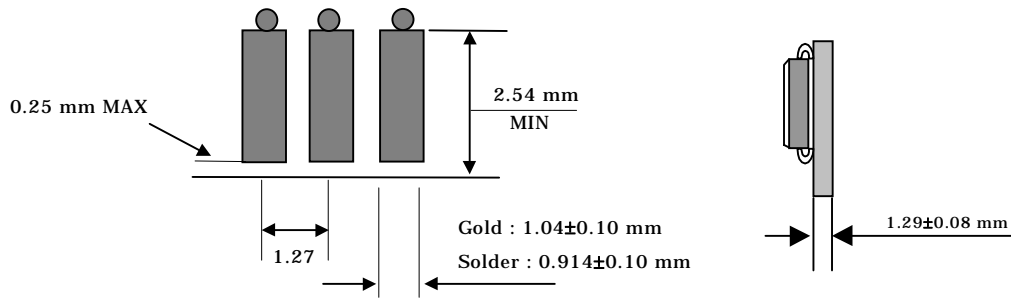
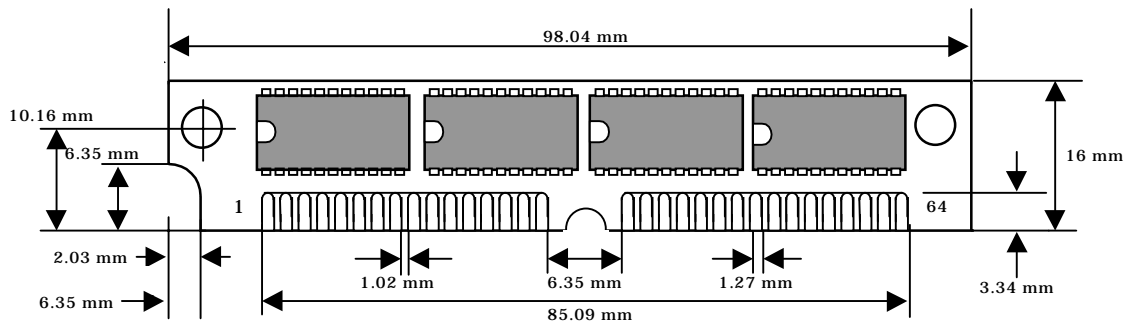
1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}$  (max.) is less than  $t_{LZ}$  (min.) both for a given device and from device to device.
5. Transition is measured  $\pm 200mV$  from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $/CE = V_{IL}$ .
7. Address valid prior to coincident with /CE transition low.

**TIMING WAVEFORM OF WRITE CYCLE (/OE=Clock )**





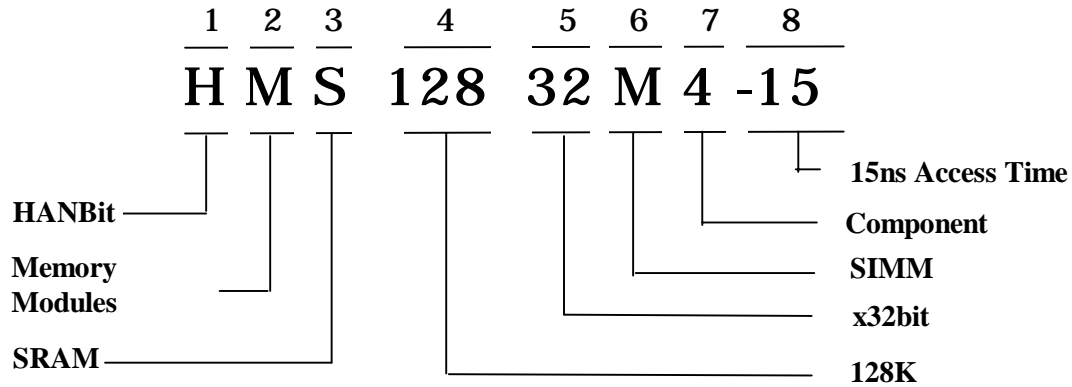
PACKAGING INFORMATION



(Solder & Gold Plating Lead)



**ORDERING INFORMATION**



**1. - Product Line Identifier**

HANBit ----- H

**2. - Memory Modules**

**3. - SRAM**

**4. - Depth : 128K**

**5. - Width : x 32bit**

**6. - Package Code**

SIMM ----- M

**7. - Number of Memory Components**

**8. - Access time**

10 ----- 10ns

12 ----- 12ns

15 ----- 15ns

17 ----- 17ns

20 ----- 20ns