DDR2 Unbuffered SDRAM MODULE

240pin Unbuffered Module based on 512Mb C-die

64/72-bit Non-ECC/ECC

DDR2 Unbuffered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
x64 Non ECC					
M378T3354CZ3-CE7/E6/D5/CC	256MB	32Mx64	32Mx16(K4T51163QC)*4	1	30mm
M378T3354CZ0-CE7/E6/D5/CC	256MB	32Mx64	32Mx16(K4T51163QC)*4	1	30mm
M378T6553CZ3-CE7/E6/D5/CC	512MB	64Mx64	64Mx8(K4T51083QC)*8	1	30mm
M378T6553CZ0-CE7/E6/D5/CC	512MB	64Mx64	64Mx8(K4T51083QC)*8	1	30mm
M378T2953CZ3-CE7/E6/D5/CC	1GB	128Mx64	64Mx8(K4T51083QC)*16	2	30mm
M378T2953CZ0-CE7/E6/D5/CC	1GB	128Mx64	64Mx8(K4T51083QC)*16	2	30mm
x72 ECC					
M391T6553CZ3-CE7/E6/D5/CC	512MB	64Mx72	64Mx8(K4T51083QC)*9	1	30mm
M391T6553CZ0-CE7/E6/D5/CC	512MB	64Mx72	64Mx8(K4T51083QC)*9	1	30mm
M391T2953CZ3-CE7/E6/D5/CC	1GB	128Mx72	64Mx8(K4T51083QC)*18	2	30mm
M391T2953CZ0-CE7/E6/D5/CC	1GB	128Mx72	64Mx8(K4T51083QC)*18	2	30mm

Note: “Z” of Part number(11th digit) stand for Lead-free products.
Note: “3” of Part number(12th digit) stand for Dummy Pad PCB products.

Features

- Performance range

	E7 (DDR2-800)	E6 (DDR2-667)	D5 (DDR2-533)	CC (DDR2-400)	Unit
Speed@CL3	400	400	400	400	Mbps
Speed@CL4	533	533	533	400	Mbps
Speed@CL5	800	667	533	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard 1.8V ± 0.1V Power Supply
- V_{DDQ} = 1.8V ± 0.1V
- 200 MHz f_{CK} for 400Mb/sec/pin, 267MHz f_{CK} for 533Mb/sec/pin, 333MHz f_{CK} for 667Mb/sec/pin, 400MHz f_{CK} for 800Mb/sec/pin
- 4 Banks
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- PASR(Partial Array Self Refresh)
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
  - support High Temperature Self-Refresh rate enable feature
- Package: 60ball FBGA - 64Mx8 , 84ball FBGA - 32Mx16
- All of Lead-free products are compliant for RoHS

Note: For detailed DDR2 SDRAM operation, please refer to Samsung’s Device operation & Timing diagram.

Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
64Mx8(512Mb) based Module	A0-A13	A0-A9	BA0-BA1	A10
32Mx16(512Mb) based Module	A0-A12	A0-A9	BA0-BA1	A10

x64 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS}$5	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0	35	V_{SS}	155	DM3	KEY				95	DQ42	215	DQ47
6	$\overline{DQS}$0	126	NC	36	$\overline{DQS}$3	156	NC	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK}$0	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	CK2
11	V_{SS}	131	DQ12	41	V_{SS}	161	NC	70	A10/AP	190	BA1	101	SA2	221	$\overline{CK}$2
12	DQ8	132	DQ13	42	NC	162	NC	71	BA0	191	V_{DDQ}	102	NC, TEST[2]	222	V_{SS}
13	DQ9	133	V_{SS}	43	NC	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6
14	V_{SS}	134	DM1	44	V_{SS}	164	NC	73	$\overline{WE}$	193	$\overline{S}$0	104	$\overline{DQS}$6	224	NC
15	$\overline{DQS}$1	135	NC	45	NC	165	NC	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	NC	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	CK1	47	V_{SS}	167	NC	76	$\overline{S}$1	196	A13[1]	107	DQ50	227	DQ55
18	NC	138	$\overline{CK}$1	48	NC	168	NC	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	NC	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DM4	113	$\overline{DQS}$7	233	NC
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{DQS}$4	203	NC	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS}$2	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	VDDSPD
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect, RFU = Reserved for Future Use
1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

x72 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS}$5	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0	35	V_{SS}	155	DM3	KEY				95	DQ42	215	DQ47
6	$\overline{DQS}$0	126	NC	36	$\overline{DQS}$3	156	NC	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK}$0	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	CK2
11	V_{SS}	131	DQ12	41	V_{SS}	161	CB4	70	A10/AP	190	BA1	101	SA2	221	$\overline{CK}$2
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V_{DDQ}	102	NC, TEST[2]	222	V_{SS}
13	DQ9	133	V_{SS}	43	CB1	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6
14	V_{SS}	134	DM1	44	V_{SS}	164	DM8	73	$\overline{WE}$	193	$\overline{S}$0	104	$\overline{DQS}$6	224	NC
15	$\overline{DQS}$1	135	NC	45	$\overline{DQS}$8	165	NC	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	DQS8	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	CK1	47	V_{SS}	167	CB6	76	$\overline{S}$1	196	A13	107	DQ50	227	DQ55
18	NC	138	$\overline{CK}$1	48	CB2	168	CB7	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	CB3	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DM4	113	$\overline{DQS}$7	233	NC
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{DQS}$4	203	NC	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS}$2	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	VDDSPD
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect, RFU = Reserved for Future Use
1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

Pin Description

Pin Name	Description	Pin Name	Description
A0-A13	DDR2 SDRAM address bus	CK0, CK1, CK2	DDR2 SDRAM clocks (positive line of differential pair)
BA0, BA1	DDR2 SDRAM bank select	$\overline{CK}$0, $\overline{CK}$1, $\overline{CK}$2	DDR2 SDRAM clocks (negative line of differential pair)
$\overline{RAS}$	DDR2 SDRAM row address strobe	SCL	I^2C serial bus clock for EEPROM
$\overline{CAS}$	DDR2 SDRAM column address strobe	SDA	I^2C serial bus data line for EEPROM
$\overline{WE}$	DDR2 SDRAM wirte enable	SA0-SA2	I^2C serial address select for EEPROM
$\overline{S}$0, $\overline{S}$1	DIMM Rank Select Lines	V_{DD}*	DDR2 SDRAM core power supply
CKE0,CKE1	DDR2 SDRAM clock enable lines	V_{DDQ}*	DDR2 SDRAM I/O Driver power supply
ODT0, ODT1	On-die termination control lines	V_{REF}	DDR2 SDRAM I/O reference supply
DQ0 - DQ63	DIMM memory data bus	V_{SS}	Power supply return (ground)
CB0 - CB7	DIMM ECC check bits	V_{DD}SPD	Serial EEPROM positive power supply
DQS0 - DQS8	DDR2 SDRAM data strobes	NC	Spare Pins(no connect)
DM(0-8)	DDR2 SDRAM data masks	RESET	Not used on UDIMM
$\overline{DQS}$0-$\overline{DQS}$8	DDR2 SDRAM differential data strobes	TEST	Used by memory bus analysis tools (unused on memory DIMMs)

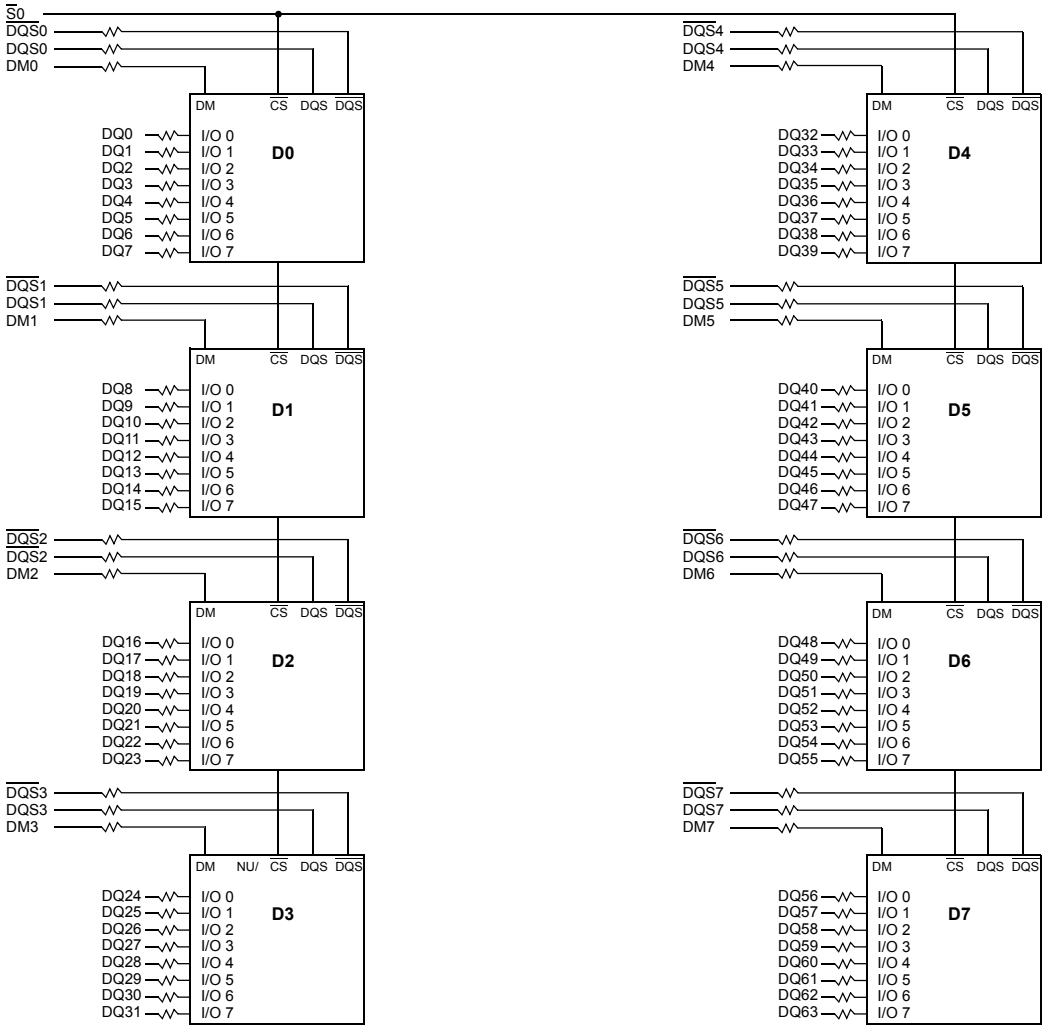
* The VDD and VDDQ pins are tied to the single power-plane on PCB.

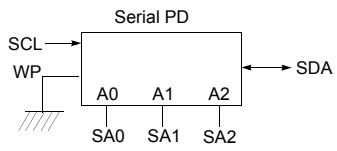
Input/Output Functional Description

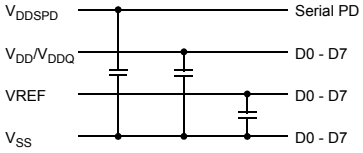
Symbol	Type	Function
CK0-CK2 CK0-CK2	Input	CK and CK are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is reference to the crossing of CK and CK (Both directions of crossing)
CKE0-CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode
S0-S1	Input	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks
RAS, CAS, WE	Input	RAS, CAS, and WE (ALONG WITH CS) define the command being entered.
ODT0-ODT1	Input	When high, termination resistance is enabled for all DQ, DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V_{REF}	Supply	Reference voltage for SSTL 18 inputs.
V_{DDQ}	Supply	Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0-BA1	Input	Selects which SDRAM BANK of four is activated.
A0-A13	Input	During a Bank Activate command cycle, Address input defines the row address (RA0-RA13) During a Read or Write command cycle, Address input defines the colum address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1. If AP is low, BA0, BA1are used to define which bank to precharge.
DQ0-DQ63 CB0-CB7	In/Out	Data and Check Bit Input/Output pins.
DM0-DM8	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply	Power and ground for DDR2 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0-DQS8 DQS0-DQS8	In/Out	Data strobe for input and output data. For Rawcards using x16 orginized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM
SA0-SA2	Input	These signals and tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EERPOM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup onthe system board.
V_{DD} SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.

Functional Block Diagram: 512MB, 64Mx64 Module(Populated as 1 rank of x8 DDR2 SDRAMs)

M378T6553CZ3 / M378T6553CZ0







* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	2 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

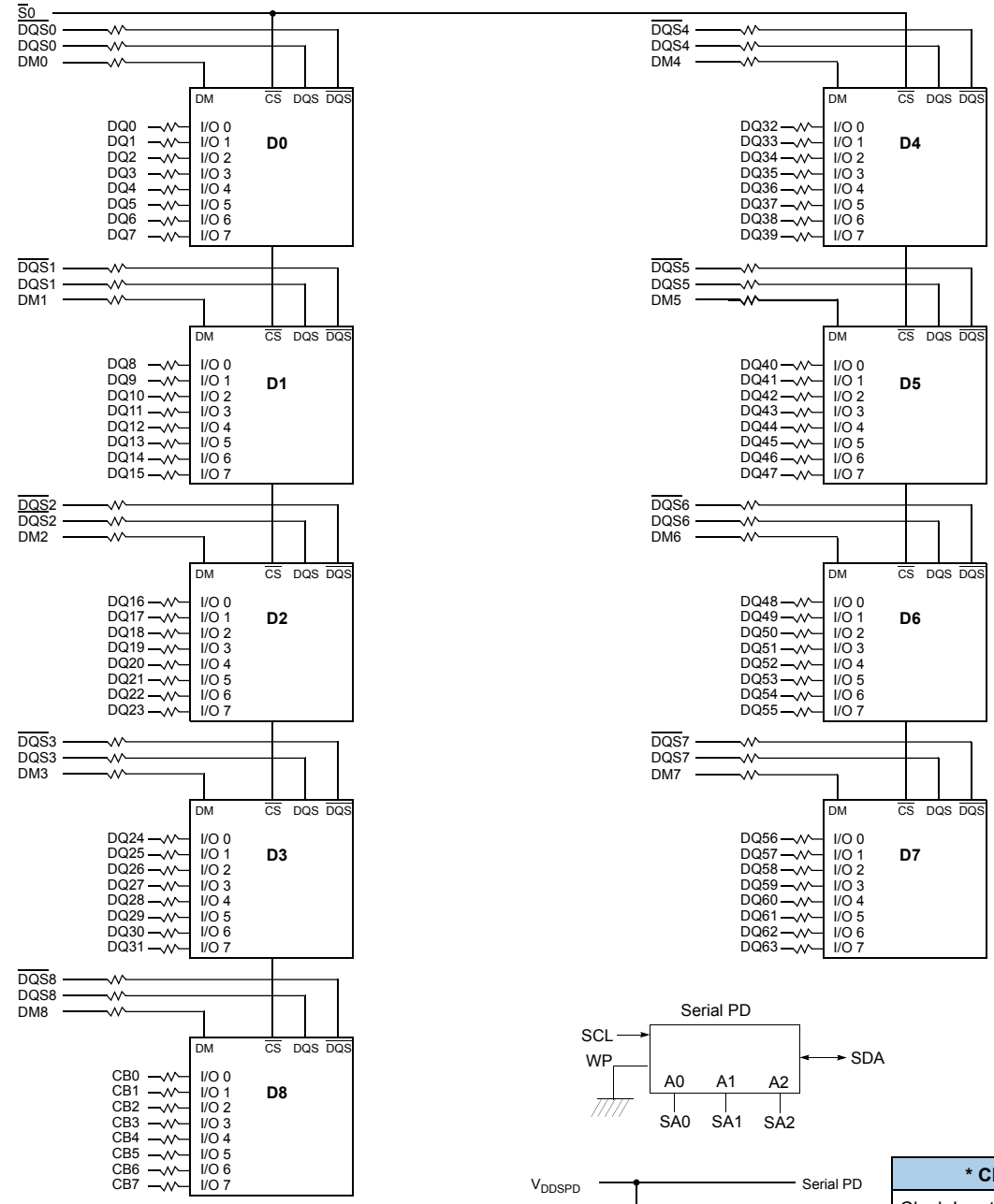
*Wire per Clock Loading Table/Wiring Diagrams

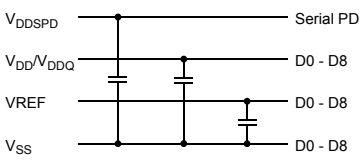
BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D7
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
RAS → RAS : DDR2 SDRAMs D0 - D7
CAS → CAS : DDR2 SDRAMs D0 - D7
CKE0 → CKE : DDR2 SDRAMs D0 - D7
WE → WE : DDR2 SDRAMs D0 - D7
ODT0 → ODT : DDR2 SDRAMs D0 - D7

Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ±5%.
2. BAx, Ax, RAS, CAS, WE resistors : 5.1 Ohms ±5%.

Functional Block Diagram: 512MB, 64Mx72 ECC Module(Populated as 1 rank of x8 DDR2 SDRAMs)

M391T6553CZ3 / M391T6553CZ0





* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	3 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

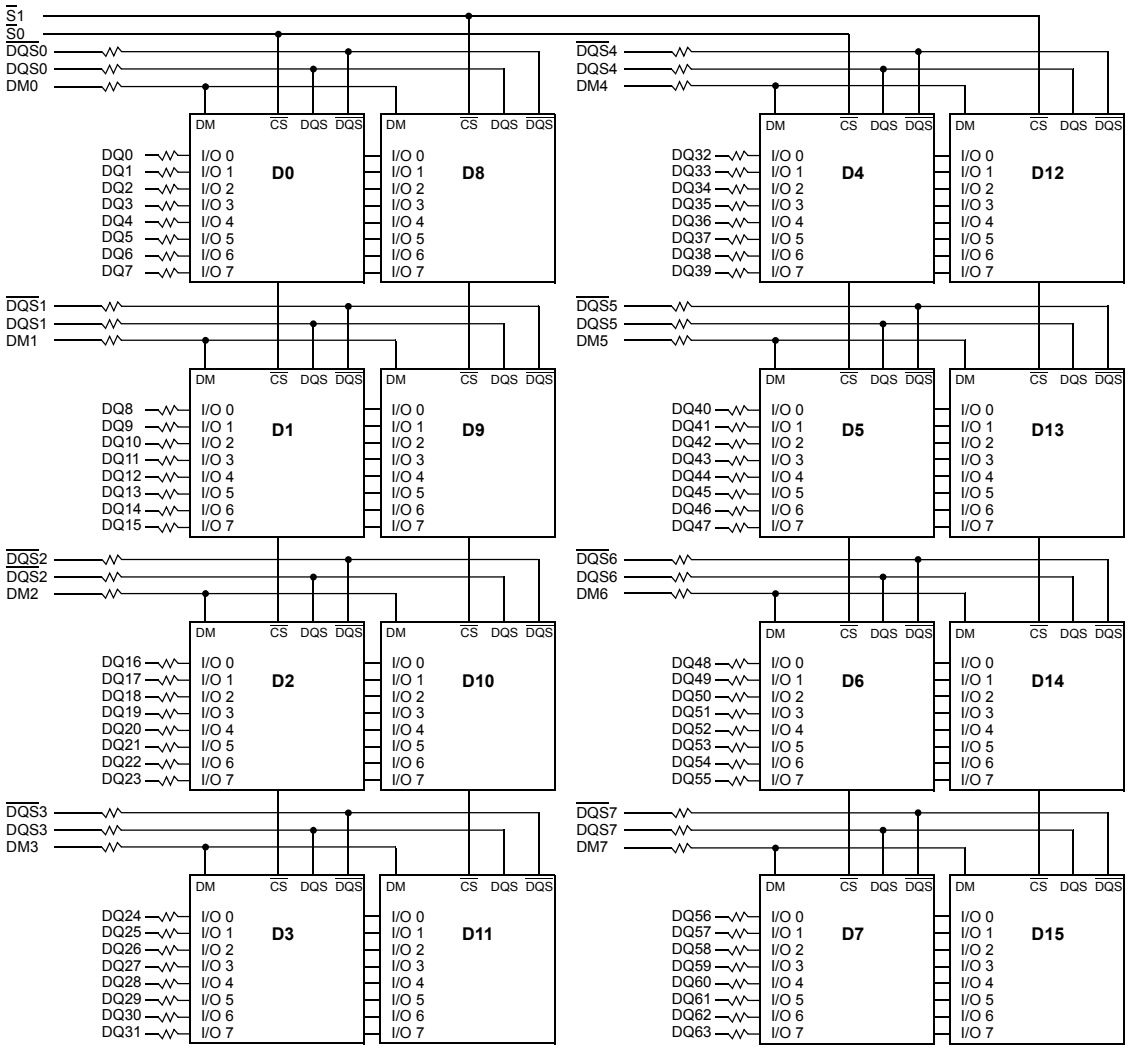
*Wire per Clock Loading Table/Wiring Diagrams

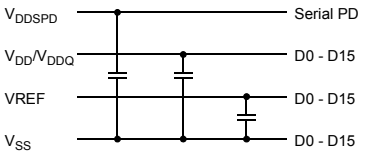
BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D8
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D8
RAS → RAS : DDR2 SDRAMs D0 - D8
CAS → CAS : DDR2 SDRAMs D0 - D8
CKE0 → CKE : DDR2 SDRAMs D0 - D8
WE → WE : DDR2 SDRAMs D0 - D8
ODT0 → ODT : DDR2 SDRAMs D0 - D8

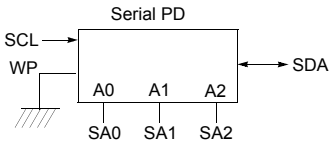
Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 5.1 Ohms ± 5%.

Functional Block Diagram: 1GB, 128Mx64 Module(Populated as 2 ranks of x8 DDR2 SDRAMs)

M378T2953CZ3 / M378T2953CZ0







BA0 - BA1	BA0-BA1 : DDR2 SDRAMs D0 - D15
A0 - A13	A0-A13 : DDR2 SDRAMs D0 - D15
CKE0	CKE : DDR2 SDRAMs D0 - D7
CKE1	CKE : DDR2 SDRAMs D8 - D15
$\overline{RAS}$	$\overline{RAS}$: DDR2 SDRAMs D0 - D15
$\overline{CAS}$	$\overline{CAS}$: DDR2 SDRAMs D0 - D15
$\overline{WE}$	$\overline{WE}$: DDR2 SDRAMs D0 - D15
ODT0	ODT : DDR2 SDRAMs D0 - D7
ODT1	ODT : DDR2 SDRAMs D8 - D15

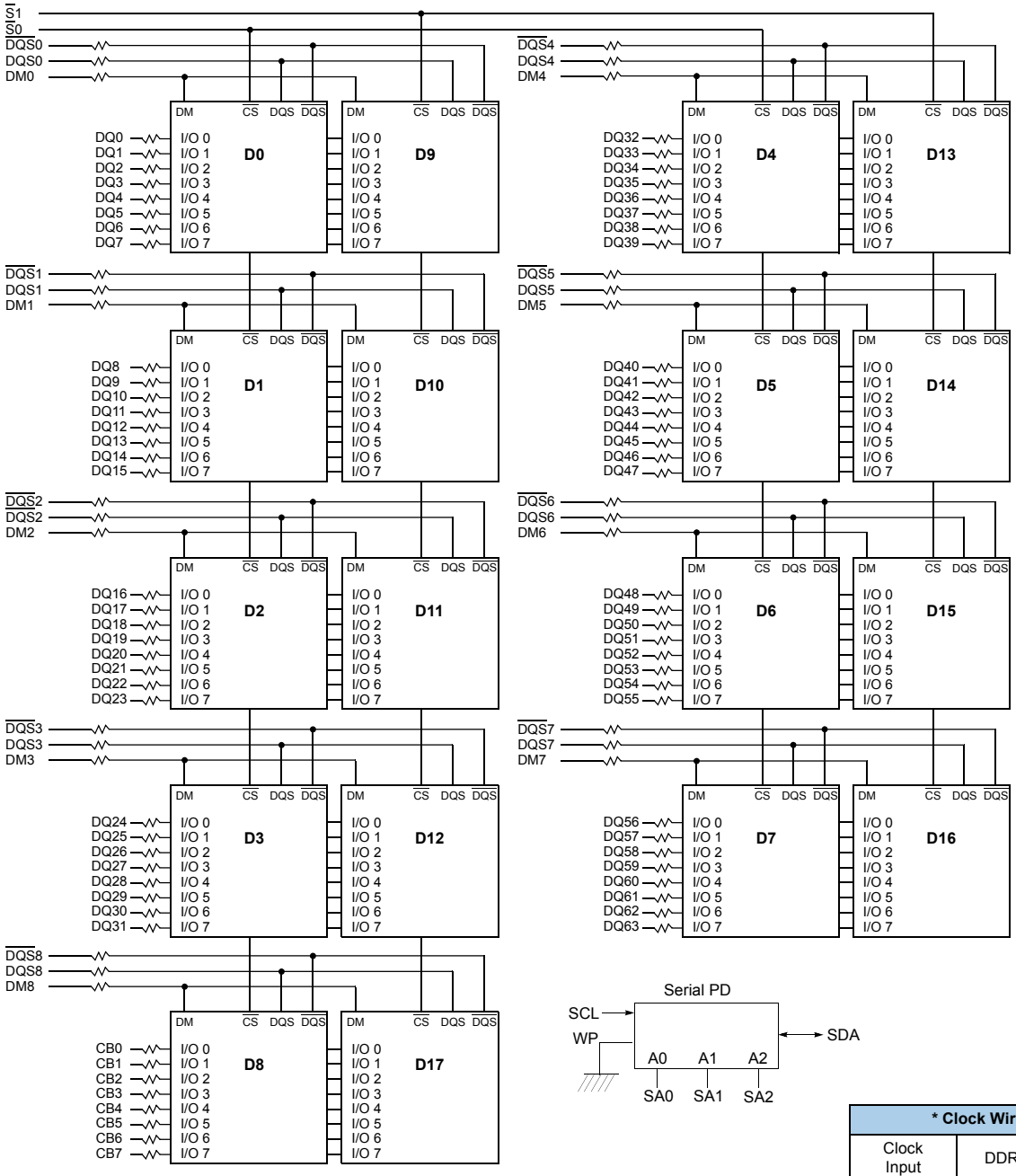
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	4 DDR2 SDRAMs
*CK1/$\overline{CK1}$	6 DDR2 SDRAMs
*CK2/$\overline{CK2}$	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

Notes :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3 Ohms ± 5%.

Functional Block Diagram: 1GB, 128Mx72 ECC Module(Populated as 2 ranks of x8 DDR2 SDRAMs)

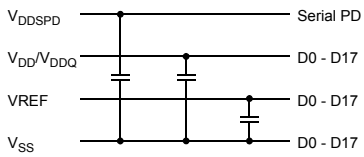
M391T2953CZ3 / M391T2953CZ0



* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	6 DDR2 SDRAMs
*CK1/$\overline{CK1}$	6 DDR2 SDRAMs
*CK2/$\overline{CK2}$	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

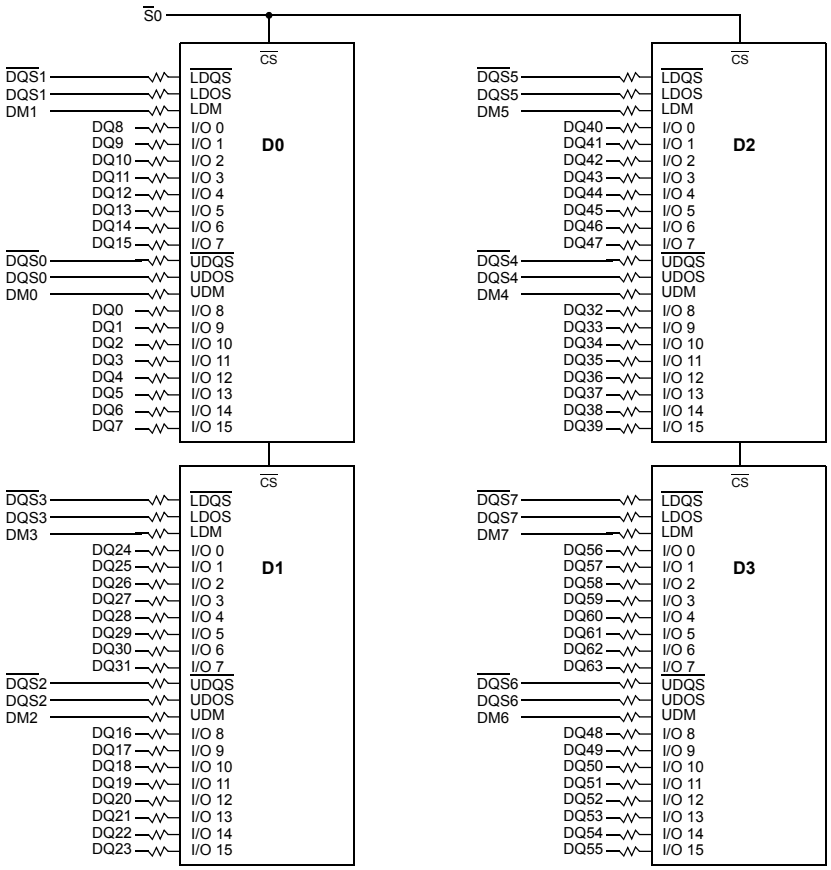
BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D17
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D17
CKE0 → CKE : DDR2 SDRAMs D0 - D8
CKE1 → CKE : DDR2 SDRAMs D9 - D17
$\overline{RAS}$ → $\overline{RAS}$: DDR2 SDRAMs D0 - D17
$\overline{CAS}$ → $\overline{CAS}$: DDR2 SDRAMs D0 - D17
$\overline{WE}$ → $\overline{WE}$: DDR2 SDRAMs D0 - D17
ODT0 → ODT : DDR2 SDRAMs D0 - D8
ODT1 → ODT : DDR2 SDRAMs D9 - D17

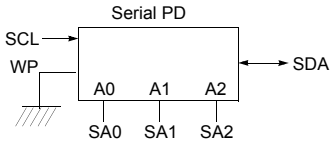


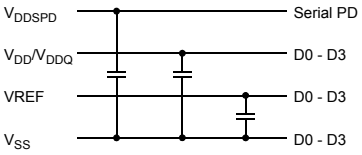
Notes :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3 Ohms ± 5%.

Functional Block Diagram: 256MB, 32Mx64 Module(Populated as 1 rank of x16 DDR2 SDRAMs)

M378T3354CZ3 / M378T3354CZ0







* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	NC
*CK1/CK1	2 DDR2 SDRAMs
*CK2/CK2	2 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D3
A0 - A12 → A0-A12 : DDR2 SDRAMs D0 - D3
CKE0 → CKE : DDR2 SDRAMs D0 - D3
RAS → RAS : DDR2 SDRAMs D0 - D3
CAS → CAS : DDR2 SDRAMs D0 - D3
WE → WE : DDR2 SDRAMs D0 - D3
ODT0 → ODT : DDR2 SDRAMs D0 - D3

Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
4. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms ± 5%.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	- 1.0 V ~ 2.3 V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Note : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature	0 to 95	°C	1, 2, 3

Note :
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (DC)	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL} (DC)	DC input logic low	- 0.3	V_{REF} - 0.125	V	

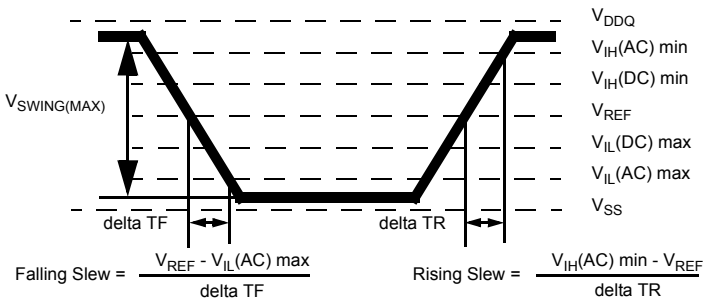
Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IH} (AC)	AC input logic high	V_{REF} + 0.250	-	V_{REF} + 0.200		V	
V_{IL} (AC)	AC input logic low	-	V_{REF} - 0.250		V_{REF} - 0.200	V	

AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:
1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.



< AC Input Test Signal Waveform >

IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions		Units	Notes
IDD0	**Operating one bank active-precharge current**; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RAS} = $t_{RASmin(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC\ (IDD)}$, t_{RAS} = $t_{RASmin(IDD)}$, t_{RCD} = $t_{RCD(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2N	**Precharge standby current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD3P	**Active power-down current**; All banks open; t_{CK} = $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA	
		Slow PDN Exit MRS(12) = 1mA	mA	
IDD3N	**Active standby current**; All banks open; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RAS-max(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst auto refresh current**; t_{CK} = $t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current**; CK and CK\ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA	
		Low Power	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RRD} = $t_{RRD(IDD)}$, t_{FAW} = $t_{FAW(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		mA	

Operating Current Table(1-1) (T_A=0°C, VDD= 1.9V)

M378T6553CZ3 / M378T6553CZ0 : 512MB(64Mx8 *8) Module

Symbol	E7(800@CL=5)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Unit	Notes
IDD0	TBD	680	640	640	mA	
IDD1	TBD	800	760	760	mA	
IDD2P	TBD	64	64	64	mA	
IDD2Q	TBD	280	240	240	mA	
IDD2N	TBD	320	280	280	mA	
IDD3P-F	TBD	240	240	240	mA	
IDD3P-S	TBD	96	96	96	mA	
IDD3N	TBD	440	400	400	mA	
IDD4W	TBD	1,120	960	880	mA	
IDD4R	TBD	1,160	1,000	880	mA	
IDD5B	TBD	1,200	1,120	1,120	mA	
IDD6	TBD	64	64	64	mA	
IDD7	TBD	1,760	1,760	1,760	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

M378T2953CZ3 / M378T2953CZ0 : 1GB(64Mx8 *16) Module

Symbol	E7(800@CL=5)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Unit	Notes
IDD0	TBD	1,000	920	920	mA	
IDD1	TBD	1,120	1,040	1,040	mA	
IDD2P	TBD	128	128	128	mA	
IDD2Q	TBD	560	480	480	mA	
IDD2N	TBD	640	560	560	mA	
IDD3P-F	TBD	480	480	480	mA	
IDD3P-S	TBD	192	192	192	mA	
IDD3N	TBD	760	680	680	mA	
IDD4W	TBD	1,440	1,240	1,160	mA	
IDD4R	TBD	1,480	1,280	1,160	mA	
IDD5B	TBD	1,520	1,400	1,400	mA	
IDD6	TBD	128	128	128	mA	
IDD7	TBD	2,080	2,040	2,040	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

Operating Current Table(1-2) (T_A=0°C, VDD= 1.9V)

M378T3354CZ3 / M378T3354CZ0 : 256MB(32Mx16 *4) Module

Symbol	E7(800@CL=5)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Unit	Notes
IDD0	TBD	400	380	380	mA	
IDD1	TBD	460	440	440	mA	
IDD2P	TBD	32	32	32	mA	
IDD2Q	TBD	140	120	120	mA	
IDD2N	TBD	160	140	140	mA	
IDD3P-F	TBD	120	120	120	mA	
IDD3P-S	TBD	48	48	48	mA	
IDD3N	TBD	220	200	200	mA	
IDD4W	TBD	700	620	540	mA	
IDD4R	TBD	720	640	560	mA	
IDD5B	TBD	600	560	560	mA	
IDD6	TBD	32	32	32	mA	
IDD7	TBD	1,200	1,200	1,200	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

M391T6553CZ3 / M391T6553CZ0 : 512MB(64Mx8 *9) ECC Module

Symbol	E7(800@CL=5)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Unit	Notes
IDD0	TBD	765	720	720	mA	
IDD1	TBD	900	855	855	mA	
IDD2P	TBD	72	72	72	mA	
IDD2Q	TBD	315	270	270	mA	
IDD2N	TBD	360	315	315	mA	
IDD3P-F	TBD	270	270	270	mA	
IDD3P-S	TBD	108	108	108	mA	
IDD3N	TBD	495	450	450	mA	
IDD4W	TBD	1,260	1,080	990	mA	
IDD4R	TBD	1,305	1,125	990	mA	
IDD5B	TBD	1,350	1,260	1,260	mA	
IDD6	TBD	72	72	72	mA	
IDD7	TBD	1,980	1,980	1,980	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

Operating Current Table(1-3) (T_A=0°C, VDD= 1.9V)

M391T2953CZ3 / M391T2953CZ0 : 1GB(64Mx8 *18) ECC Module

Symbol	E7(800@CL=5)	E6(667@CL=5)	D5(533@CL=4)	CC(400@CL=3)	Unit	Notes
IDD0	TBD	1,125	1,035	1,035	mA	
IDD1	TBD	1,260	1,170	1,170	mA	
IDD2P	TBD	144	144	144	mA	
IDD2Q	TBD	630	540	540	mA	
IDD2N	TBD	720	630	630	mA	
IDD3P-F	TBD	540	540	540	mA	
IDD3P-S	TBD	216	216	216	mA	
IDD3N	TBD	855	765	765	mA	
IDD4W	TBD	1,620	1,395	1,305	mA	
IDD4R	TBD	1,665	1,440	1,305	mA	
IDD5B	TBD	1,710	1,575	1,575	mA	
IDD6	TBD	144	144	144	mA	
IDD7	TBD	2,340	2,295	2,295	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

Input/Output Capacitance(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A=25°C)

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Non-ECC		M378T6553CZ3 M378T6553CZ0		M378T2953CZ3 M378T2953CZ0		M378T3354CZ3 M378T3354CZ0		
Input capacitance, CK and $\overline{CK}$	CCK0	-	24	-	26	-	22	pF
	CCK1	-	25	-	28	-	24	
	CCK2	-	25		28		24	
Input capacitance, CKE and $\overline{CS}$	CI1	-	42	-	42	-	34	
Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI2	-	42	-	42	-	34	
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO(400/533)	-	6	-	10	-	6	
	CIO(667/800)	-	5.5	-	9	-	5.5	
ECC	Symbol	M391T6553CZ3 M391T6553CZ0		M391T2953CZ3 M391T2953CZ0				Units
Input capacitance, CK and $\overline{CK}$	CCK0	-	25	-	28			pF
	CCK1	-	25	-	28			
	CCK2		25		28			
Input capacitance, CKE and $\overline{CS}$	CI_1	-	44	-	44			
Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI_2	-	44	-	44			
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO(400/533)	-	6	-	10			
	CIO(667/800)	-	5.5	-	9			

Note: DM is internally loaded to match DQ and DQS identically.

Electrical Characteristics & AC Timing for DDR2-800/667/533/400

(0 °C ≤ T_{OPER} ≤ 95 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR2-800(E7)		DDR2-667(E6)		DDR2-533(D5)		DDR2-400(CC)		Units
Bin(CL - tRCD - tRP)	5 - 5 - 5		5 - 5 - 5		4 - 4 - 4		3 - 3 - 3		
Parameter	min	max	min	max	min	max	min	max	
tCK, CL=3	5	8	5	8	5	8	5	8	ns
tCK, CL=4	3.75	8	3.75	8	3.75	8	5	8	ns
tCK, CL=5	2.5	8	3	8	3.75	8	-	-	ns
tRCD	12.5	-	15	-	15	-	15	-	ns
tRP	12.5	-	15	-	15	-	15	-	ns
tRC	51.5	-	54	-	55	-	55	-	ns
tRAS	39	70000	39	70000	40	70000	40	70000	ns

Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

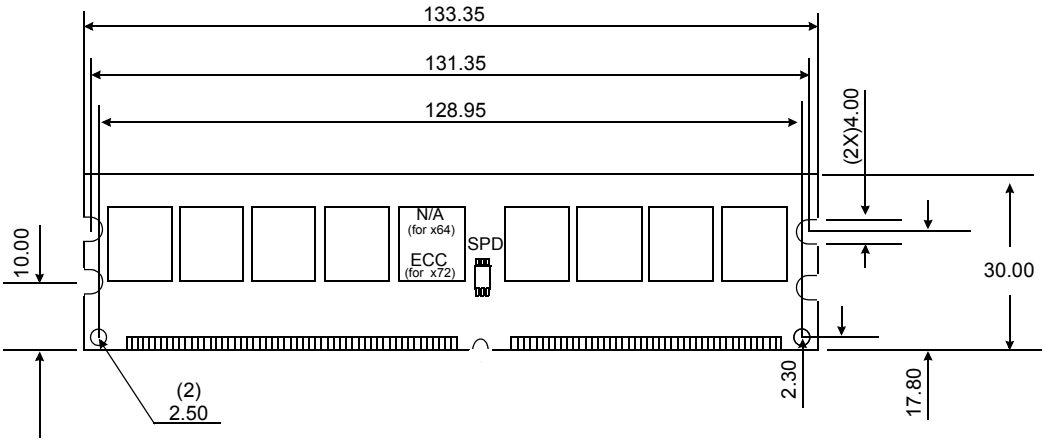
Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units	Note
		min	max	min	max	min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	- 400	400	-450	+450	-500	+500	-600	+600	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	- 350	350	-400	+400	-450	+450	-500	+500	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	x	min(tCL,tCH)	x	min(tCL,tCH)	x	min(tCL,tCH)	x	ps	
Clock cycle time, CL=x	tCK	2500	8000	3000	8000	3750	8000	5000	8000	ps	
DQ and DM input hold time	tDH(base)	125	x	175	x	225	x	275	x	ps	
DQ and DM input setup time	tDS(base)	50	x	100	x	100	x	150	x	ps	
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	x	tAC max	x	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC min	tAC max	2*tAC min	tAC max	2* tACmin	tAC max	2* tACmin	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	x	300	x	350	ps	
DQ hold skew factor	tQHS	x	300	x	340	x	400	x	450	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	tHP - tQHS	x	ps	
First DQS latching transition to associated clock edge	tDQSS	- 0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK	
DQS input high pulse width	tDQSH	0.35	x	0.35	x	0.35	x	0.35	x	tCK	
DQS input low pulse width	tDQSL	0.35	x	0.35	x	0.35	x	0.35	x	tCK	

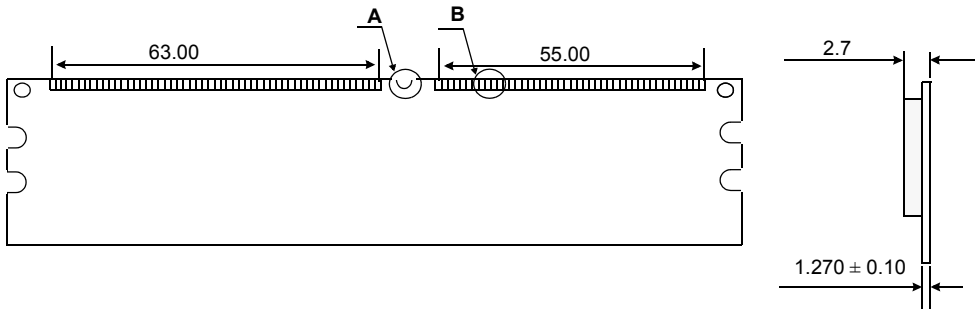
Parameter	Symbol	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Units	Note
		min	max	min	max	min	max	min	max		
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	2	x	2	x	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	x	0.35	x	0.35	x	0.35	x	tCK	
Address and control input hold time	tIH(base)	250	x	275	x	375	x	475	x	ps	
Address and control input setup time	tIS(base)	175	x	200	x	250	x	350	x	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	7.5	x	7.5	x	ns	
Active to active command period for 2KB page size products	tRRD	10	x	10	x	10	x	10	x	ns	
Four Activate Window for 1KB page size products	tFAW	35		37.5		37.5		37.5		ns	
Four Activate Window for 2KB page size products	tFAW	45		50		50		50		ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	x	2		2		2		tCK	
Write recovery time	tWR	15	x	15	x	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+tRP	x	WR+tRP	x	WR+tRP	x	tCK	
Internal write to read command delay	tWTR	7.5		7.5	x	7.5	x	10	x	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	x	200		200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	2	x	2	x	tCK	
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL		7 - AL		6 - AL		6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		3		3		tCK	
ODT turn-on delay	tAOND	2	2	2	2	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(max) +0.7	tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +1	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+ 2	2tCK + tAC(max) +1	tAC(min)+ 2	2tCK+tA C(max)+1	tAC(min)+ 2	2tCK+tA C(max)+ 1	tAC(min)+ 2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+ 2	2.5tCK + tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	ns	
ODT to power down entry latency	tANPD	3		3		3		3		tCK	
ODT power down exit latency	tAXPD	8		8		8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns	

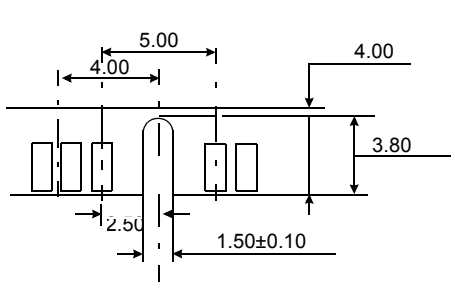
Physical Dimensions: 64Mbx8 based 64Mx64/x72 Module(1 Rank)

M378T6553CZ3 / M378T6553CZ0
M391T6553CZ3 / M391T6553CZ0

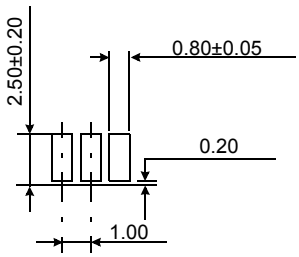
Units : Millimeters



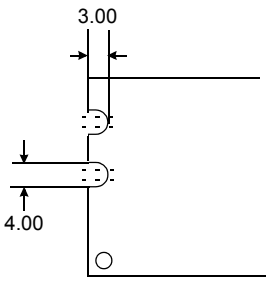




Detail A



Detail B

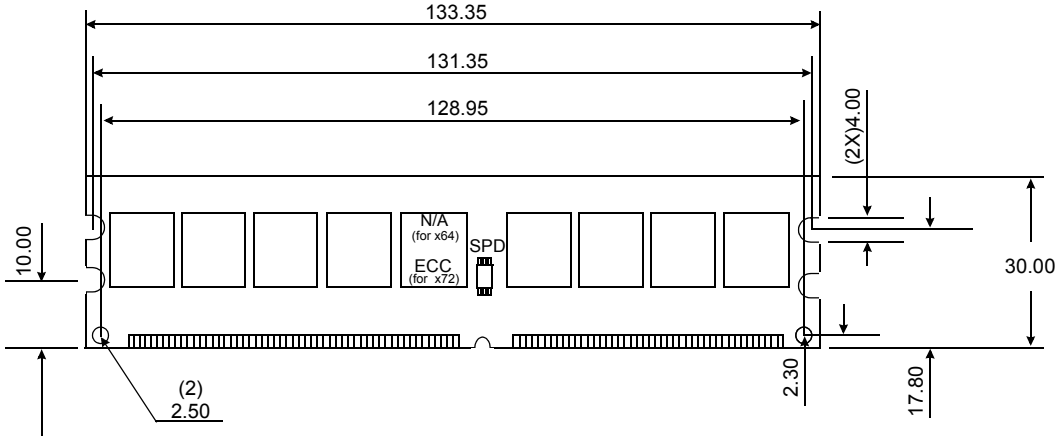


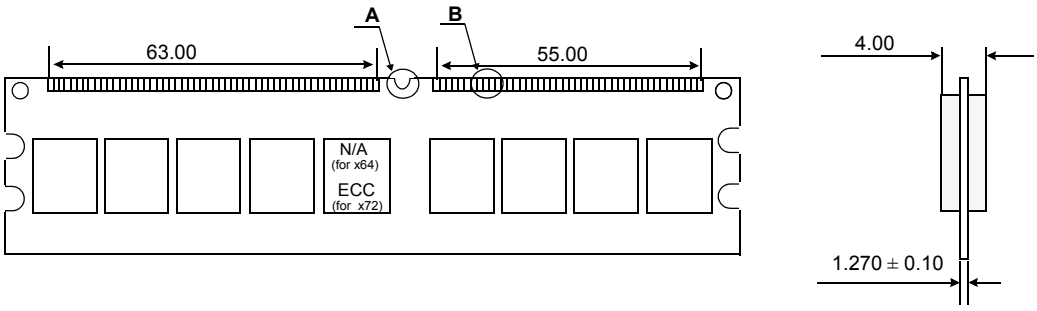
The used device is 64M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QC

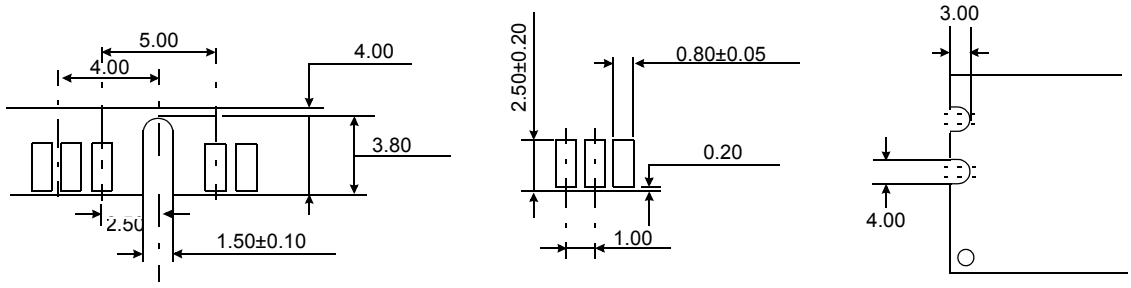
Physical Dimensions: 64Mbx8 based 128Mx64/x72 Module(2 Ranks)

M378T2953CZ3 / M378T2953CZ0
M391T2953CZ3 / M391T2953CZ0

Units : Millimeters





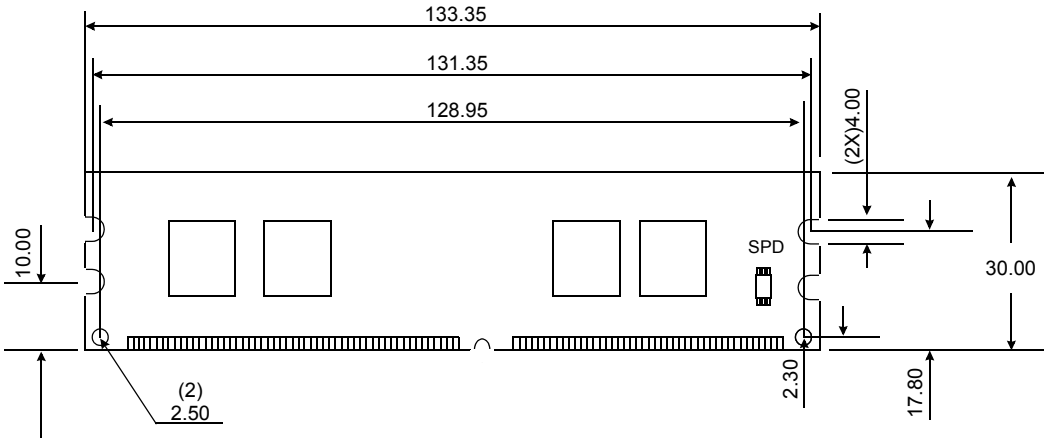


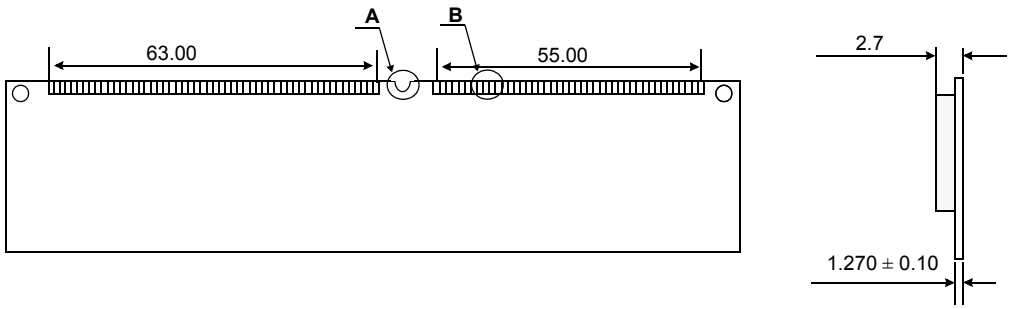
Detail A **Detail B**

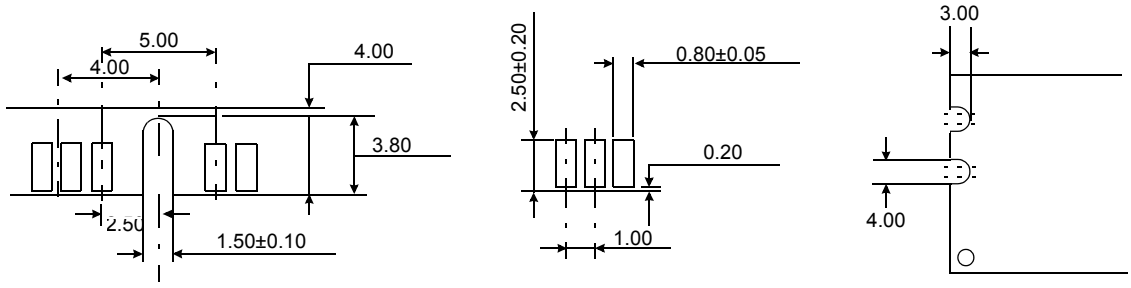
The used device is 64M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QC

Physical Dimensions: 32Mbx16 based 32Mx64 Module(1 Rank)
M378T3354CZ3 / M378T3354CZ0

Units : Millimeters







Detail A **Detail B**

The used device is 32M x16 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51163QC

Revision History

Revision 1.0 (Feb. 2005)

- Initial Release

Revision 1.1 (Mar. 2005)

- Changed the IDD0/IDD3N/IDD3P current values.

Revision 1.2 (Aug. 2005)

- Revised the IDD Current Values.