

#### Features

- High speed access times  
Com'l: 10, 12 and 15 ns  
Ind'l: 12 and 15 ns
- Low power operation (typical)
  - PDM41028SA  
Active: 400 mW  
Standby: 150 mW
  - PDM41028LA  
Active: 350 mW  
Standby: 100 mW
- Single +5V ( $\pm 10\%$ ) power supply
- TTL-compatible inputs and outputs
- Packages
  - Plastic SOJ (300 mil) - TSO
  - Plastic SOJ (400 mil) - SO

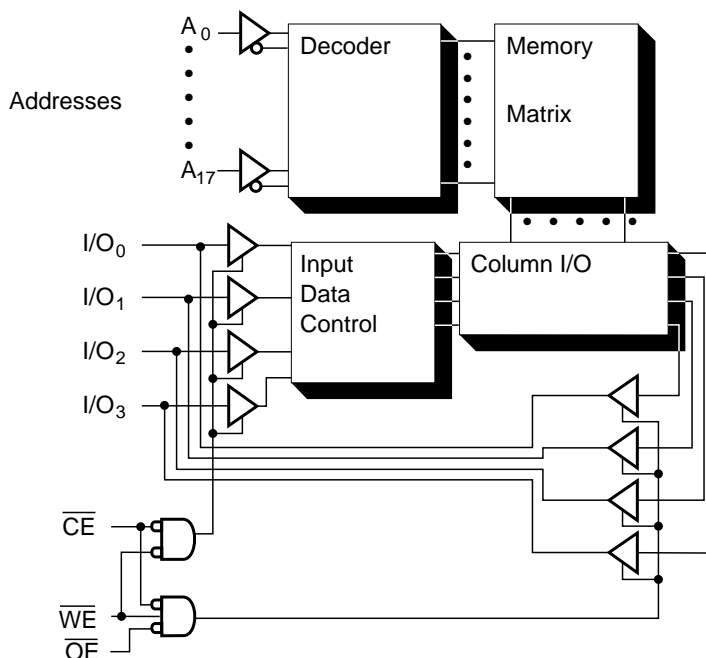
#### Description

The PDM41028 is a high-performance CMOS static RAM organized as 262,144 x 4 bits. Writing to this device is accomplished when the write enable ( $\overline{WE}$ ) and the chip enable ( $\overline{CE}$ ) inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  and  $\overline{OE}$  are both LOW.

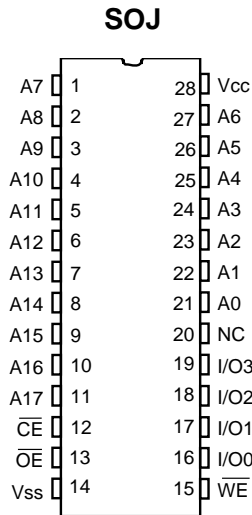
The PDM41028 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41028 comes in two versions, the standard power version PDM41028SA and a low power version the PDM41028LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41028 is available in a 28-pin 300-mil SOJ, and a 28-pin 400-mil SOJ for surface mount applications.

#### Functional Block Diagram



Pin Configuration



Pin Description

Name	Description
A17-A0	Address Inputs
I/O3-I/O0	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input
WE	Write Enable Input
$\overline{CE}$	Chip Enable Input
NC	No Connect
V <sub>CC</sub>	Power (+5V)
V <sub>SS</sub>	Ground

Truth Table<sup>(1)</sup>

$\overline{OE}$	WE	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D <sub>OUT</sub>	Read
X	L	L	D <sub>IN</sub>	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = DON'T CARE

Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Com'l.	Ind.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to V <sub>SS</sub>	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA
T <sub>j</sub>	Maximum Junction Temperature <sup>(2)</sup>	125	145	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form:  $T_j = T_a + P * \theta_{ja}$  where T<sub>a</sub> is the ambient temperature, P is average operating power and  $\theta_{ja}$  the thermal resistance of the package. For this product, use the following  $\theta_{ja}$  values:

SOJ: 76° C/W  
 TSOP: 100° C/W

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

### DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41028SA		PDM41028LA		Unit
				Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	Com'l/ Ind.	-5	5	-5	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = MAX., CE = V <sub>IH</sub> , V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>	Com'l/ Ind.	-5	5	-5	5	μA
V <sub>IL</sub>	Input Low Voltage			-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	V
V <sub>IH</sub>	Input High Voltage			2.2	6.0	2.2	6.0	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = Min. I <sub>OL</sub> = 10 mA, V <sub>CC</sub> = Min.		—	0.4	—	0.4	V
				—	0.5	—	0.5	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.		2.4	—	2.4	—	V

NOTE: 1. V<sub>IL</sub>(min) = -3.0V for pulse width less than 20 ns

### Power Supply Characteristics

Symbol	Parameter	Power	-10		-12		-15		Unit
			Com'l.	Com'l	Ind.	Com'l	Ind.		
I <sub>CC</sub>	Operating Current CE = V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	SA	250	230	240	185	195	mA	
		LA	230	210	220	165	175	mA	
I <sub>SB</sub>	Standby Current CE = V <sub>IH</sub> , f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max.	SA	80	70	70	55	55	mA	
		LA	75	65	65	50	50	mA	
I <sub>SB1</sub>	Full Standby Current CE ≥ V <sub>HC</sub> , f = 0 V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or ≤ 0.2V	SA	20	15	25	10	15	mA	
		LA	10	10	10	5	10	mA	

SHADED AREA = PRELIMINARY DATA

NOTES: All values are maximum guaranteed values.

$$V_{LC} \leq 0.2V, V_{HC} \geq V_{CC} - 0.2V$$

**Capacitance<sup>(1)</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Symbol	Parameter	Max.	Unit
$C_{IN}$	Input Capacitance	8	pF
$C_{OUT}$	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

**AC Test Conditions**

Input pulse levels	$V_{SS}$ to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

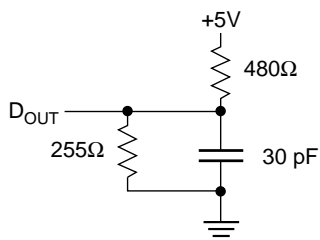


Figure 1. Output Load Equivalent

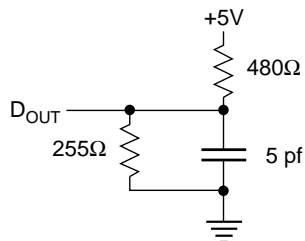
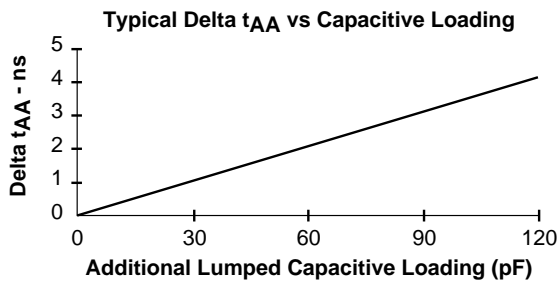
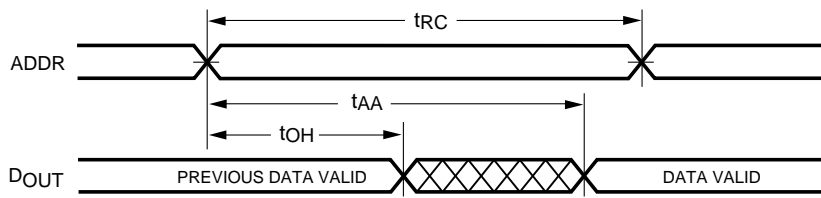


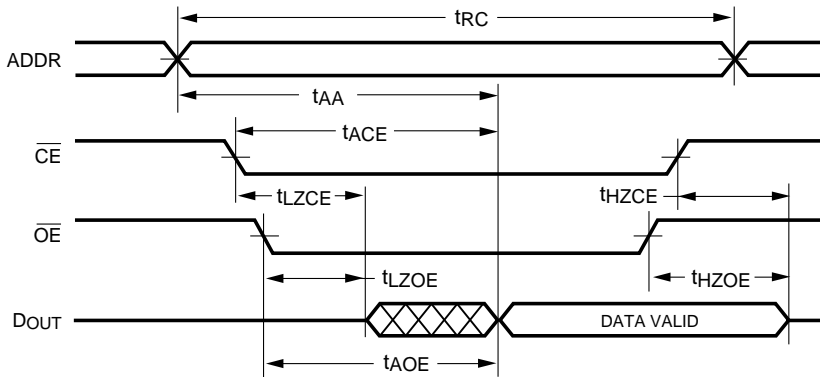
Figure 2. Output Load Equivalent  
(for  $t_{LZCE}$ ,  $t_{HZCE}$ ,  $t_{LZWE}$ ,  $t_{HZWE}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ )



Read Cycle No. 1<sup>(4, 5)</sup>



Read Cycle No. 2<sup>(2, 4, 6)</sup>

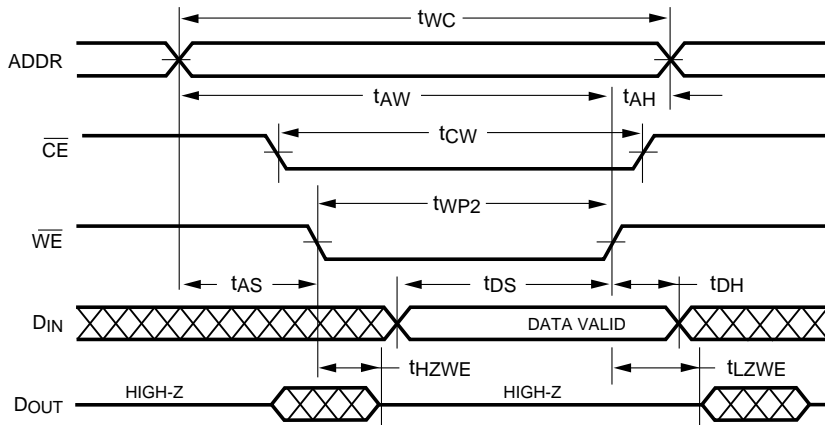


AC Electrical Characteristics

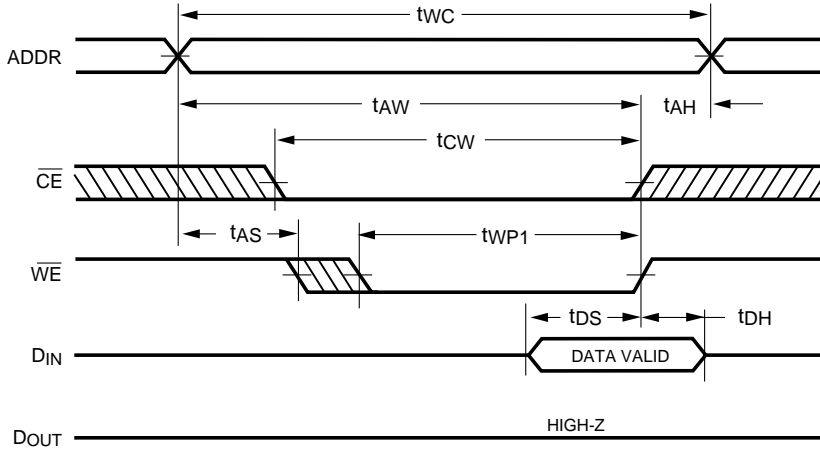
Description		-10 <sup>(7)</sup>		-12 <sup>(7)</sup>		-15		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t <sub>RC</sub>	10		12		15		ns
Address access time	t <sub>AA</sub>		10		12		15	ns
Chip enable access time	t <sub>ACE</sub>		10		12		15	ns
Output hold from address change	t <sub>OH</sub>	3		3		3		ns
Chip enable to output in low Z <sup>(1,3)</sup>	t <sub>LZCE</sub>	5		5		5		ns
Chip disable to output in high Z <sup>(1,2,3)</sup>	t <sub>HZCE</sub>		6		6		7	ns
Chip enable to power up time <sup>(3)</sup>	t <sub>PU</sub>	0		0		0		ns
Chip disable to power down time <sup>(3)</sup>	t <sub>PD</sub>		10		12		15	ns
Output enable access time	t <sub>AOE</sub>		6		6		6	ns
Output enable to output in low Z <sup>(1,3)</sup>	t <sub>LZOE</sub>	0		0		0		ns
Output disable to output in high Z <sup>(1,3)</sup>	t <sub>HZOE</sub>		6		6		6	ns

SHADED AREA = PRELIMINARY DATA  
 Notes referenced are after Data Retention Table.

**Write Cycle No. 1 (Write Enable Controlled)**

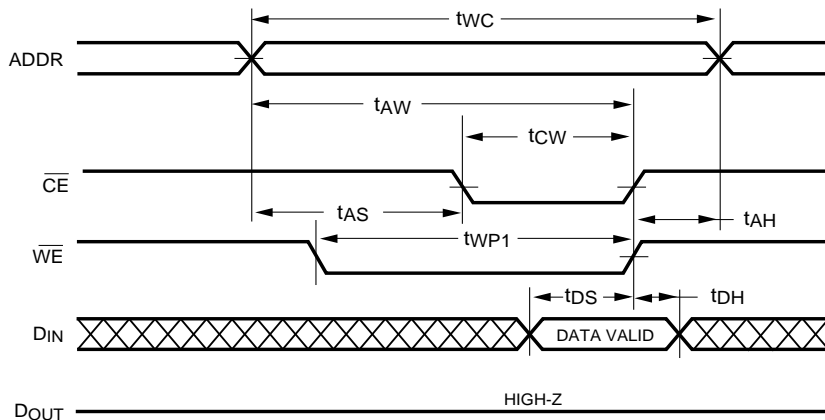


**Write Cycle No. 2 (Write Enable Controlled)**



NOTE: Output Enable ( $\overline{OE}$ ) is inactive (high)

**Write Cycle No. 3 (Chip Enable Controlled)**



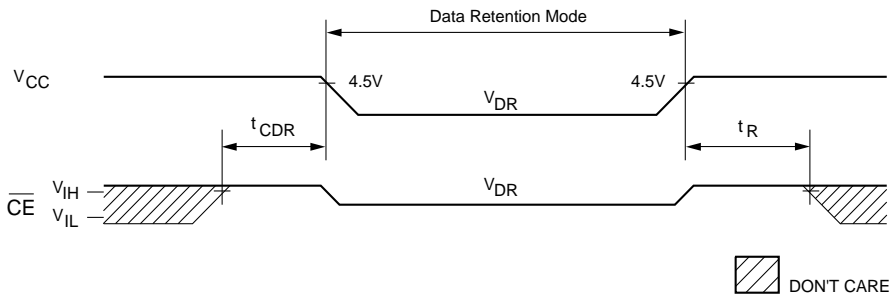
**AC Electrical Characteristics**

Description		-10 <sup>(7)</sup>		-12 <sup>(7)</sup>		-15		
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
WRITE Cycle time	t <sub>WC</sub>	10		12		15		ns
Chip enable active time	t <sub>CW</sub>	10		10		11		ns
Address Valid to end of write	t <sub>AW</sub>	10		10		11		ns
Address setup time	t <sub>AS</sub>	0		0		0		ns
Address hold from end of write	t <sub>AH</sub>	0		0		0		ns
Write pulse width	t <sub>WP1</sub>	9		10		11		ns
Write pulse width	t <sub>WP2</sub>	10		11		12		ns
Data setup time	t <sub>DS</sub>	7		7		7		ns
Data hold time	t <sub>DH</sub>	0		0		0		ns
Write disable to output in low Z <sup>(1,3)</sup>	t <sub>LZWE</sub>	0		0		0		ns
Write enable to output in high Z <sup>(1,3)</sup>	t <sub>HZWE</sub>		7		7		7	ns

SHADED AREA = PRELIMINARY DATA

Notes referenced are after Data Retention Table

**Low V<sub>CC</sub> Data Retention Waveform**



**Data Retention Electrical Characteristics (LA Version Only)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	VCC for Retention Data		2	—	—	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$ $V_{CC} = 3V$	—	500 750	$\mu A$ $\mu A$
t <sub>CDR</sub>	Chip Deselect to Data Retention Time		0	—	—	ns
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub>	—	—	ns

NOTES: (For three previous Electrical Characteristics tables)

1. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>.
3. This parameter is sampled.
4. WE is high for a READ cycle.
5. The device is continuously selected. Chip Enable is held in its active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.
7. Vcc = 5V ± 5%.

Ordering Information

