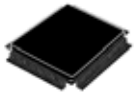
Freescale Semiconductor
Data Sheet: Advance Information

Document Number: MPC5643L
Rev. 3, 10/2009

MPC5643L



LQFP 144
20 x 20 x 1.4 mm

257 MAPBGA
14 x 14 x 1.4 mm

MPC5643L Microcontroller Data Sheet

- High-performance e200z4d dual core
  - 32-bit Power Architecture™ Book E CPU
  - Core frequency as high as 120 MHz
  - Dual issue five-stage pipeline core
  - Variable Length Encoding (VLE)
  - Memory Management Unit (MMU)
  - 4 KB instruction cache with error detection code
  - Signal processing engine (SPE)
- Memory available
  - 1 MB Flash memory with ECC
  - Built-in RWW capabilities for EEPROM emulation
  - As much as 128 KB on-chip RAM with ECC
- SIL3/ASILD innovative safety concept: LockStep mode and Fail-safe protection
  - Sphere of replication (SoR) for key components (such as CPU core, DMA, crossbar switch)
  - Fault collection and control unit (FCCU)
  - Redundancy control and checker unit (RCCU) on outputs of the SoR connected to FCCU
  - Boot-time Built-In Self-Test for Memory (MBIST) and Logic (LBIST) triggered by hardware
  - Boot-time Built-In Self-Test for ADC and flash memory triggered by software
  - Replicated safety enhanced watchdog
  - Replicated junction temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) unit
- Decoupled Parallel mode for high performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority controller
  - Replicated 16-channel eDMA controller
- GPIOs individually programmable as input, output or special function
- Three 6-channel general-purpose eTimer units
- Two FlexPWM units
  - Four 16-bit channels per module
- Communications interfaces
  - Two LINFlex channels
  - Three DSPI channels with automatic chip select generation
  - Two FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1) with dual channel, up to 64 message objects and speed as fast as 10 Mbit/s
- Two 12-bit analog-to-digital converters (ADCs)
  - 16 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADCs conversion with timer and PWM
- Sine wave generator (D/A with low pass filter)
- On-chip CAN/UART/FlexRay Bootstrap loader
- Single 3.0 V to 3.6 V voltage supply
- Ambient temperature range –40 °C to 125 °C
- Junction temperature range –40 °C to 150 °C

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Preliminary—Subject to Change Without Notice

Table of Contents

1 Overview 3
1.1 Device comparison 3
1.2 Block diagram 6
1.3 Feature details 7
1.3.1 High-performance e200z4d core 7
1.3.2 Crossbar switch (XBAR) 8
1.3.3 Memory Protection Unit (MPU) 8
1.3.4 Enhanced Direct Memory Access (eDMA) 8
1.3.5 On-chip flash memory with ECC 9
1.3.6 On-chip SRAM with ECC 9
1.3.7 Platform flash controller 9
1.3.8 Platform Static RAM Controller (SRAMC) 10
1.3.9 Memory subsystem access time 10
1.3.10 Error Correction Status Module (ECSM) 11
1.3.11 Peripheral bridge (PBRIDGE/AIPS-Lite) 11
1.3.12 Interrupt Controller (INTC) 11
1.3.13 System clocks and clock generation 12
1.3.14 Frequency-Modulated Phase-Locked Loop (FMPLL) 12
1.3.15 Main oscillator 12
1.3.16 Internal Reference Clock (RC) oscillator 13
1.3.17 Clock, reset, power, mode and test control module 13
1.3.18 Periodic Interrupt Timer Module (PIT) 13
1.3.19 System Timer Module (STM) 13
1.3.20 Software Watchdog Timer (SWT) 13
1.3.21 Fault Collection and Control Unit (FCCU) 14
1.3.22 System Integration Unit Lite (SIUL) 14
1.3.23 Non-Maskable Interrupt (NMI) 14
1.3.24 Boot Assist Module (BAM) 14
1.3.25 System Status and Configuration Module (SSCM) 15
1.3.26 FlexCAN 15
1.3.27 FlexRay 16
1.3.28 Serial communication interface module (LINFlex) 16
1.3.29 Serial Peripheral Interface module (DSPI) 17
1.3.30 FlexPWM 17
1.3.31 eTimer module 18
1.3.32 Sine Wave Generator (SWG) 18
1.3.33 Analog-to-Digital Converter module (ADC) 19
1.3.34 Cross Triggering Unit (CTU) 19
1.3.35 Cyclic Redundancy Checker (CRC) Unit 20
1.3.36 Redundancy Control and Checker Unit (RCCU) 20
1.3.37 Junction temperature sensor 20
1.3.38 Nexus Port Controller (NPC) 20
1.3.39 IEEE 1149.1 JTAG Controller (JTAGC) 21
1.3.40 Voltage regulator / Power Management Unit (PMU) 22
1.3.41 Built-In Self-Test (BIST) capability 22
2 Package pinouts and signal descriptions 22
2.1 Package pinouts 22
2.2 Pin descriptions 25
2.2.1 Concatenated pins 25
2.2.2 Power supply and reference voltage pins 38
2.2.3 System pins 41
2.2.4 Pin muxing 41
3 Electrical characteristics 58
3.1 Introduction 58
3.2 Absolute maximum ratings 58
3.3 Recommended operating conditions 59
3.4 Thermal characteristics 60
3.4.1 General notes for specifications at maximum junction temperature 61
3.5 Electromagnetic Interference (EMI) characteristics . . . 63
3.6 Electrostatic discharge (ESD) characteristics 63
3.7 Static latch-up (LU) 64
3.8 Voltage regulator electrical characteristics 64
3.9 DC electrical characteristics 66
3.10 Temperature sensor electrical characteristics 67
3.11 Main oscillator electrical characteristics 68
3.12 FMPLL electrical characteristics 69
3.13 16 MHz RC oscillator electrical characteristics 71
3.14 ADC electrical characteristics 72
3.14.1 Input Impedance and ADC Accuracy 72
3.15 Flash memory electrical characteristics 77
3.16 AC specifications 78
3.16.1 Pad AC specifications 78
3.17 AC timing characteristics 79
3.17.1 $\overline{\text{RESET}}$ pin characteristics 79
3.17.2 IEEE 1149.1 interface timing 80
3.17.3 Nexus timing 82
3.17.4 External interrupt timing (IRQ pin) 84
3.17.5 FlexCAN timing 85
3.17.6 DSPI timing 85
4 Package characteristics 92
4.1 Package mechanical data 92
5 Ordering information 96
6 Document revision history 97

1 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5643L series of microcontroller units (MCUs). For functional characteristics, refer to the *MPC5643L Microcontroller Reference Manual.* For use of the MPC5643Lin a fail-safe system according to safety standard IEC 61508, refer to the *MPC5643LSafety Application Guide*.

The MPC5643L series microcontrollers are system-on-chip devices that are built on Power Architecture™ technology and:

- Are 100% user-mode compatible with the classic Power Architecture instruction set
- Contain enhancements that improve the architecture's fit in embedded applications
- Include additional instruction support for digital signal processing (DSP)
- Integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

The MPC5643L family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the MPC5643L automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original PowerPC user instruction set architecture (UISA). It operates at speeds as high as 120 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.1 Device comparison

Table 1. MPC5643L device summary

Feature		MPC5643L
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)
	Architecture	Harvard
	Execution speed	0 – 120 MHz (+2% FM)
	DMIPS intrinsic performance	> 240 MIPS
	SIMD (DSP + FPU)	Yes
	MMU	16 entry
	Instruction set PPC	Yes
	Instruction set VLE	Yes
	Instruction cache	4 KB, EDC
	MPU-16 regions	Yes, replicated module
	Semaphore unit (SEMA4)	Yes
Buses	Core bus	AHB, 32-bit address, 64-bit data
	Internal periphery bus	32-bit address, 32-bit data
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3

Table 1. MPC5643L device summary (continued)

Feature		MPC5643L
Memory	Code/data flash	1 MB, ECC, RWW
	Static RAM	128 KB, ECC
Modules	Interrupt controller	16 interrupt levels, replicated module
	Periodic Interrupt Timer (PIT)	1 × 4 channels
	System timer module	1 × 4 channels, replicated module
	Software watchdog timer	Yes, replicated module
	eDMA	16 channels, replicated module
	FlexRay	1 × 64 message buffer, dual channel
	FlexCAN	2 × 32 message buffer
	LINFlex (UART and LIN)	2
	Clock out	Yes
	Fault control & collection unit (FCCU)	Yes
	Cross triggering unit (CTU)	Yes
	eTimer	3 × 6 channels[1]
	FlexPWM	2 Module 4 × (2 + 1) channels[2]
	ADC	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)
	Sine-wave generator	32 point
	DSPI	3 × DSPI as many as 8 chip selects
	Cyclic redundancy checker (CRC) unit	Yes
	Junction temperature sensor with analog comparator	Yes, replicated module
	Digital I/Os	≥ 16
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2
	Internal RC oscillator	16 MHz
	External crystal oscillator	4 – 40 MHz
Debug	Nexus	Level 3+

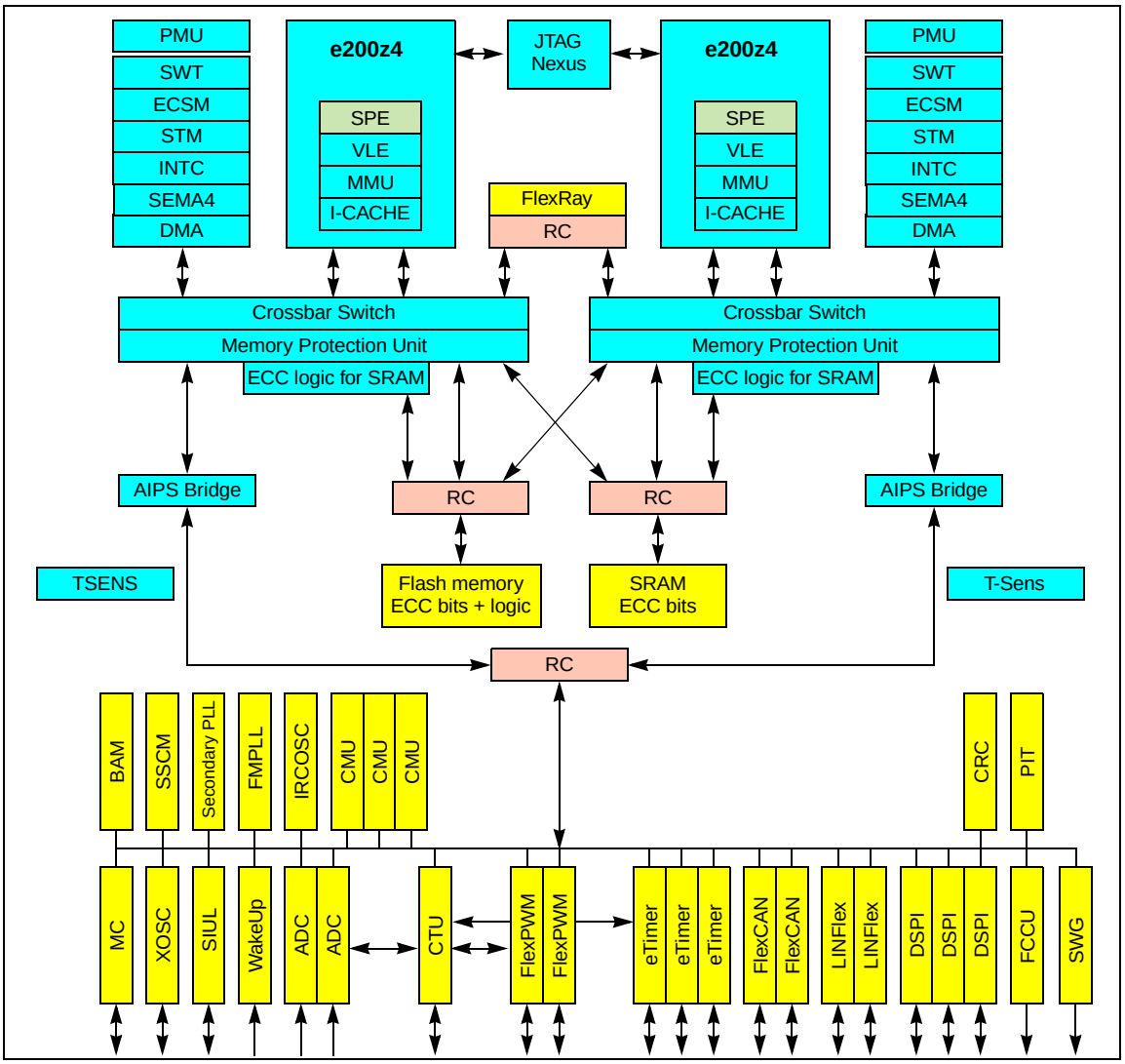
Table 1. MPC5643L device summary (continued)

Feature		MPC5643L
Packages	Known Good Die (KGD)	Yes
	LQFP	144 pins
	MAPBGA	257 MAPBGA
Temperature	Temperature range (junction)	–40 to 150 °C
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C
	Ambient temperature range using external ballast transistor (BGA)	TBD

NOTES:
1 The third eTimer is available only in the BGA package.
2 The second FlexPWM module is available only in the BGA package.

1.2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5643L device.



ADC – Analog-to-Digital Converter
AIPS – AHB to IP Slave Bus bridge
BAM – Boot Assist Module
CMU – Clock Monitoring Unit
CRC – Cyclic Redundancy Check unit
CTU – Cross Triggering Unit
DMA – Direct Memory Access controller
DSPI – Serial Peripherals Interface
ECC – Error Correction Code
ECSM – Error Correction Status Module
FCCU – Fault Collection and Control Unit
FlexCAN – Controller Area Network controller
FMPLL – Frequency Modulated Phase Locked Loop
INTC – Interrupt Controller
IRCOSC – Internal RC Oscillator
JTAG – Joint Test Action Group interface
MC – Mode Entry, Clock, Reset, & Power
PIT – Periodic Interrupt Timer
PMU – Power Management Unit
RC – Redundancy Checker
RTC – Real Time Clock
SEMA4 – Semaphore Unit
SIUL – System Integration Unit Lite
SSCM – System Status and Configuration Module
STM – System Timer Module
SWG – Sine Wave Generator
SWT – Software Watchdog Timer
TSENS – Temperature Sensor
XOSC – Crystal Oscillator

Figure 1. MPC5643L block diagram

1.3 Feature details

1.3.1 High-performance e200z4d core

The e200z4d Power Architecture™ core provides the following features:

- Two independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture™ (Book E) compliant
  - Five-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- Three cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported
  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (two-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target nine cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs
- Extensive system development and tracing support via Nexus debug port

1.3.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- Four masters and three slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (two masters), one DMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with two slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with one slave port each and one redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processor.

1.3.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (DMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processor.

1.3.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop

- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processor.

1.3.5 On-chip flash memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB Test and 16 KB shadow sector for test, censorship device and user option bits
- 3 wait states at 120 MHz
- Flash line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.3.6 On-chip SRAM with ECC

The MPC5643L SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB
- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection

1.3.7 Platform flash controller

The following list summarizes the key features of the flash controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.
- Single-cycle read responses (zero AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Data flash (bank1) interface includes a 128-bit register to temporarily hold a single flash page. This logic supports single-cycle read responses (0 AHB data-phase wait states) for accesses that hit in the holding register.
  - No prefetch support is provided for this bank.

- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort, and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

1.3.8 Platform Static RAM Controller (SRAMC)

The SRAMC module is the platform RAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- RAM array

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the RAM Array

The platform RAM controller is replicated for each processor.

1.3.9 Memory subsystem access time

Every memory access the CPU performs requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform memory access time summary

AHB Transfer	Data Phase Wait States	Description
e200z4d Instruction Fetch	TBD[1]	Flash prefetch buffer hit (page hit)
e200z4d Instruction Fetch	TBD	Flash prefetch buffer miss (at 120 MHz) (based on 4-cycle random flash array access time)
e200z4d Data Read	TBD	RAM read
e200z4d Data Write	TBD	RAM 32-bit write
e200z4d Data Write	TBD	RAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d Data Write	TBD	RAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d Data Flash Read	TBD	Flash prefetch buffer hit (page hit)
e200z4d Data Flash Read	TBD	Flash prefetch buffer miss (includes 1-cycle of program flash controller arbitration)

Table 2. Platform memory access time summary (continued)

AHB Transfer	Data Phase Wait States	Description
e200z4d Peripheral Read	TBD	Peripheral Bridge read
e200z4d Peripheral Write	TBD	Peripheral Bridge write

NOTES:
1 To be determined

1.3.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for RAM

1.3.11 Peripheral bridge (PBRIDGE/AIPS-Lite)

The peripheral bridge (referred to as PBRIDGE or AIPS-Lite throughout this document) implements the following features:

- Duplicated periphery
- Protocol translator bridge from AMBA to internal periphery interface (IPI)
- Master access right per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on AIPS-Lite output toward periphery
- Byte endianess swap capability

1.3.12 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

1.3.13 System clocks and clock generation

The following list summarizes the system clock and clock generation on this device:

- Lock status continuously monitored by lock detect circuitry
- Loss-of-clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and fewer external components required)
- Programmable output clock divider of system clock (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and as many as three eTimer modules running on an auxiliary clock independent from system clock (with max frequency 120 MHz)
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up
  - Supports automated frequency trimming by hardware during device startup and by user application
- Auxiliary clock domain for motor control periphery (FlexPWM, eTimer, CTU, ADC, and SWG)

1.3.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Two FMPLLs are available on each device.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- Three modes of operation
  - Bypass mode
  - Normal PLL mode with crystal reference (default)
  - Normal PLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.3.15 Main oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- PLL reference

1.3.16 Internal Reference Clock (RC) oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of PLL(s) in case XOSC fails

1.3.17 Clock, reset, power, mode and test control module

The Clock, Reset, Power, Mode and Test control module has the following features:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable System and auxiliary clock dividers
- Various execution modes
  - Reset, Idle, Test, Safe
  - Various RUN modes with software selectable powered modules
  - No stand-by mode implemented (no internal switchable power domains)

1.3.18 Periodic Interrupt Timer Module (PIT)

The PIT module implements the following features:

- Four general purpose interrupt timers
- 32-bit counter resolution
- 32-bit counter for real time interrupt, clocked from main external oscillator
- Can be used for software tick or DMA trigger operation

1.3.19 System Timer Module (STM)

The STM implements the following features:

- Up-counter with four output compare registers
- OS task protection and hardware tick implementation per AutoSar requirement

The STM is replicated for each processor.

1.3.20 Software Watchdog Timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

The SWT module is replicated for each processor.

1.3.21 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.3.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized pad control on per pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

1.3.23 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high priority core exceptions.

1.3.24 Boot Assist Module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (FlexCAN or LINFlex-UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either classic PowerPC Book E code (default) or Freescale VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.3.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either classic PowerPC Book E code (default) or as Freescale VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.3.26 FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- Three programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - Eight mailboxes configurable as a 6-entry receive FIFO
  - Eight programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter

1.3.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit, receive, or receive FIFO
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO message buffers
- Memory mapped message buffers (shared using the MPU)
- ECC to cover lookup table and data SRAM

1.3.28 Serial communication interface module (LINFlex)

The LINFlex on this device features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (Loop back, LIN bus stuck dominant detection)
  - Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, or 16-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (Parity, Noise and Framing errors)
  - Interrupt driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- Support for DMA enabled transfers

1.3.29 Serial Peripheral Interface module (DSPI)

The serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5643L and external devices.

A DSPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as eight chip select lines available, depending on package and pin multiplexing
- Four clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as five transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.3.30 FlexPWM

The pulse width modulator module (FlexPWM) contains four PWM channels, each of which is configured to control a single half-bridge power stage. Two modules are instantiated on the 257 MAPBGA device; on the 144 LQFP package, only one module is present. Additionally, four fault input channels are provided per FlexPWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via auxiliary PLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs

- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high and low limit registers
- DMA support

1.3.31 eTimer module

The Leopard provides three eTimer modules on the 257 MAPBGA device, and two eTimer modules on the 144 LQFP package. Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency 120 MHz
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

1.3.32 Sine Wave Generator (SWG)

A customized digital-to-analog converter is available to generate a sine wave based on 32 stored values for external devices (ex: resolver).

- Frequency range from 1 kHz to 50 kHz
- Sine wave amplitude from 0.47 V to 2.26 V

1.3.33 Analog-to-Digital Converter module (ADC)

The ADC module features are as follows:

Analog part:

- Two on-chip ADCs
  - 12-bit resolution SAR architecture
  - Same digital interface as in the MPC5604P family
  - A/D Channels: Nine external, Three internal and Four shared with other A/D. Total 16
  - One channel dedicated to each T-sensor to enable temperature reading during application
  - Separated reference for each ADC
  - Shared analog supply voltage for both ADCs
  - One sample and hold unit per ADC
  - Adjustable sampling and conversion time

Digital part:

- Four analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- Two modes of operation: Motor Control Mode or Regular Mode
- Regular mode features
  - Register based interface with the CPU: one result register per channel
  - ADC state machine managing three request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - Four analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- Motor control mode features
  - Triggered mode only
  - Four independent result queues (1×16 entries, 2×8 entries, 1×4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit parts
  - DMA compatible interfaces
- Built-in self-test features triggered by software

1.3.34 Cross Triggering Unit (CTU)

The ADC cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands

- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.3.35 Cyclic Redundancy Checker (CRC) Unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to input register.

The CRC unit has the following features:

- Three sets of registers to allow three concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register. The following standard CRC polynomials are implemented:
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads core from cycle-consuming CRC and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on internal peripheral bus
- DMA support

1.3.36 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Multiple times replicated IPs are used as checkers on the SoR outputs

1.3.37 Junction temperature sensor

The junction temperature sensor is used by the ADC to measure the temperature of the silicon.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

1.3.38 Nexus Port Controller (NPC)

The NPC block provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2008 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2008 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes

- MCKO (message clock out) pin
- Four or 12 MDO (message data out) pins[1]
- Two $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- Five-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Supports JTAG mode
- Host processor (e200) development support features
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint messaging (WPM) via the auxiliary port
  - Watchpoint trigger enable of program and/or data trace messaging
  - Data tracing of instruction fetches via private opcodes

1.3.39 IEEE 1149.1 JTAG Controller (JTAGC)

The JTAGC block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with five pins:
  - TDI
  - TMS
  - TCK
  - TDO
  - JCOMP
- Selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- Three test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1. Four MDO pins on 144 LQFP package, 12 MDO pins on 257 MAPBGA package.

1.3.40 Voltage regulator / Power Management Unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V both for packaged and Known Good Die option
  - Packaged option requires external ballast transistor due to reduced dissipation capacity at high temperature but can use embedded transistor if power dissipation is maintained within package dissipation capacity (lower frequency of operation)
  - Known Good Die option uses embedded ballast transistor as dissipation capacity is increased to reduce system cost
- All I/Os are at same voltage as external supply (3.3 V nominal)
- Duplicated Low-Voltage Detectors (LVD) to guarantee proper operation at all stages (reset, configuration, normal operation) and, to maximize safety coverage, one LVD can be tested while the other operates (on-line self-testing feature)

1.3.41 Built-In Self-Test (BIST) capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the MPC5643L in the 144 LQFP package. Figure 3 shows the MPC5643L in the 257 MAPBGA package.

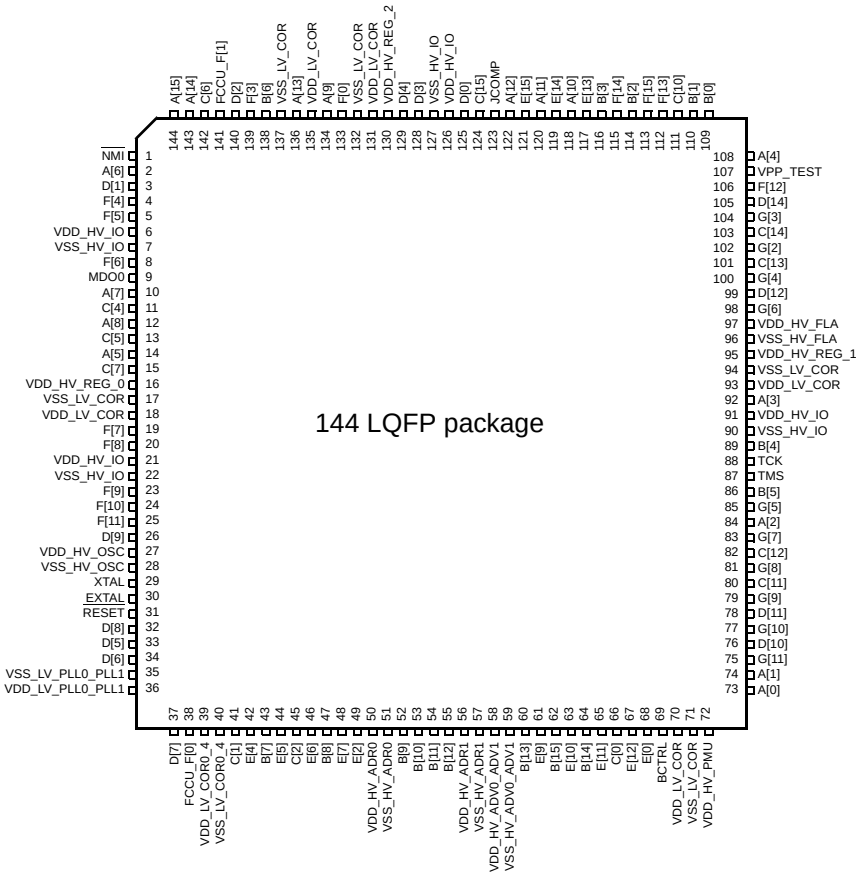


Figure 2. MPC5643L 144 LQFP pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	V_{SS}	V_{SS}	V_{DD_HV}	H[2]	H[0]	G[14]	D[3]	C[15]	V_{DD_HV}	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	V_{SS}	V_{SS}
B	V_{SS}	V_{SS}	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	V_{SS}	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	V_{DD_HV}	V_{SS}
C	V_{DD_HV}	NC	V_{SS}	FCCU_F[1]	D[2]	A[13]	V_{DD_HV}	V_{DD_HV}	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	V_{SS}	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	V_{SS}	V_{DD_LV}	F[0]	V_{DD_HV}	V_{SS}	NC	A[11]	E[13]	F[15]	V_{DD_HV}	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		NC	C[13]	I[2]	G[4]
G	H[3]	V_{DD_HV}	C[5]	A[6]		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		D[12]	H[13]	H[9]	G[6]
H	G[13]	V_{SS}	C[4]	A[5]		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		V_{SS}	V_{DD_HV}	V_{DD_HV}	H[6]
J	F[7]	G[15]	V_{DD_HV}	V_{DD_HV}		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		V_{DD_LV}	V_{DD_HV}	V_{SS}	H[15]
K	F[9]	F[8]	NC	C[7]		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	V_{DD_HV}	V_{DD_HV}	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	V_{SS}	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	V_{SS}	$\overline{RESET}$	D[6]	$V_{DD\_LV\_PLL}$	V_{DD_LV}	V_{SS}	B[8]	NC	V_{SS}	V_{DD_HV}	B[14]	V_{DD_LV}	V_{SS}	V_{DD_HV}	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	V_{SS}	D[7]	B[7]	E[6]	$V_{REFP\_HV\_AD0}$	B[10]	$V_{REFP\_HV\_AD1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	V_{SS}	D[11]	G[9]
T	V_{SS}	V_{DD_HV}	NC	C[1]	E[5]	E[7]	$V_{REFN\_HV\_AD0}$	B[11]	$V_{REFN\_HV\_AD1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	V_{DD_HV}	V_{SS}
U	V_{SS}	V_{SS}	NC	E[4]	C[2]	E[2]	B[9]	B[12]	V_{DD_HV}	V_{SS}	E[11]	NC	NC	V_{DD_HV}	G[11]	V_{SS}	V_{SS}
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 3. MPC5643L 257 MAPBGA pinout (top view)

Table 3 provides the concatenated pin names (pin muxing) for the pins shown in Figure 2, including the functional group for the pin. Table 3 provides the concatenated ball names (pin muxing) for the pins shown in Figure 3, including the functional group for the pin. For more information, see Table 7.

2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration for this device.

2.2.1 Concatenated pins

Table 3 provides the concatenated ball names (pin muxing) for the pins shown in Figure 2 and the balls shown in Figure 3, including the functional group for the pin. This table provides a cross-reference for the two packages. Table 3 lists the concatenated ball names (pin muxing) in alphanumeric order for the balls shown in Figure 3, including the functional group.

Table 3. Concatenated pin names

Pin No. 144 LQFP	Ball No. 257 MAPBGA	Concatenated Pin Names
1	E4	$\overline{\text{NMI}}$
2	G4	A[6] / siul_GPIO[6] / dspi1_SCK / siul_EIRQ[6]
3	E3	D[1] / siul_GPIO[49] / etimer1_ETC[2] / ctu0_EXT_TGR / flexray_CA_RX
4	D2	F[4] / siul_GPIO[84] / npc_wrapper_MDO[3]
5	D1	F[5] / siul_GPIO[85] / npc_wrapper_MDO[2]
6	VDD_HV[1]	$V_{DD\_HV\_IO}$
7	VSS_HV[2]	$V_{SS\_HV\_IO}$
8	E2	F[6] / siul_GPIO[86] / npc_wrapper_MDO[1]
9	E1	MDO0
10	F3	A[7] / siul_GPIO[7] / dspi1_SOUT / siul_EIRQ[7]
11	H3	C[4] / siul_GPIO[36] / dspi0_$\overline{\text{CS0}}$ / flexpwm0_X[1] / sscm_DEBUG[4] / siul_EIRQ[22]
12	F4	A[8] / siul_GPIO[8] / dspi1_SIN / siul_EIRQ[8]
13	G3	C[5] / siul_GPIO[37] / dspi0_SCK / sscm_DEBUG[5] / flexpwm0_FAULT[3] / siul_EIRQ[23]
14	H4	A[5] / siul_GPIO[5] / dspi1_$\overline{\text{CS0}}$ / etimer1_ETC[5] / dspi0_$\overline{\text{CS7}}$ / siul_EIRQ[5]
15	K4	C[7] / siul_GPIO[39] / flexpwm0_A[1] / sscm_DEBUG[7] / dspi0_SIN
16	J3	$V_{DD\_HV\_REG\_0}$
17	VSS_LV[3]	$V_{SS\_LV\_COR}$
18	VDD_LV[4]	$V_{DD\_LV\_COR}$
19	J1	F[7] / siul_GPIO[87] / npc_wrapper_MCKO
20	K2	F[8] / siul_GPIO[88] / npc_wrapper_$\overline{\text{MSEO[1]}}$
21	VDD_HV[3]	$V_{DD\_HV\_IO}$
22	VSS_HV[4]	$V_{SS\_HV\_IO}$
23	K1	F[9] / siul_GPIO[89] / npc_wrapper_$\overline{\text{MSEO[0]}}$
24	L1	F[10] / siul_GPIO[90] / npc_wrapper_$\overline{\text{EVTO}}$
25	L2	F[11] / siul_GPIO[91] / leo_sor0_$\overline{\text{EVTI}}$

Table 3. Concatenated pin names (continued)

Pin No. 144 LQFP	Ball No. 257 MAPBGA	Concatenated Pin Names
26	L3	D[9] / siul_GPIO[57] / flexpwm0_X[0] / lin1_TXD
27	M1	$V_{DD\_HV\_OSC}$
28	P1	$V_{SS\_HV\_OSC}$
29	N1	XTAL[5]
30	R1	EXTAL[5]
31	P2	$\overline{\text{RESET}}$
32	M3	D[8] / siul_GPIO[56] / dspi1_$\overline{\text{CS2}}$ / etimer1_ETC[4] / dspi0_$\overline{\text{CS5}}$ / flexpwm0_FAULT[3]
33	N3	D[5] / siul_GPIO[53] / dspi0_$\overline{\text{CS3}}$ / flexpwm0_FAULT[2]
34	P3	D[6] / siul_GPIO[54] / dspi0_$\overline{\text{CS2}}$ / flexpwm0_X[3] / flexpwm0_FAULT[1]
35	N4	$V_{SS\_LV\_PLL0\_PLL1}$
36	P4	$V_{DD\_LV\_PLL0\_PLL1}$
37	R4	D[7] / siul_GPIO[55] / dspi1_$\overline{\text{CS3}}$ / dspi0_$\overline{\text{CS4}}$
38	R2	FCCU_F[0]
39	VDD_LV[1]	$V_{DD\_LV\_COR0\_4}$
40	VSS_LV[2]	$V_{SS\_LV\_COR0\_4}$
41	T4	C[1] / siul_GPIO[33]
42	U4	E[4] / siul_GPIO[68]
43	R5	B[7] / siul_GPIO[23] / lin0_RXD
44	T5	E[5] / siul_GPIO[69]
45	U5	C[2] / siul_GPIO[34]
46	R6	E[6] / siul_GPIO[70]
47	P7	B[8] / siul_GPIO[24] / etimer0_ETC[5]
48	T6	E[7] / siul_GPIO[71]
49	U6	E[2] / siul_GPIO[66]
50	R7	$V_{DD\_HV\_ADR0}$
51	T7	$V_{SS\_HV\_ADR0}$
52	U7	B[9] / siul_GPIO[25]
53	R8	B[10] / siul_GPIO[26]
54	T8	B[11] / siul_GPIO[27]
55	U8	B[12] / siul_GPIO[28]
56	R9	$V_{DD\_HV\_ADR1}$
57	T9	$V_{SS\_HV\_ADR1}$
58	U9	$V_{DD\_HV\_ADV}$

Table 3. Concatenated pin names (continued)

Pin No. 144 LQFP	Ball No. 257 MAPBGA	Concatenated Pin Names
59	U10	$V_{SS\_HV\_ADV}$
60	R10	B[13] / siul_GPIO[29] / lin1_RXD
61	T10	E[9] / siul_GPIO[73]
62	R11	B[15] / siul_GPIO[31] / siul_EIRQ[20]
63	T11	E[10] / siul_GPIO[74]
64	P11	B[14] / siul_GPIO[30] / etimer0_ETC[4] / siul_EIRQ[19]
65	U11	E[11] / siul_GPIO[75]
66	R12	C[0] / siul_GPIO[32]
67	T12	E[12] / siul_GPIO[76]
68	T13	E[0] / siul_GPIO[64]
69	R13	BCTRL
70	VDD_LV[1]	$V_{DD\_LV\_COR}$
71	VSS_LV[2]	$V_{SS\_LV\_COR}$
72	U14	$V_{DD\_HV\_PMU}$
73	T14	A[0] / siul_GPIO[0] / etimer0_ETC[0] / dspi2_SCK / siul_EIRQ[0]
74	R14	A[1] / siul_GPIO[1] / etimer0_ETC[1] / dspi2_SOUT / siul_EIRQ[1]
75	U15	G[11] / siul_GPIO[107] / flexray_DBG3 / flexpwm0_FAULT[3]
76	T15	D[10] / siul_GPIO[58] / flexpwm0_A[0] / etimer0_ETC[0]
77	P15	G[10] / siul_GPIO[106] / flexray_DBG2 / dspi2_$\overline{CS3}$ / flexpwm0_FAULT[2]
78	R16	D[11] / siul_GPIO[59] / flexpwm0_B[0] / etimer0_ETC[1]
79	R17	G[9] / siul_GPIO[105] / flexray_DBG1 / dspi1_$\overline{CS1}$ / flexpwm0_FAULT[1] / siul_EIRQ[29]
80	M14	C[11] / siul_GPIO[43] / etimer0_ETC[4] / dspi2_$\overline{CS2}$
81	P16	G[8] / siul_GPIO[104] / flexray_DBG0 / dspi0_$\overline{CS1}$ / flexpwm0_FAULT[0] / siul_EIRQ[21]
82	N15	C[12] / siul_GPIO[44] / etimer0_ETC[5] / dspi2_$\overline{CS3}$
83	P17	G[7] / siul_GPIO[103] / flexpwm0_B[3]
84	N16	A[2] / siul_GPIO[2] / etimer0_ETC[2] / flexpwm0_A[3] / dspi2_SIN / mc_rgm_ABS[0] / siul_EIRQ[2]
85	N17	G[5] / siul_GPIO[101] / flexpwm0_X[3] / dspi2_$\overline{CS3}$
86	M15	B[5] / siul_GPIO[21] / jtagc_TDI
87	M16	TMS
88	L15	TCK
89	L17	B[4] / siul_GPIO[20] / jtagc_TDO
90	VSS_HV[4]	$V_{SS\_HV\_IO}$

Table 3. Concatenated pin names (continued)

Pin No. 144 LQFP	Ball No. 257 MAPBGA	Concatenated Pin Names
91	VDD_HV[3]	$V_{DD\_HV\_IO}$
92	K17	A[3] / siul_GPIO[3] / etimer0_ETC[3] / dspi2_$\overline{CS0}$ / flexpwm0_B[3] / mc_rgm_ABS[2] / siul_EIRQ[3]
93	VDD_LV[1]	$V_{DD\_LV\_COR}$
94	VSS_LV[2]	$V_{SS\_LV\_COR}$
95	H15	$V_{DD\_HV\_REG\_1}$
96	J16	$V_{SS\_HV\_FLA}$
97	H16	$V_{DD\_HV\_FLA}$
98	G17	G[6] / siul_GPIO[102] / flexpwm0_A[3]
99	G14	D[12] / siul_GPIO[60] / flexpwm0_X[1] / lin1_RXD
100	F17	G[4] / siul_GPIO[100] / flexpwm0_B[2] / etimer0_ETC[5]
101	F15	C[13] / siul_GPIO[45] / etimer1_ETC[1] / ctu0_EXT_IN / flexpwm0_EXT_SYNC
102	E16	G[2] / siul_GPIO[98] / flexpwm0_X[2] / dspi1_$\overline{CS1}$
103	E15	C[14] / siul_GPIO[46] / etimer1_ETC[2] / ctu0_EXT_TGR
104	D17	G[3] / siul_GPIO[99] / flexpwm0_A[2] / etimer0_ETC[4]
105	D16	D[14] / siul_GPIO[62] / flexpwm0_B[1] / etimer0_ETC[3]
106	C17	F[12] / siul_GPIO[92] / etimer1_ETC[3] / siul_EIRQ[30]
107	D15	V_{PP_TEST}[6]
108	C16	A[4] / siul_GPIO[4] / etimer1_ETC[0] / dspi2_$\overline{CS1}$ / etimer0_ETC[4] / mc_rgm_FAB / siul_EIRQ[4]
109	B15	B[0] / siul_GPIO[16] / can0_TXD / etimer1_ETC[2] / sscm_DEBUG[0] / siul_EIRQ[15]
110	C14	B[1] / siul_GPIO[17] / etimer1_ETC[3] / sscm_DEBUG[1] / can0_RXD / can1_RXD / siul_EIRQ[16]
111	A15	C[10] / siul_GPIO[42] / dspi2_$\overline{CS2}$ / flexpwm0_A[3] / flexpwm0_FAULT[1]
112	B14	F[13] / siul_GPIO[93] / etimer1_ETC[4] / siul_EIRQ[31]
113	D13	F[15] / siul_GPIO[95] / lin1_RXD
114	A14	B[2] / siul_GPIO[18] / lin0_TXD / sscm_DEBUG[2] / siul_EIRQ[17]
115	C13	F[14] / siul_GPIO[94] / lin1_TXD
116	B13	B[3] / siul_GPIO[19] / sscm_DEBUG[3] / lin0_RXD
117	D12	E[13] / siul_GPIO[77] / etimer0_ETC[5] / dspi2_$\overline{CS3}$ / siul_EIRQ[25]
118	A13	A[10] / siul_GPIO[10] / dspi2_$\overline{CS0}$ / flexpwm0_B[0] / flexpwm0_X[2] / siul_EIRQ[9]
119	B12	E[14] / siul_GPIO[78] / etimer1_ETC[5] / siul_EIRQ[26]
120	D11	A[11] / siul_GPIO[11] / dspi2_SCK / flexpwm0_A[0] / flexpwm0_A[2] / siul_EIRQ[10]
121	B11	E[15] / siul_GPIO[79] / dspi0_$\overline{CS1}$ / siul_EIRQ[27]

Table 3. Concatenated pin names (continued)

Pin No. 144 LQFP	Ball No. 257 MAPBGA	Concatenated Pin Names
122	A10	A[12] / siul_GPIO[12] / dspi2_SOUT / flexpwm0_A[2] / flexpwm0_B[2] / siul_EIRQ[11]
123	C10	JCOMP
124	A8	C[15] / siul_GPIO[47] / flexray_CA_TR_EN / etimer1_ETC[0] / flexpwm0_A[1] / ctu0_EXT_IN / flexpwm0_EXT_SYNC
125	B8	D[0] / siul_GPIO[48] / flexray_CA_TX / etimer1_ETC[1] / flexpwm0_B[1]
126	VDD_HV[3]	$V_{DD\_HV\_IO}$
127	VSS_HV[4]	$V_{SS\_HV\_IO}$
128	A7	D[3] / siul_GPIO[51] / flexray_CB_TX / etimer1_ETC[4] / flexpwm0_A[3]
129	B7	D[4] / siul_GPIO[52] / flexray_CB_TR_EN / etimer1_ETC[5] / flexpwm0_B[3]
130	C7	$V_{DD\_HV\_REG\_2}$
131	VDD_LV[1]	$V_{DD\_LV\_COR}$
132	VSS_LV[2]	$V_{SS\_LV\_COR}$
133	D7	F[0] / siul_GPIO[80] / flexpwm0_A[1] / etimer0_ETC[2] / siul_EIRQ[28]
134	B6	A[9] / siul_GPIO[9] / dspi2_$\overline{CS1}$ / flexpwm0_B[3] / flexpwm0_FAULT[0]
135	VDD_LV[1]	$V_{DD\_LV\_COR}$
136	C6	A[13] / siul_GPIO[13] / flexpwm0_B[2] / dspi2_SIN / flexpwm0_FAULT[0] / siul_EIRQ[12]
137	VSS_LV[2]	$V_{SS\_LV\_COR}$
138	B3	B[6] / siul_GPIO[22] / mc_cgl_clk_out / dspi2_$\overline{CS2}$ / siul_EIRQ[18]
139	B5	F[3] / siul_GPIO[83] / dspi0_$\overline{CS6}$
140	C5	D[2] / siul_GPIO[50] / etimer1_ETC[3] / flexpwm0_X[3] / flexray_CB_RX
141	C4	FCCU_F[1]
142	D4	C[6] / siul_GPIO[38] / dspi0_SOUT / flexpwm0_B[1] / sscm_DEBUG[6] / siul_EIRQ[24]
143	B4	A[14] / siul_GPIO[14] / can1_TXD / etimer1_ETC[4] / siul_EIRQ[13]
144	D3	A[15] / siul_GPIO[15] / etimer1_ETC[5] / can1_RXD / can0_RXD / siul_EIRQ[14]

NOTES:
1 VDD_HV balls are tied together on the 257 MAPBGA substrate.
2 VSS_HV balls are tied together on the 257 MAPBGA substrate.
3 VSS_LV balls are tied together on the 257 MAPBGA substrate.
4 VDD_LV balls are tied together on the 257 MAPBGA substrate.
5 The XTAL and EXTAL pins have different functions from the pins with these names on the MPC5604P.
6 V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. 257 MAPBGA concatenated ball names

Ball No.	Concatenated Pin Names
A1	$V_{SS\_HV\_IO\_RING}$
A2	$V_{SS\_HV\_IO\_RING}$
A3	$V_{DD\_HV\_IO\_RING}$
A4	H[2] / siul_GPIO[114] / npc_wrapper_MDO[5]
A5	H[0] / siul_GPIO[112] / npc_wrapper_MDO[7]
A6	G[14] / siul_GPIO[110] / npc_wrapper_MDO[9]
A7	D[3] / siul_GPIO[51] / flexray_CB_TX / etimer1_ETC[4] / flexpwm0_A[3]
A8	C[15] / siul_GPIO[47] / flexray_CA_TR_EN / etimer1_ETC[0] / flexpwm0_A[1] / ctu0_EXT_IN / flexpwm0_EXT_SYNC
A9	$V_{DD\_HV\_IO\_RING}$
A10	A[12] / siul_GPIO[12] / dspi2_MOSI / flexpwm0_A[2] / flexpwm0_B[2] / siul_EIRQ[11]
A11	H[10] / siul_GPIO[122] / flexpwm1_X[2] / etimer2_ETC[2]
A12	H[14] / siul_GPIO[126] / flexpwm1_A[3] / etimer2_ETC[4]
A13	A[10] / siul_GPIO[10] / dspi2_CS0 / flexpwm0_B[0] / flexpwm0_X[2] / siul_EIRQ[9]
A14	B[2] / siul_GPIO[18] / lin0_TXD / sscm_DEBUG[2] / siul_EIRQ[17]
A15	C[10] / siul_GPIO[42] / dspi2_CS2 / flexpwm0_A[3] / flexpwm0_FAULT[1]
A16	$V_{SS\_HV\_IO\_RING}$
A17	$V_{SS\_HV\_IO\_RING}$
B1	$V_{SS\_HV\_IO\_RING}$
B2	$V_{SS\_HV\_IO\_RING}$
B3	B[6] / siul_GPIO[22] / mc_cgl_clk_out / dspi2_CS2 / siul_EIRQ[18]
B4	A[14] / siul_GPIO[14] / can1_TXD / etimer1_ETC[4] / siul_EIRQ[13]
B5	F[3] / siul_GPIO[83] / dspi0_CS6
B6	A[9] / siul_GPIO[9] / dspi2_CS1 / flexpwm0_B[3] / flexpwm0_FAULT[0]
B7	D[4] / siul_GPIO[52] / flexray_CB_TR_EN / etimer1_ETC[5] / flexpwm0_B[3]
B8	D[0] / siul_GPIO[48] / flexray_CA_TX / etimer1_ETC[1] / flexpwm0_B[1]
B9	$V_{SS\_HV\_IO\_RING}$
B10	H[12] / siul_GPIO[124] / flexpwm1_B[2]
B11	E[15] / siul_GPIO[79] / dspi0_CS1 / siul_EIRQ[27]
B12	E[14] / siul_GPIO[78] / etimer1_ETC[5] / siul_EIRQ[26]
B13	B[3] / siul_GPIO[19] / sscm_DEBUG[3] / lin0_RXD
B14	F[13] / siul_GPIO[93] / etimer1_ETC[4] / siul_EIRQ[31]
B15	B[0] / siul_GPIO[16] / can0_TXD / etimer1_ETC[2] / sscm_DEBUG[0] / siul_EIRQ[15]
B16	$V_{DD\_HV\_IO\_RING}$
B17	$V_{SS\_HV\_IO\_RING}$

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
C1	$V_{DD\_HV\_IO\_RING}$
C2	NC[1]
C3	$V_{SS\_HV\_IO\_RING}$
C4	FCCU_F[1]
C5	D[2] / siul_GPIO[50] / etimer1_ETC[3] / flexpwm0_X[3] / flexray_CB_RX
C6	A[13] / siul_GPIO[13] / flexpwm0_B[2] / dspi2_MISO / flexpwm0_FAULT[0] / siul_EIRQ[12]
C7	$V_{DD\_HV\_REG\_2}$
C8	$V_{DD\_HV\_REG\_2}$
C9	I[0] / siul_GPIO[128] / etimer2_ETC[0] / dspi0_CS4 / flexpwm1_FAULT[0]
C10	JCOMP
C11	H[11] / siul_GPIO[123] / flexpwm1_A[2]
C12	I[1] / siul_GPIO[129] / etimer2_ETC[1] / dspi0_CS5 / flexpwm1_FAULT[1]
C13	F[14] / siul_GPIO[94] / lin1_TXD
C14	B[1] / siul_GPIO[17] / etimer1_ETC[3] / sscm_DEBUG[1] / can0_RXD / can1_RXD / siul_EIRQ[16]
C15	$V_{SS\_HV\_IO\_RING}$
C16	A[4] / siul_GPIO[4] / etimer1_ETC[0] / dspi2_CS1 / etimer0_ETC[4] / mc_rgm_FAB / siul_EIRQ[4]
C17	F[12] / siul_GPIO[92] / etimer1_ETC[3] / siul_EIRQ[30]
D1	F[5] / siul_GPIO[85] / npc_wrapper_MDO[2]
D2	F[4] / siul_GPIO[84] / npc_wrapper_MDO[3]
D3	A[15] / siul_GPIO[15] / etimer1_ETC[5] / can1_RXD / can0_RXD / siul_EIRQ[14]
D4	C[6] / siul_GPIO[38] / dspi0_MOSI / flexpwm0_B[1] / sscm_DEBUG[6] / siul_EIRQ[24]
D5	$V_{SS\_LV\_CORE\_RING}$
D6	$V_{DD\_LV\_CORE\_RING}$
D7	F[0] / siul_GPIO[80] / flexpwm0_A[1] / etimer0_ETC[2] / siul_EIRQ[28]
D8	$V_{DD\_HV\_IO\_RING}$
D9	$V_{SS\_HV\_IO\_RING}$
D10	NC[1]
D11	A[11] / siul_GPIO[11] / dspi2_SCK / flexpwm0_A[0] / flexpwm0_A[2] / siul_EIRQ[10]
D12	E[13] / siul_GPIO[77] / etimer0_ETC[5] / dspi2_CS3 / siul_EIRQ[25]
D13	F[15] / siul_GPIO[95] / lin1_RXD
D14	$V_{DD\_HV\_IO\_RING}$
D15	V_{PP_TEST}[2]
D16	D[14] / siul_GPIO[62] / flexpwm0_B[1] / etimer0_ETC[3]
D17	G[3] / siul_GPIO[99] / flexpwm0_A[2] / etimer0_ETC[4]
E1	MDO0

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
E2	F[6] / siul_GPIO[86] / npc_wrapper_MDO[1]
E3	D[1] / siul_GPIO[49] / etimer1_ETC[2] / ctu0_EXT_TGR / flexray_CA_RX
E4	NMI
E5	NP[3]
E6	NP[3]
E7	NP[3]
E8	NP[3]
E9	NP[3]
E10	NP[3]
E11	NP[3]
E12	NP[3]
E13	NP[3]
E14	NC[1]
E15	C[14] / siul_GPIO[46] / etimer1_ETC[2] / ctu0_EXT_TGR
E16	G[2] / siul_GPIO[98] / flexpwm0_X[2] / dspi1_CS1
E17	I[3] / siul_GPIO[131] / etimer2_ETC[3] / dspi0_CS7 / ctu0_EXT_TGR / flexpwm1_FAULT[3]
F1	H[1] / siul_GPIO[113] / npc_wrapper_MDO[6]
F2	G[12] / siul_GPIO[108] / npc_wrapper_MDO[11]
F3	A[7] / siul_GPIO[7] / dspi1_MOSI / siul_EIRQ[7]
F4	A[8] / siul_GPIO[8] / dspi1_MISO / siul_EIRQ[8]
F5	NP[3]
F6	$V_{DD\_LV\_CORE\_RING}$
F7	$V_{DD\_LV\_CORE\_RING}$
F8	$V_{DD\_LV\_CORE\_RING}$
F9	$V_{DD\_LV\_CORE\_RING}$
F10	$V_{DD\_LV\_CORE\_RING}$
F11	$V_{DD\_LV\_CORE\_RING}$
F12	$V_{DD\_LV\_CORE\_RING}$
F13	NP[3]
F14	NC[1]
F15	C[13] / siul_GPIO[45] / etimer1_ETC[1] / ctu0_EXT_IN / flexpwm0_EXT_SYNC
F16	I[2] / siul_GPIO[130] / etimer2_ETC[2] / dspi0_CS6 / flexpwm1_FAULT[2]
F17	G[4] / siul_GPIO[100] / flexpwm0_B[2] / etimer0_ETC[5]
G1	H[3] / siul_GPIO[115] / npc_wrapper_MDO[4]
G2	$V_{DD\_HV\_IO\_RING}$

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
G3	C[5] / siul_GPIO[37] / dspi0_SCK / sscm_DEBUG[5] / flexpwm0_FAULT[3] / siul_EIRQ[23]
G4	A[6] / siul_GPIO[6] / dspi1_SCK / siul_EIRQ[6]
G5	NP[3]
G6	$V_{DD\_LV\_CORE\_RING}$
G7	$V_{SS\_LV\_CORE\_RING}$
G8	$V_{SS\_LV\_CORE\_RING}$
G9	$V_{SS\_LV\_CORE\_RING}$
G10	$V_{SS\_LV\_CORE\_RING}$
G11	$V_{SS\_LV\_CORE\_RING}$
G12	$V_{DD\_LV\_CORE\_RING}$
G13	NP[3]
G14	D[12] / siul_GPIO[60] / flexpwm0_X[1] / lin1_RXD
G15	H[13] / siul_GPIO[125] / flexpwm1_X[3] / etimer2_ETC[3]
G16	H[9] / siul_GPIO[121] / flexpwm1_B[1] / dspi0_CS7
G17	G[6] / siul_GPIO[102] / flexpwm0_A[3]
H1	G[13] / siul_GPIO[109] / npc_wrapper_MDO[10]
H2	$V_{SS\_HV\_IO\_RING}$
H3	C[4] / siul_GPIO[36] / dspi0_CS0 / flexpwm0_X[1] / sscm_DEBUG[4] / siul_EIRQ[22]
H4	A[5] / siul_GPIO[5] / dspi1_CS0 / etimer1_ETC[5] / dspi0_CS7 / siul_EIRQ[5]
H5	NP[3]
H6	V_{DD_LV}
H7	V_{SS_LV}
H8	V_{SS_LV}
H9	V_{SS_LV}
H10	V_{SS_LV}
H11	V_{SS_LV}
H12	V_{DD_LV}
H13	NP[3]
H14	V_{SS_LV}
H15	$V_{DD\_HV\_REG\_1}$
H16	$V_{DD\_HV\_FLA0}$
H17	H[6] / siul_GPIO[118] / flexpwm1_B[0] / dspi0_CS5
J1	F[7] / siul_GPIO[87] / npc_wrapper_MCKO
J2	G[15] / siul_GPIO[111] / npc_wrapper_MDO[8]
J3	$V_{DD\_HV\_REG\_0}$

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
J4	$V_{DD\_HV\_REG\_0}$
J5	NP[3]
J6	V_{DD_LV}
J7	V_{SS_LV}
J8	V_{SS_LV}
J9	V_{SS_LV}
J10	V_{SS_LV}
J11	V_{SS_LV}
J12	V_{DD_LV}
J13	NP[3]
J14	V_{DD_LV}
J15	$V_{DD\_HV\_REG\_1}$
J16	$V_{SS\_HV\_FLA0}$
J17	H[15] / siul_GPIO[127] / flexpwm1_B[3] / etimer2_ETC[5]
K1	F[9] / siul_GPIO[89] / npc_wrapper_MSEO_B[0]
K2	F[8] / siul_GPIO[88] / npc_wrapper_MSEO_B[1]
K3	NC[1]
K4	C[7] / siul_GPIO[39] / flexpwm0_A[1] / sscm_DEBUG[7] / dspi0_MISO
K5	NP[3]
K6	V_{DD_LV}
K7	V_{SS_LV}
K8	V_{SS_LV}
K9	V_{SS_LV}
K10	V_{SS_LV}
K11	V_{SS_LV}
K12	V_{DD_LV}
K13	NP[3]
K14	NC[1]
K15	H[8] / siul_GPIO[120] / flexpwm1_A[1] / dspi0_CS6
K16	H[7] / siul_GPIO[119] / flexpwm1_X[1] / etimer2_ETC[1]
K17	A[3] / siul_GPIO[3] / etimer0_ETC[3] / dspi2_CS0 / flexpwm0_B[3] / mc_rgm_ABS[2] / siul_EIRQ[3]
L1	F[10] / siul_GPIO[90] / npc_wrapper_EVTO_B
L2	F[11] / siul_GPIO[91] / leo_sor_proxy_EVTI_B
L3	D[9] / siul_GPIO[57] / flexpwm0_X[0] / lin1_TXD
L4	NC[1]

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
L5	NP[3]
L6	V_{DD_LV}
L7	V_{SS_LV}
L8	V_{SS_LV}
L9	V_{SS_LV}
L10	V_{SS_LV}
L11	V_{SS_LV}
L12	V_{DD_LV}
L13	NP[3]
L14	NC[1]
L15	TCK
L16	H[4] / siul_GPIO[116] / flexpwm1_X[0] / etimer2_ETC[0]
L17	B[4] / siul_GPIO[20] / jtagc_TDO
M1	$V_{DD\_HV\_OSC0}$
M2	$V_{DD\_HV\_IO\_RING}$
M3	D[8] / siul_GPIO[56] / dspi1_CS2 / etimer1_ETC[4] / dspi0_CS5 / flexpwm0_FAULT[3]
M4	NC[1]
M5	NP[3]
M6	V_{DD_LV}
M7	V_{DD_LV}
M8	V_{DD_LV}
M9	V_{DD_LV}
M10	V_{DD_LV}
M11	V_{DD_LV}
M12	V_{DD_LV}
M13	NP[3]
M14	C[11] / siul_GPIO[43] / etimer0_ETC[4] / dspi2_CS2
M15	B[5] / siul_GPIO[21] / jtagc_TDI
M16	TMS
M17	H[5] / siul_GPIO[117] / flexpwm1_A[0] / dspi0_CS4
N1	XTAL
N2	$V_{SS\_HV\_IO\_RING}$
N3	D[5] / siul_GPIO[53] / dspi0_CS3 / flexpwm0_FAULT[2]
N4	$V_{SS\_LV\_PLL0\_PLL1}$
N5	NP[3]

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
N6	NP[3]
N7	NP[3]
N8	NP[3]
N9	NP[3]
N10	NP[3]
N11	NP[3]
N12	NP[3]
N13	NP[3]
N14	NC[1]
N15	C[12] / siul_GPIO[44] / etimer0_ETC[5] / dspi2_CS3
N16	A[2] / siul_GPIO[2] / etimer0_ETC[2] / flexpwm0_A[3] / dspi2_MISO / mc_rgm_ABS[0] / siul_EIRQ[2]
N17	G[5] / siul_GPIO[101] / flexpwm0_X[3] / dspi2_CS3
P1	$V_{SS\_HV\_OSC0}$
P2	$\overline{RESET}$
P3	D[6] / siul_GPIO[54] / dspi0_CS2 / flexpwm0_X[3] / flexpwm0_FAULT[1]
P4	$V_{DD\_LV\_PLL0\_PLL1}$
P5	$V_{DD\_LV\_CORE\_RING}$
P6	$V_{SS\_LV\_CORE\_RING}$
P7	B[8] / siul_GPIO[24] / etimer0_ETC[5]
P8	NC[1]
P9	$V_{SS\_HV\_IO\_RING}$
P10	$V_{DD\_HV\_IO\_RING}$
P11	B[14] / siul_GPIO[30] / etimer0_ETC[4] / siul_EIRQ[19]
P12	$V_{DD\_LV\_CORE\_RING}$
P13	$V_{SS\_LV\_CORE\_RING}$
P14	$V_{DD\_HV\_IO\_RING}$
P15	G[10] / siul_GPIO[106] / flexray_DBG2 / dspi2_CS3 / flexpwm0_FAULT[2]
P16	G[8] / siul_GPIO[104] / flexray_DBG0 / dspi0_CS1 / flexpwm0_FAULT[0] / siul_EIRQ[21]
P17	G[7] / siul_GPIO[103] / flexpwm0_B[3]
R1	EXTAL
R2	FCCU_F[0]
R3	$V_{SS\_HV\_IO\_RING}$
R4	D[7] / siul_GPIO[55] / dspi1_CS3 / dspi0_CS4
R5	B[7] / siul_GPIO[23] / lin0_RXD
R6	E[6] / siul_GPIO[70]

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
R7	$V_{DD\_HV\_ADR0}$
R8	B[10] / siul_GPIO[26]
R9	$V_{DD\_HV\_ADR1}$
R10	B[13] / siul_GPIO[29] / lin1_RXD
R11	B[15] / siul_GPIO[31] / siul_EIRQ[20]
R12	C[0] / siul_GPIO[32]
R13	BCTRL
R14	A[1] / siul_GPIO[1] / etimer0_ETC[1] / dspi2_MOSI / siul_EIRQ[1]
R15	$V_{SS\_HV\_IO\_RING}$
R16	D[11] / siul_GPIO[59] / flexpwm0_B[0] / etimer0_ETC[1]
R17	G[9] / siul_GPIO[105] / flexray_DBG1 / dspi1_CS1 / flexpwm0_FAULT[1] / siul_EIRQ[29]
T1	$V_{SS\_HV\_IO\_RING}$
T2	$V_{DD\_HV\_IO\_RING}$
T3	NC[1]
T4	C[1] / siul_GPIO[33]
T5	E[5] / siul_GPIO[69]
T6	E[7] / siul_GPIO[71]
T7	$V_{SS\_HV\_ADR0}$
T8	B[11] / siul_GPIO[27]
T9	$V_{SS\_HV\_ADR1}$
T10	E[9] / siul_GPIO[73]
T11	E[10] / siul_GPIO[74]
T12	E[12] / siul_GPIO[76]
T13	E[0] / siul_GPIO[64]
T14	A[0] / siul_GPIO[0] / etimer0_ETC[0] / dspi2_SCK / siul_EIRQ[0]
T15	D[10] / siul_GPIO[58] / flexpwm0_A[0] / etimer0_ETC[0]
T16	$V_{DD\_HV\_IO\_RING}$
T17	$V_{SS\_HV\_IO\_RING}$
U1	$V_{SS\_HV\_IO\_RING}$
U2	$V_{SS\_HV\_IO\_RING}$
U3	NC[1]
U4	E[4] / siul_GPIO[68]
U5	C[2] / siul_GPIO[34]
U6	E[2] / siul_GPIO[66]
U7	B[9] / siul_GPIO[25]

Table 4. 257 MAPBGA concatenated ball names (continued)

Ball No.	Concatenated Pin Names
U8	B[12] / siul_GPIO[28]
U9	$V_{DD\_HV\_ADV}$
U10	$V_{SS\_HV\_ADV}$
U11	E[11] / siul_GPIO[75]
U12	NC[1]
U13	NC[1]
U14	$V_{DD\_HV\_PMU}$
U15	G[11] / siul_GPIO[107] / flexray_DBG3 / flexpwm0_FAULT[3]
U16	$V_{SS\_HV\_IO\_RING}$
U17	$V_{SS\_HV\_IO\_RING}$

NOTES:
1 Not connected.
2 V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.
3 Ball not populated on substrate.

2.2.2 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for this device.

Table 5. Supply pins

Supply		Package	
Symbol	**Description**	**144 LQFP**	**257 MAPBGA**
VREG control and power supply pins			
BCTRL	Voltage regulator external NPN Ballast base control pin	69	R13
$V_{DD\_LV\_COR}$	Voltage regulator supply voltage	70	VDD_LV[1]
$V_{SS\_LV\_COR}$	Core regulator ground	71	VSS_LV[2]
$V_{DD\_HV\_PMU}$	Core regulator supply	72	U14
ADC0/ADC1 reference voltage and ADC supply			
$V_{DD\_HV\_ADR0}$	ADC0 high reference voltage	50	R7
$V_{SS\_HV\_ADR0}$	ADC0 low reference voltage	51	T7
$V_{DD\_HV\_ADR1}$	ADC1 high reference voltage	56	R9
$V_{SS\_HV\_ADR1}$	ADC1 low reference voltage	57	T9
$V_{DD\_HV\_ADV}$	ADC voltage supply for ADC0 and ADC1	58	U9
$V_{SS\_HV\_ADV}$	ADC ground for ADC0 and ADC1	59	U10
Power Supply pins (3.3 V)			
$V_{DD\_HV\_IO}$	3.3 V Input/Output supply voltage	6	VDD_HV[3]

Table 5. Supply pins (continued)

Supply		Package	
Symbol	**Description**	**144 LQFP**	**257 MAPBGA**
$V_{SS\_HV\_IO}$	3.3 V Input/Output ground	7	VSS_HV[4]
$V_{DD\_HV\_REG\_0}$	VDD_HV_REG_0	16	J3
$V_{DD\_HV\_IO}$	3.3 V Input/Output supply voltage	21	VDD_HV[3]
$V_{SS\_HV\_IO}$	3.3 V Input/Output ground	22	VSS_HV[4]
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	27	M1
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	28	P1
$V_{DD\_HV\_PMU}$	VDD_HV_PMU	72	U14
$V_{SS\_HV\_IO}$	3.3 V Input/Output ground	90	VSS_HV[4]
$V_{DD\_HV\_IO}$	3.3 V Input/Output supply voltage	91	VDD_HV[3]
$V_{DD\_HV\_REG\_1}$	VDD_HV_REG_1	95	H15
$V_{SS\_HV\_FLA}$	VSS_HV_FLA	96	J16
$V_{DD\_HV\_FLA}$	VDD_HV_FLA	97	H16
V_{PP_TEST}[5]	V_{PP_TEST}	107	D15
$V_{DD\_HV\_IO}$	VDD_HV_IO	126	VDD_HV[3]
$V_{SS\_HV\_IO}$	VSS_HV_IO	127	VSS_HV[4]
$V_{DD\_HV\_REG\_2}$	VDD_HV_REG_2	130	C7
Power Supply pins (1.2 V)			
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	17	VSS_HV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	18	VDD_LV[1]
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.	35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.	36	P4
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	39	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	40	VSS_LV[2]

Table 5. Supply pins (continued)

Supply		Package	
Symbol	**Description**	**144 LQFP**	**257 MAPBGA**
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	70	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	71	VSS_LV[2]
$V_{DD\_LV\_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	93	VDD_LV[1]
$V_{SS\_LV\_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	94	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	131	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	132	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	135	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	137	VSS_LV[2]

NOTES:
1 VDD_LV balls are tied together on the 257 MAPBGA substrate.
2 VSS_LV balls are tied together on the 257 MAPBGA substrate.
3 VDD_HV balls are tied together on the 257 MAPBGA substrate.
4 VSS_HV balls are tied together on the 257 MAPBGA substrate.
5 V_{PP_TEST} must always be tied to ground (V_{SS}) for normal operations.

2.2.3 System pins

Table 6 and Table 7 contain information on pin functions for this device. The pins listed in Table 6 are single-function pins. The pins shown in Table 7 are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Package	
			144-pin	257-ball
Dedicated pins				
MDO0	Nexus Message Data Output — line 0	Output only	9	E1
$\overline{\text{NMI}}$	Non Maskable Interrupt	Input only	1	E4
XTALIN	Input for oscillator amplifier circuit and internal clock generator	Input only	29	N1
XTALOUT	Oscillator amplifier output	Output only	30	R1
TMS	JTAG state machine control	Input only	87	M16
TCK	JTAG clock	Input only	88	L15
JCOMP	JTAG compliance select	Input only	123	C10
Reset pin				
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength.	Bidirectional	31	P2

2.2.4 Pin muxing

Table 7 defines the pin list and muxing for this device.

Each row of Table 7 shows all the possible configurations for each pin, via the alternate functions. The alternate functions are shown in the Alternate Function column and are labeled ALT0, ALT1, ALT2, and ALT3. The default function assigned to each pin after reset is indicated by ALT0.

Some pins have more than four alternate functions. These additional alternate functions are shown in the Other Functions column. This column also contains information related to the External Interrupt capability and the boot configuration. Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

NOTE

Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled “Reserved” are to be tied to ground. Not doing so may cause unpredictable device behavior.

Table 7. Pin muxing

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
Port A (16-bit)											
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 DSPI2 —	GPIO[0] ETC[0] SCK —	I/O I/O O —	SIU Lite	Ext. IRQ #0 (input)	S	M	73	T14
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 DSPI2 —	GPIO[1] ETC[1] MOSI —	I/O I/O O —	SIU Lite	Ext. IRQ #1 (input)	S	M	74	R14
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 — FlexPWM0	GPIO[2] ETC[2] — A[3]	I/O I/O — I/O	SIU Lite	Ext. IRQ #2 (input) DSPI2 SIN (input) Boot pin ABS[0] (input) Weak pull down during reset	S	M	84	N16
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 DSPI2 FlexPWM0	GPIO[3] ETC[3] $\overline{CS0}$ B[3]	I/O I/O I/O I/O	SIU Lite	Ext. IRQ #3 (input) Boot pin ABS[2] (input) Weak pull down during reset	S	M	92	K17
A[4]	PCR[4]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer1 DSPI2 eTimer0	GPIO[4] ETC[0] $\overline{CS1}$ ETC[4]	I/O I/O O I/O	SIU Lite	Ext. IRQ #4 (input) Boot pin FAB (input) Weak pull down during reset	S	M	108	C16
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI1 eTimer1 DSPI0	GPIO[5] $\overline{CS0}$ ETC[5] $\overline{CS7}$	I/O I/O I/O O	SIU Lite	Ext. IRQ #5 (input)	S	M	14	H4
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI1 — —	GPIO[6] SCK — —	I/O I/O — —	SIU Lite	Ext. IRQ #6 (input)	S	M	2	G4
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI1 — —	GPIO[7] SOUT — —	I/O O — —	SIU Lite	Ext. IRQ #7 (input)	S	M	10	F3

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[8] — — —	I/O — — —	SIU Lite	Ext. IRQ #8 (input) DSPI1 SIN (input)	S	M	12	F4
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI2 — FlexPWM0	GPIO[9] $\overline{CS1}$ — B[3]	I/O O — I/O		FlexPWM0 FAULT[0] (input)	S	M	134	B6
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI2 FlexPWM0 FlexPWM0	GPIO[10] $\overline{CS0}$ B[0] X[2]	I/O I/O I/O I/O	SIU Lite	Ext. IRQ #9 (input)	S	M	118	A13
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI2 FlexPWM0 FlexPWM0	GPIO[11] SCK A[0] A[2]	I/O I/O I/O I/O	SIU Lite	Ext. IRQ #10 (input)	S	M	120	D11
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI2 FlexPWM0 FlexPWM0	GPIO[12] SOUT A[2] B[2]	I/O O I/O I/O	SIU Lite	Ext. IRQ #11 (input)	S	M	122	A10
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3	SIU Lite — FlexPWM0 —	GPIO[13] — B[2] —	I/O — I/O —	SIU Lite	Ext. IRQ #12 (input) DSPI2 SIN (input) FlexPWM0 FAULT[0] (input)	S	M	136	C6
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3	SIU Lite CAN1 eTimer1 —	GPIO[14] TXD ETC[4] —	I/O O I/O —	SIU Lite	Ext. IRQ #13 (input)	S	M	143	B4
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3	SIU Lite — eTimer1 —	GPIO[15] — ETC[5] —	I/O — I/O —	SIU Lite	Ext. IRQ #14 (input) CAN1 RXD (input) CAN0 RXD (input)	S	M	144	D3

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
Port B (16-bit)											
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3	SIU Lite CAN0 eTimer1 SSCM	GPIO[16] TXD ETC[2] DEBUG[0]	I/O O I/O I/O	SIU Lite	Ext. IRQ #15 (input)	S	M	109	B15
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3	SIU Lite — eTimer1 SSCM	GPIO[17] — ETC[3] DEBUG[1]	I/O — I/O I/O	SIU Lite	Ext. IRQ #16 (input) CAN0 RXD (input) CAN1 RXD (input)	S	M	110	C14
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3	SIU Lite LIN0 — SSCM	GPIO[18] TXD — DEBUG[2]	I/O O — I/O	SIU Lite	Ext. IRQ #17 (input)	S	M	114	A14
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — SSCM	GPIO[19] — — DEBUG[3]	I/O — — I/O		LIN0 RXD (input)	S	M	116	B13
B[4][6]	PCR[20]	ALT0 ALT1 ALT2 ALT3	SIU Lite JTAG — —	GPIO[20] TDO — —	I/O O — —		—	S	F	89	L17
B[5]	PCR[21]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[21] — — —	I/O — — —		JTAG0 TDI (input)	S	M	86	M15
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3	SIU Lite MC_CGM DSPI2 —	GPIO[22] CLKOUT $\overline{CS2}$ —	I/O O O —	SIU Lite	Ext. IRQ #18 (input)	S	M	138	B3
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[23] — — —	I — — —		LIN0 RXD (input) ADC0 AN[0]	—[7]	—[6]	43	R5

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[24] — — —	I — — —		eTimer0 ETC[5] ADC0 AN[1] (input)	—[6]	—[6]	47	P7
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[25] — — —	I — — —		ADC0 – ADC1 AN[11] (input)	—[6]	—[6]	52	U7
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[26] — — —	I — — —		ADC0 – ADC1 AN[12] (input)	—[6]	—[6]	53	R8
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[27] — — —	I — — —		ADC0 – ADC1 AN[13] (input)	—[6]	—[6]	54	T8
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[28] — — —	I — — —		ADC0 – ADC1 AN[14] (input)	—[6]	—[6]	55	U8
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[29] — — —	I — — —		ADC1 AN[0] (input) LIN1 RXD (input)	—[6]	—[6]	60	R10
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[30] — — —	I — — —		Ext. IRQ #19 (input) ADC1 AN[1] (input) eTimer0 ETC[4]	—[6]	—[6]	64	P11
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[31] — — —	I — — —		Ext. IRQ #20 (input) ADC1 AN[2]	—[6]	—[6]	62	R11

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
Port C (16-bit)											
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[32] — — —	I — — —		ADC1 AN[3] (input)	—[6]	—[6]	66	R12
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[33] — — —	I — — —		ADC0 AN[2] (input)	—[6]	—[6]	41	T4
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[34] — — —	I — — —		ADC0 AN[3] (input)	—[6]	—[6]	45	U5
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 FlexPWM0 SSCM	GPIO[36] $\overline{CS0}$ X[1] DEBUG[4]	I/O I/O I/O I/O	SIU Lite	Ext. IRQ #22 (input)	S	M	11	H3
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 — SSCM	GPIO[37] SCK — DEBUG[5]	I/O I/O — I/O	SIU Lite	Ext. IRQ #23 (input) FlexPWM0 FAULT[3] (input)	S	M	13	G3
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 FlexPWM0 SSCM	GPIO[38] SOUT B[1] DEBUG[6]	I/O O I/O I/O	SIU Lite	Ext. IRQ #24 (input)	S	M	142	D4
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3	SIU Lite — FlexPWM0 SSCM	GPIO[39] — A[1] DEBUG[7]	I/O — I/O I/O		DSPI0 SIN (input)	S	M	15	K4
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI2 — FlexPWM0	GPIO[42] $\overline{CS2}$ — A[3]	I/O O — I/O		FlexPWM0 FAULT[1] (input)	S	M	111	A15

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 DSPI2 —	GPIO[43] ETC[4] $\overline{CS2}$ —	I/O I/O O —		—	S	M	80	M14
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 DSPI2 —	GPIO[44] ETC[5] $\overline{CS3}$ —	I/O I/O O —		—	S	M	82	N15
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer1 — —	GPIO[45] ETC[1] — —	I/O I/O — —		FlexPWM0 ext. sync (input) CTU0 EXT_IN (input)	S	M	101	F15
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer1 CTU0 —	GPIO[46] ETC[2] EXT TGR —	I/O I/O O —		—	S	M	103	E15
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay0 eTimer1 FlexPWM0	GPIO[47] CA_TR_ EN ETC[0] A[1]	I/O O I/O I/O		FlexPWM0 ext. sync (input) CTU0 EXT_IN (input)	S	SYM	124	A8
Port D (16-bit)											
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay0 eTimer1 FlexPWM0	GPIO[48] CA_TX ETC[1] B[1]	I/O O I/O I/O		—	S	SYM	125	B8
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	SIU Lite — eTimer1 CTU0	GPIO[49] — ETC[2] EXT_TRG	I/O — I/O O		FlexRay0 CA_RX (input)	S	M	3	E3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	SIU Lite — eTimer1 FlexPWM0	GPIO[50] — ETC[3] X[3]	I/O — I/O I/O		FlexRay0 CB_RX (input)	S	M	140	C5

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay0 eTimer1 FlexPWM0	GPIO[51] CB_TX ETC[4] A[3]	I/O O I/O I/O		—	S	SYM	128	A7
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay0 eTimer1 FlexPWM0	GPIO[52] CB_TR_EN ETC[5] B[3]	I/O O I/O I/O		—	S	SYM	129	B7
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 — —	GPIO[53] $\overline{CS3}$ — —	I/O O — —		FlexPWM0 FAULT[2] (input)	S	M	33	N3
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 — FlexPWM0	GPIO[54] $\overline{CS2}$ — X[3]	I/O O — I/O		FlexPWM0 FAULT[1] (input)	S	M	34	P3
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI1 — DSPI0	GPIO[55] $\overline{CS3}$ — $\overline{CS4}$	I/O O — O		SWG ANAOUT	S	M	37	R4
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI1 eTimer1 DSPI0	GPIO[56] $\overline{CS2}$ ETC[4] $\overline{CS5}$	I/O O I/O O		FlexPWM0 FAULT[3] (input)	S	M	32	M3
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 LIN1 —	GPIO[57] X[0] TXD —	I/O I/O O —		—	S	M	26	L3
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[58] A[0] — —	I/O I/O — —		eTimer0 ETC[0]	S	M	76	T15

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[59] B[0] — —	I/O I/O — —		eTimer0 ETC[1]	S	M	78	R16
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[60] X[1] — —	I/O I/O — —		LIN1 RXD (input)	S	M	99	G14
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[62] B[1] — —	I/O I/O — —		eTimer0 ETC[3]	S	M	105	D16
Port E (16-bit)											
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[64] — — —	I — — —		ADC1 AN[5] (input)	—[6]	—[6]	68	T13
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[66] — — —	I — — —		ADC0 AN[5] (input)	—[6]	—[6]	49	U6
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[68] — — —	I — — —		ADC0 AN[7] (input)	—[6]	—[6]	42	U4
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[69] — — —	I — — —		ADC0 AN[8] (input)	—[6]	—[6]	44	T5
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[70] — — —	I — — —		ADC0 AN[4] (input)	—[6]	—[6]	46	R6

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[71] — — —	I — — —		ADC0 AN[6] (input)	—[6]	—[6]	48	T6
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[73] — — —	I — — —		ADC1 AN[7] (input)	—[6]	—[6]	61	T10
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[74] — — —	I — — —	—	ADC1 AN[8] (input)	—[6]	—[6]	63	T11
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[75] — — —	I — — —	—	ADC1 AN[4] (input)	—[6]	—[6]	65	U11
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[76] — — —	I — — —	—	ADC1 AN[6] (input)	—[6]	—[6]	67	T12
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer0 DSPI3 —	GPIO[77] ETC[5] $\overline{CS3}$ —	I/O I/O O —	—	Ext. IRQ #25 (input)	S	M	117	D12
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer1 — —	GPIO[78] ETC[5] — —	I/O I/O — —	—	Ext. IRQ #26 (input)	S	M	119	B12
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 — —	GPIO[79] $\overline{CS1}$ — —	I/O O — —	—	Ext. IRQ #27 (input)	S	M	121	B11

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
Port F (16-bit)											
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[80] A[1] — —	I/O I/O — —	SIU Lite	Ext. IRQ #28 (input) eTimer0 ETC[2]	S	M	133	D7
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	SIU Lite DSPI0 — —	GPIO[83] $\overline{CS6}$ — —	I/O O — —	—		S	M	139	B5
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[84] — MDO[3] —	I/O — O —	—	—	S	F	4	D2
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[85] — MDO[2] —	I/O — O —	—	—	S	F	5	D1
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[86] — MDO[1] —	I/O — O —	—	—	S	F	8	E2
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[87] — MCKO —	I/O — O —	—	—	S	F	19	J1
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[88] — $\overline{MSEO1}$ —	I/O — O —	—	—	S	F	20	K2
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[89] — $\overline{MSEO0}$ —	I/O — O —	—	—	S	F	23	K1

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[90] — $\overline{\text{EVTO}}$ —	I/O — O —	—	—	S	F	24	L1
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[91] — NEX_EN —	I/O — I —		Nexus0 $\overline{\text{EVTI}}$ (input)	S	M	25	L2
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer1 — —	GPIO[92] ETC[3] — —	I/O I/O — —	SIU Lite	Ext. IRQ #30 (input)	S	M	106	C17
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer1 — —	GPIO[93] ETC[4] — —	I/O I/O — —	SIU Lite	Ext. IRQ #31 (input)	S	M	112	B14
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	SIU Lite LIN1 — —	GPIO[94] TXD — —	I/O O — —	—	—	S	M	115	C13
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3	SIU Lite — — —	GPIO[95] — — —	I/O — — —		LIN1 RXD (input)	S	M	113	D13
Port G (16-bit)											
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3	SIU Lite FCCU0 — —	GPIO[96] F[0] — —	I/O I/O — —		Ext. IRQ #30 (input)	S	M	38	R2
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3	SIU Lite FCCU0 — —	GPIO[97] F[1] — —	I/O I/O — —		Ext. IRQ #31 (input)	S	M	141	C4

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 DSPI1 —	GPIO[98] X[2] $\overline{CS1}$ —	I/O I/O O —	—	—	S	M	102	E16
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[99] A[2] — —	I/O I/O — —	—	eTimer ETC[4]	S	M	104	D17
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[100] B[2] — —	I/O I/O — —		eTimer ETC[5]	S	M	100	F17
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 DSPI2 —	GPIO[101] X[3] $\overline{CS2}$ —	I/O I/O O —	—	—	S	M	85	N17
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[102] A[3] — —	I/O I/O — —	—	—	S	M	98	G17
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM0 — —	GPIO[103] B[3] — —	I/O I/O — —	—	—	S	M	83	P17
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay DSPI0 —	GPIO[104] DBG0 $\overline{CS1}$ —	I/O O O —		Ext. IRQ #21 (input) FlexPWM0 FAULT[0] (input)	S	M	81	P16
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay DSPI1 —	GPIO[105] DBG1 $\overline{CS1}$ —	I/O O O —		Ext. IRQ #29 (input) FlexPWM0 FAULT[1] (input)	S	M	79	R17

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay DSPI2 —	GPIO[106] DBG2 $\overline{CS3}$ —	I/O O O —		FlexPWM0 FAULT[2] (input)	S	M	77	P15
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexRay — —	GPIO[107] DBG3 — —	I/O O — —		FlexPWM0 FAULT[3] (input)	S	M	75	U15
G[12]	PCR[108]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[108] — MDO[11] —	I/O — O —	—	—			—	F2
G[13]	PCR[109]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[109] — MDO[10] —	I/O — O —	—	—			—	H1
G[14]	PCR[110]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[110] — MDO[9] —	I/O — O —	—	—			—	A6
G[15]	PCR[111]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[111] — MDO[8] —	I/O — O —	—	—			—	J2
Port H (16-bit)											
H[0]	PCR[112]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[112] — MDO[7] —	I/O — O —	—	—			—	A5
H[1]	PCR[113]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[113] — MDO[6] —	I/O — O —	—	—			—	F1

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
H[2]	PCR[114]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[114] — MDO[5] —	I/O — O —	—	—			—	A4
H[3]	PCR[115]	ALT0 ALT1 ALT2 ALT3	SIU Lite — Nexus0 —	GPIO[115] — MDO[4] —	I/O — O —	—	—			—	G1
H[4]	PCR[116]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 eTimer2 —	GPIO[116] X[0] ETC[0] —	I/O I/O I/O —	—	—			—	L16
H[5]	PCR[117]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 — DSPI0	GPIO[117] A[0] — CS4	I/O I/O — O	—	—			—	M17
H[6]	PCR[118]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 — DSPI0	GPIO[118] B[0] — CS5	I/O I/O — O	—	—			—	H17
H[7]	PCR[119]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 eTimer2 —	GPIO[119] X[1] ETC[1] —	I/O I/O I/O —	—	—			—	K16
H[8]	PCR[120]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 — DSPI0	GPIO[120] A[1] — CS6	I/O I/O — O	—	—			—	K15
H[9]	PCR[121]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 — DSPI0	GPIO[121] B[1] — CS7	I/O I/O — O	—	—			—	G16

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
H[10]	PCR[122]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 eTimer2 —	GPIO[122] X[2] ETC[2] —	I/O I/O I/O —	—	—			—	A11
H[11]	PCR[123]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1	GPIO[123] A[2]	I/O I/O	—	—			—	C11
H[12]	PCR[124]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1	GPIO[124] B[2]	I/O I/O — —	—	—			—	B10
H[13]	PCR[125]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 eTimer2 —	GPIO[125] X[3] ETC[3] —	I/O I/O I/O —	—	—			—	G15
H[14]	PCR[126]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 eTimer2 —	GPIO[126] A[3] ETC[4] —	I/O I/O I/O —	—	—			—	A12
H[15]	PCR[127]	ALT0 ALT1 ALT2 ALT3	SIU Lite FlexPWM1 eTimer2 —	GPIO[127] B[3] ETC[5] —	I/O I/O I/O —	—	—			—	J17
Port I (4-bit)											
I[0]	PCR[128]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer2 DSPI0 —	GPIO[128] ETC[0] CS4 —	I/O I/O O —	FlexPWM1	Fault[0]			—	C9
I[1]	PCR[129]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer2 DSPI0 —	GPIO[129] ETC[1] CS5 —	I/O I/O O —	FlexPWM1	Fault[1]			—	C12

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

Table 7. Pin muxing (continued)

Port Pin	PCR Register	Functions						Pad Speed[1]		Pin	
		Alternate Function[2,3]	IBE = 0[4]			IBE = 1 (always inputs)					
			Peripheral[5]	Function	I/O Direction	Peripheral	Functions	SRC = 0	SRC = 1	144-pin	257-ball
I[2]	PCR[130]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer2 DSPI0 —	GPIO[130] ETC[2] CS6 —	I/O I/O O —	FlexPWM1	Fault[2			—	F16
I[3]	PCR[131]	ALT0 ALT1 ALT2 ALT3	SIU Lite eTimer2 DSPI0 CTU0	GPIO[131] ETC[3] CS7 EXT. TGR	I/O I/O O O	FlexPWM1	Fault[3]			—	E17

NOTES:

1 Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register. S = Slow, M = Medium, F = Fast, SYM = Symmetric (FlexRay).

2 ALT0 is the primary (default) function for each port after reset.

3 Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module.
– PCR[PA] = 00 → ALT0
– PCR[PA] = 01 → ALT1
– PCR[PA] = 10 → ALT2
– PCR[PA] = 11→ ALT3
This bitfield selects the output and input/output functions. To use one of the input-only functions, the PCR[IBE] bit must be written to ‘1’, regardless of the value of PCR[PA]. For this reason, the value corresponding to an input-only function is reported as “—”.

4 Alternate input functions are chosen by setting the values of the PCR[IBE] bit in the SIU module.
– PCR[IBE] = 0 → Input/out alternate functions (default)
– PCR[IBE] = 1 → Input-only alternate functions
To use one of the input-only functions, the PCR[IBE] bit must be written to ‘1’, regardless of the value of PCR[PA]. For this reason, the value corresponding to an input-only function is reported as “—”.

5 Module included on the device.

6 The default function of this pin out of reset is ALT1 (TDO).

7 Input-only. Pad speed does not apply.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5643L products in 257 MAPBGA packages

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - — P: parameter is guaranteed by production testing of each individual device.
  - — C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - — T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - — D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	4.0[3, 4]	V
$V_{SS\_HV\_REG}$	SR	3.3 V voltage regulator reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	3.6[3, 4]	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	3.6[3, 4]	V
$V_{SS\_HV\_FLA}$	SR	Flash ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.0[3, 4]	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADR0}$[5] $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC0 high reference voltage 3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC0 ground and low reference voltage ADC1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.0[3, 4]	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V

Table 8. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Min	Max[2]	Unit
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up	—	0.5	3.0×10^6 (3.0 V/sec)	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3[6]	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

NOTES:
1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. 5.3 V for 10 hours cumulative over lifetime of device, 3.3 V +10% for time remaining.
4. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
5. $V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$ cannot be operated be operated at different voltages, and need to be supplied by the same voltage source.
6. Only when V_{DD} < 5.2 V.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_REG}$	SR	3.3 V voltage regulator reference voltage	—	0	0	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_FLA}$	SR	Flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_ADR0}$[2] $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC0 high reference voltage 3.3 V / 5.0 V ADC1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.3		V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_AD0}$ $V_{SS\_HV\_AD1}$	SR	ADC0 ground and low reference voltage ADC1 ground and low reference voltage	—	0	0	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD\_LV\_REGCOR}$[3]	SR	Internal supply voltage	—	—	—	V

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{SS\_LV\_REGCOR}$[4]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$[2]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$[2]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_PLL}$[3]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} ≤ 120 MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

NOTES:
1. Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. $V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$ cannot be operated be operated at different voltages, and need to be supplied by the same voltage source.
3. Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.
4. For the device to function properly, the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter, if one is used.

3.4 Thermal characteristics

Table 10. Thermal characteristics for 144 LQFP package[1]

No.	Symbol		Parameter	Conditions	Value	Unit
1	$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	TBD	°C/W
2	$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Four layer board – 2s2p	TBD	°C/W
5	$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	TBD	°C/W
6	$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	TBD	°C/W
7	Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	TBD	°C/W

NOTES:
1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 257 MAPBGA package[1]

No.	Symbol		Parameter	Conditions	Value	Unit
1	$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	TBD	°C/W
2	$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Four layer board – 2s2p	TBD	°C/W
5	$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	TBD	°C/W
6	$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	TBD	°C/W
7	Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	TBD	°C/W

NOTES:
1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.4.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.5 Electromagnetic Interference (EMI) characteristics

Table 12. EMI testing specifications[1]

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1		SR	Scan range	—	0.15	—	1000	MHz
2		SR	Operating frequency	—	—	—	120	MHz
3	$V_{DD\_LV\_REGCOR}$ $V_{DD\_LV\_CORx}$ $V_{DD\_LV\_PLL}$	SR	LV operating voltages	—	—	1.2	—	V
4	$V_{DD\_HV\_REG}$ $V_{DD\_HV\_AD1}$ $V_{DD\_HV\_AD0}$ $V_{DD\_HV\_FL}$ $V_{DD\_HV\_OSC}$ $V_{DD\_HV\_IOx}$	SR	HV operating voltages	—	—	3.3	—	V
5	$V_{DD\_HV\_REG}$ $V_{DD\_HV\_AD1}$ $V_{DD\_HV\_AD0}$ $V_{DD\_HV\_FL}$ $V_{DD\_HV\_OSC}$ $V_{DD\_HV\_IOx}$	SR	Maximum amplitude	Device settings chosen for worst-case emissions from typical use configuration[2]	—	—	TBD	dBµV
6	$V_{DD\_HV\_REG}$ $V_{DD\_HV\_AD1}$ $V_{DD\_HV\_AD0}$ $V_{DD\_HV\_FL}$ $V_{DD\_HV\_OSC}$ $V_{DD\_HV\_IOx}$	SR	Maximum amplitude	No PLL frequency modulation	—	—	TBD	dBµV
7	$V_{DD\_HV\_REG}$ $V_{DD\_HV\_AD1}$ $V_{DD\_HV\_AD0}$ $V_{DD\_HV\_FL}$ $V_{DD\_HV\_OSC}$ $V_{DD\_HV\_IOx}$	SR	Maximum amplitude	± 2% PLL frequency modulation	—	—	TBD	dBµV
8	T_A	SR	Operating temperature	—	–40	—	125	°C

NOTES:
1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03 and IEC 61967-1, 2.
2 Design target only, subject to change after silicon characterization.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (*n* + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 13. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

NOTES:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 14. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The MPC5643L always powers up using HPREG1 if an external NPN transistor is present. Then the MPC5643L makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off. The supported bipolar transistor is a BCP68 from ON Semiconductor.

Table 15. HPREG1, HPREG2, Main LVDs, Digital HVD, and Digital LVD electrical specifications

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Units
1		SR	External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
2		SR	Combined ESR of external capacitor	—	0.03	—	0.5	Ω
3		SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
4	C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	—	—	300	nF
5	t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms
6			Main high voltage detectors upper threshold	—	—	—	2.9	V
7			Main high voltage detectors lower threshold	—	2.6	—	—	V
8			Digital high voltage detector upper threshold	Before a destructive reset initialization phase completion		—	1.5	V
9			Digital high voltage detector upper threshold	After a destructive reset initialization phase completion	1.32	—	1.4	V
10			Digital high voltage detector lower threshold	Before a destructive reset initialization phase completion	1.330	—	1.4	V
11			Digital low voltage detector lower threshold	—	1.080	—	1.110	V
12			POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V
13		SR	Supply ramp time	—	0.5×10^6	—	3	V/s

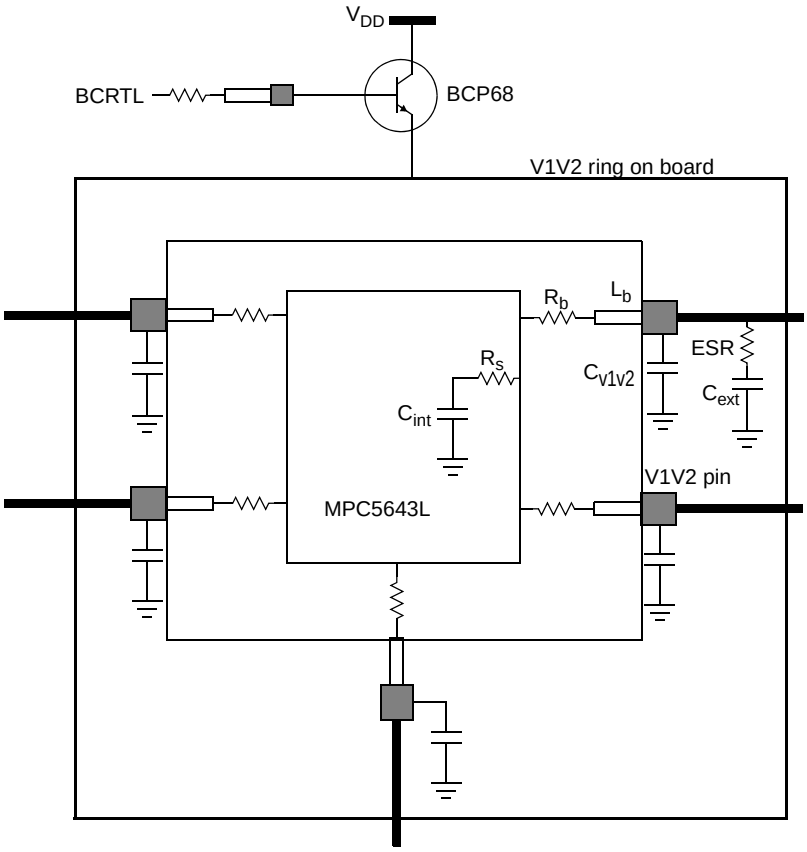


Figure 4. BCP68 Board schematic example

NOTE

The combined ESR of the capacitors used on 1.2 V pins (V1V2 in the picture) shall be in the range of 30 mΩ to 150 mΩ. The minimum value of the ESR is constrained by the resonance caused by the external components, bonding inductance, and internal decoupling. The minimum ESR is required to avoid the resonance and make the regulator stable.

3.9 DC electrical characteristics

Table 16 gives the DC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IOx} < 3.6\ V$).

Table 16. DC electrical characteristics[1]

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1[2]	—	V
V_{IL}	P	Maximum level input voltage	—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IOx}$ + 0.1[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V

Table 16. DC electrical characteristics[1] (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{INJ}	P	DC injection current per pin	—	–1	1	mA
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	µA
			$V_{IN} = V_{IH}$	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_J = –40 to +150 °C	—	1 µA	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_J = –40 to +150 °C	—	0.5 µA	µA
V_{ILR}	P	$\overline{\text{RESET}}$, low level input voltage	—	–0.1[2]	0.35 $V_{DD\_HV\_IOx}$	V
V_{IHR}	P	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$+0.1[2]	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	0.5	V
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	

NOTES:
1 These specifications are design targets and subject to change per device characterization.
2 "SR" parameter values must not exceed the absolute maximum ratings shown in Table 8.

3.10 Temperature sensor electrical characteristics

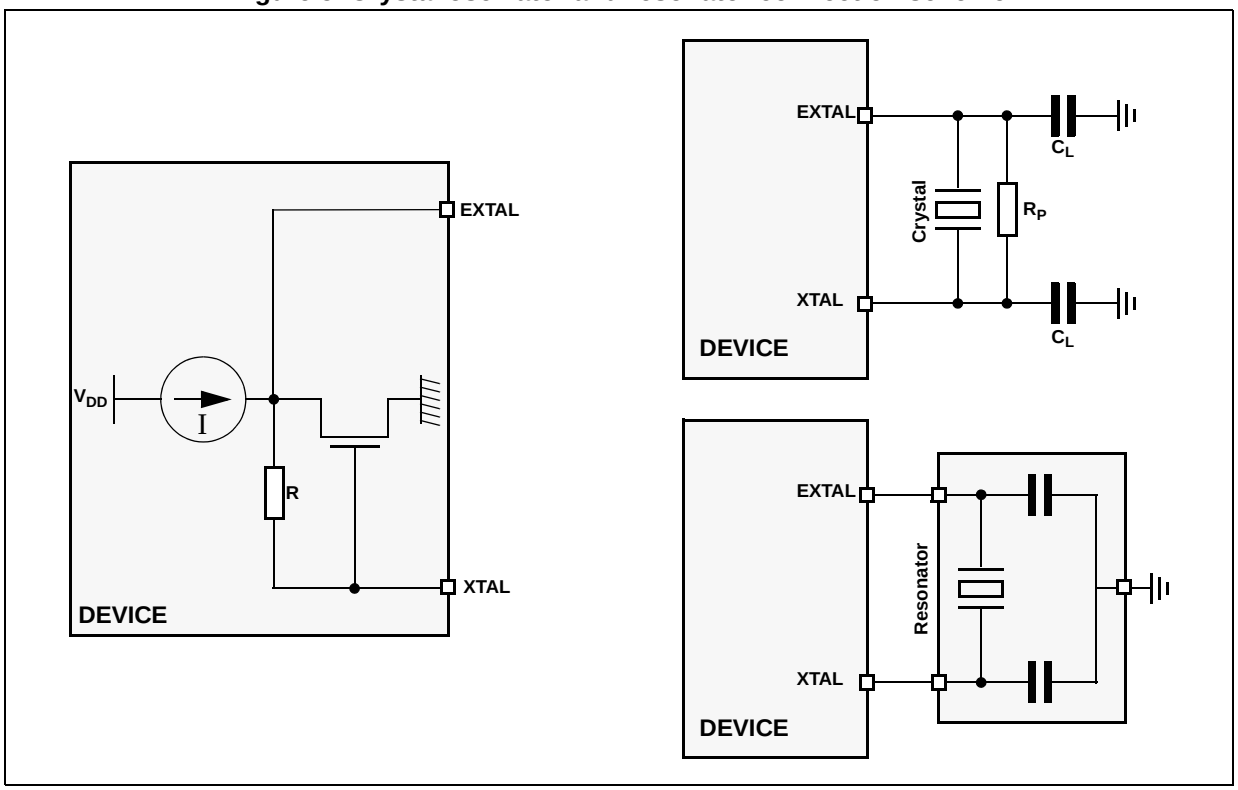
Table 17. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = –40 °C to T_A = 25 °C	–10	10	°C
			$T_J = T_A$ to 125 °C	–7	7	°C
T_S	D	Minimum sampling period	—	4	—	µs

3.11 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver. Figure 5 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Figure 5. Crystal oscillator and resonator connection scheme



NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Figure 6. Main oscillator electrical characteristics

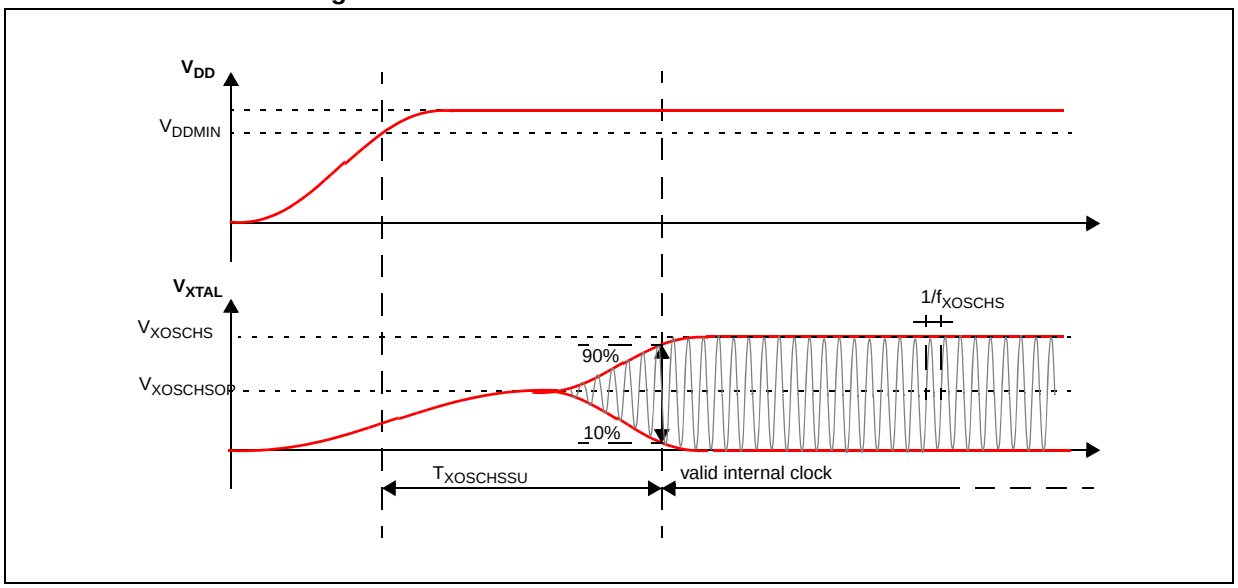


Table 18. Main oscillator electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	D	Oscillator transconductance	V_{DD} = 3.3 V ±10%	4.5	—	11	mA/V
V_{XOSCHS}	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz	1.3	—	—	V
			f_{OSC} = 40 MHz	1.1	—	—	
$V_{XOSCHSOP}$	D	Oscillation operating point	—	—	0.82	—	V
I_{XOSCHS}	D	Oscillator consumption	—	—	—	3.5	mA
$T_{XOSCHSSU}$	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
			f_{OSC} = 16, 40 MHz, OSCILLATOR_MARGIN = 1	—	—	2	
V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

NOTES:
1 V_{DD} = 3.3 V ±10%, T_J = –40 to +150 °C, unless otherwise specified.

3.12 FMPLL electrical characteristics

Table 19. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	PLL reference frequency range[1]	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120[2]	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip PLL frequency[2]	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window[3]	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency[4,5]	—	20	—	TBD	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs

Table 19. FMPLL electrical characteristics (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
t_{lpll}	D	PLL lock time [6, 7]	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge), f_{SYS} maximum	TBD	—	TBD	% f_{CLKOUT}
			Long-term jitter (avg. over 2 ms interval), f_{SYS} maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±500	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% f_{sys}
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth	Center spread	±0.25	—	±4.0[12]	% f_{sys}
			Down Spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency[13]	—	—	—	100	kHz

NOTES:
1 Considering operation with PLL not bypassed.
2 With FM, +2% maximum.
3 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5 f_{VCO} self clock range is 20-150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8 This value is determined by the crystal manufacturer and board design.
9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
10 Proper PC board layout procedures must be followed to achieve specifications.
11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
12 This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
13 Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50kHz.

3.13 16 MHz RC oscillator electrical characteristics

Table 20. RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_J = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation with respect to f_{RC}.	—	—	—	±5	%
$\Delta_{RCMTRIM}$	P	Post trim accuracy: The variation of the PTF[1] from the 16 MHz clock	T_J = 25 °C	—	—	±1	%

NOTES:
1 PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature.

3.14 ADC electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

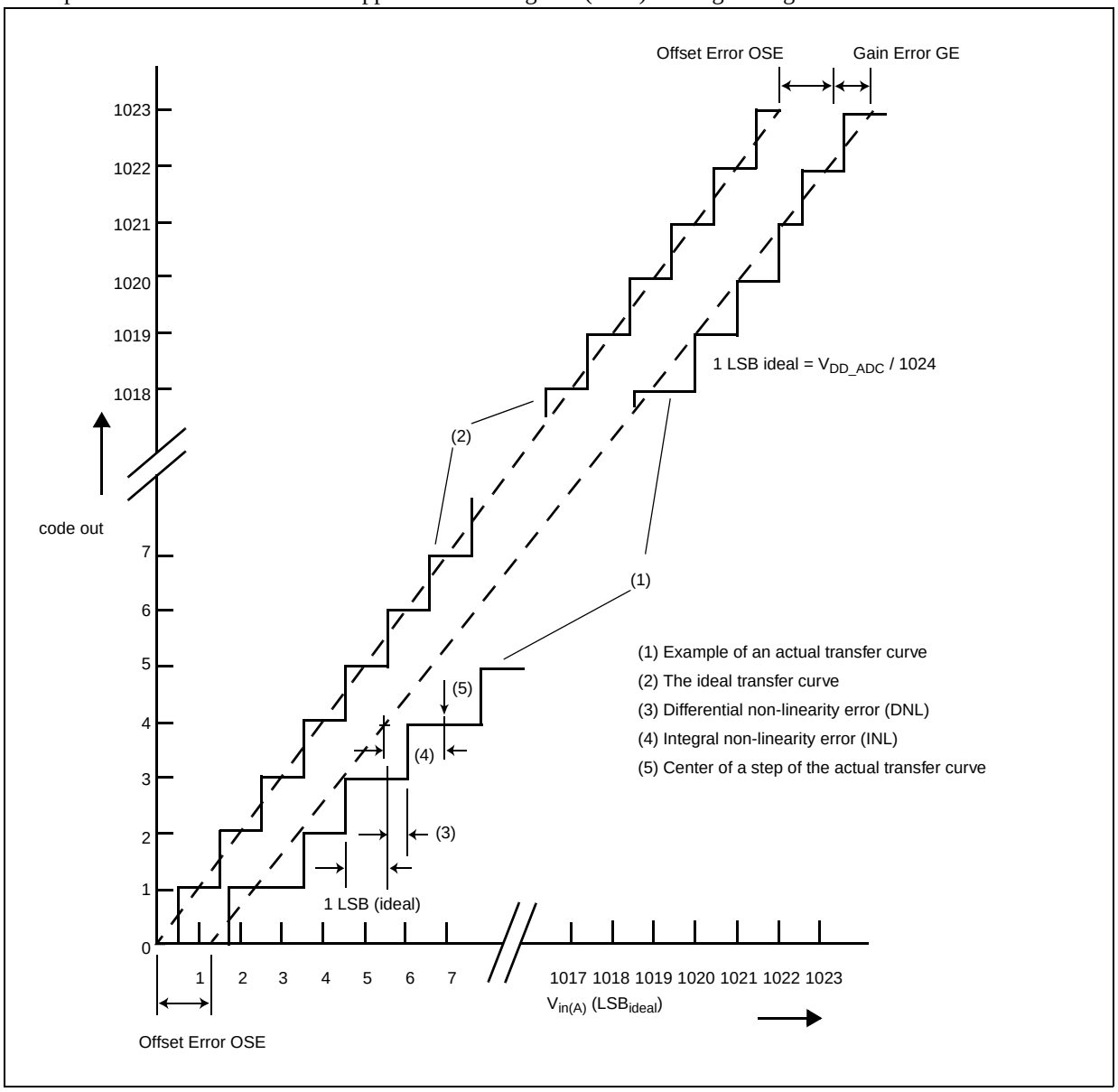


Figure 21. ADC Characteristics and Error Definitions

3.14.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_C \times C_S)$), where f_C represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 7:

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 7}$$

Equation 7 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

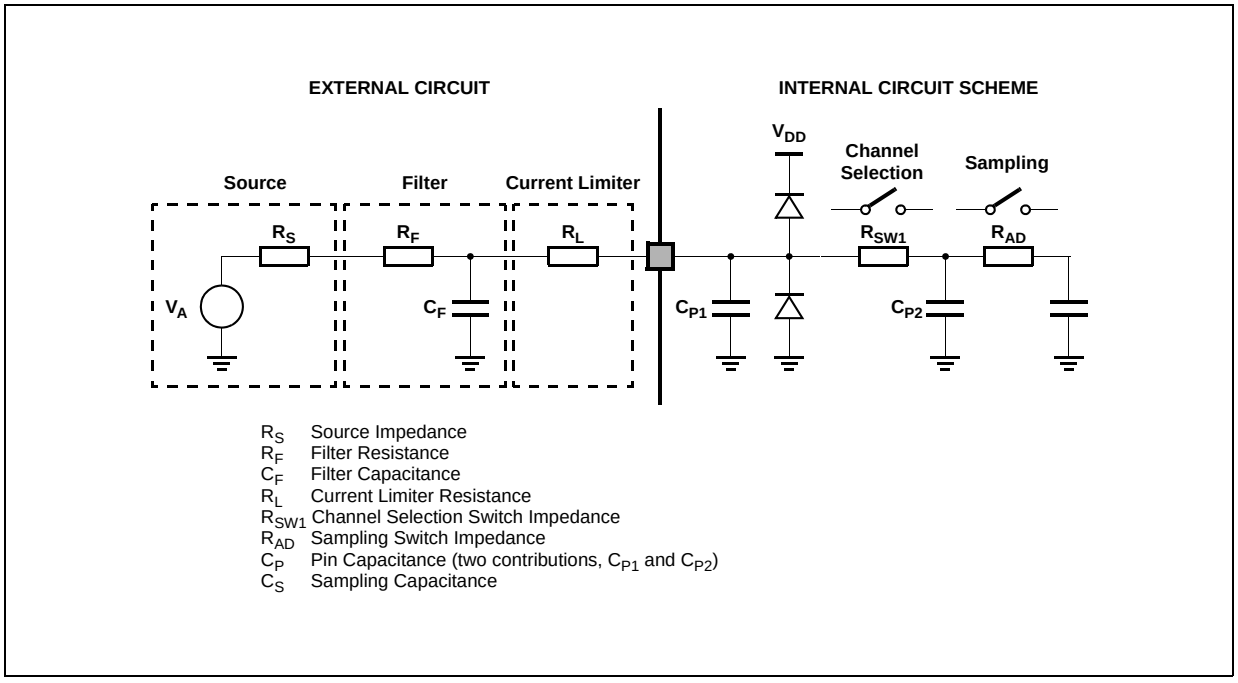


Figure 22. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 22): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

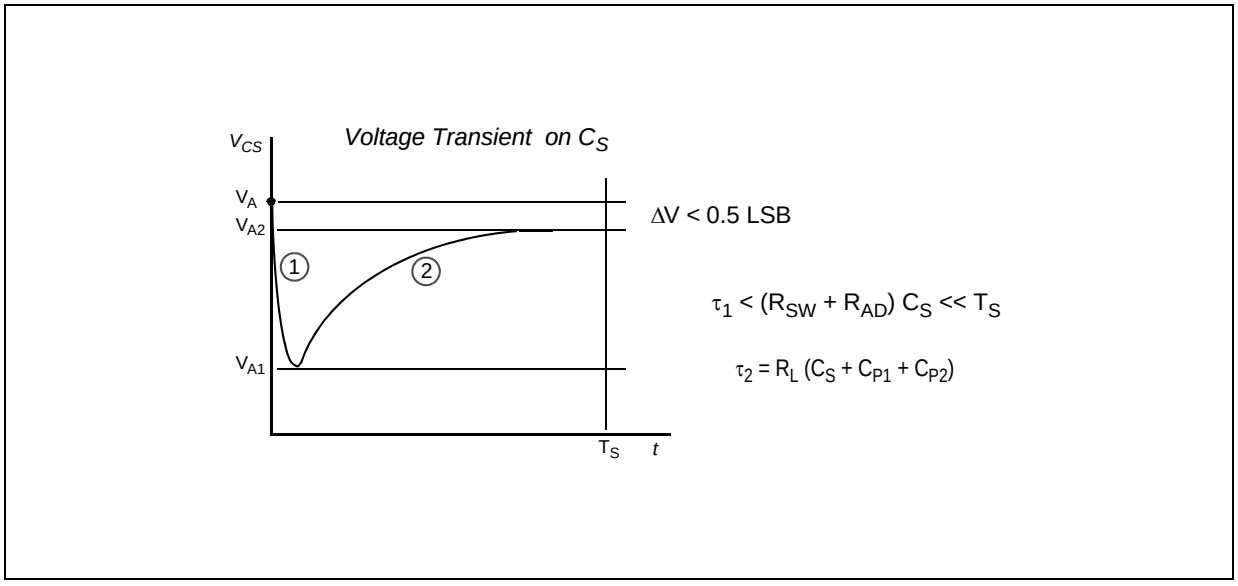


Figure 23. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 8}$$

  Equation 8 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S \qquad \textit{Eqn. 9}$$

  The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 10:

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2}) \qquad \textit{Eqn. 10}$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2}) \qquad \textit{Eqn. 11}$$

  In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S \quad \textit{Eqn. 12}$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 13 must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S) \quad \textit{Eqn. 13}$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

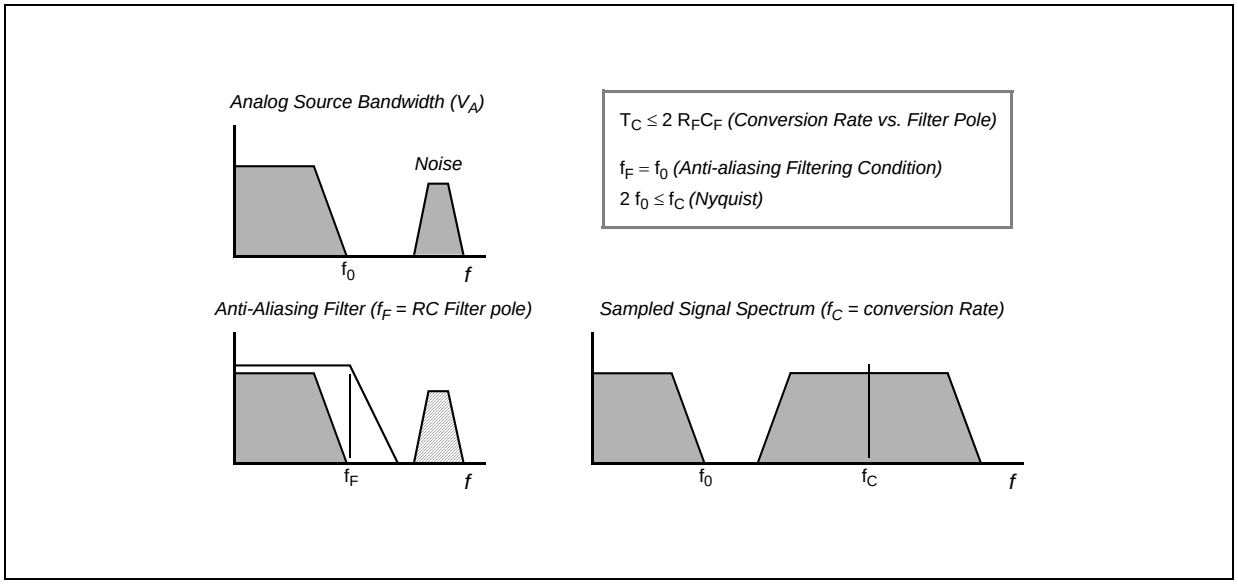


Figure 24. Spectral Representation of Input Signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 14 between the ideal and real sampled voltage on C_S:

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S} \quad \textit{Eqn. 14}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 15

$$C_F > 2048 \bullet C_S$$

Table 25. ADC conversion characteristics (operating)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
f_s	SR	Sampling frequency	—	—	—	1.00	MHz
t_{ADC_S}	D	Sample time[3]	TBD	TBD	—	—	ns
			TBD	—	—	TBD	µs
t_{ADC_C}	P	Conversion time[4]	TBD	0.625	—	—	µs
C_S[5]	D	ADC input sampling capacitance	—	—	—	7.32	pF
C_{P1}[5]	D	ADC input pin capacitance 1	—	—	—	TBD	pF
C_{P2}[5]	D	ADC input pin capacitance 2	—	—	—	TBD	pF
R_{SW1}[5]	D	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.6	kΩ
			V_{REF} range = 3.0 to 3.6 V	—	—	0.9	kΩ
R_{AD}[5]	D	Internal resistance of analog source	—	—	—	825	Ω
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	TBD	—	TBD	mA
INL	P	Integral non linearity	—	–3	—	3	LSB
DNL	P	Differential non linearity	—	–1.0	—	1.0	LSB
OFS	T	Offset error	—	–4	—	4	LSB
GNE	T	Gain error	—	—	±1	—	LSB
TUE	P	Total unadjusted error without current injection	—	–6	—	6	LSB
TUE	T	Total unadjusted error with current injection	—	TBD	—	TBD	LSB

NOTES:
1. V_{DD} = 3.3 V, T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within tADC_S. After the end of the sample time tADC_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock tADC_S depend on programming.
4. This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 22.

3.15 Flash memory electrical characteristics

Table 26. Flash program and erase electrical specifications

No.	Symbol		Parameter	Min	Typ[1]	Factory Avg[2]	Initial Max[3]	Lifetime Max[4]	Unit
1	$T_{DWPROGRAM}$	*[5]	Double word (64 bits) program time[6]	—	39	—	—	500	µs
2	$T_{PPROGRAM}$	*[5]	Page(128 bits) program time[6]	—	48	53	100	500	µs
3	$T_{16KPPERASE}$	*[5]	16 KB block pre-program and erase time	—	TBD	TBD	500	5000	ms
4	$T_{48KPPERASE}$	*[5]	48 KB block pre-program and erase time	—	TBD	TBD	750	5000	ms
5	$T_{64KPPERASE}$	*[5]	64 KB block pre-program and erase time	—	TBD	TBD	900	5000	ms
6	$T_{128KPPERASE}$	*[5]	128 KB block pre-program and erase time	—	TBD	TBD	1300	7500	ms
7	$T_{256KPPERASE}$	*[5]	256 KB block pre-program and erase time	—	TBD	TBD	2600	15000	ms

NOTES:
1 Typical program and erase times assume nominal supply values and operation at T_J = 25 °C. These values are characterized, but not tested.

2 Factory Average program and erase times represent the effective performance averaged over > 1024 pages or blocks, and are provided for factory throughput estimation assuming < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are characterized, but not tested.

3 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are verified at production test.

4 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.

5 See Notes for individual specifications, as shown in column headings.

6 Actual hardware programming times. These do not include software overhead.

Table 27. Flash module life

No.	Symbol		Parameter	Value			Unit
				Min	Typ	Max	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range[1]	100,000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range[1].	1,000	100,000[2] (TBD)	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature[3] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

NOTES:
1 Operating temperature range is T_J from –40 °C to 150 °C.

Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

3 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 28. Pad AC specifications (3.3 V, IPP_HVE = 0)[1]

No.	Pad		Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25
5	Pull Up/Down (3.6 V max)	D	—	—	—	—	—	TBD	—	—	—	—	—	—	50

NOTES:
1 Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition.
2 Slope at rising/falling edge.
3 Data based on characterization results, not tested in production.

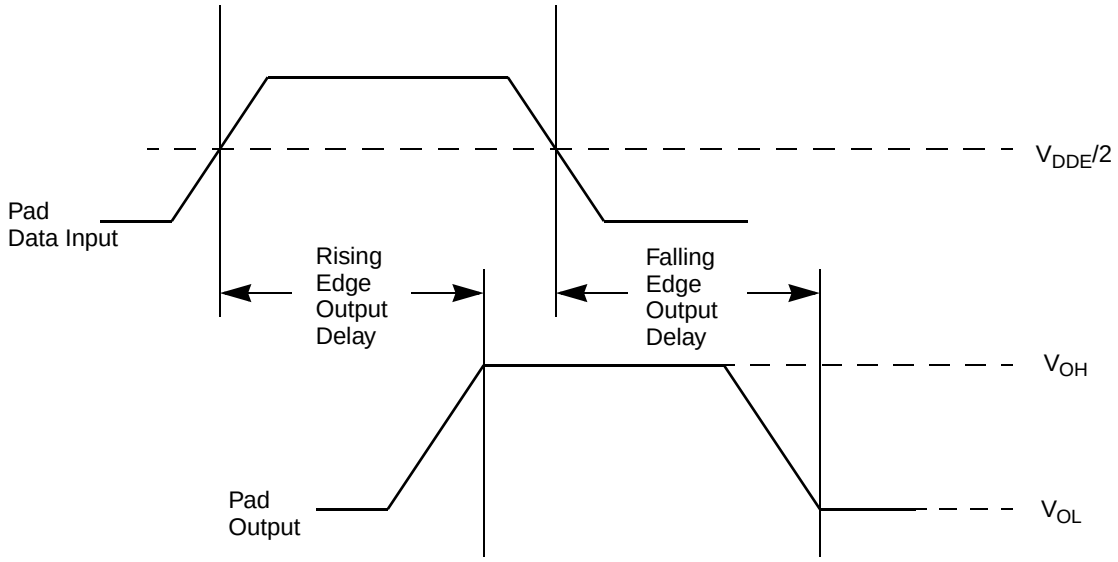


Figure 16. Pad output delay

3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The MPC5643L implements a dedicated bidirectional RESET pin.

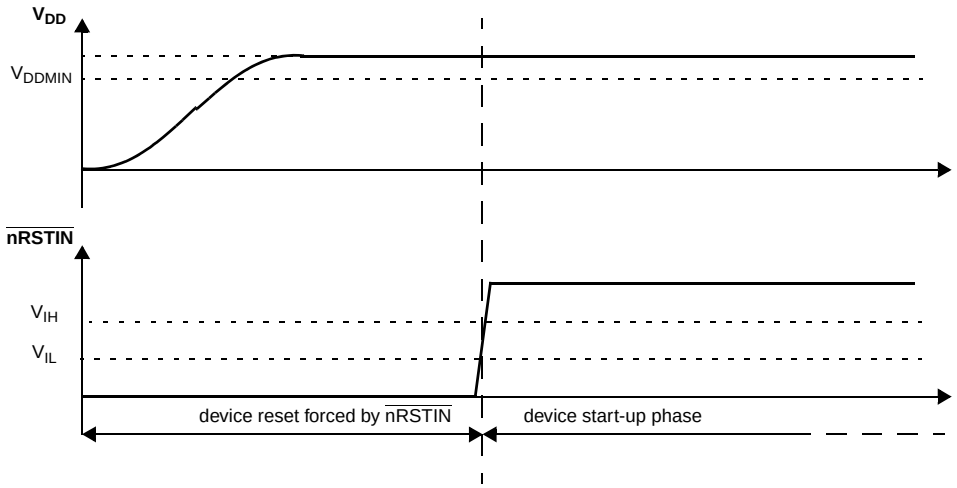


Figure 29. Start-up reset requirements

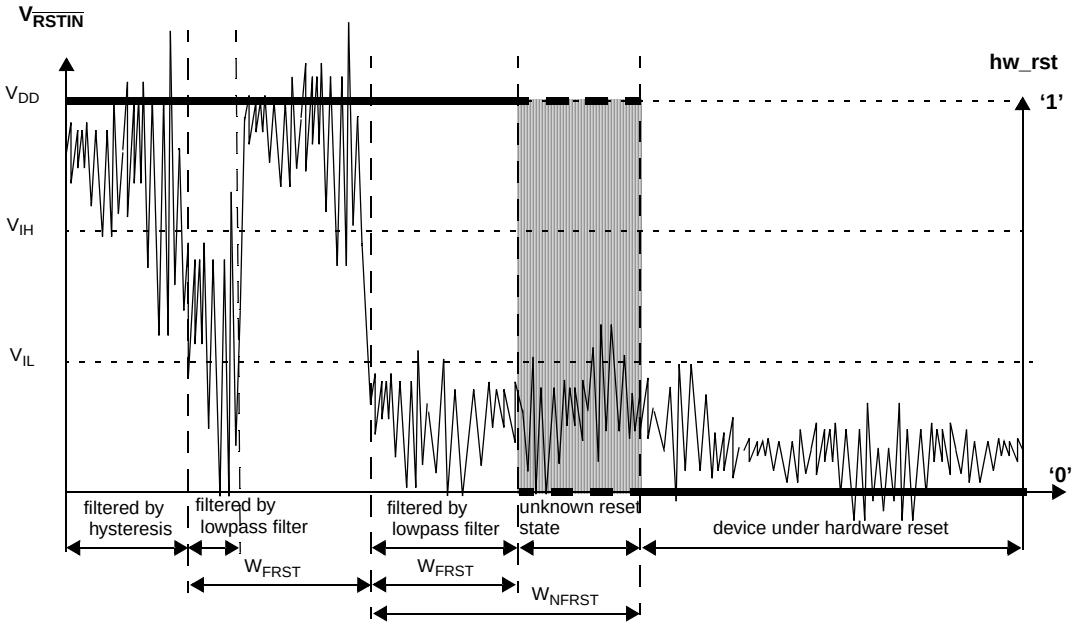


Figure 30. Noise filtering on reset signal

Table 31. $\overline{\text{RESET}}$ electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	$\overline{\text{nRSTIN}}$ input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	$\overline{\text{nRSTIN}}$ input not filtered pulse	—	500	—	—	ns

NOTES:
1 V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified
2 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.17.2 IEEE 1149.1 interface timing

Table 32. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDE}/2)	—	40	60	ns
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns

Table 32. JTAG pin AC electrical characteristics (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

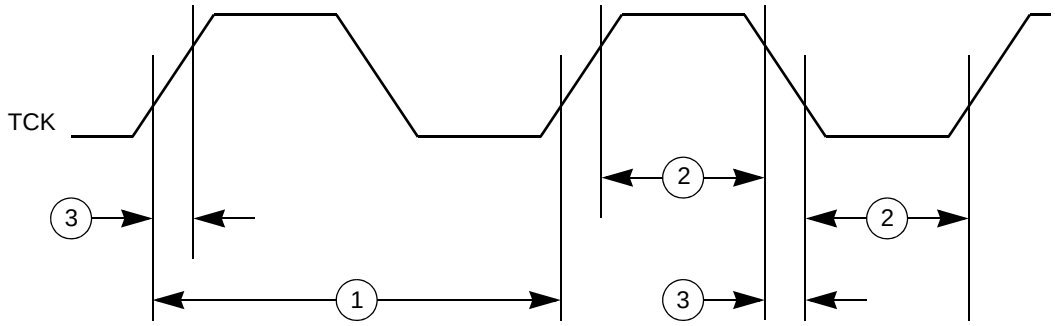


Figure 17. JTAG test clock input timing

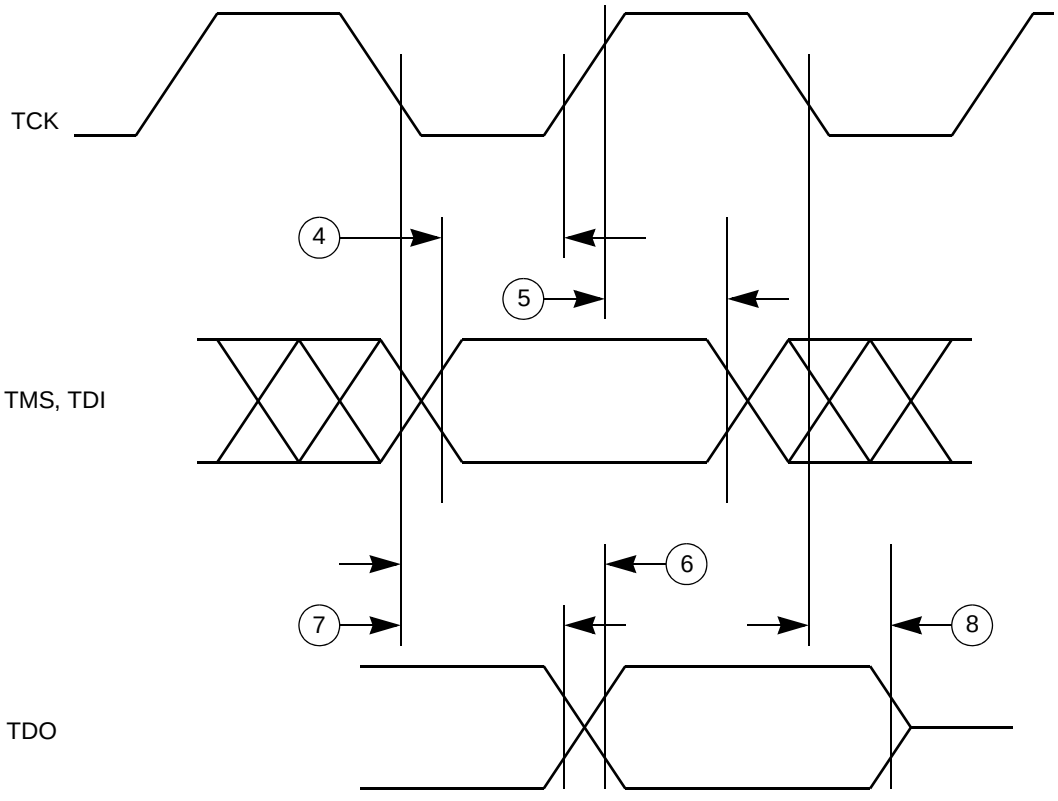


Figure 18. JTAG test access port timing

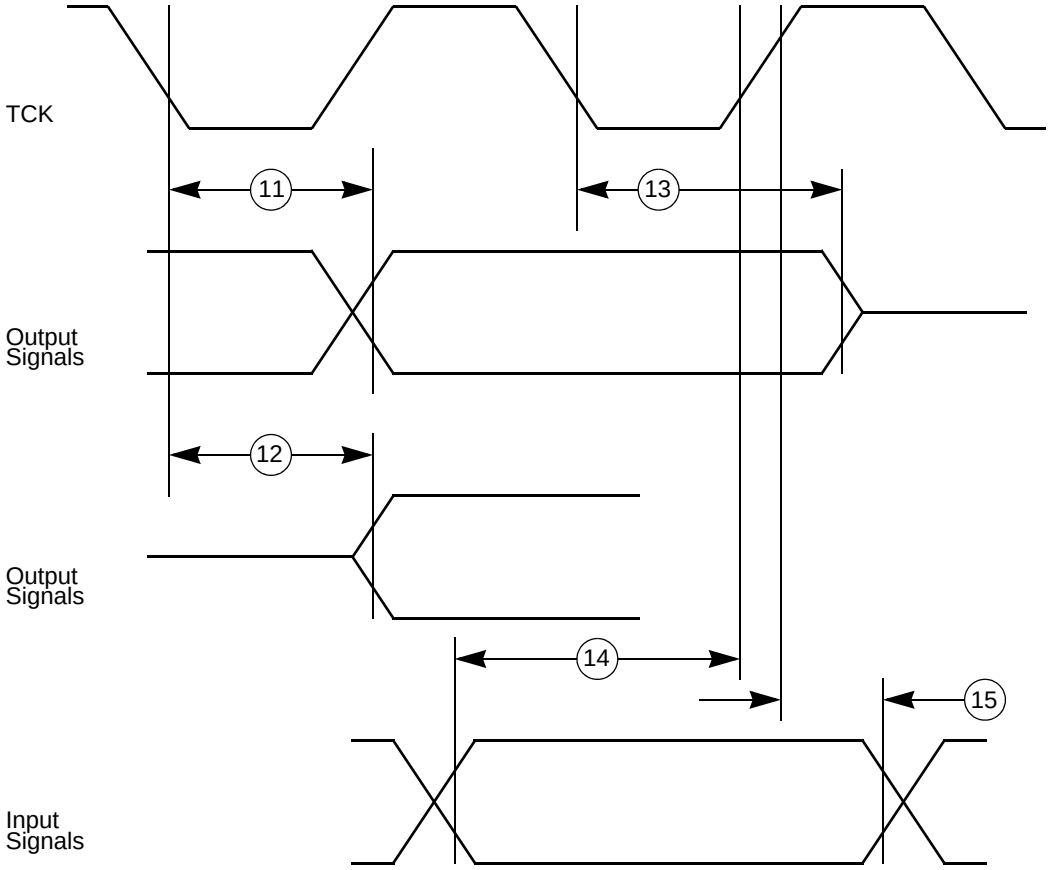


Figure 19. JTAG boundary scan timing

3.17.3 Nexus timing

Table 33. Nexus debug port timing[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	D	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	D	$\overline{\text{EVTI}}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	D	$\overline{\text{EVTO}}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	D	TCK Cycle Time[3]	—	40	—	ns
7	t_{TDC}	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	D	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time		5	—	ns
10	t_{JOV}	D	TCK Low to TDO Data Valid		0	25	ns

NOTES:
1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3 The system clock frequency needs to be three times faster than the TCK frequency.

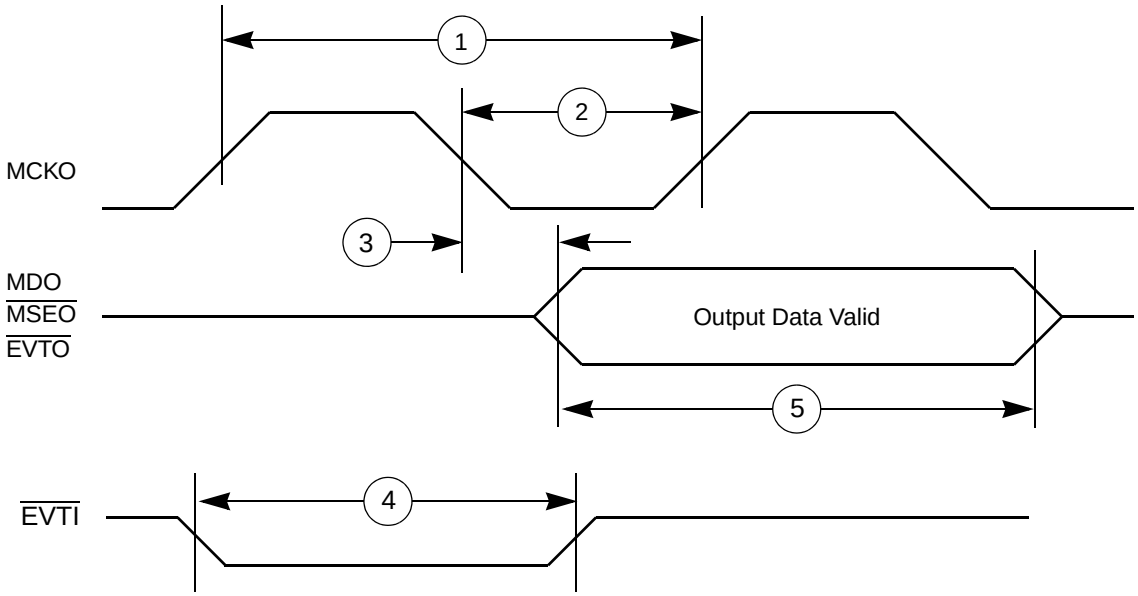


Figure 20. Nexus output timing

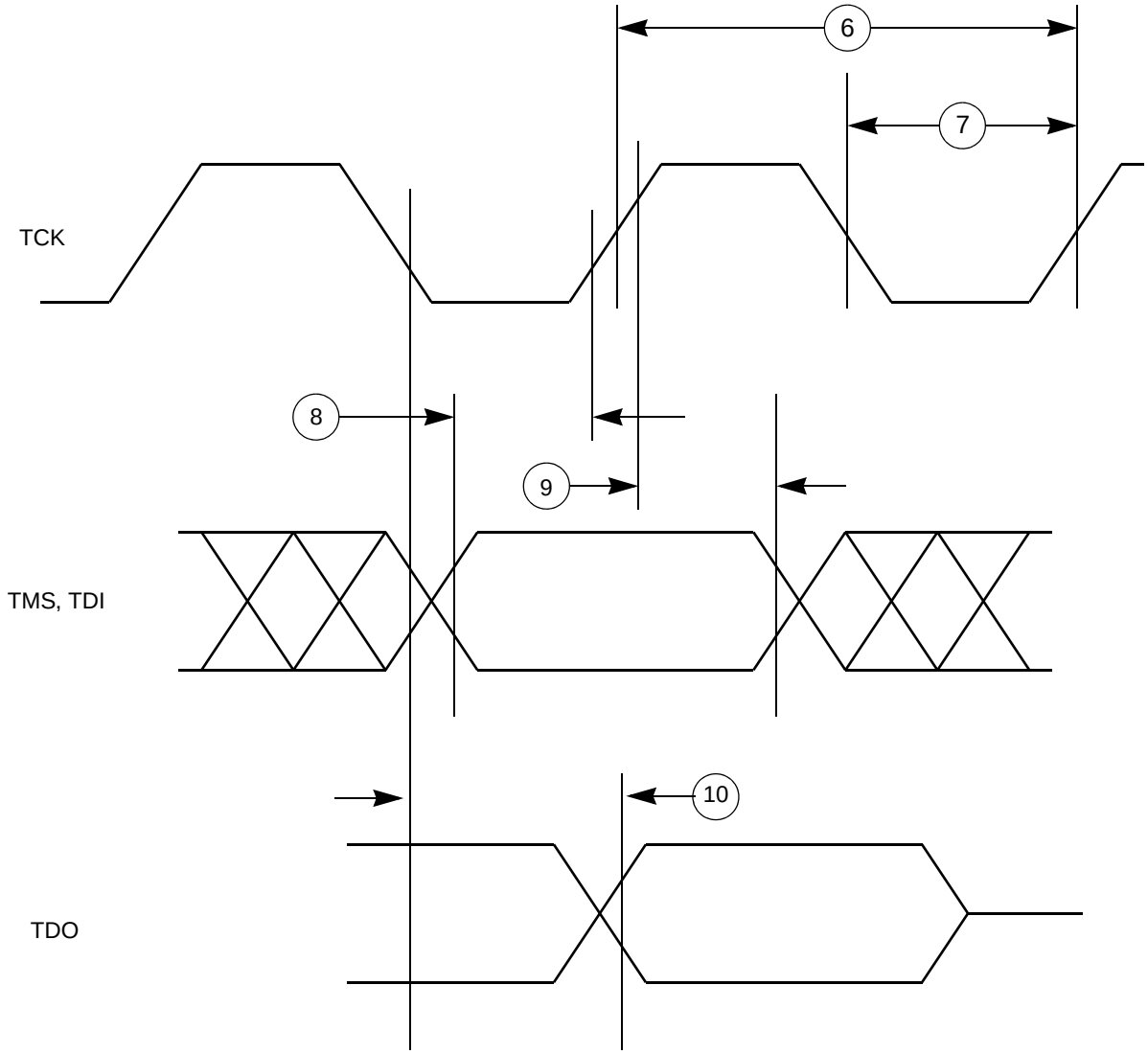


Figure 21. Nexus TDI, TMS, TDO timing

3.17.4 External interrupt timing (IRQ pin)

Table 34. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time[1]	—	6	—	t_{CYC}

NOTES:
1 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

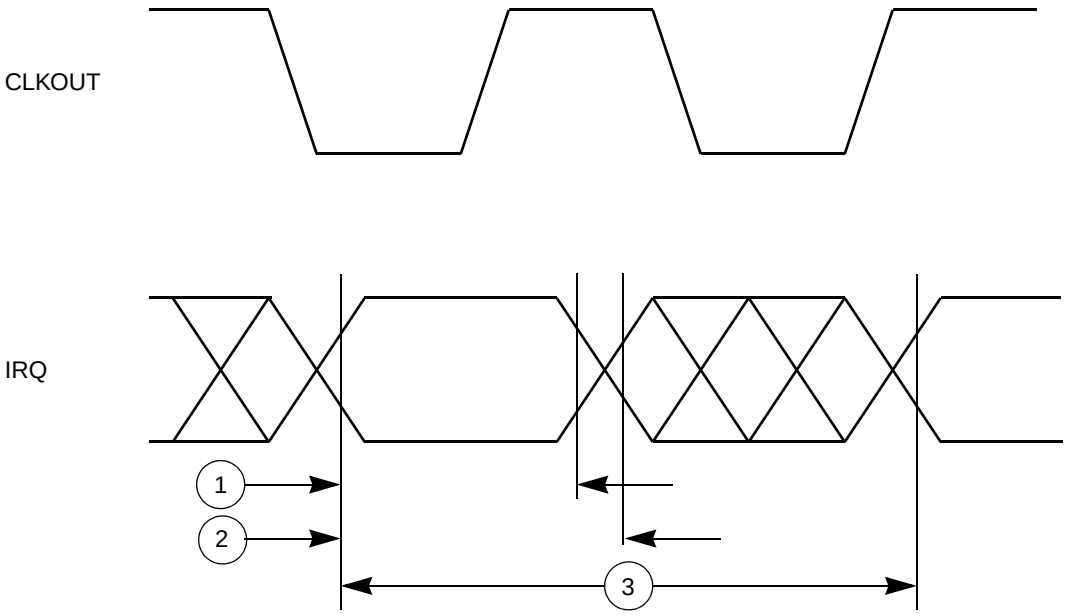


Figure 22. External interrupt timing

3.17.5 FlexCAN timing

Table 35. FlexCAN timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{CANOV}		CTNX output valid after CLKOUT rising edge (output delay)	—	—	26.0	ns
2	t_{CANSU}		CNRX input valid to CLKOUT rising edge (setup time)	—	—	9.8	ns

3.17.6 DSPI timing

Table 36. DSPI timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode[1]	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	0.4 × t_{SCK}	0.6 × t_{SCK}	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns

Table 36. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	
13	f_{max}	D	Maximum DSPI speed	—	—	4	MHz

NOTES:
1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. Note that in this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

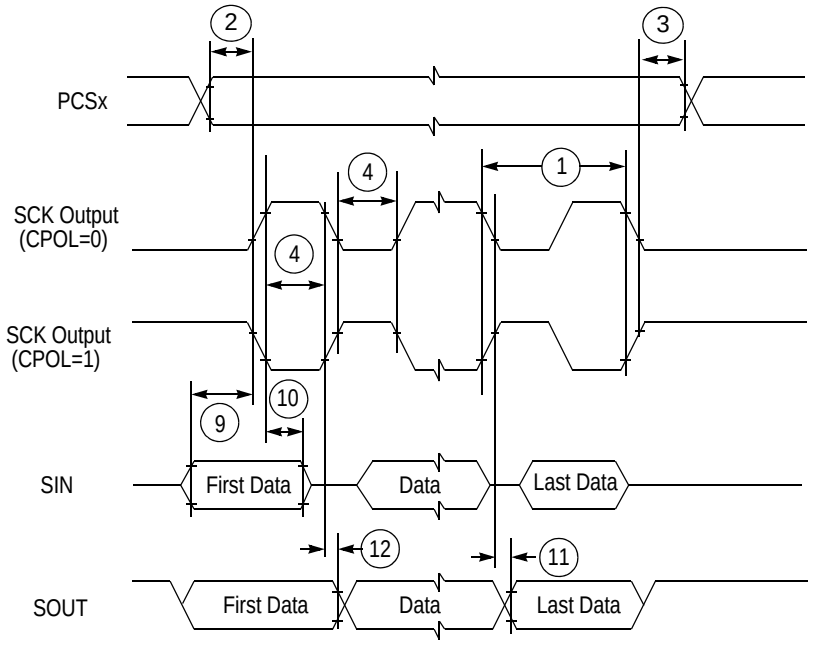


Figure 23. DSPI classic SPI timing — master, CPHA = 0

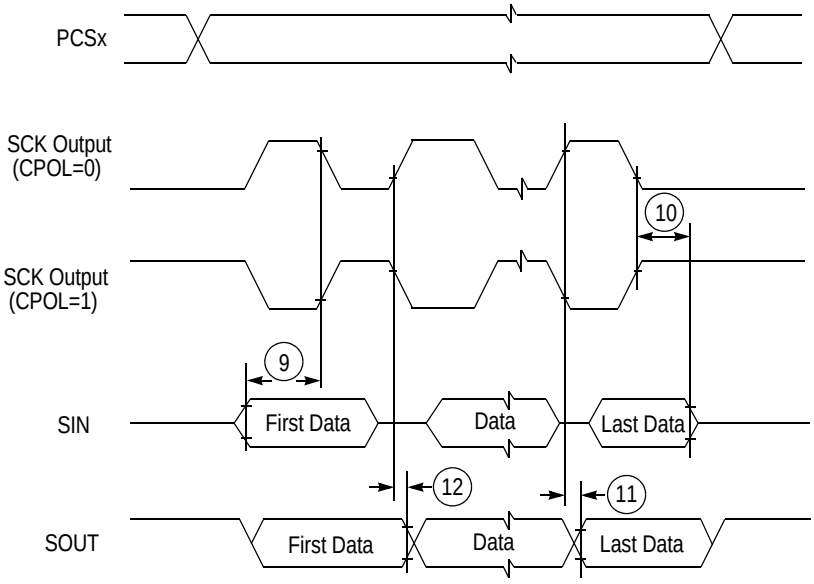


Figure 24. DSPI classic SPI timing — master, CPHA = 1

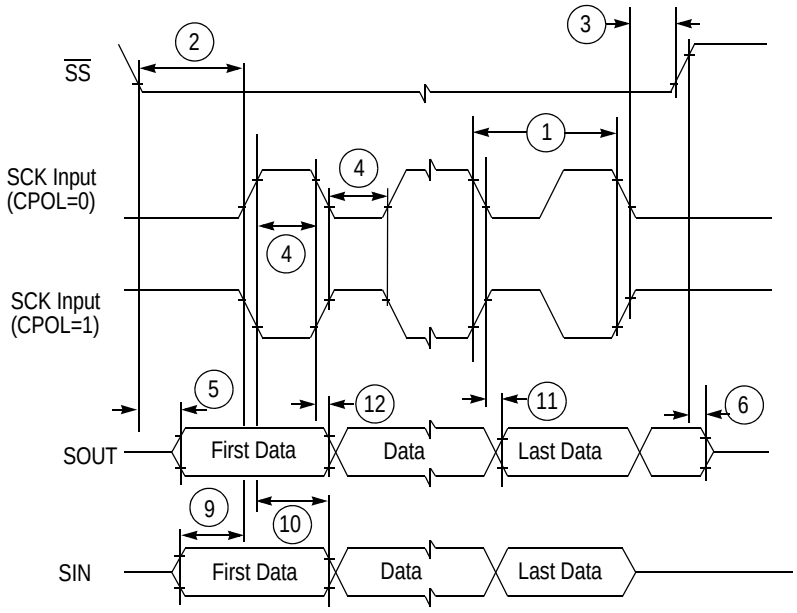


Figure 25. DSPI classic SPI timing — slave, CPHA = 0

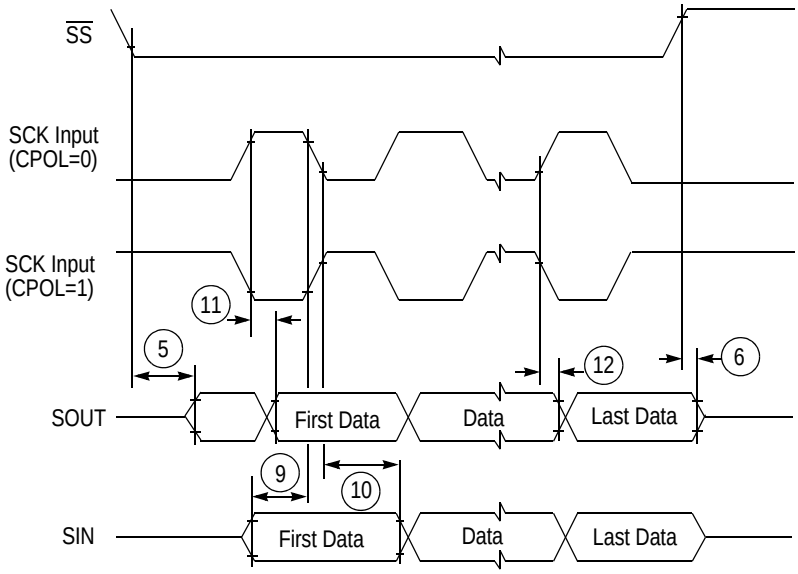


Figure 26. DSPI classic SPI timing — slave, CPHA = 1

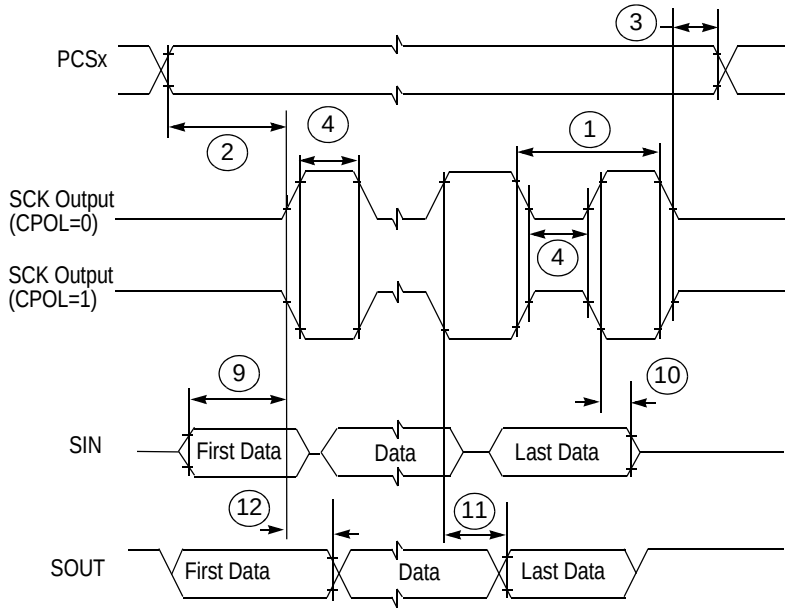


Figure 27. DSPI modified transfer format timing — master, CPHA = 0

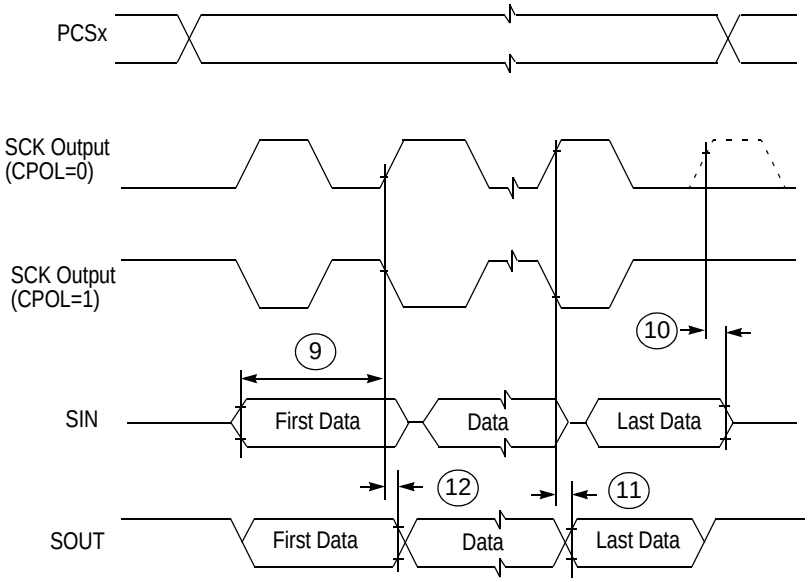


Figure 28. DSPI modified transfer format timing — master, CPHA = 1

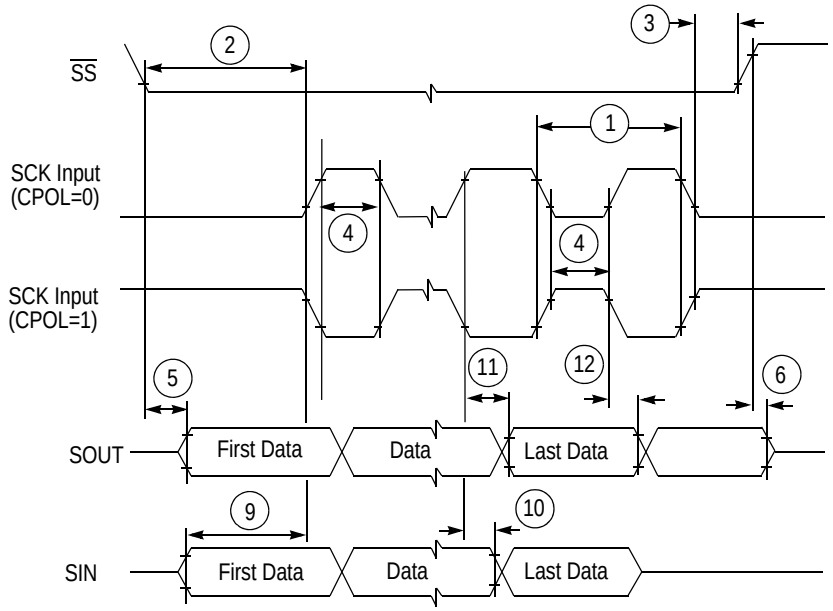


Figure 29. DSPI modified transfer format timing – slave, CPHA = 0

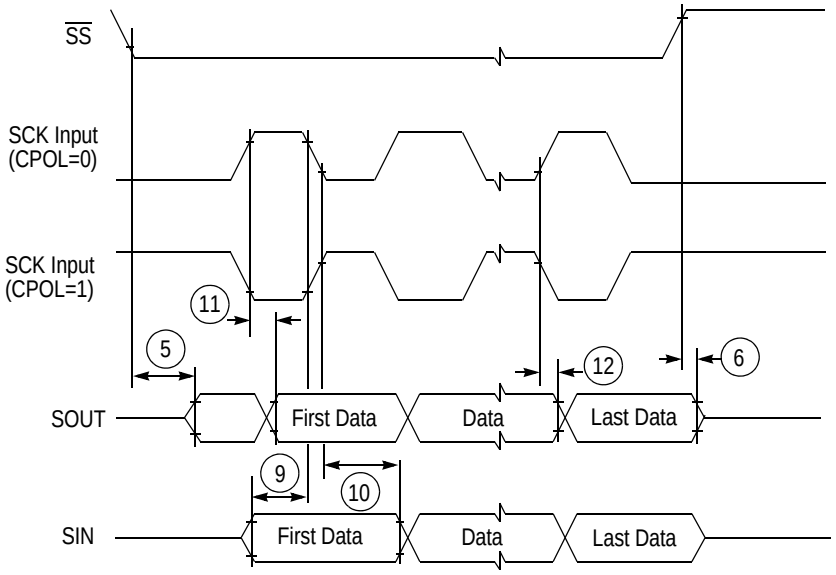


Figure 30. DSPI modified transfer format timing — slave, CPHA = 1

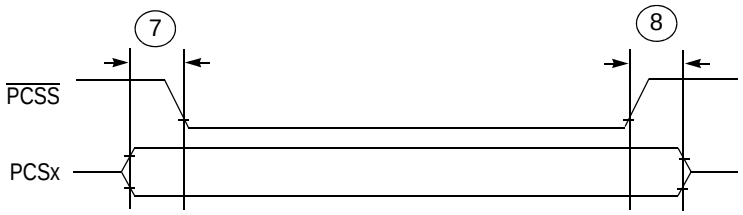


Figure 31. DSPI PCS strobe (PCSS) timing

4 Package characteristics

4.1 Package mechanical data

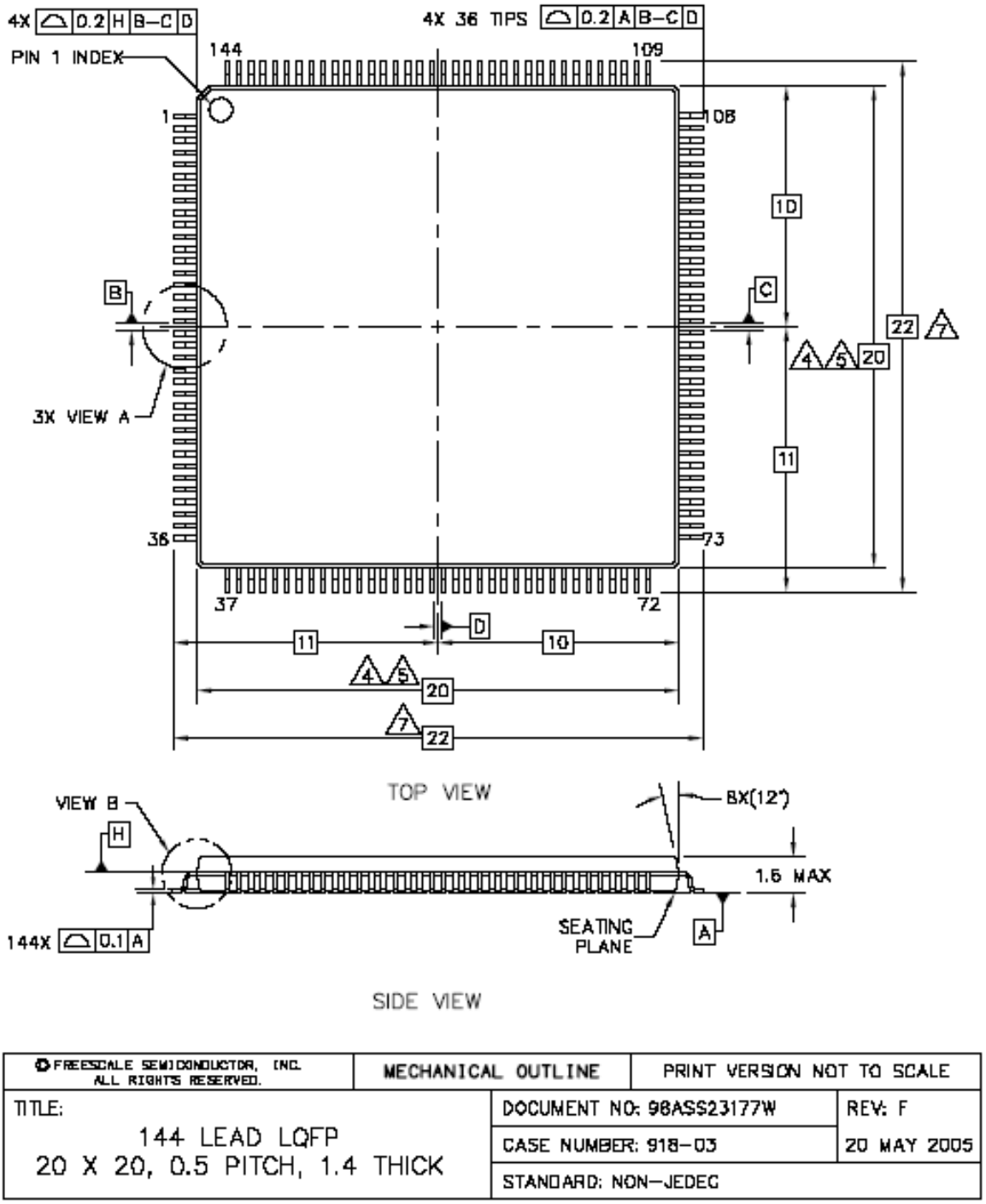
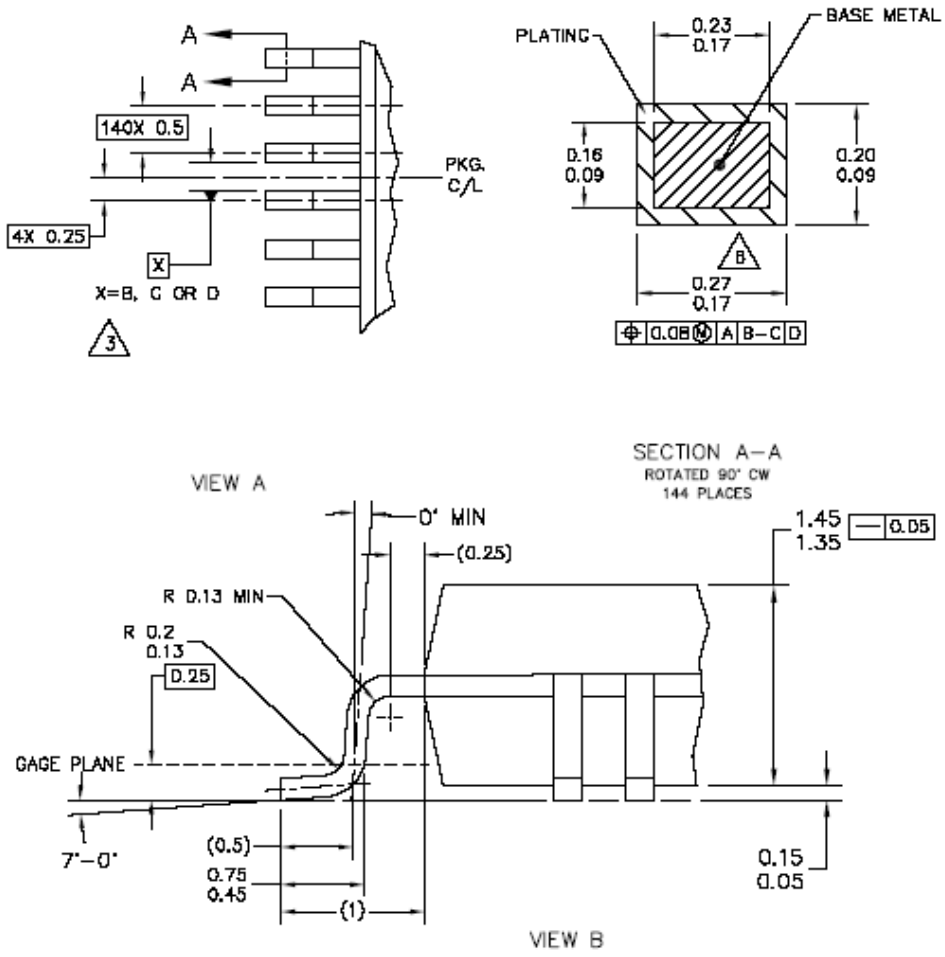


Figure 32. 144 LQFP package mechanical drawing (1 of 2)

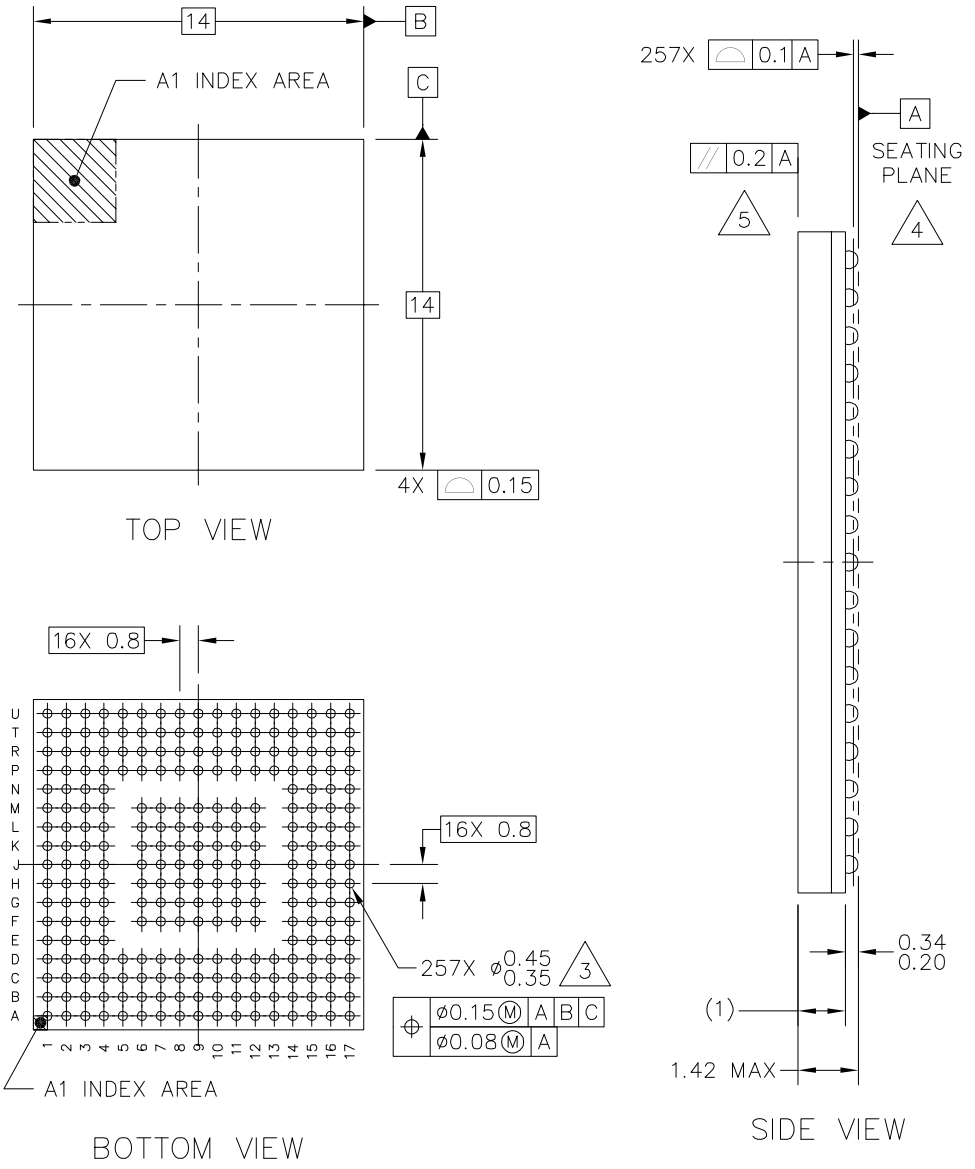


FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918-03	20 MAY 2005
	STANDARD: NON-JEDEC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 33. 144 LQFP package mechanical drawing (2 of 2)



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00081D	REV: X0
	CASE NUMBER: 2082–01	13 MAY 2009
	STANDARD: NON–JEDEC	

Figure 34. 257 MAPBGA package mechanical drawing (1 of 2)

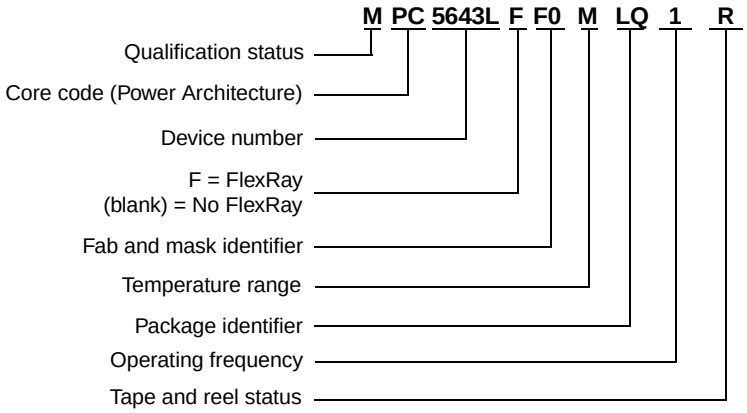
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00081D	REV: X0
	CASE NUMBER: 2082–01	13 MAY 2009
	STANDARD: NON–JEDEC	

Figure 35. 257 MAPBGA package mechanical drawing (2 of 2)

5 Ordering information



Temperature range

M = –40 °C to 125 °C
V = –40 °C to 105 °C

Package identifier

LQ = 144 LQFP
MM = 257 MAPBGA

Operating frequency

1 = 120 MHz
8 = 80 MHz

Tape and reel status

R = Tape and reel
(blank) = Trays

Qualification status

P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 37.

Table 37. Orderable part number summary

Part number[1]	Flash/SRAM	Package	Speed (MHz)	Other features
PPC5643LFF0MLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	FlexRay –40–125 °C
PPC5643LFF0MMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	FlexRay –40–125 °C
PPC5643LF0MLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	No FlexRay –40–125 °C
PPC5643LF0MMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	No FlexRay –40–125 °C
PPC5643LFF0VLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	FlexRay –40–105 °C
PPC5643LFF0VMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	FlexRay –40–105 °C
PPC5643LF0VLQ1	1 MB/128 KB	144 LQFP (Pb free)	120	No FlexRay –40–105 °C
PPC5643LF0VMM1	1 MB/128 KB	257 MAPBGA (Pb free)	120	No FlexRay –40–105 °C
PPC5643LFF0MLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	FlexRay –40–125 °C
PPC5643LFF0MMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	FlexRay –40–125 °C

Table 37. Orderable part number summary (continued)

Part number[1]	Flash/SRAM	Package	Speed (MHz)	Other features
PPC5643LF0MLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	No FlexRay –40–125 °C
PPC5643LF0MMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	No FlexRay –40–125 °C
PPC5643LFF0VLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	FlexRay –40–105 °C
PPC5643LFF0VMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	FlexRay –40–105 °C
PPC5643LF0VLQ8	1 MB/128 KB	144 LQFP (Pb free)	80	No FlexRay –40–105 °C
PPC5643LF0VMM8	1 MB/128 KB	257 MAPBGA (Pb free)	80	No FlexRay –40–105 °C

NOTES:
1 All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete. Not all configurations are available in the PPC parts.

6 Document revision history

Table 38 summarizes revisions to this document.

Table 38. Revision history

Revision	Date	Description of Changes
1	2 Mar 2009	Initial release.
2	5 May 2009	Updated, Advance Information. —Revised SINAD/SNR specifications. — Updated pinout and pin multiplexing information.
3	5 Oct 2009	Updated, Advance Information, Public release. — Throughout this document, added information for 257 MAPBGA package. — Updated Table 1, MPC5643L device summary. — Updated Section 1.3, Feature Details. — Updated pin-out and pin multiplexing tables. — In Section 3, Electrical characteristics, added symbols for signal characterization methods. — In Table 8, updated maximum ratings. — In Table 10 and Table 11, removed moving-air thermal characteristics. — Updated Section 3.8, Voltage regulator electrical characteristics. — Updated Section 3.14, ADC electrical characteristics. — Updated Section 3.15, Flash memory electrical characteristics. — Updated Section 3.17.1, RESET pin characteristics. — Removed External interrupt timing (IRQ pin) timing specifications. — Updated Section 3.17.6, DSPI timing. — Updated Section 5, Ordering information.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MPC5643L
Rev. 3
10/2009