QL4016 QuickRAM Data Sheet

16,000 Usable PLD Gate QuickRAM ESP Combining Performance, Density and Embedded RAM

Device Highlights

High Performance & High Density

- 16,000 Usable PLD Gates with 118 I/Os
- 300 MHz 16-bit Counters, 400 MHz Datapaths, 160+ MHz FIFOs
- 0.35 µm four-layer metal non-volatile CMOS process for smallest die sizes

High Speed Embedded SRAM

- 10 dual-port RAM modules, organized in user-configurable 1,152 bit blocks
- 5 ns access times, each port independently accessible
- Fast and efficient for FIFO, RAM, and ROM functions

Easy to Use / Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with both 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V busses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O Cells with individually controlled Registered Input Path and Output Enables

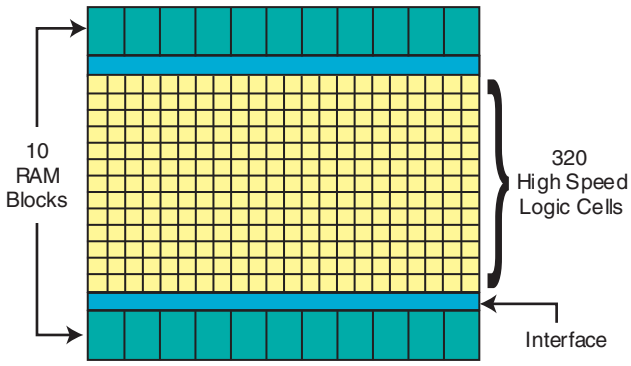


Figure 1: QuickRAM Block Diagram

Architecture Overview

The QuickRAM family of ESPs (Embedded Standard Products) offers FPGA logic in combination with Dual-Port SRAM modules. The QL4016 is a 16,000 usable PLD gate member of the QuickRAM family of ESPs. QuickRAM ESPs are fabricated on a 0.35 µm four-layer metal process using QuickLogic's patented ViaLink®™ technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL4016 contains 320 logic cells and 10 Dual Port RAM modules (see **Figure 1**). Each RAM module has 1,152 RAM bits, for a total of 11,520 bits. RAM Modules are Dual Port (one read port, one write port) and can be configured into one of four modes: 64 (deep) × 18 (wide), 128 × 9, 256 × 4, or 512 × 2 (see **Figure 4**). With a maximum of 82 I/Os, the QL4016 is available in 84-pin PLCC, 100-pin TQFP, 100-pin CQFP and 144-pin TQFP packages.

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see **Figure 2**). This approach allows up to 512-deep configurations as large as 16 bits wide in the smallest QuickRAM device and 44 bits wide in the largest device.

Software support for the complete QuickRAM family, including the QL4016, is available through two basic packages. The turnkey QuickWorks®™ package provides the most complete ESP software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools package provides a solution for designers who use Cadence, Exemplar, Mentor, Synopsys, Synplicity, Viewlogic, Aldec, or other third-party tools for design entry, synthesis, or simulation.

The QuickLogic®™ variable grain logic cell features up to 16 simultaneous inputs and five outputs within a cell that can be fragmented into five independent cells. Each cell has a fan-in of 29 including register and control lines (see **Figure 3**).

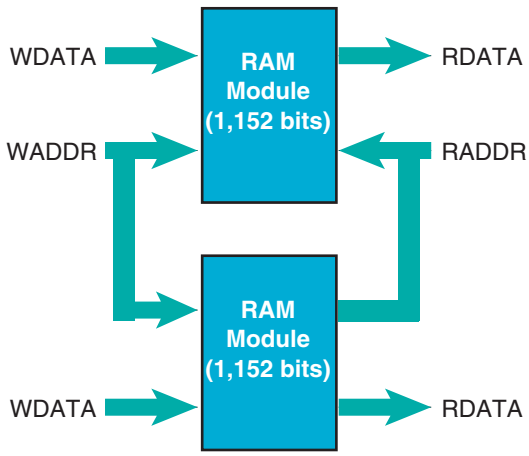


Figure 2: QuickRAM Module Bits

Product Summary

Total of 118 I/O Pins

- 110 bi-directional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- 8 high-drive input/distributed network pins

Eight Low-Skew Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs—each driven by an input-only pin
- Six global clock/control networks available to the logic cell F1, clock, set and reset inputs and the input and I/O register clock, reset and enable inputs as well as the output enable contro—each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance Silicon

- Input + logic cell + output total delays = under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz
- FIFO speeds over 160+ MHz

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 10: Operating Range** by the following numbers in the tables provided.

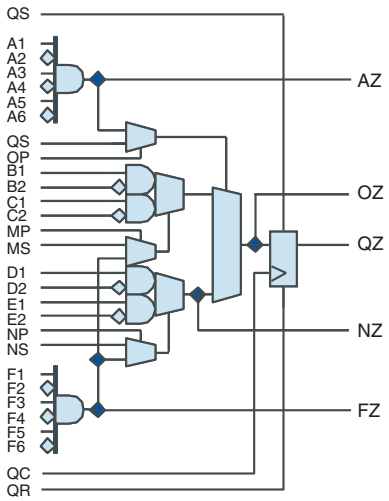


Figure 3: QuickRAM Logic Cell

Table 1: Logic Cell

Symbol	Parameter	Propagation Delays (ns) Fanout (5)				
		1	2	3	4	5
t_{PD}	Combinatorial Delay[a]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time[a]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

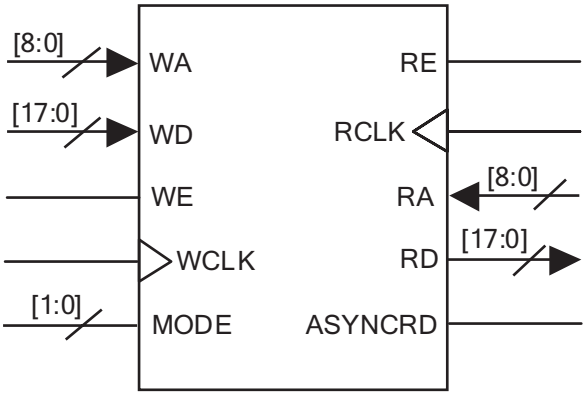


Figure 4: QuickRAM Module

Table 2: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SWA}	WA Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWA}	WA Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWD}	WD Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWD}	WD Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWE}	WE Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWE}	WE Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{WCRD}	WCLK to RD (WA=RA)[a]	5.0	5.3	5.6	5.9	7.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25° C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 3: RAM Cell Synchronous Read Timing

Symbol Logic Cells	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
t_{SRA}	RA Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRA}	RA Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{SRE}	RE Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRE}	RE Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{RCRD}	RCLK to RD[a]	4.0	4.3	4.6	4.9	6.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25 × C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 4: RAM Cell Asynchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	5
RPDRD	RA to RD[a]	3.0	3.3	3.6	3.9	5.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 5: Input-Only / Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	.19	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register Clock Enable Setup Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Table 6: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 11 loads per half column.

Table 7: I/O Cell Input Delays

Symbol	Parameter	Propagation Delays (ns) Fanout[a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock to Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register Clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25° C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 8: I/O Cell Output Delays

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		3	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-state[a]	2.0	-	-	-	-
t_{PLZ}	Output Delay High to Tri-state[a]	1.2	-	-	-	-

a. These loads are used for t_{PXZ} (see **Figure 5**)

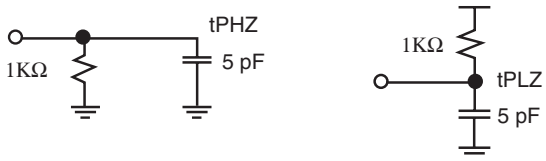


Figure 5: Loads Used for t_{PXZ}

DC Characteristics

The DC specifications are provided in the tables below.

Table 9: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	**DC Input Current**	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	**ESD Pad Protection**	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	**Storage Temperature**	-65°C to +150°C
Latch-up Immunity	±200 mA	**Lead Temperature**	300°C

Table 10: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55	-	-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-0 Speed Grade	0.42	2.03	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 11: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
VIH	Input HIGH Voltage		0.5VCC	VCCIO+0.5	V
VIL	Input LOW Voltage		-0.5	0.3 V_{cc}	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 µA	0.9VCC		V
VOL	Output LOW Voltage	IOL = 16 mA[a]		0.45	V
		IOL = 1.5 mA		0.1 V_{CC}	V
II	I or I/O Input Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
CI	Input Capacitance[b]			10	pF
IOS	Output Short Circuit Current[c]	VO = GND	-15	-180	mA
		VO = V_{CC}	40	210	mA
ICC	D.C. Supply Current[d]	VI, VIO = V_{CCIO} or GND	0.50 (typ)	2	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. For -1/-2/-3/-4 commercial grade devices only. Maximum ICC is 3 mA for -0 commercial grade and all industrial grade devices and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group (see **Contact Information**) .

Kv and Kt Graphs

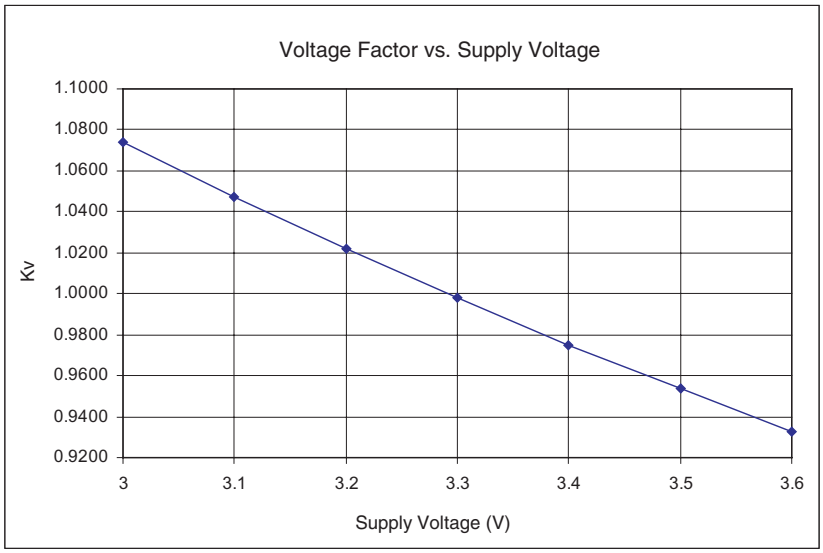


Figure 6: Voltage Factor vs. Supply Voltage

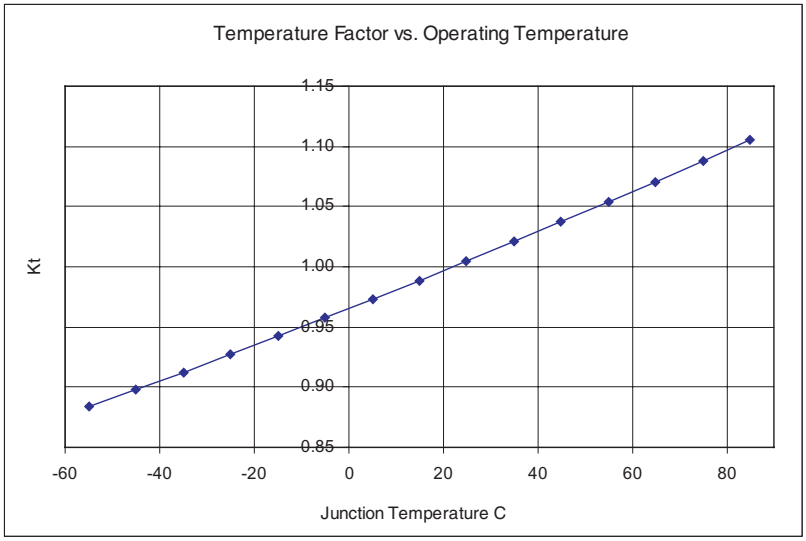


Figure 7: Temperature Factor vs. Operating Temperature

Power-up Sequencing

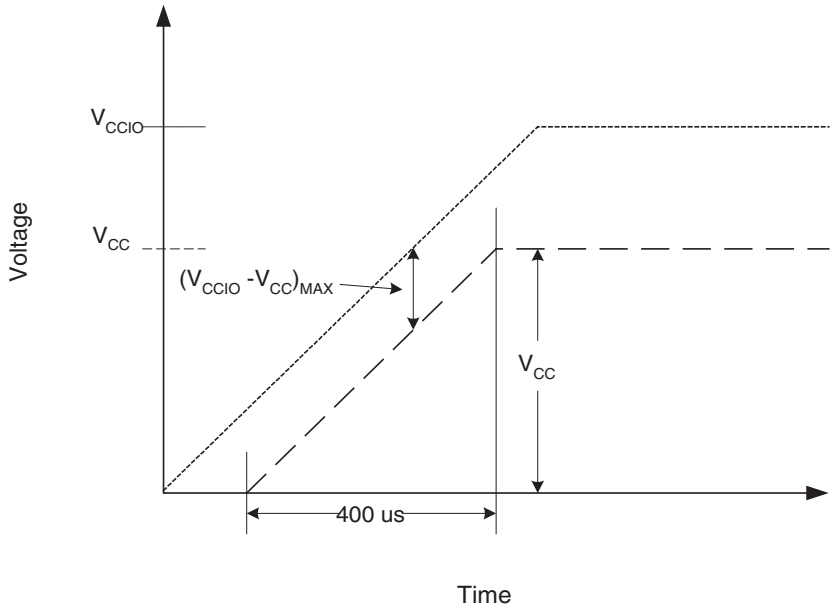


Figure 8: Power-up Requirements

The following requirements must be met when powering up the device (refer to **Figure 8**):

- When ramping up the power supplies keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV. Deviation from this recommendation can cause permanent damage to the device.
- V_{CCIO} must lead V_{CC} when ramping the device.
- The power supply must take greater than or equal to 400 µs to reach VCC. Ramping to V_{CC}/V_{CCIO} earlier than 400 µs can cause the device to behave improperly.

An internal diode is present in-between V_{CC} and V_{CCIO}, as shown in **Figure 9**.

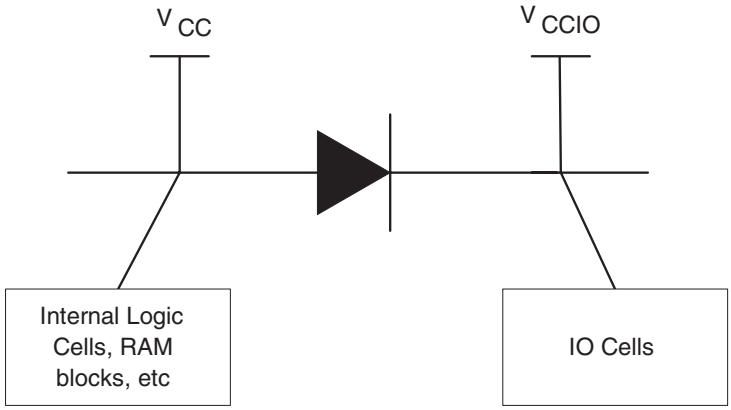


Figure 9: Internal Diode Between VCC and VCCIO

JTAG

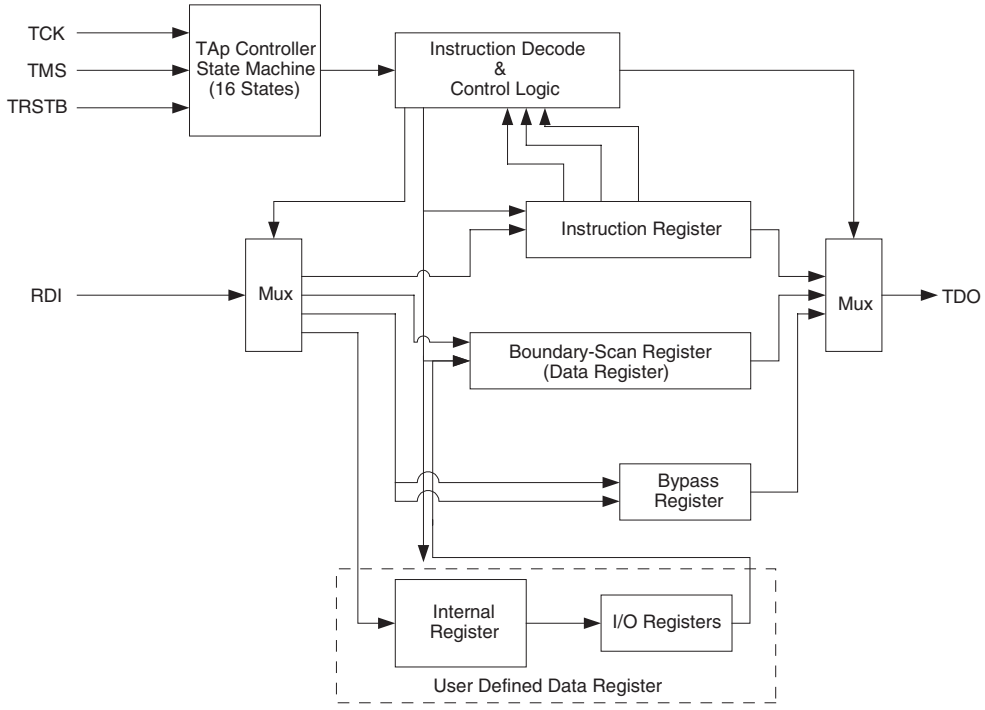


Figure 10: JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges. One of these challenges concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 JTAG standard requires the following three tests:

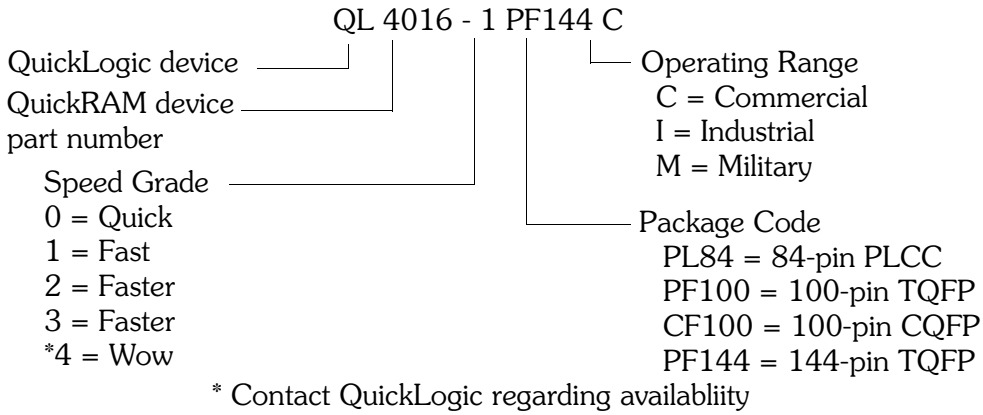
- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register connects the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Pin Descriptions

Table 12: Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG /RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused.
TRSTB/RRO	Active low Reset for JTAG /RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG.
TDO/RCO	Test data out for JTAG /RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0V supply if 5V input tolerance is required, otherwise connect to 3.3V supply.
GND	Ground pin	Connect to ground.
GND/THERM	Ground/Thermal pin	Available on 456-PBGA only. Connect to ground plane on PCB if heat sinking desired. Otherwise may be left unconnected.

Ordering Information



* Contact QuickLogic regarding availabliity

84 PLCC Pinout Diagram

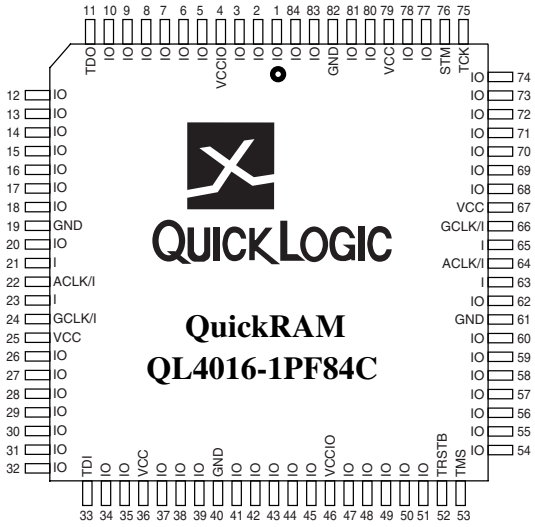


Figure 11: Top View of 84 Pin PLCC

84 PLCC Pinout Table

Table 13: 84 PLCC Pinout Table

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	VCCIO	25	VCC	46	VCCIO	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	VCC	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	VCC
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

100 TQFP/CQFP Pinout Diagram

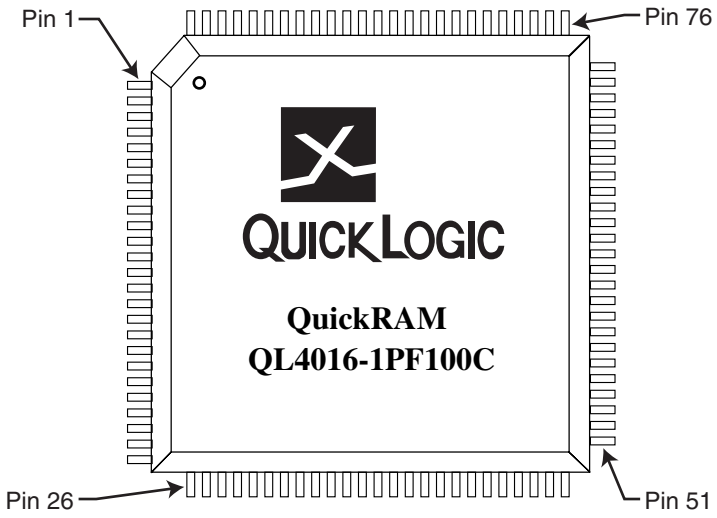


Figure 12: Top View of 100 Pin TQFP/CQFP

144 TQFP Pinout Diagram

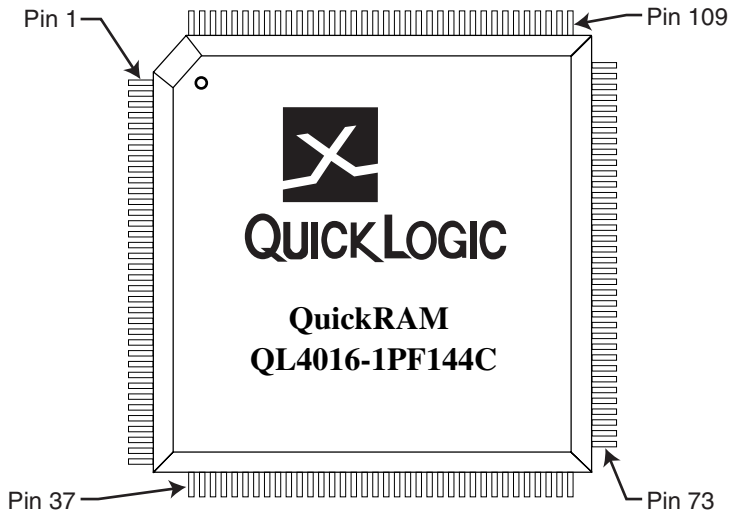


Figure 13: Top View of 144 Pin TQFP

144 & 100 TQFP Pinout Table

Table 14: 144 & 100 TQFP Pinout Table

144TQFP	100TQFP	Function	144TQFP	100TQFP	Function	144TQFP	100TQFP	Function	144TQFP	100TQFP	Function
1	2	I/O	38	26	TDI	75	53	I/O	111	78	I/O
2	3	I/O	39	27	I/O	76	54	I/O	112	79	I/O
3	NC	I/O	40	28	I/O	77	55	I/O	113	80	I/O
4	4	I/O	41	29	I/O	78	NC	I/O	114	NC	VCC
5	NC	I/O	42	NC	VCC	79	NC	VCC	115	81	I/O
6	5	I/O	43	30	I/O	80	NC	I/O	116	82	I/O
7	NC	VCC	44	31	I/O	81	56	I/O	117	83	I/O
8	6	I/O	45	NC	I/O	82	NC	I/O	118	NC	I/O
9	NC	I/O	46	32	I/O	83	57	I/O	119	84	I/O
10	7	I/O	47	33	I/O	84	NC	I/O	120	NC	I/O
11	NC	I/O	48	NC	I/O	85	58	I/O	121	NC	I/O
12	NC	I/O	49	34	I/O	86	NC	I/O	122	85	GND
13	8	I/O	50	35	GND	87	59	GND	123	NC	I/O
14	NC	I/O	51	36	I/O	88	60	I/O	124	86	I/O
15	9	GND	52	NC	I/O	89	61	I	125	87	I/O
16	10	I/O	53	37	I/O	90	62	ACLK / I	126	88	GND
17	11	I	54	38	GND	91	63	VCC	127	89	I/O
18	12	ACLK / I	55	39	I/O	92	64	I	128	90	I/O
19	13	VCC	56	40	I/O	93	65	GCLK / I	129	91	I/O
20	14	I	57	41	I/O	94	66	VCC	130	92	VCCIO
21	15	GCLK / I	58	42	VCCIO	95	67	I/O	131	NC	I/O
22	16	VCC	59	NC	I/O	96	NC	I/O	132	93	I/O
23	17	I/O	60	43	I/O	NC	68	I/O	133	NC	I/O
24	18	I/O	61	44	I/O	97	NC	I/O	134	94	I/O
25	NC	I/O	62	45	I/O	98	69	I/O	135	NC	I/O
26	19	I/O	63	NC	I/O	99	NC	I/O	136	NC	I/O
27	NC	I/O	64	NC	I/O	100	70	I/O	NC	95	I/O
28	20	I/O	65	46	I/O	101	71	I/O	137	NC	I/O
29	21	I/O	66	NC	GND	102	NC	GND	138	NC	GND
30	NC	GND	67	NC	I/O	103	NC	I/O	139	96	I/O
31	NC	I/O	68	NC	I/O	104	72	I/O	140	97	I/O
32	22	I/O	69	47	I/O	105	NC	I/O	141	98	I/O
33	23	I/O	70	48	I/O	106	73	I/O	142	99	I/O
34	NC	I/O	71	49	TRSTB	107	74	I/O	143	100	TDO
35	NC	I/O	72	50	TMS	108	75	I/O	144	1	I/O
36	24	I/O	73	51	I/O	109	76	TCK			
37	25	I/O	74	52	I/O	110	77	STM			

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Revision History

Table 15: Revision History

Revision	Date	Comments
A	not avail.	First release.
B	not avail.	
C	not avail.	
D	not avail.	
E	not avail.	
F	not avail.	
G	not avail.	
H	May 2000	Update of AC/DC Specs and reformat
I	May 2002	Added Kfactor, Power-up, JTAG and mechanical drawing information. Reformatted.

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