1. Overview

1.1 Features

The R8C/56E Group, R8C/56F Group, R8C/56G Group, R8C/56H Group single-chip microcontrollers (MCUs) incorporate the R8C CPU core, which provides sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, the CPU core is capable of executing instructions at high speed. In addition, it features a multiplier for high-speed arithmetic processing.
Power consumption is low, and additional power control is possible by selecting the operating mode. The R8C/56E Group, R8C/56F Group, R8C/56G Group, R8C/56H Group are also designed to maximize EMI/EMS performance. Integration of many peripheral functions, including multifunction timer and serial interface on the same chip, reduces the number of system components.
The R8C/56E Group and R8C/56F Group incorporate one channel of CAN module, ideal for the LAN systems of automotive and factory automation applications.
The R8C/56G Group and R8C/56H Group do not incorporate the CAN module.
The R8C/56E Group and R8C/56G Group also have on-chip data flash (1 KB × 4 blocks) with background operation (BGO) function.

1.1.1 Applications

Automotive, etc.

1.1.2 Specifications

Tables 1.1 to 1.3 outline the R8C/56E Group Specifications. Tables 1.4 to 1.6 outline the R8C/56F Group Specifications. Tables 1.7 to 1.9 outline the R8C/56G Group Specifications. Tables 1.10 to 1.12 outline the R8C/56H Group Specifications.

Table 1.1 R8C/56E Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 2.7 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	See **Table 1.13 R8C/56E Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • Simplified peripheral mapping controller (PMC) allows either timer priority or communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 42 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.2 R8C/56E Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuits integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0 and RC_1	16 bits (with 4 capture/compare registers) × 1: 2 circuits integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin) (2 channels can be used only when 64 pins and timer function priority pin assignment are selected (only 1 channel for others))
	Timer RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
	Timer RF	16 bits × 1 Input capture function mode (input capture function), output compare mode (output compare function)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output: 1 pin), phase counting mode (the counts of the 2-phase encoder can be automatically counted.)
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (Timers RJ_0 and RJ_1, UART0_0 and UART0_1 are used)
CAN module	CAN_0	1 channel: 16 mailboxes (ISO11898-1 standard compliant)
A/D converter		Resolution: 10 bits × 16 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)

Table 1.3 R8C/56E Group Specifications (3)

Item	Function	Description
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 2.7 V)
Current consumption		T.B.D.
Operating ambient temperature		-40 °C to 85 °C (J version) -40 °C to 125 °C (K version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Note:
1. Specify the K version if it is to be used.

Table 1.4 R8C/56F Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 2.7 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	See **Table 1.14 R8C/56F Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • Simplified peripheral mapping controller (PMC) allows either timer priority or communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 42 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.5 R8C/56F Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuits integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0 and RC_1	16 bits (with 4 capture/compare registers) × 1: 2 circuits integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin) (2 channels can be used only when 64 pins and timer function priority pin assignment are selected (only 1 channel for others))
	Timer RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
	Timer RF	16 bits × 1 Input capture function mode (input capture function), output compare mode (output compare function)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output: 1 pin), phase counting mode (the counts of the 2-phase encoder can be automatically counted.)
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (Timers RJ_0 and RJ_1, UART0_0 and UART0_1 are used)
CAN module	CAN_0	1 channel: 16 mailboxes (ISO11898-1 standard compliant)
A/D converter		Resolution: 10 bits × 16 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 1.8 V to 5.5 V • Program/erase endurance: 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function

Table 1.6 R8C/56F Group Specifications (3)

Item	Function	Description
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 2.7 V)
Current consumption		T.B.D.
Operating ambient temperature		-40 °C to 85 °C (J version) -40 °C to 125 °C (K version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Note:
1. Specify the K version if it is to be used.

Table 1.7 R8C/56G Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 2.7 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	See **Table 1.15 R8C/56G Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • Simplified peripheral mapping controller (PMC) allows either timer priority or communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 42 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.8 R8C/56G Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuits integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0 and RC_1	16 bits (with 4 capture/compare registers) × 1: 2 circuits integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin) (2 channels can be used only when 64 pins and timer function priority pin assignment are selected (only 1 channel for others))
	Timer RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
	Timer RF	16 bits × 1 Input capture function mode (input capture function), output compare mode (output compare function)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output: 1 pin), phase counting mode (the counts of the 2-phase encoder can be automatically counted.)
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (Timers RJ_0 and RJ_1, UART0_0 and UART0_1 are used)
A/D converter		Resolution: 10 bits × 16 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)

Table 1.9 R8C/56G Group Specifications (3)

Item	Function	Description
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 2.7 V)
Current consumption		T.B.D.
Operating ambient temperature		-40 °C to 85 °C (J version) -40 °C to 125 °C (K version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Note:
1. Specify the K version if it is to be used.

Table 1.10 R8C/56H Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) 200 ns (CPU clock = 5 MHz, VCC = 1.8 V to 2.7 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	See **Table 1.16 R8C/56H Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 59, selectable pull-up resistor • Simplified peripheral mapping controller (PMC) allows either timer priority or communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (30 sources × 10 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 42 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.11 R8C/56H Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2_0	16 bits × 1: 1 circuits integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0 and RC_1	16 bits (with 4 capture/compare registers) × 1: 2 circuits integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin) (2 channels can be used only when 64 pins and timer function priority pin assignment are selected (only 1 channel for others))
	Timer RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
	Timer RF	16 bits × 1 Input capture function mode (input capture function), output compare mode (output compare function)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output: 1 pin), phase counting mode (the counts of the 2-phase encoder can be automatically counted.)
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (Timers RJ_0 and RJ_1, UART0_0 and UART0_1 are used)
A/D converter		Resolution: 10 bits × 16 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 1.8 V to 5.5 V • Program/erase endurance: 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function

Table 1.12 R8C/56H Group Specifications (3)

Item	Function	Description
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 2.7 V)
Current consumption		T.B.D.
Operating ambient temperature		-40 °C to 85 °C (J version) -40 °C to 125 °C (K version) (1)
Package		64-pin LQFP Package code: PLQP0064KB-A (previous code: 64P6Q-A)

Note:
1. Specify the K version if it is to be used.

1.2 Product List

Table 1.13 shows the R8C/56E Group Product List. Figure 1.1 shows the R8C/56E Group Product Part Number Structure. Table 1.14 shows the R8C/56F Group Product List. Figure 1.2 shows the R8C/56F Group Product Part Number Structure. Table 1.15 shows the R8C/56G Group Product List. Figure 1.3 shows the R8C/56G Group Product Part Number Structure. Table 1.16 shows the R8C/56H Group Product List. Figure 1.4 shows the R8C/56H Group Product Part Number Structure.

Table 1.13 R8C/56E Group Product List **Current of Mar 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21566EJFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A	J version
R5F21567EJFP	48 Kbytes		4 Kbytes		
R5F21568EJFP	64 Kbytes		6 Kbytes		
R5F2156AEJFP	96 Kbytes		8 Kbytes		
R5F2156CEJFP	128 Kbytes		10 Kbytes		
R5F21566EKFP	32 Kbytes		2.5 Kbytes		K version
R5F21567EKFP	48 Kbytes		4 Kbytes		
R5F21568EKFP	64 Kbytes		6 Kbytes		
R5F2156AEKFP	96 Kbytes		8 Kbytes		
R5F2156CEKFP	128 Kbytes		10 Kbytes		

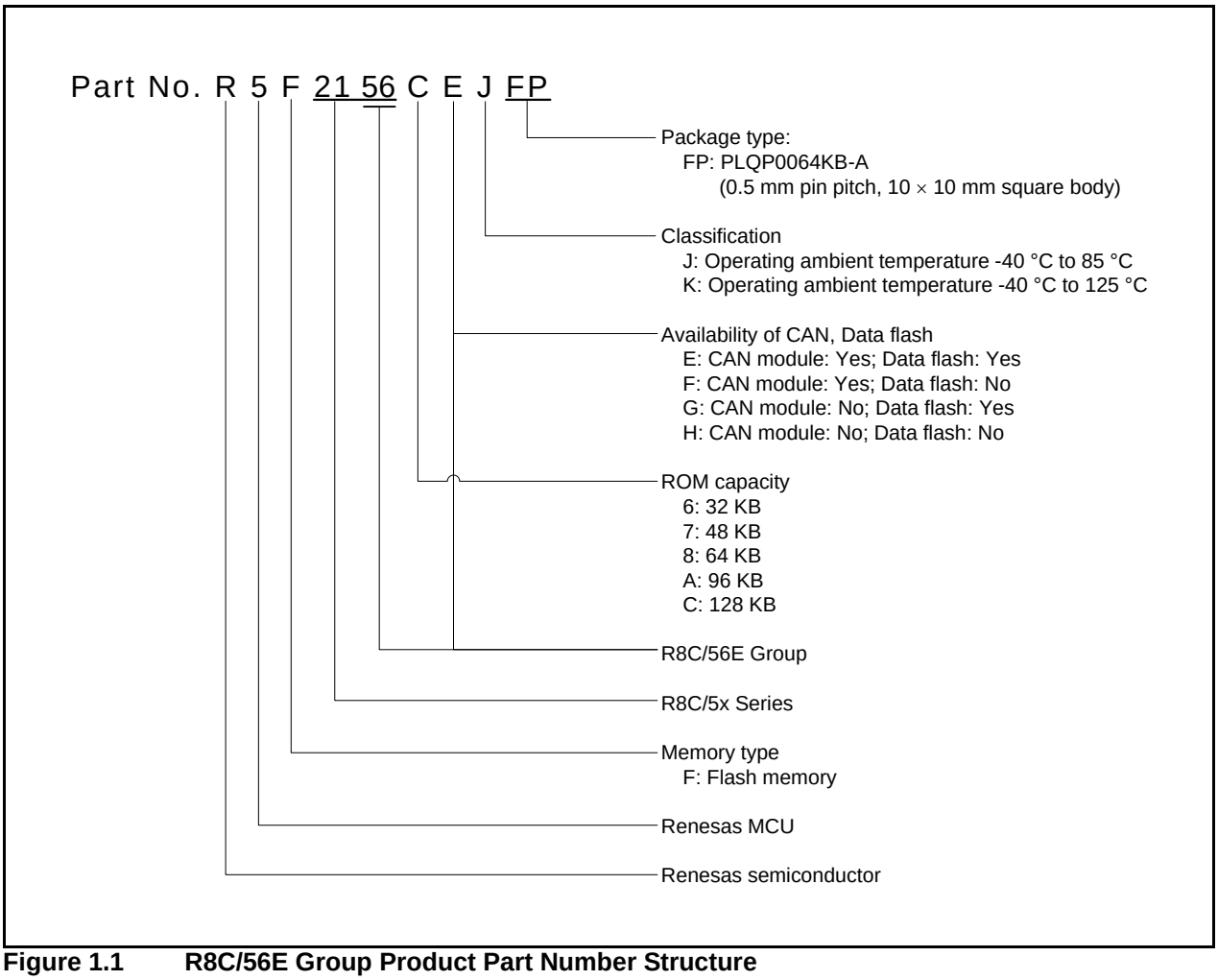


Figure 1.1 R8C/56E Group Product Part Number Structure

Table 1.14 R8C/56F Group Product List **Current of Mar 2011**

Part No.	Internal ROM Capacity	Internal RAM Capacity	Package Type	Remarks
	Program ROM			
R5F21566FJFP	32 Kbytes	2.5 Kbytes	PLQP0064KB-A	J version
R5F21567FJFP	48 Kbytes	4 Kbytes		
R5F21568FJFP	64 Kbytes	6 Kbytes		
R5F2156AFJFP	96 Kbytes	8 Kbytes		
R5F2156CFJFP	128 Kbytes	10 Kbytes		
R5F21566FKFP	32 Kbytes	2.5 Kbytes		K version
R5F21567FKFP	48 Kbytes	4 Kbytes		
R5F21568FKFP	64 Kbytes	6 Kbytes		
R5F2156AFKFP	96 Kbytes	8 Kbytes		
R5F2156CFKFP	128 Kbytes	10 Kbytes		

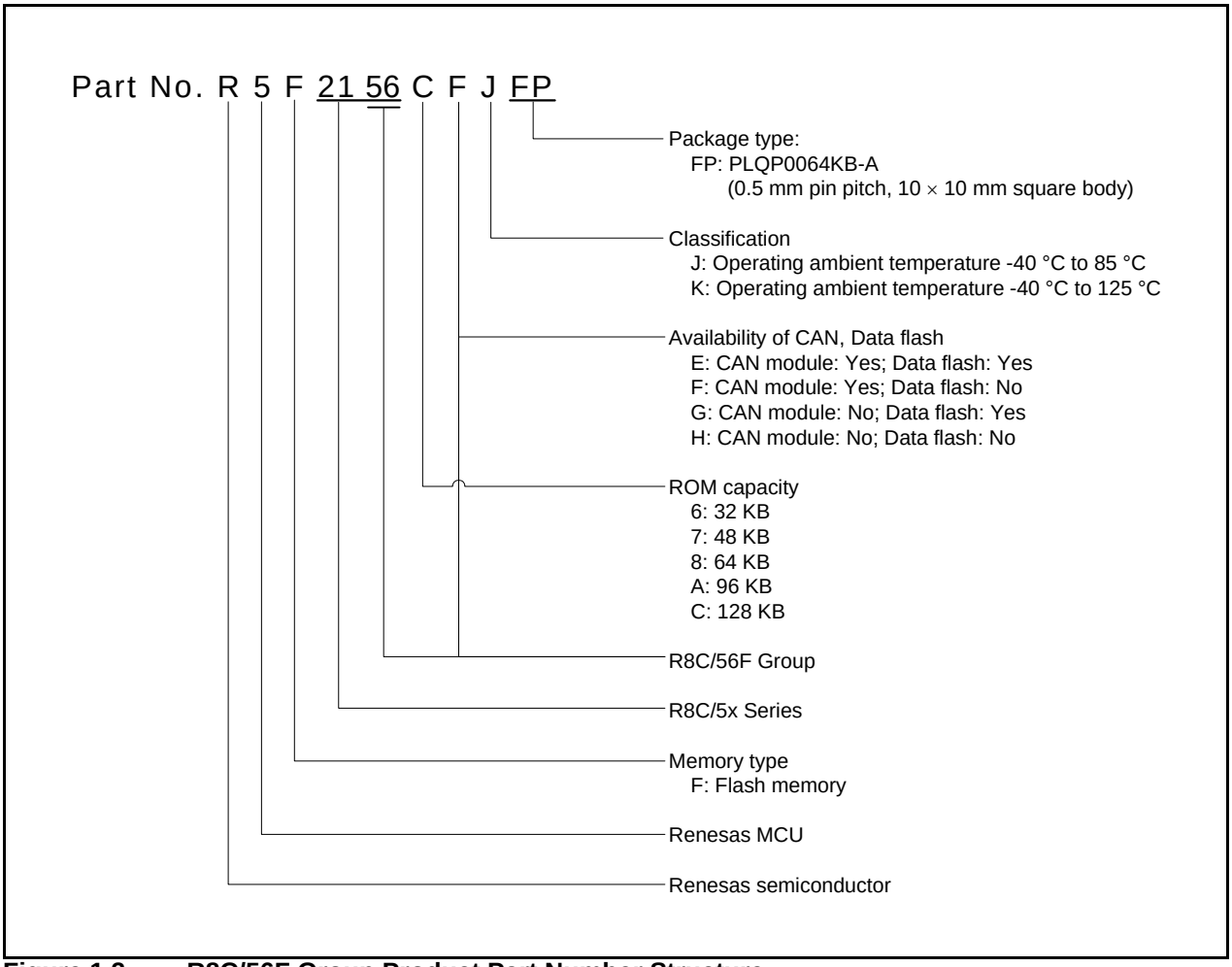


Figure 1.2 R8C/56F Group Product Part Number Structure

Table 1.15 R8C/56G Group Product List **Current of Mar 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21566GJFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A	J version
R5F21567GJFP	48 Kbytes		4 Kbytes		
R5F21568GJFP	64 Kbytes		6 Kbytes		
R5F2156AGJFP	96 Kbytes		8 Kbytes		
R5F2156CGJFP	128 Kbytes		10 Kbytes		
R5F21566GKFP	32 Kbytes		2.5 Kbytes		K version
R5F21567GKFP	48 Kbytes		4 Kbytes		
R5F21568GKFP	64 Kbytes		6 Kbytes		
R5F2156AGKFP	96 Kbytes		8 Kbytes		
R5F2156CGKFP	128 Kbytes		10 Kbytes		

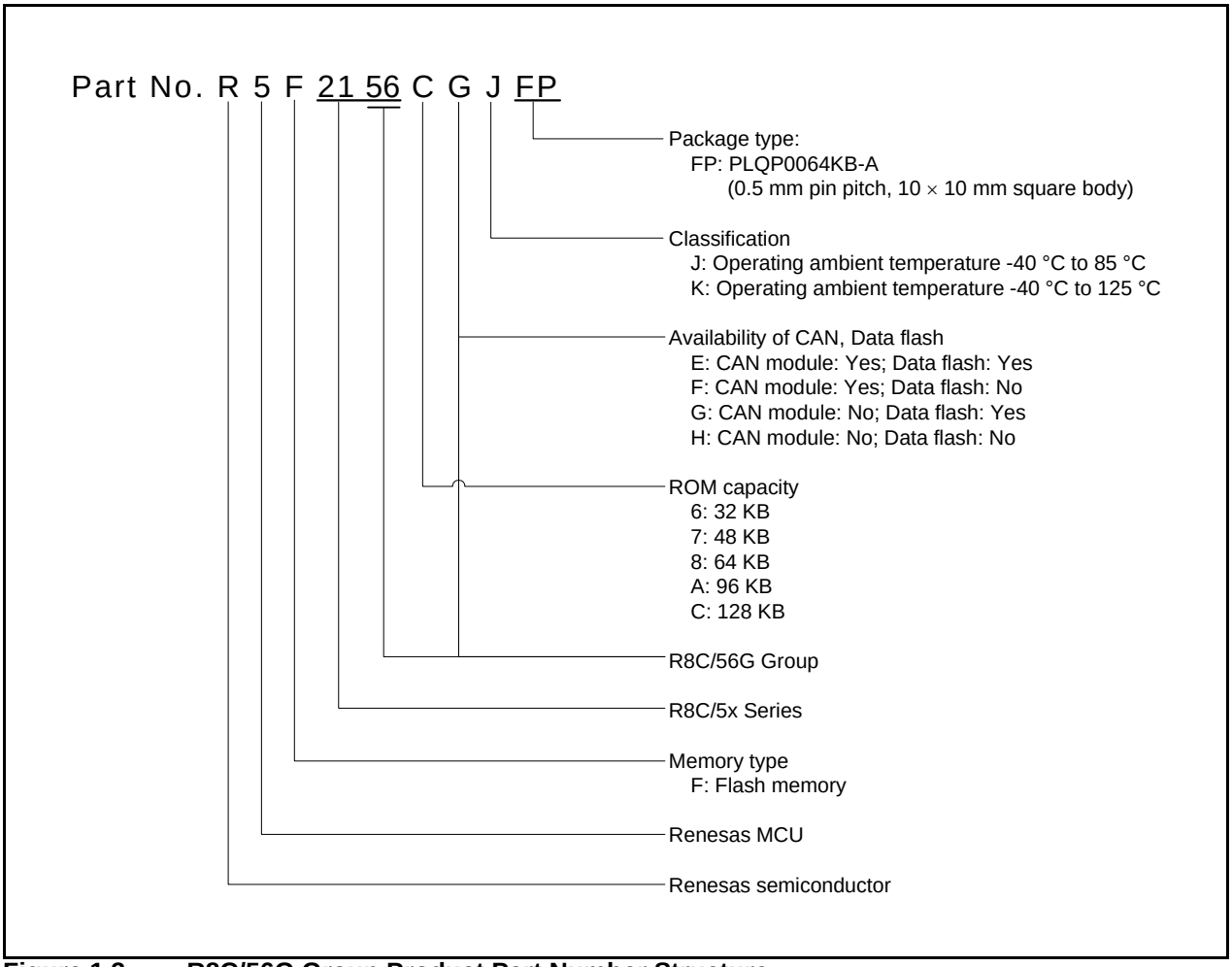


Figure 1.3 R8C/56G Group Product Part Number Structure

Table 1.16 R8C/56H Group Product List **Current of Mar 2011**

Part No.	Internal ROM Capacity Program ROM	Internal RAM Capacity	Package Type	Remarks
R5F21566HJFP	32 Kbytes	2.5 Kbytes	PLQP0064KB-A	J version
R5F21567HJFP	48 Kbytes	4 Kbytes		
R5F21568HJFP	64 Kbytes	6 Kbytes		
R5F2156AHJFP	96 Kbytes	8 Kbytes		
R5F2156CHJFP	128 Kbytes	10 Kbytes		
R5F21566HKFP	32 Kbytes	2.5 Kbytes		K version
R5F21567HKFP	48 Kbytes	4 Kbytes		
R5F21568HKFP	64 Kbytes	6 Kbytes		
R5F2156AHKFP	96 Kbytes	8 Kbytes		
R5F2156CHKFP	128 Kbytes	10 Kbytes		

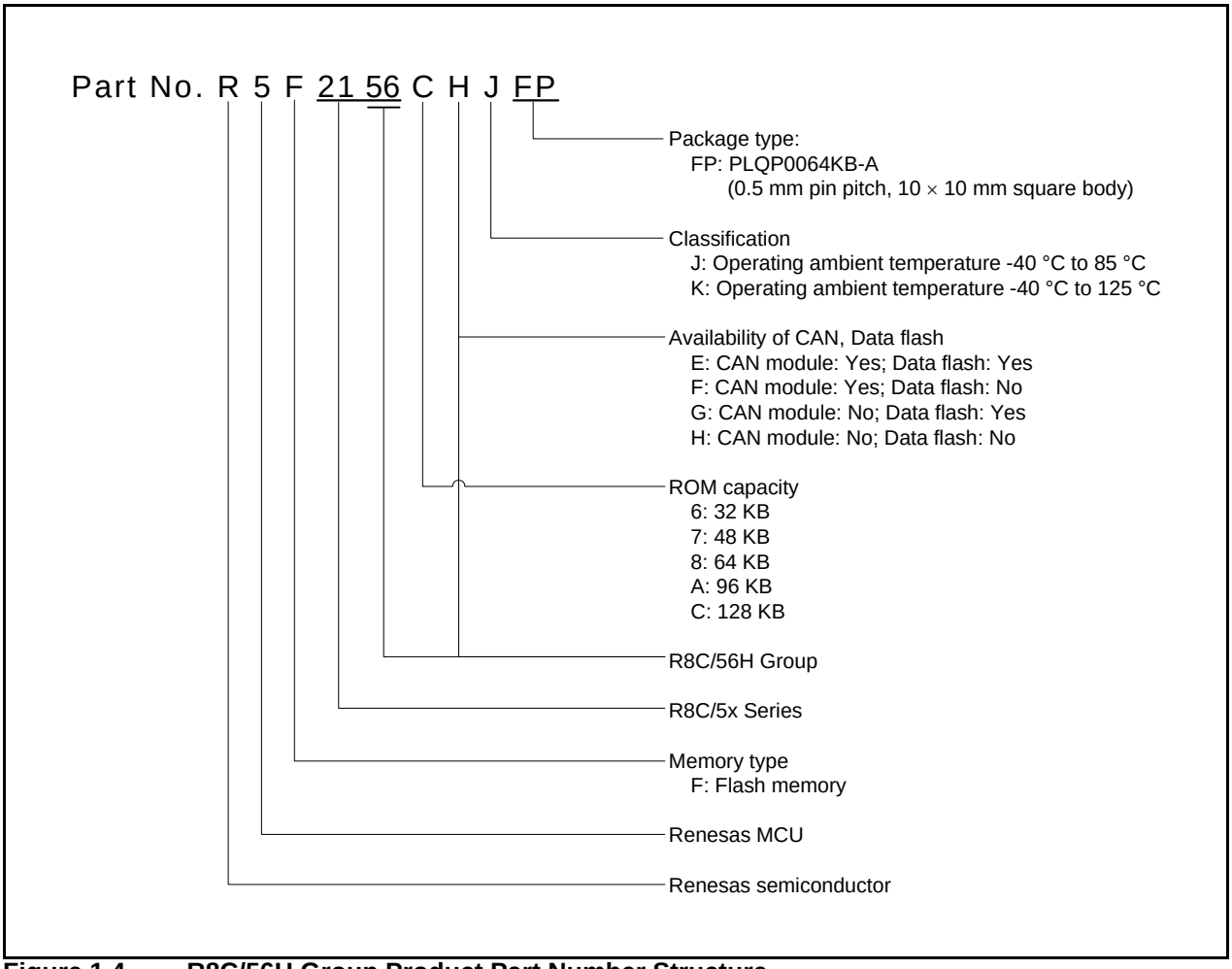
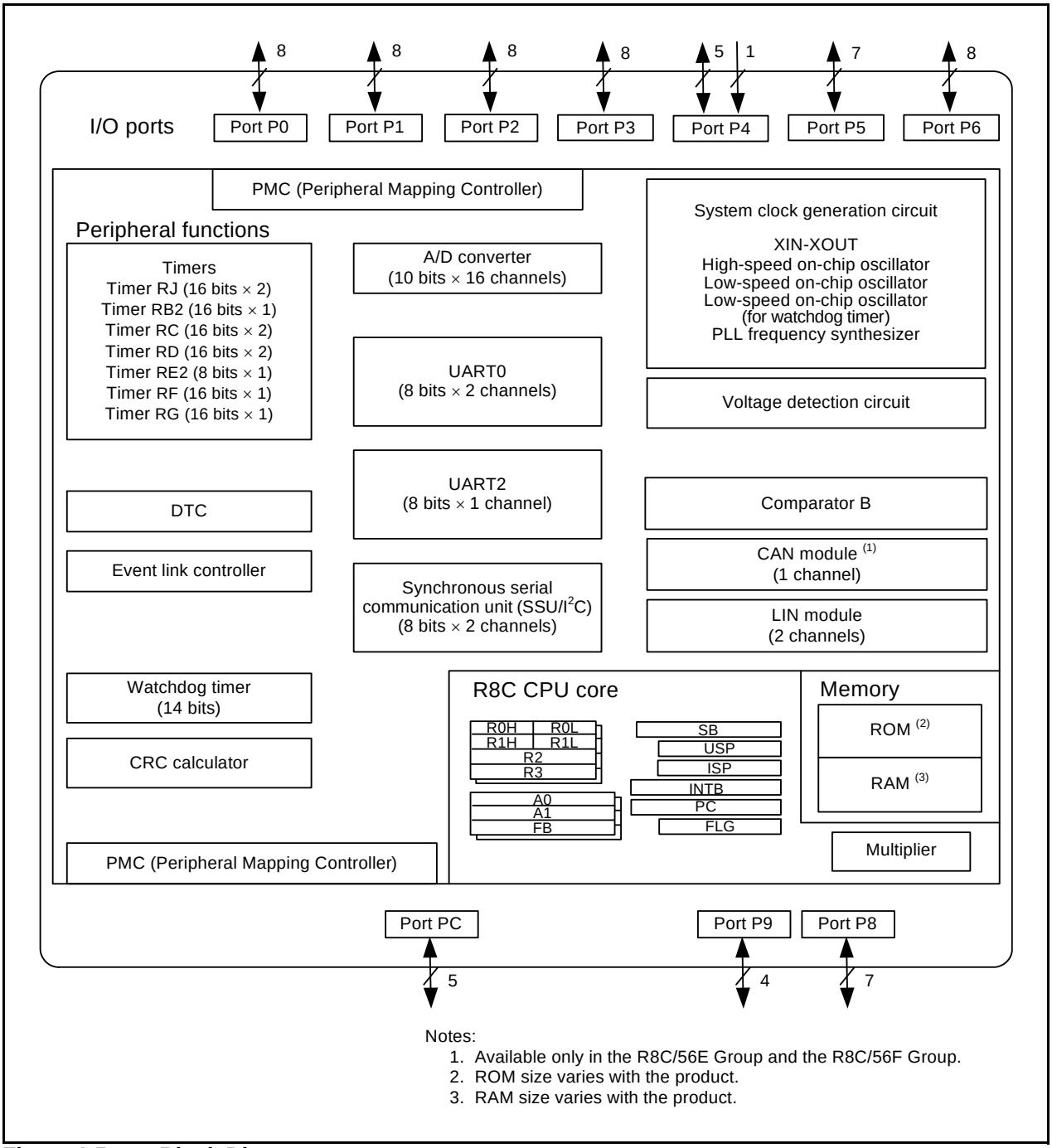


Figure 1.4 R8C/56H Group Product Part Number Structure

1.3 Block Diagram

Figure 1.5 shows the Block Diagram.

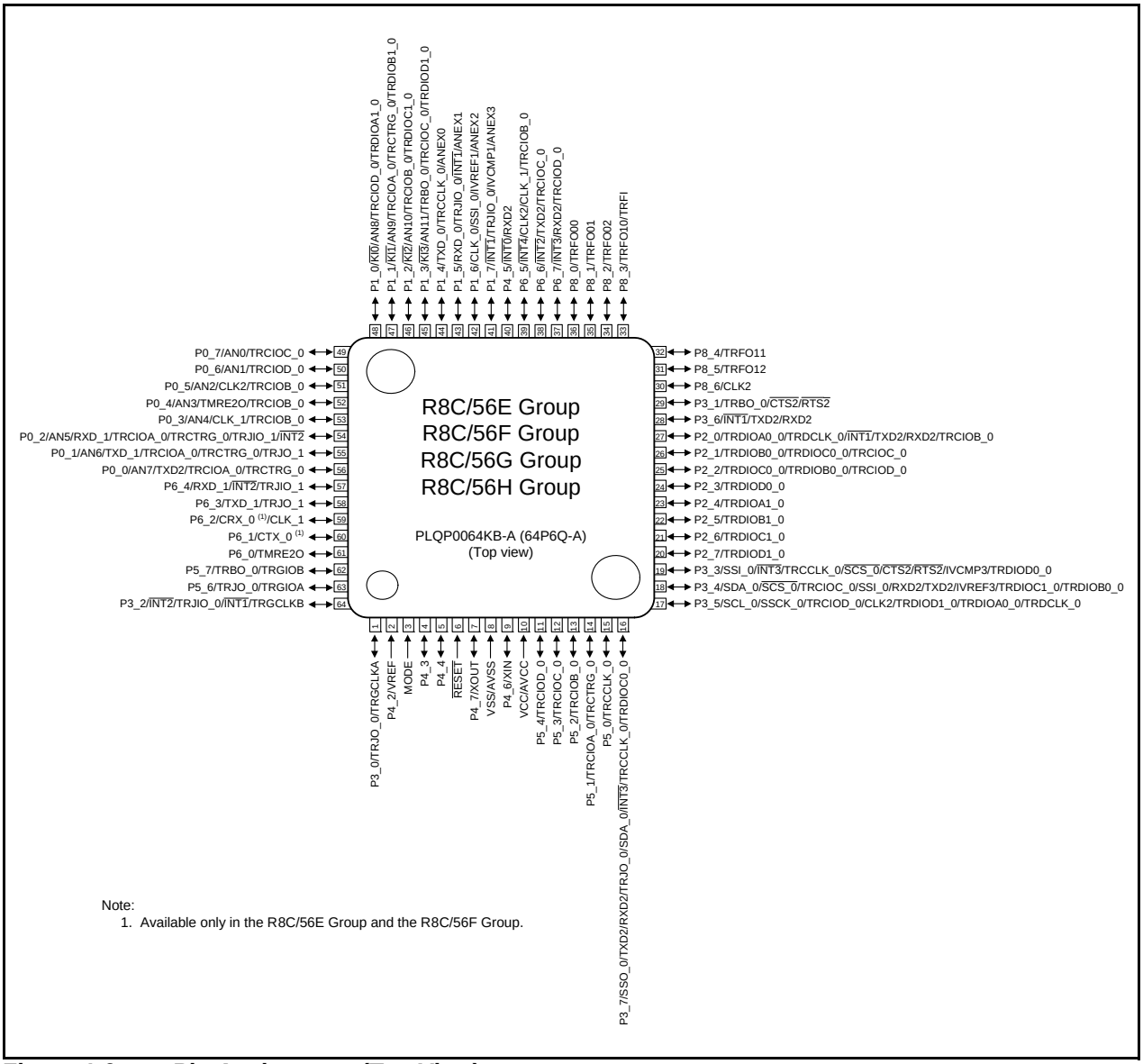


Notes:
1. Available only in the R8C/56E Group and the R8C/56F Group.
2. ROM size varies with the product.
3. RAM size varies with the product.

Figure 1.5 Block Diagram

1.4 Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.17 to 1.22 list the Pin Name Information by Pin Number.



Note:
1. Available only in the R8C/56E Group and the R8C/56F Group.

Figure 1.6 Pin Assignment (Top View)

Table 1.17 Pin Name Information by Pin Number (INT, URAT0, and UART2)

Port	Pin No.	INT					UART0						UART2				
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	CLK2
P0_0	56												TXD2				
P0_1	55							TXD_1									
P0_2	54			$\overline{INT2}$						RXD_1							
P0_3	53											CLK_1					
P0_4	52																
P0_5	51																CLK2
P0_6	50																
P0_7	49																
P1_0	48																
P1_1	47																
P1_2	46																
P1_3	45																
P1_4	44						TXD_0										
P1_5	43		$\overline{INT1}$						RXD_0								
P1_6	42										CLK_0						
P1_7	41 (1)		$\overline{INT1}$														
P2_0	27		$\overline{INT1}$										TXD2	RXD2			
P2_1	26																
P2_2	25																
P2_3	24																
P2_4	23 (1)																
P2_5	22 (1)																
P2_6	21 (1)																
P2_7	20 (1)																
P3_0	1																
P3_1	29														$\overline{CTS2}$	$\overline{RTS2}$	
P3_2	64		$\overline{INT1}$	$\overline{INT2}$													
P3_3	19				$\overline{INT3}$										$\overline{CTS2}$	$\overline{RTS2}$	
P3_4	18												TXD2	RXD2			
P3_5	17																CLK2
P3_6	28		$\overline{INT1}$										TXD2	RXD2			
P3_7	16				$\overline{INT3}$								TXD2	RXD2			
P4_2	2																
P4_3	4																
P4_4	5																
P4_5	40 (1)	$\overline{INT0}$												RXD2			
P4_6	9																
P4_7	7																
P5_0	15																
P5_1	14																
P5_2	13																
P5_3	12																
P5_4	11																
P5_6	63																
P5_7	62																
P6_0	61																
P6_1	60																
P6_2	59											CLK_1					
P6_3	58							TXD_1									
P6_4	57			$\overline{INT2}$						RXD_1							
P6_5	39 (1)					$\overline{INT4}$						CLK_1					CLK2
P6_6	38 (1)			$\overline{INT2}$									TXD2				
P6_7	37 (1)				$\overline{INT3}$									RXD2			
P8_0	36																
P8_1	35																
P8_2	34																
P8_3	33																
P8_4	32																
P8_5	31																
P8_6	30																CLK2
P9_4	23 (1)																
P9_5	22 (1)																
P9_6	21 (1)																
P9_7	20 (1)																
PC_0	41 (1)																
PC_1	40 (1)																
PC_2	39 (1)																
PC_3	38 (1)																
PC_4	37 (1)																

Note:
1. Pin assignments change depending on the PMC function.

Table 1.18 Pin Name Information by Pin Number (CAN and SSU)

Port	Pin No.	CAN (1)		SSU/I²C											
		CTX_0	CRX_0	SCL_0	SCL_1	SDA_0	SDA_1	SSI_0	SSI_1	$\overline{SCS_0}$	$\overline{SCS_1}$	SSCK_0	SSCK_1	SSO_0	SSO_1
P0_0	56														
P0_1	55														
P0_2	54														
P0_3	53														
P0_4	52														
P0_5	51														
P0_6	50														
P0_7	49														
P1_0	48														
P1_1	47														
P1_2	46														
P1_3	45														
P1_4	44														
P1_5	43														
P1_6	42							SSI_0							
P1_7	41 (2)														
P2_0	27														
P2_1	26														
P2_2	25														
P2_3	24														
P2_4	23 (2)														
P2_5	22 (2)														
P2_6	21 (2)														
P2_7	20 (2)														
P3_0	1														
P3_1	29														
P3_2	64														
P3_3	19							SSI_0		$\overline{SCS_0}$					
P3_4	18					SDA_0		SSI_0		$\overline{SCS_0}$					
P3_5	17			SCL_0								SSCK_0			
P3_6	28														
P3_7	16					SDA_0								SSO_0	
P4_2	2														
P4_3	4														
P4_4	5														
P4_5	40 (2)														
P4_6	9														
P4_7	7														
P5_0	15														
P5_1	14														
P5_2	13														
P5_3	12														
P5_4	11														
P5_6	63														
P5_7	62														
P6_0	61														
P6_1	60	CTX_0													
P6_2	59		CRX_0												
P6_3	58														
P6_4	57														
P6_5	39 (2)														
P6_6	38 (2)														
P6_7	37 (2)														
P8_0	36														
P8_1	35														
P8_2	34														
P8_3	33														
P8_4	32														
P8_5	31														
P8_6	30														
P9_4	23 (2)								SSI_1						
P9_5	22 (2)						SDA_1				$\overline{SCS_1}$				
P9_6	21 (2)				SCL_1								SSCK_1		
P9_7	20 (2)														SSO_1
PC_0	41 (2)														
PC_1	40 (2)														
PC_2	39 (2)														
PC_3	38 (2)														
PC_4	37 (2)														

Notes:
1. Available only in the R8C/56E Group and the R8C/56F Group.
2. Pin assignments change depending on the PMC function.

Table 1.19 Pin Name Information by Pin Number (Timer RC)

Port	Pin No.	Timer RC												
		TRCCLK_0	TRCCLK_1	TRCIOA_0	TRCIOB_0	TRCIOC_0	TRCIOD_0	TRCTRG_0	TRCCLK_1	TRCIOA_1	TRCIOB_1	TRCIOC_1	TRCIOD_1	TRCTRG_1
P0_0	56			TRCIOA_0				TRCTRG_0						
P0_1	55			TRCIOA_0				TRCTRG_0						
P0_2	54			TRCIOA_0				TRCTRG_0						
P0_3	53				TRCIOB_0									
P0_4	52				TRCIOB_0									
P0_5	51				TRCIOB_0									
P0_6	50						TRCIOD_0							
P0_7	49					TRCIOC_0								
P1_0	48						TRCIOD_0							
P1_1	47			TRCIOA_0				TRCTRG_0						
P1_2	46				TRCIOB_0									
P1_3	45					TRCIOC_0								
P1_4	44	TRCCLK_0												
P1_5	43													
P1_6	42													
P1_7	41 (1)													
P2_0	27				TRCIOB_0									
P2_1	26					TRCIOC_0								
P2_2	25						TRCIOD_0							
P2_3	24													
P2_4	23 (1)													
P2_5	22 (1)													
P2_6	21 (1)													
P2_7	20 (1)													
P3_0	1													
P3_1	29													
P3_2	64													
P3_3	19	TRCCLK_0												
P3_4	18					TRCIOC_0								
P3_5	17						TRCIOD_0							
P3_6	28													
P3_7	16	TRCCLK_0												
P4_2	2													
P4_3	4													
P4_4	5													
P4_5	40 (1)													
P4_6	9													
P4_7	7													
P5_0	15	TRCCLK_0												
P5_1	14			TRCIOA_0				TRCTRG_0						
P5_2	13				TRCIOB_0									
P5_3	12					TRCIOC_0								
P5_4	11						TRCIOD_0							
P5_6	63													
P5_7	62													
P6_0	61													
P6_1	60													
P6_2	59													
P6_3	58													
P6_4	57													
P6_5	39 (1)				TRCIOB_0									
P6_6	38 (1)					TRCIOC_0								
P6_7	37 (1)						TRCIOD_0							
P8_0	36													
P8_1	35													
P8_2	34													
P8_3	33													
P8_4	32													
P8_5	31													
P8_6	30													
P9_4	23 (1)													
P9_5	22 (1)													
P9_6	21 (1)													
P9_7	20 (1)													
PC_0	41 (1)								TRCCLK_1					
PC_1	40 (1)									TRCIOA_1				TRCTRG_1
PC_2	39 (1)										TRCIOB_1			
PC_3	38 (1)											TRCIOC_1		
PC_4	37 (1)												TRCIOD_1	

Note:
1. Pin assignments change depending on the PMC function.

Table 1.20 Pin Name Information by Pin Number (Timer RD)

Port	Pin No.	Timer RD								
		TRDCLK_0	TRDIOA0_0	TRDIOB0_0	TRDIOC0_0	TRDIOD0_0	TRDIOA1_0	TRDIOB1_0	TRDIOC1_0	TRDIOD1_0
P0_0	56									
P0_1	55									
P0_2	54									
P0_3	53									
P0_4	52									
P0_5	51									
P0_6	50									
P0_7	49									
P1_0	48						TRDIOA1_0			
P1_1	47							TRDIOB1_0		
P1_2	46								TRDIOC1_0	
P1_3	45									TRDIOD1_0
P1_4	44									
P1_5	43									
P1_6	42									
P1_7	41 (1)									
P2_0	27	TRDCLK_0	TRDIOA0_0							
P2_1	26			TRDIOB0_0	TRDIOC0_0					
P2_2	25			TRDIOB0_0	TRDIOC0_0					
P2_3	24					TRDIOD0_0				
P2_4	23 (1)						TRDIOA1_0			
P2_5	22 (1)							TRDIOB1_0		
P2_6	21 (1)								TRDIOC1_0	
P2_7	20 (1)									TRDIOD1_0
P3_0	1									
P3_1	29									
P3_2	64									
P3_3	19					TRDIOD0_0				
P3_4	18			TRDIOB0_0					TRDIOC1_0	
P3_5	17	TRDCLK_0	TRDIOA0_0							TRDIOD1_0
P3_6	28									
P3_7	16				TRDIOC0_0					
P4_2	2									
P4_3	4									
P4_4	5									
P4_5	40 (1)									
P4_6	9									
P4_7	7									
P5_0	15									
P5_1	14									
P5_2	13									
P5_3	12									
P5_4	11									
P5_6	63									
P5_7	62									
P6_0	61									
P6_1	60									
P6_2	59									
P6_3	58									
P6_4	57									
P6_5	39 (1)									
P6_6	38 (1)									
P6_7	37 (1)									
P8_0	36									
P8_1	35									
P8_2	34									
P8_3	33									
P8_4	32									
P8_5	31									
P8_6	30									
P9_4	23 (1)									
P9_5	22 (1)									
P9_6	21 (1)									
P9_7	20 (1)									
PC_0	41 (1)									
PC_1	40 (1)									
PC_2	39 (1)									
PC_3	38 (1)									
PC_4	37 (1)									

Note:
1. Pin assignments change depending on the PMC function.

Table 1.21 Pin Name Information by Pin Number (Timer RJ, Timer RB2, Timer RE2, and Timer RF)

Port	Pin No.	Timer RJ				Timer RB2	Timer RE2	Timer RF						
		TRJO_0	TRJO_1	TRJIO_0	TRJIO_1	TRBO_0	TMRE2O	TRFI	TRFO00	TRFO01	TRFO02	TRFO10	TRFO11	TRFO12
P0_0	56													
P0_1	55		TRJO_1											
P0_2	54				TRJIO_1									
P0_3	53													
P0_4	52						TMRE2O							
P0_5	51													
P0_6	50													
P0_7	49													
P1_0	48													
P1_1	47													
P1_2	46													
P1_3	45					TRBO_0								
P1_4	44													
P1_5	43			TRJIO_0										
P1_6	42													
P1_7	41 (1)			TRJIO_0										
P2_0	27													
P2_1	26													
P2_2	25													
P2_3	24													
P2_4	23 (1)													
P2_5	22 (1)													
P2_6	21 (1)													
P2_7	20 (1)													
P3_0	1	TRJO_0												
P3_1	29					TRBO_0								
P3_2	64			TRJIO_0										
P3_3	19													
P3_4	18													
P3_5	17													
P3_6	28													
P3_7	16	TRJO_0												
P4_2	2													
P4_3	4													
P4_4	5													
P4_5	40 (1)													
P4_6	9													
P4_7	7													
P5_0	15													
P5_1	14													
P5_2	13													
P5_3	12													
P5_4	11													
P5_6	63	TRJO_0												
P5_7	62					TRBO_0								
P6_0	61						TMRE2O							
P6_1	60													
P6_2	59													
P6_3	58		TRJO_1											
P6_4	57				TRJIO_1									
P6_5	39 (1)													
P6_6	38 (1)													
P6_7	37 (1)													
P8_0	36								TRFO00					
P8_1	35									TRFO01				
P8_2	34										TRFO02			
P8_3	33							TRFI				TRFO10		
P8_4	32												TRFO11	
P8_5	31													TRFO12
P8_6	30													
P9_4	23 (1)													
P9_5	22 (1)													
P9_6	21 (1)													
P9_7	20 (1)													
PC_0	41 (1)													
PC_1	40 (1)													
PC_2	39 (1)													
PC_3	38 (1)													
PC_4	37 (1)													

Note:
1. Pin assignments change depending on the PMC function.

Table 1.22 Pin Name Information by Pin Number (Timer RG and Others)

Port	Pin No.	Timer RG				Others		
		TRGCLKA	TRGCLKB	TRGIOA	TRGGIOB			
P0_0	56					AN7		
P0_1	55					AN6		
P0_2	54					AN5		
P0_3	53					AN4		
P0_4	52					AN3		
P0_5	51					AN2		
P0_6	50					AN1		
P0_7	49					AN0		
P1_0	48					$\overline{KI0}$	AN8	
P1_1	47					$\overline{KI1}$	AN9	
P1_2	46					$\overline{KI2}$	AN10	
P1_3	45					$\overline{KI3}$	AN11	
P1_4	44						ANEX0	
P1_5	43						ANEX1	
P1_6	42					IVREF1		ANEX2
P1_7	41 (1)					IVCMP1	ANEX3	
P2_0	27							
P2_1	26							
P2_2	25							
P2_3	24							
P2_4	23 (1)							
P2_5	22 (1)							
P2_6	21 (1)							
P2_7	20 (1)							
P3_0	1	TRGCLKA						
P3_1	29							
P3_2	64		TRGCLKB					
P3_3	19					IVCMP3		
P3_4	18					IVREF3		
P3_5	17							
P3_6	28							
P3_7	16							
P4_2	2					VREF		
P4_3	4							
P4_4	5							
P4_5	40 (1)							
P4_6	9					XIN		
P4_7	7					XOUT		
P5_0	15							
P5_1	14							
P5_2	13							
P5_3	12							
P5_4	11							
P5_6	63			TRGIOA				
P5_7	62				TRGGIOB			
P6_0	61							
P6_1	60							
P6_2	59							
P6_3	58							
P6_4	57							
P6_5	39 (1)							
P6_6	38 (1)							
P6_7	37 (1)							
P8_0	36							
P8_1	35							
P8_2	34							
P8_3	33							
P8_4	32							
P8_5	31							
P8_6	30							
P9_4	23 (1)							
P9_5	22 (1)							
P9_6	21 (1)							
P9_7	20 (1)							
PC_0	41 (1)							
PC_1	40 (1)							
PC_2	39 (1)							
PC_3	38 (1)							
PC_4	37 (1)							

Note:
1. Pin assignments change depending on the PMC function.

1.5 Pin Functions

Tables 1.23 and 1.24 list Pin Functions.

Table 1.23 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 2. 7 V through 5.5 V to the VCC pin when the CPU clock = 32 MHz and apply 1.8 V through 2.7 V to this pin when the CPU clock = 5 MHz. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
Timers RJ_0 and RJ_1	TRJIO_0, TRJIO_1	I/O	Input/output for timer RJ.
	TRJO_0, TRJO_1	O	Output for timer RJ.
Timers RB2_0	TRBO_0	O	Output for timer RB2.
Timers RC_0 and RC_1	TRCCLK_0, TRCCLK_1	I	External clock input.
	TRCTRG_0, TRCTRG_1	I	External trigger input.
	TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, TRCIOA_1, TRCIOB_1, TRCIOC_1, TRCIOD_1	I/O	Input/output for timer RC.
Timers RD_0	TRDIOA0_0, TRDIOA1_0, TRDIOB0_0, TRDIOB1_0, TRDIOC0_0, TRDIOC1_0, TRDIOD0_0, TRDIOD1_0	I/O	Input/output for timer RD.
	TRDCLK_0	I	External clock input.
Timer RE2	TMRE2O	O	Divided clock output.
Timer RF	TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12	O	Output for timer RF.
	TRFI	I	Input for timer RF.
Timer RG	TRGIOA, TRGIOB	I/O	Input/output for timer RG.
	TRGCLKA, TRGCLKB	I	External clock input.
Serial interface (UART0)	CLK_0, CLK_1	I/O	Transfer clock input/output.
	RXD_0, RXD_1	I	Serial data input.
	TXD_0, TXD_1	O	Serial data output.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

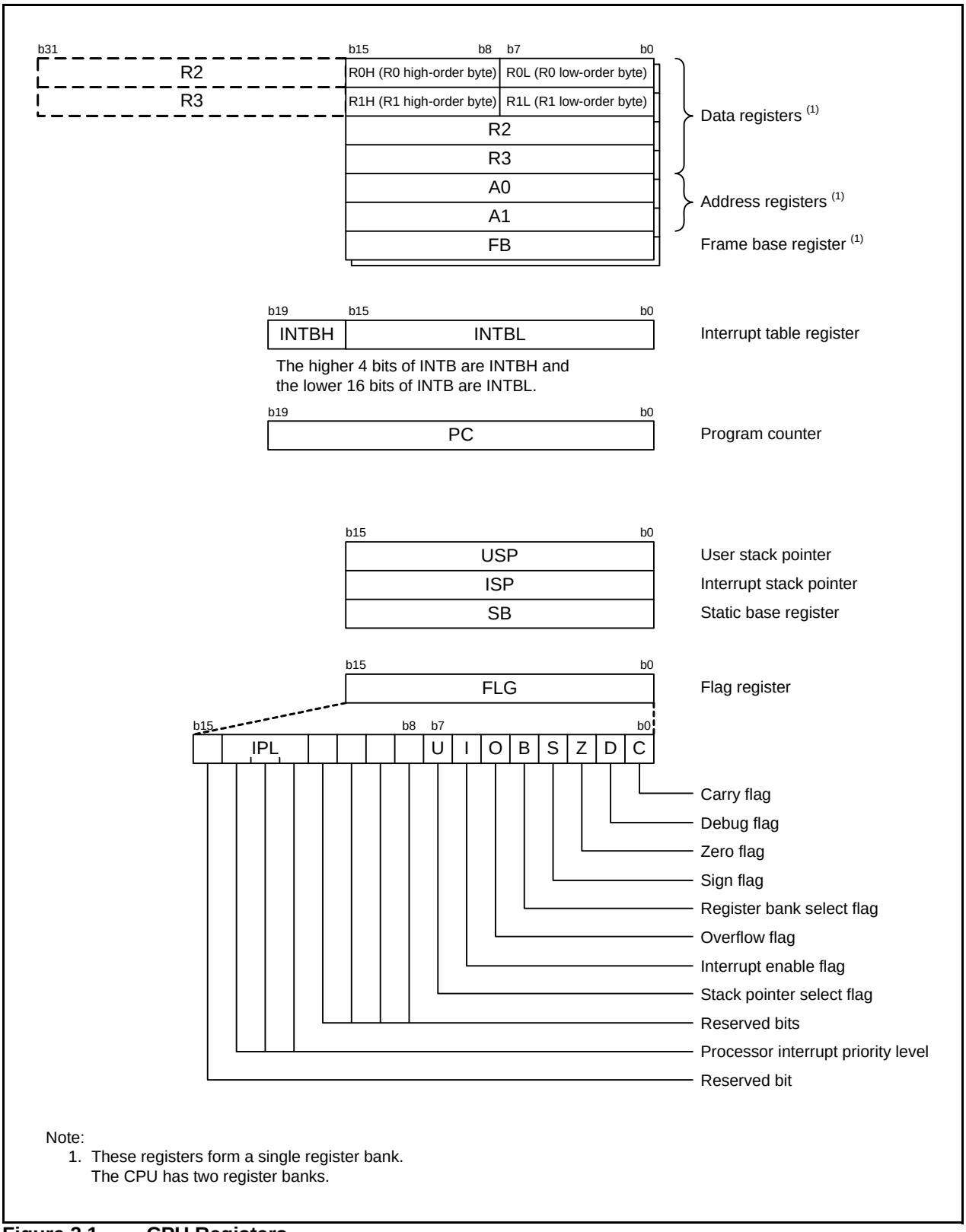
Table 1.24 Pin Functions (2)

Item	Pin Name	I/O	Description
Serial interface (UART2)	$\overline{\text{CTS2}}$	I	Input for transmission control.
	$\overline{\text{RTS2}}$	O	Output for reception control.
	RXD2	I	Serial data input.
	TXD2	O	Serial data output.
	CLK2	I/O	Transfer clock input/output.
Synchronous serial communication unit (SSU_0, SSU_1)	SSI_0, SSI_1	I/O	Data input/output.
	$\overline{\text{SCS_0}}$, $\overline{\text{SCS_1}}$	I/O	Chip-select input/output.
	SSCK_0, SSCK_1	I/O	Clock input/output.
	SSO_0, SSO_1	I/O	Data input/output.
I^2C bus (I^2C_0 and I^2C_1)	SCL_0, SCL_1	I/O	Clock input/output.
	SDA_0, SDA_1	I/O	Data input/output.
CAN module (CAN_0) (1)	CRX_0	I	Data input for CAN.
	CTX_0	O	Data output for CAN.
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.
A/D converter	AN0 to AN11, ANEX0 to ANEX3	I	Analog input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6, P9_4 to P9_7, PC_0 to PC_4	I/O	8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports.
Input port	P4_2	I	Input-only port.

Note:
1. Available only in the R8C/56E Group and the R8C/56F Group.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). In the same way as with R0 and R2, R3 and R1 can be used as a 32-bit data register (R3R1).

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

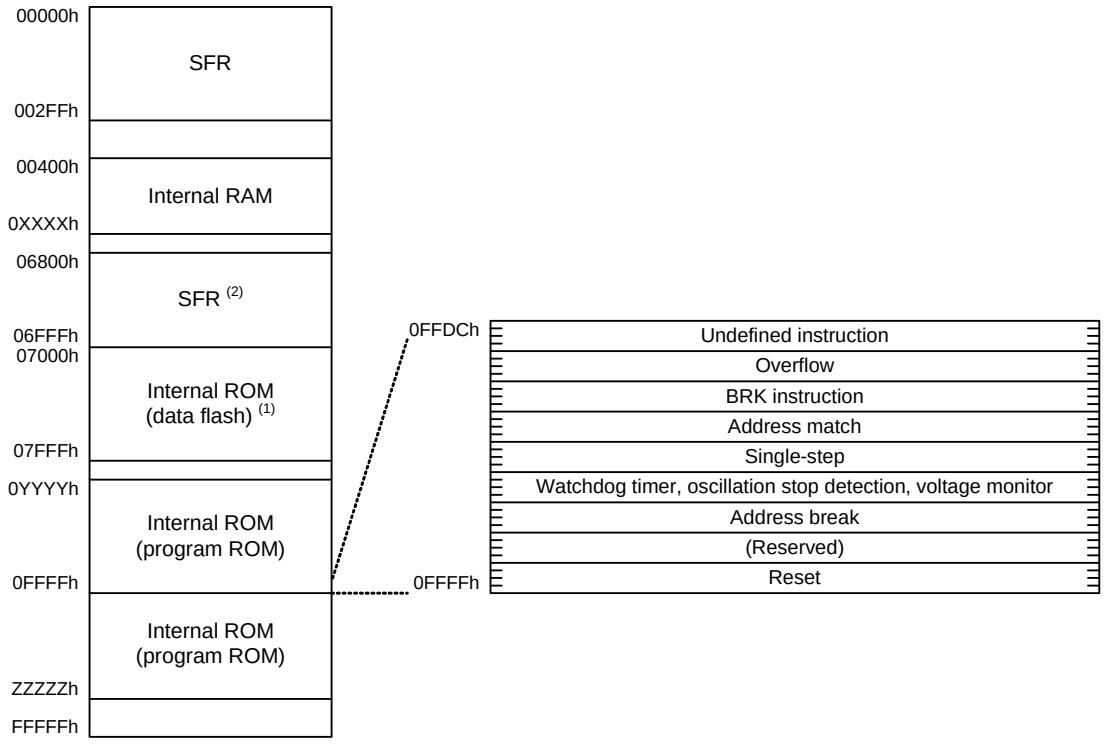
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 R8C/56E Group Memory Map

Figure 3.1 shows the R8C/56E Group Memory Map. The R8C/56E Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



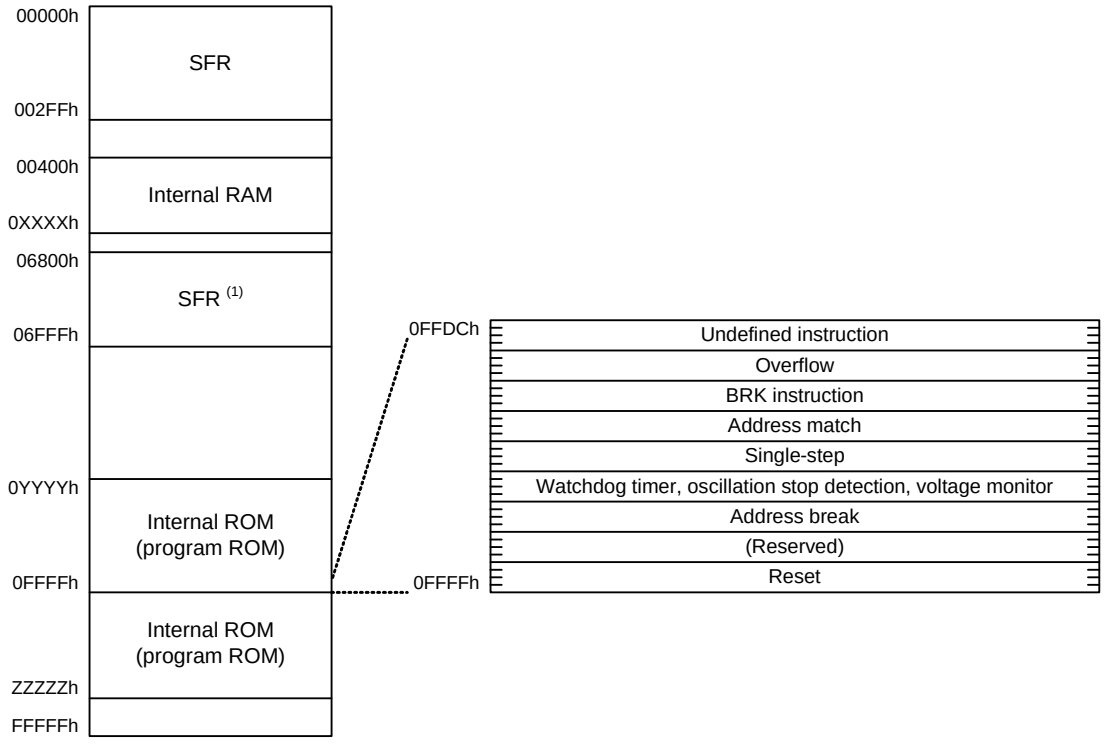
Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the CAN, DTC, and other SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21566EJFP, R5F21566EKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21567EJFP, R5F21567EKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21568EJFP, R5F21568EKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2156AEJFP, R5F2156AEKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2156CEJFP, R5F2156CEKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.1 R8C/56E Group Memory Map

3.2 R8C/56F Group Memory Map

Figure 3.2 shows the R8C/56F Group Memory Map. The R8C/56F Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh.
Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



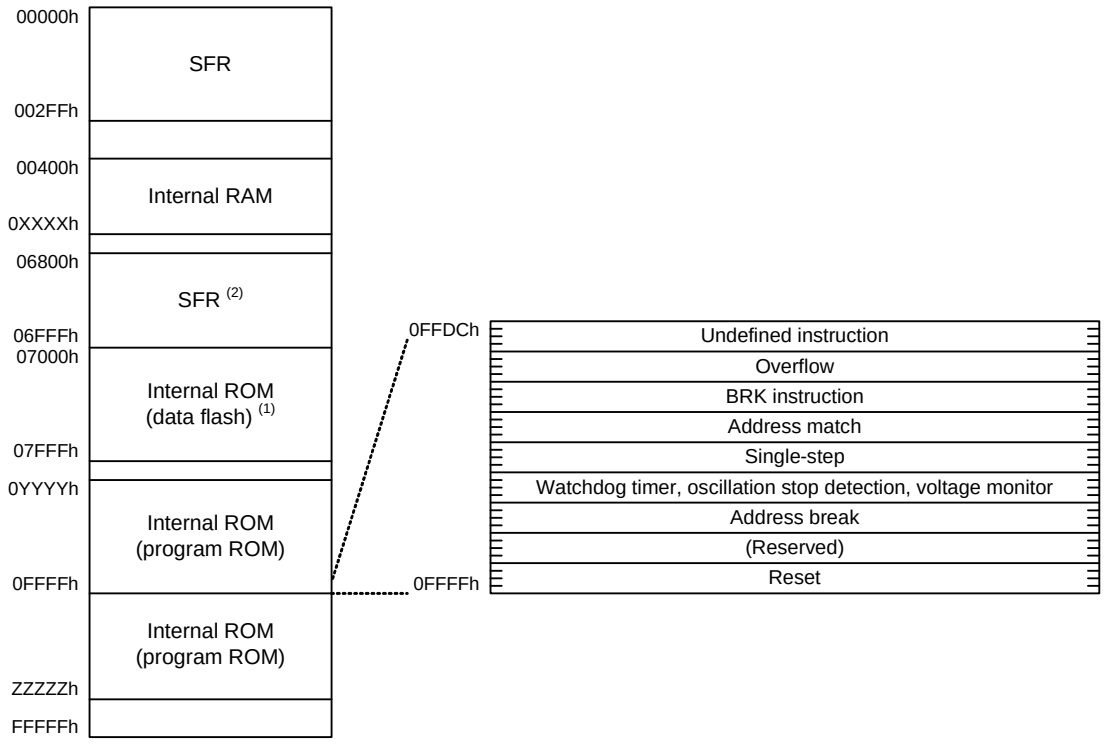
Notes:
1. Addresses 06800h to 06FFFh are used for the CAN, DTC, and other SFR areas.
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21566FJFP, R5F21566FKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21567FJFP, R5F21567FKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21568FJFP, R5F21568FKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2156AFJFP, R5F2156AFKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2156CFJFP, R5F2156CFKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.2 R8C/56F Group Memory Map

3.3 R8C/56G Group Memory Map

Figure 3.3 shows the R8C/56G Group Memory Map. The R8C/56G Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh.
Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



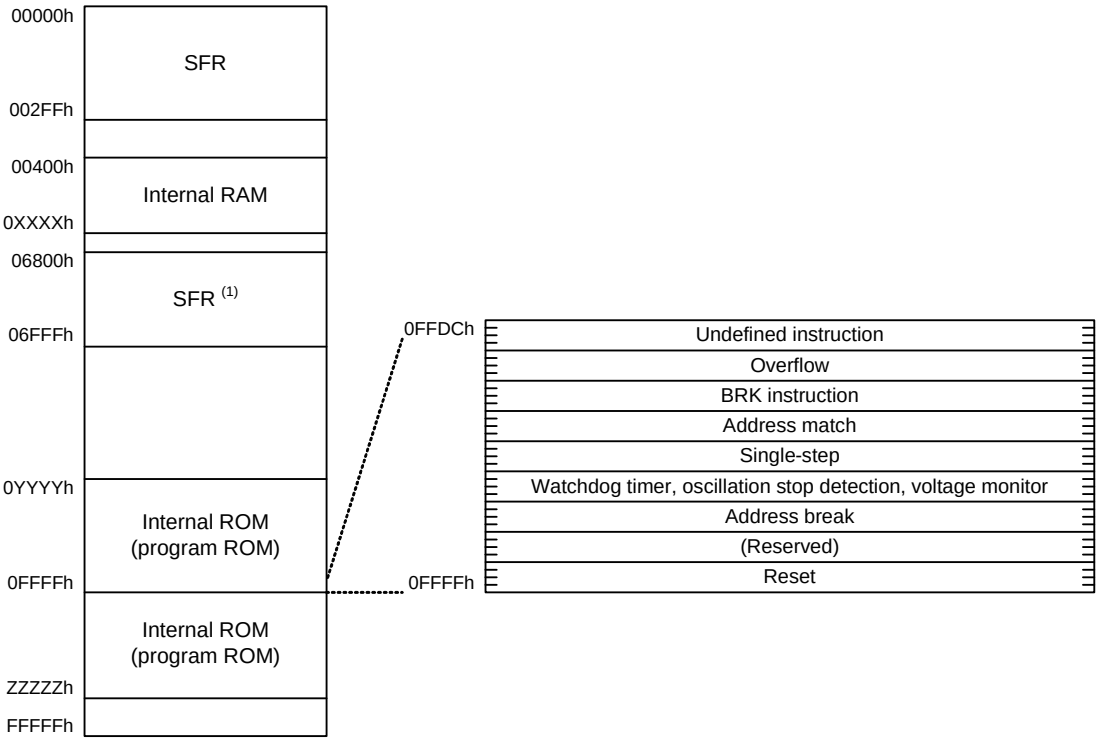
Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the DTC and other SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21566GJFP, R5F21566GKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21567GJFP, R5F21567GKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21568GJFP, R5F21568GKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2156AGJFP, R5F2156AGKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2156CGJFP, R5F2156CGKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.3 R8C/56G Group Memory Map

3.4 R8C/56H Group Memory Map

Figure 3.4 shows the R8C/56H Group Memory Map. The R8C/56H Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Addresses 06800h to 06FFFh are used for the DTC and other SFR areas.
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21566HJFP, R5F21566HKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21567HJFP, R5F21567HKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21568HJFP, R5F21568HKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2156AHJFP, R5F2156AHKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2156CHJFP, R5F2156CHKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.4 R8C/56H Group Memory Map

3.5 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.23 list the SFR Information. Table 3.24 lists the ID code Area, Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Symbol	Register Name	After Reset	Remarks
00000h				
00001h				
00002h				
00003h				
00004h	PM0	Processor Mode Register 0	00h	
00005h	PM1	Processor Mode Register 1	10000000b	
00006h				
00007h	PRCR	Protect Register	00h	
00008h	CM0	System Clock Control Register 0	00101000b	
00009h	CM1	System Clock Control Register 1	00100000b	
0000Ah	OCD	Oscillation Stop Detection Register	00h	
0000Bh	CM3	System Clock Control Register 3	00h	
0000Ch	CM4	System Clock Control Register 4	00000001b	
0000Dh				
0000Eh				
0000Fh	PCLKR1	Peripheral Clock Select Register 1	00h	
00010h				
00011h				
00012h	FRA0	High-Speed On-Chip Oscillator Control Register 0	00h	
00013h				
00014h	FRA2	High-Speed On-Chip Oscillator Control Register 2	00h	
00015h				
00016h				
00017h				
00018h				
00019h				
0001Ah				
0001Bh				
0001Ch	PLC0	PLL Control Register 0	00010010b	
0001Dh	PLCF	PLL Function Clock Control Register 1	00h	
0001Eh				
0001Fh				
00020h	RISR	Reset Interrupt Select Register	10000000b or 00000000b	(Note 2)
00021h	WDTR	Watchdog Timer Reset Register	FFh	
00022h	WDTS	Watchdog Timer Start Register	FFh	
00023h	WDTC	Watchdog Timer Control Register	01111111b	
00024h	CSPR	Count Source Protection Mode Register	10000000b or 00000000b	(Note 2)
00025h				
00026h				
00027h				
00028h	RSTFR	Reset Source Determination Register	00XXXXXXb	
00029h				
0002Ah				
0002Bh				
0002Ch	SVDC	STBY VDC Power Control Register	00h	
0002Dh				
0002Eh				
0002Fh				
00030h	CMPA	Voltage Monitor Circuit Control Register	00h	
00031h	VCAC	Voltage Monitor Circuit Edge Select Register	00h	
00032h	OCVREFCR	On-Chip Reference Voltage Control Register	00h	
00033h				
00034h	VCA2	Voltage Detection Register 2	00000000b or 00100000b	(Note 3)
00035h				
00036h	VD1LS	Voltage Detection 1 Level Select Register	00000111b	
00037h				
00038h	VW0C	Voltage Monitor 0 Circuit Control Register	11001010b or 11001011b	(Note 3)
00039h	VW1C	Voltage Monitor 1 Circuit Control Register	10001010b	

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.

Table 3.2 SFR Information (2) (1)

Address	Symbol	Register Name	After Reset	Remarks
0003Ah	VW2C	Voltage Monitor 2 Circuit Control Register	10001010b	
0003Bh				
0003Ch				
0003Dh				
0003Eh				
0003Fh				
00040h				
00041h	FMRDYIC	Interrupt Control Register	00h	
00042h	TRJIC_1	Interrupt Control Register	00h	
00043h				
00044h				
00045h				
00046h	INT4IC	Interrupt Control Register	00h	
00047h	TRCIC_0	Interrupt Control Register	00h	
00048h	TRD0IC_0	Interrupt Control Register	00h	
00049h	TRD1IC_0	Interrupt Control Register	00h	
0004Ah	TRE2IC	Interrupt Control Register	00h	
0004Bh	U2TIC	Interrupt Control Register	00h	
0004Ch	U2RIC	Interrupt Control Register	00h	
0004Dh	KUPIC	Interrupt Control Register	00h	
0004Eh	ADIC	Interrupt Control Register	00h	
0004Fh	SSUIC_0/IICIC_0	Interrupt Control Register	00h	
00050h	TRFIC	Interrupt Control Register	00h	
00051h	U0TIC_0	Interrupt Control Register	00h	
00052h	U0RIC_0	Interrupt Control Register	00h	
00053h	U0TIC_1	Interrupt Control Register	00h	
00054h	U0RIC_1	Interrupt Control Register	00h	
00055h	INT2IC	Interrupt Control Register	00h	
00056h	TRJIC_0	Interrupt Control Register	00h	
00057h				
00058h	TRB2IC_0	Interrupt Control Register	00h	
00059h	INT1IC	Interrupt Control Register	00h	
0005Ah	INT3IC	Interrupt Control Register	00h	
0005Bh				
0005Ch				
0005Dh	INT0IC	Interrupt Control Register	00h	
0005Eh	U2BCNIC	Interrupt Control Register	00h	
0005Fh				
00060h				
00061h				
00062h				
00063h				
00064h				
00065h				
00066h				
00067h				
00068h				
00069h				
0006Ah				
0006Bh	TRGIC	Interrupt Control Register	00h	
0006Ch	CANRXIC_0	Interrupt Control Register	00h	
0006Dh	CANTXIC_0	Interrupt Control Register	00h	
0006Eh	CANERIC_0	Interrupt Control Register	00h	
0006Fh				
00070h				
00071h				
00072h	VCMP1IC	Interrupt Control Register	00h	
00073h	VCMP2IC	Interrupt Control Register	00h	
00074h				
00075h				
00076h				
00077h				
00078h				
00079h	SSUIC_1/IICIC_1	Interrupt Control Register	00h	

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.3 SFR Information (3) (1)

Address	Symbol	Register Name	After Reset	Remarks
0007Ah				
0007Bh				
0007Ch				
0007Dh				
0007Eh				
0007Fh	TRCIC_1	Interrupt Control Register	00h	
00080h	U0MR_0	UART0_0 Transmit/Receive Mode Register	00h	
00081h	U0BRG_0	UART0_0 Bit Rate Register	XXh	
00082h	U0TB_0	UART0_0 Transmit Buffer Register	XXh	
00083h			XXh	
00084h	U0C0_0	UART0_0 Transmit/Receive Control Register 0	00001000b	
00085h	U0C1_0	UART0_0 Transmit/Receive Control Register 1	00000010b	
00086h	U0RB_0	UART0_0 Receive Buffer Register	XXXXh	
00087h				
00088h	U0IR_0	UART0_0 Interrupt Flag and Enable Register	00h	
00089h				
0008Ah				
0008Bh				
0008Ch	LINCR2_0	LIN_0 Special Function Register	00h	
0008Dh				
0008Eh	LINCT_0	LIN_0 Control Register	00h	
0008Fh	LINST_0	LIN_0 Status Register	00h	
00090h	U0MR_1	UART0_1 Transmit/Receive Mode Register	00h	
00091h	U0BRG_1	UART0_1 Bit Rate Register	XXh	
00092h	U0TB_1	UART0_1 Transmit Buffer Register	XXh	
00093h			XXh	
00094h	U0C0_1	UART0_1 Transmit/Receive Control Register 0	00001000b	
00095h	U0C1_1	UART0_1 Transmit/Receive Control Register 1	00000010b	
00096h	U0RB_1	UART0_1 Receive Buffer Register	XXXXh	
00097h				
00098h	U0IR_1	UART0_1 Interrupt Flag and Enable Register	00h	
00099h				
0009Ah				
0009Bh				
0009Ch	LINCR2_1	LIN_1 Special Function Register	00h	
0009Dh				
0009Eh	LINCT_1	LIN_1 Control Register	00h	
0009Fh	LINST_1	LIN_1 Status Register	00h	
000A0h				
000A1h				
000A2h				
000A3h				
000A4h				
000A5h				
000A6h				
000A7h				
000A8h				
000A9h				
000AAh				
000ABh				
000ACh				
000ADh				
000AEh				
000AFh				
000B0h				
000B1h				
000B2h				
000B3h				
000B4h				
000B5h				
000B6h				
000B7h				
000B8h				
000B9h				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Symbol	Register Name	After Reset	Remarks
000BAh				
000BBh				
000BCh				
000BDh				
000BEh				
000BFh				
000C0h	U2MR	UART2 Transmit/Receive Mode Register	00h	
000C1h	U2BRG	UART2 Bit Rate Register	00h	
000C2h	U2TB	UART2 Transmit Buffer Register	00h	
000C3h			00h	
000C4h	U2C0	UART2 Transmit/Receive Control Register 0	00001000b	
000C5h	U2C1	UART2 Transmit/Receive Control Register 1	00000010b	
000C6h	U2RB	UART2 Receive Buffer Register	0000h	
000C7h				
000C8h	U2RXDF	UART2 Digital Filter Function Select Register	00h	
000C9h				
000CAh				
000CBh				
000CCh				
000CDh				
000CEh				
000CFh				
000D0h	U2SMR5	UART2 Special Mode Register 5	00h	
000D1h				
000D2h				
000D3h				
000D4h				
000D5h	U2SMR3	UART2 Special Mode Register 3	00h	
000D6h				
000D7h	U2SMR	UART2 Special Mode Register	00h	
000D8h				
000D9h				
000DAh				
000DBh				
000DCh				
000DDh				
000DEh				
000DFh				
000E0h	IICCR_0	I²C_0 Control Register	00001110b	
000E1h	SSBR_0	SS_0 Bit Counter Register	11111000b	
000E2h	SITDR_0	SI_0 Transmit Data Register	FFh	
000E3h			FFh	
000E4h	SIRDR_0	SI_0 Receive Data Register	FFh	
000E5h			FFh	
000E6h	SICR1_0	SI_0 Control Register 1	00h	
000E7h	SICR2_0	SI_0 Control Register 2	01111101b	
000E8h	SIMR1_0	SI_0 Mode Register 1	00010000b	
000E9h	SIER_0	SI_0 Interrrupt Enable Register	00h	
000EAh	SISR_0	SI_0 Status Register	00h	
000EBh	SIMR2_0	SI_0 Mode Register 2	00h	
000ECh				
000EDh				
000EEh				
000EFh				
000F0h	IICCR_1	I²C_1 Control Register	00001110b	
000F1h	SSBR_1	SS_1 Bit Counter Register	11111000b	
000F2h	SITDR_1	SI_1 Transmit Data Register	FFh	
000F3h			FFh	
000F4h	SIRDR_1	SI_1 Receive Data Register	FFh	
000F5h			FFh	
000F6h	SICR1_1	SI_1 Control Register 1	00h	
000F7h	SICR2_1	SI_1 Control Register 2	01111101b	
000F8h	SIMR1_1	SI_1 Mode Register 1	00010000b	
000F9h	SIER_1	SI_1 Interrrupt Enable Register	00h	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh	SISR_1	SI_1 Status Register	00h	
000FBh	SIMR2_1	SI_1 Mode Register 2	00h	
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h	TRJ_1	Timer RJ_1 Counter Register	FFFFh	
00119h				
0011Ah	TRJCR_1	Timer RJ_1 Control Register	00h	
0011Bh	TRJIOC_1	Timer RJ_1 I/O Control Register	00h	
0011Ch	TRJMR_1	Timer RJ_1 Mode Register	00h	
0011Dh	TRJISR_1	Timer RJ_1 Event Pin Select Register	00h	
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	Timer RB2_0 Prescaler Register Timer RB2_0 Primary/Secondary Register (Lower 8 Bits)	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register Timer RB2_0 Primary Register (Higher 8 Bits)	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register Timer RB2_0 Secondary Register (Higher 8 Bits)	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request and Status Register	00h	
00138h	TRCCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h	TRCCNT_1	Timer RC_1 Counter	0000h	
00159h				
0015Ah	TRCGRA_1	Timer RC_1 General Register A	FFFFh	
0015Bh				
0015Ch	TRCGRB_1	Timer RC_1 General Register B	FFFFh	
0015Dh				
0015Eh	TRCGRC_1	Timer RC_1 General Register C	FFFFh	
0015Fh				
00160h	TRCGRD_1	Timer RC_1 General Register D	FFFFh	
00161h				
00162h	TRCMR_1	Timer RC_1 Mode Register	01001000b	
00163h	TRCCR1_1	Timer RC_1 Control Register 1	00h	
00164h	TRCIER_1	Timer RC_1 Interrupt Enable Register	01110000b	
00165h	TRCSR_1	Timer RC_1 Status Register	01110000b	
00166h	TRCIOR0_1	Timer RC_1 I/O Control Register 0	10001000b	
00167h	TRCIOR1_1	Timer RC_1 I/O Control Register 1	10001000b	
00168h	TRCCR2_1	Timer RC_1 Control Register 2	00011000b	
00169h	TRCDF_1	Timer RC_1 Digital Filter Function Select Register	00h	
0016Ah	TRCOER_1	Timer RC_1 Output Enable Register	01111111b	
0016Bh	TRCADCR_1	Timer RC_1 A/D Conversion trigger Control Register	11110000b	
0016Ch	TRCOPR_1	Timer RC_1 Output Waveform Manipulation Register	00h	
0016Dh	TRCELCCR_1	Timer RC_1 ELC Cooperation Control Register	00h	
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register	00h	
00172h				
00173h				
00174h				
00175h				
00176h				
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Symbol	Register Name	After Reset	Remarks
0017Ah	TREIFR	Timer RE2 Interrupt Flag Register	00h	
0017Bh	TREIER	Timer RE2 Interrupt Enable Register	00h	
0017Ch				
0017Dh				
0017Eh				
0017Fh	TREPRC	Timer RE2 Protect Register	00h	
00180h	TRDELC_0	Timer RD_0 ELC Register	00h	
00181h				
00182h	TRDADCR_0	Timer RD_0 Trigger Control Register	00h	
00183h	TRDSTR_0	Timer RD_0 Start Register	11111100b	
00184h	TRDMR_0	Timer RD_0 Mode Register	00001110b	
00185h	TRDPMR_0	Timer RD_0 PWM Mode Register	10001000b	
00186h	TRDFCR_0	Timer RD_0 Function Control Register	10000000b	
00187h	TRDOER1_0	Timer RD_0 Output Master Enable Register 1	FFh	
00188h	TRDOER2_0	Timer RD_0 Output Master Enable Register 2	01111111b	
00189h	TRDOCR_0	Timer RD_0 Output Control Register	00h	
0018Ah	TRDDF0_0	Timer RD_0 Digital Filter Function Select Register 0	00h	
0018Bh	TRDDF1_0	Timer RD_0 Digital Filter Function Select Register 1	00h	
0018Ch				
0018Dh				
0018Eh				
0018Fh				
00190h	TRDCR0_0	Timer RD_0 Control Register 0	00h	
00191h	TRDIORA0_0	Timer RD_0 I/O Control Register A0	10001000b	
00192h	TRDIORC0_0	Timer RD_0 I/O Control Register C0	10001000b	
00193h	TRDSR0_0	Timer RD_0 Status Register 0	11100000b	
00194h	TRDIER0_0	Timer RD_0 Interrupt Enable Register 0	11100000b	
00195h	TRDPOCR0_0	Timer RD_0 PWM Mode Output Level Control Register 0	11111000b	
00196h	TRD0_0	Timer RD_0 Counter 0	0000h	
00197h				
00198h	TRDGRA0_0	Timer RD_0 General Register A0	FFFFh	
00199h				
0019Ah	TRDGRB0_0	Timer RD_0 General Register B0	FFFFh	
0019Bh				
0019Ch	TRDGRC0_0	Timer RD_0 General Register C0	FFFFh	
0019Dh				
0019Eh	TRDGRD0_0	Timer RD_0 General Register D0	FFFFh	
0019Fh				
001A0h	TRDCR1_0	Timer RD_0 Control Register 1	00h	
001A1h	TRDIORA1_0	Timer RD_0 I/O Control Register A1	10001000b	
001A2h	TRDIORC1_0	Timer RD_0 I/O Control Register C1	10001000b	
001A3h	TRDSR1_0	Timer RD_0 Status Register 1	11000000b	
001A4h	TRDIER1_0	Timer RD_0 Interrupt Enable Register 1	11100000b	
001A5h	TRDPOCR1_0	Timer RD_0 PWM Mode Output Level Control Register 1	11111000b	
001A6h	TRD1_0	Timer RD_0 Counter 1	0000h	
001A7h				
001A8h	TRDGRA1_0	Timer RD_0 General Register A1	FFFFh	
001A9h				
001AAh	TRDGRB1_0	Timer RD_0 General Register B1	FFFFh	
001ABh				
001ACh	TRDGRC1_0	Timer RD_0 General Register C1	FFFFh	
001ADh				
001AEh	TRDGRD1_0	Timer RD_0 General Register D1	FFFFh	
001AFh				
001B0h	TRF	Timer RF Register	0000h	
001B1h				
001B2h	TRFOUT	Timer RF Output Control Register	00h	
001B3h	TRFIN	Timer RF Input Control Register	00h	
001B4h	TRFSR	Timer RF Status Register	00h	
001B5h				
001B6h	TRFIER	Timer RF Interrupt Enable Register	00h	
001B7h				
001B8h				
001B9h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Symbol	Register Name	After Reset	Remarks
001BAh	TRFCR0	Timer RF Control Register 0	00h	
001BBh	TRFCR1	Timer RF Control Register 1	00h	
001BCh	TRFM0	Timer RF Capture Compare 0 Register	0000h	
001BDh				
001BEh	TRFM1	Timer RF Compare 1 Register	FFFFh	
001BFh				
001C0h				
001C1h				
001C2h				
001C3h				
001C4h				
001C5h				
001C6h				
001C7h				
001C8h				
001C9h				
001CAh				
001CBh				
001CCh				
001CDh				
001CEh				
001CFh				
001D0h				
001D1h				
001D2h				
001D3h				
001D4h				
001D5h				
001D6h				
001D7h				
001D8h				
001D9h				
001DAh				
001DBh				
001DCh				
001DDh				
001DEh				
001DFh				
001E0h				
001E1h				
001E2h				
001E3h				
001E4h				
001E5h				
001E6h				
001E7h				
001E8h				
001E9h				
001EAh				
001EBh				
001ECh				
001EDh				
001EEh				
001EFh				
001F0h	TRGMR	Timer RG Mode Register	00h	
001F1h	TRGCNTC	Timer RG Counter Control Register	00h	
001F2h	TRGCR	Timer RG Control Register	10000000h	
001F3h	TRGIER	Timer RG Interrupt Enable Register	11110000h	
001F4h	TRGSR	Timer RG Status Register	11100000h	
001F5h	TRGIOR	Timer RG I/O Control Register	00h	
001F6h	TRG	Timer RG Counter	0000h	
001F7h				
001F8h	TRGGRA	Timer RG General Register A	FFFFh	
001F9h				
001FAh	TRGGRB	Timer RG General Register B	FFFFh	
001FBh				
001FCh	TRGGRC	Timer RG General Register C	FFFFh	
001FDh				
001FEh	TRGGRD	Timer RG General Register D	FFFFh	
001FFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 SFR Information (9) (1)

Address	Symbol	Register Name	After Reset	Remarks
00200h	AD0	A/D Register 0	00h	
00201h			00h	
00202h	AD1	A/D Register 1	00h	
00203h			00h	
00204h	AD2	A/D Register 2	00h	
00205h			00h	
00206h	AD3	A/D Register 3	00h	
00207h			00h	
00208h	AD4	A/D Register 4	00h	
00209h			00h	
0020Ah	AD5	A/D Register 5	00h	
0020Bh			00h	
0020Ch	AD6	A/D Register 6	00h	
0020Dh			00h	
0020Eh	AD7	A/D Register 7	00h	
0020Fh			00h	
00210h				
00211h				
00212h				
00213h				
00214h	ADMOD	A/D Mode Register	00h	
00215h	ADINSEL	A/D Input Select Register	11000000b	
00216h	ADCON0	A/D Control Register 0	00h	
00217h	ADCON1	A/D Control Register 1	00h	
00218h				
00219h				
0021Ah				
0021Bh				
0021Ch				
0021Dh				
0021Eh				
0021Fh				
00220h				
00221h				
00222h				
00223h				
00224h				
00225h				
00226h				
00227h				
00228h	INTCMP	Comparator B Control Register 0	00h	
00229h				
0022Ah				
0022Bh				
0022Ch				
0022Dh				
0022Eh				
0022Fh				
00230h	INTEN	External Input Enable Register 0	00h	
00231h	INTEN1	External Input Enable Register 1	00h	
00232h	INTF	INT Input Filter Select Register 0	00h	
00233h	INTF1	INT Input Filter Select Register 1	00h	
00234h	INTPOL	INT Input Polarity Switch Register	00h	
00235h				
00236h	KIEN	Key Input Interrupt Enable Register	00h	
00237h				
00238h	MSTCR0	Module Standby Control Register 0	00h	
00239h	MSTCR1	Module Standby Control Register 1	00h	
0023Ah	MSTCR2	Module Standby Control Register 2	00h	
0023Bh	MSTCR3	Module Standby Control Register 3	00h	
0023Ch				
0023Dh				
0023Eh				
0023Fh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.10 SFR Information (10) (1)

Address	Symbol	Register Name	After Reset	Remarks
00240h				
00241h				
00242h				
00243h				
00244h				
00245h				
00246h				
00247h				
00248h				
00249h				
0024Ah				
0024Bh				
0024Ch				
0024Dh				
0024Eh				
0024Fh				
00250h				
00251h				
00252h	FST	Flash Memory Status Register	10000X00b	
00253h				
00254h	FMR0	Flash Memory Control Register 0	00h	
00255h	FMR1	Flash Memory Control Register 1	00h	
00256h	FMR2	Flash Memory Control Register 2	00h	
00257h				
00258h				
00259h				
0025Ah				
0025Bh				
0025Ch				
0025Dh				
0025Eh				
0025Fh				
00260h	AIADR0L	Address Match Interrupt Address 0L Register	XXXXh	
00261h				
00262h	AIADR0H	Address Match Interrupt Address 0H Register	0000XXXXb	
00263h	AIEN0	Address Match Interrupt Enable 0 Register	00h	
00264h	AIADR1L	Address Match Interrupt Address 1L Register	XXXXh	
00265h				
00266h	AIADR1H	Address Match Interrupt Address 1H Register	0000XXXXb	
00267h	AIEN1	Address Match Interrupt Enable 1 Register	00h	
00268h				
00269h				
0026Ah				
0026Bh				
0026Ch				
0026Dh				
0026Eh				
0026Fh				
00270h				
00271h				
00272h				
00273h				
00274h				
00275h				
00276h				
00277h				
00278h				
00279h				
0027Ah				
0027Bh				
0027Ch				
0027Dh				
0027Eh				
0027Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.11 SFR Information (11) (1)

Address	Symbol	Register Name	After Reset	Remarks
00280h	DTCTL	DTC Activation Control Register	00h	
00281h				
00282h				
00283h				
00284h				
00285h				
00286h				
00287h				
00288h	DTCEN0	DTC Activation Enable Register 0	00h	
00289h	DTCEN1	DTC Activation Enable Register 1	00h	
0028Ah	DTCEN2	DTC Activation Enable Register 2	00h	
0028Bh	DTCEN3	DTC Activation Enable Register 3	00h	
0028Ch	DTCEN4	DTC Activation Enable Register 4	00h	
0028Dh	DTCEN5	DTC Activation Enable Register 5	00h	
0028Eh	DTCEN6	DTC Activation Enable Register 6	00h	
0028Fh				
00290h	CRCSAR	SFR Snoop Address Register	0000h	
00291h				
00292h	CRCMR	CRC Control Register	00h	
00293h				
00294h	CRCD	CRC Data Register	0000h	
00295h				
00296h	CRCIN	CRC Input Register	00h	
00297h				
00298h				
00299h				
0029Ah				
0029Bh				
0029Ch				
0029Dh				
0029Eh				
0029Fh				
002A0h	TRJ_0SR	Timer RJ_0 Pin Select Register	00h	
002A1h	TRJ_1SR	Timer RJ_1 Pin Select Register	00h	
002A2h				
002A3h				
002A4h	TRBSR	Timer RB2 Pin Select Register	00h	
002A5h	TRCCLKSR	Timer RCCLK Pin Select Register	00h	
002A6h	TRC_0SR0	Timer RC_0 Pin Select Register 0	00h	
002A7h	TRC_0SR1	Timer RC_0 Pin Select Register 1	00h	
002A8h	TRC_1SR	Timer RC_1 Pin Select Register	00h	
002A9h	TRD_0SR0	Timer RD_0 Pin Select Register 0	00h	
002AAh	TRD_0SR1	Timer RD_0 Pin Select Register 1	00h	
002ABh				
002ACh				
002ADh	TIMSR	Timer Pin Select Register	00h	
002AEh	U_0SR	UART0_0 Pin Select Register	00h	
002AFh	U_1SR	UART0_1 Pin Select Register	00h	
002B0h				
002B1h				
002B2h	U2SR0	UART2 Pin Select Register 0	00h	
002B3h	U2SR1	UART2 Pin Select Register 1	00h	
002B4h	SSUIIC_0SR	SSU/IIC_0 Pin Select Register	00h	
002B5h				
002B6h	INTSR0	INT Interrupt Input Pin Select Register 0	00h	
002B7h				
002B8h				
002B9h	PINSR	I/O Function Pin Select Register	00h	
002BAh				
002BBh				
002BCh				
002BDh				
002BEh	PMCSEL	Pin Assignment Select Register	00h	
002BFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.12 SFR Information (12) (1)

Address	Symbol	Register Name	After Reset	Remarks
002C0h	PUR0	Pull-Up Control Register 0	00h	
002C1h	PUR1	Pull-Up Control Register 1	00h	
002C2h	PUR2	Pull-Up Control Register 2	00h	
002C3h	PUR3	Pull-Up Control Register 3	00h	
002C4h				
002C5h				
002C6h				
002C7h				
002C8h	P1DRR	Port P1 Drive Capacity Control Register	00h	
002C9h	P2DRR	Port P2 Drive Capacity Control Register	00h	
002CAh				
002CBh	PCDRR	Port PC Drive Capacity Control Register	00h	
002CCh	DRR0	Drive Capacity Control Register 0	00h	
002CDh	DRR1	Drive Capacity Control Register 1	00h	
002CEh	DRR2	Drive Capacity Control Register 2	00h	
002CFh				
002D0h	VLT0	Input Threshold Control Register 0	00h	
002D1h	VLT1	Input Threshold Control Register 1	00h	
002D2h	VLT2	Input Threshold Control Register 2	00h	
002D3h	VLT3	Input Threshold Control Register 3	00h	
002D4h				
002D5h				
002D6h				
002D7h				
002D8h				
002D9h				
002DAh				
002DBh				
002DCh				
002DDh				
002DEh				
002DFh				
002E0h	PORT0	Port P0 Register	XXh	
002E1h	PORT1	Port P1 Register	XXh	
002E2h	PD0	Port P0 Direction Register	00h	
002E3h	PD1	Port P1 Direction Register	00h	
002E4h	PORT2	Port P2 Register	XXh	
002E5h	PORT3	Port P3 Register	XXh	
002E6h	PD2	Port P2 Direction Register	00h	
002E7h	PD3	Port P3 Direction Register	00h	
002E8h	PORT4	Port P4 Register	XXh	
002E9h	PORT5	Port P5 Register	XXh	
002EAh	PD4	Port P4 Direction Register	00h	
002EBh	PD5	Port P5 Direction Register	00h	
002ECh	PORT6	Port P6 Register	XXh	
002EDh				
002EEh	PD6	Port P6 Direction Register	00h	
002EFh				
002F0h	PORT8	Port P8 Register	XXh	
002F1h	PORT9	Port P9 Register	XXh	
002F2h	PD8	Port P8 Direction Register	00h	
002F3h	PD9	Port P9 Direction Register	00h	
002F4h				
002F5h				
002F6h				
002F7h				
002F8h	PORTC	Port PC Register	XXh	
002F9h				
002FAh	PDC	Port PC Direction Register	00h	
002FBh				
002FCh				
002FDh				
002FEh				
002FFh				
00300h to 003FFh	On-chip RAM for firmware	On-chip RAM for firmware		

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.13 SFR Information (13) (1)

Address	Symbol	Register Name	After Reset	Remarks
00400h to 02BFFh	On-chip RAM	On-chip RAM		
02C00h to 069FFh				
06A00h	ELSELR0	Event Output Destination Select Register 0	00h	
06A01h	ELSELR1	Event Output Destination Select Register 1	00h	
06A02h	ELSELR2	Event Output Destination Select Register 2	00h	
06A03h	ELSELR3	Event Output Destination Select Register 3	00h	
06A04h	ELSELR4	Event Output Destination Select Register 4	00h	
06A05h				
06A06h				
06A07h				
06A08h	ELSELR8	Event Output Destination Select Register 8	00h	
06A09h	ELSELR9	Event Output Destination Select Register 9	00h	
06A0Ah	ELSELR10	Event Output Destination Select Register 10	00h	
06A0Bh	ELSELR11	Event Output Destination Select Register 11	00h	
06A0Ch	ELSELR12	Event Output Destination Select Register 12	00h	
06A0Dh	ELSELR13	Event Output Destination Select Register 13	00h	
06A0Eh	ELSELR14	Event Output Destination Select Register 14	00h	
06A0Fh	ELSELR15	Event Output Destination Select Register 15	00h	
06A10h	ELSELR16	Event Output Destination Select Register 16	00h	
06A11h	ELSELR17	Event Output Destination Select Register 17	00h	
06A12h	ELSELR18	Event Output Destination Select Register 18	00h	
06A13h	ELSELR19	Event Output Destination Select Register 19	00h	
06A14h	ELSELR20	Event Output Destination Select Register 20	00h	
06A15h	ELSELR21	Event Output Destination Select Register 21	00h	
06A16h	ELSELR22	Event Output Destination Select Register 22	00h	
06A17h	ELSELR23	Event Output Destination Select Register 23	00h	
06A18h	ELSELR24	Event Output Destination Select Register 24	00h	
06A19h	ELSELR25	Event Output Destination Select Register 25	00h	
06A1Ah	ELSELR26	Event Output Destination Select Register 26	00h	
06A1Bh	ELSELR27	Event Output Destination Select Register 27	00h	
06A1Ch	ELSELR28	Event Output Destination Select Register 28	00h	
06A1Dh				
06A1Eh				
06A1Fh				
06A20h				
06A21h				
06A22h				
06A23h				
06A24h				
06A25h				
06A26h				
06A27h				
06A28h				
06A29h				
06A2Ah				
06A2Bh				
06A2Ch				
06A2Dh	ELSELR45	Event Output Destination Select Register 45	00h	
06A2Eh	ELSELR46	Event Output Destination Select Register 46	00h	
06A2Fh	ELSELR47	Event Output Destination Select Register 47	00h	
06A30h	ELSELR48	Event Output Destination Select Register 48	00h	
06A31h to 06BFFh				
06C00h		Area for storing DTC transfer vector 0	XXh	
06C01h		Area for storing DTC transfer vector 1	XXh	
06C02h		Area for storing DTC transfer vector 2	XXh	
06C03h		Area for storing DTC transfer vector 3	XXh	
06C04h		Area for storing DTC transfer vector 4	XXh	
06C05h				
06C06h				
06C07h				
06C08h		Area for storing DTC transfer vector 8	XXh	
06C09h		Area for storing DTC transfer vector 9	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.14 SFR Information (14) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C0Ah		Area for storing DTC transfer vector 10	XXh	
06C0Bh		Area for storing DTC transfer vector 11	XXh	
06C0Ch		Area for storing DTC transfer vector 12	XXh	
06C0Dh		Area for storing DTC transfer vector 13	XXh	
06C0Eh		Area for storing DTC transfer vector 14	XXh	
06C0Fh		Area for storing DTC transfer vector 15	XXh	
06C10h		Area for storing DTC transfer vector 16	XXh	
06C11h		Area for storing DTC transfer vector 17	XXh	
06C12h		Area for storing DTC transfer vector 18	XXh	
06C13h		Area for storing DTC transfer vector 19	XXh	
06C14h		Area for storing DTC transfer vector 20	XXh	
06C15h		Area for storing DTC transfer vector 21	XXh	
06C16h		Area for storing DTC transfer vector 22	XXh	
06C17h		Area for storing DTC transfer vector 23	XXh	
06C18h		Area for storing DTC transfer vector 24	XXh	
06C19h		Area for storing DTC transfer vector 25	XXh	
06C1Ah		Area for storing DTC transfer vector 26	XXh	
06C1Bh		Area for storing DTC transfer vector 27	XXh	
06C1Ch		Area for storing DTC transfer vector 28	XXh	
06C1Dh		Area for storing DTC transfer vector 29	XXh	
06C1Eh		Area for storing DTC transfer vector 30	XXh	
06C1Fh		Area for storing DTC transfer vector 31	XXh	
06C20h		Area for storing DTC transfer vector 32	XXh	
06C21h		Area for storing DTC transfer vector 33	XXh	
06C22h				
06C23h				
06C24h				
06C25h				
06C26h		Area for storing DTC transfer vector 38	XXh	
06C27h		Area for storing DTC transfer vector 39	XXh	
06C28h				
06C29h				
06C2Ah		Area for storing DTC transfer vector 42	XXh	
06C2Bh		Area for storing DTC transfer vector 43	XXh	
06C2Ch		Area for storing DTC transfer vector 44	XXh	
06C2Dh		Area for storing DTC transfer vector 45	XXh	
06C2Eh		Area for storing DTC transfer vector 46	XXh	
06C2Fh		Area for storing DTC transfer vector 47	XXh	
06C30h		Area for storing DTC transfer vector 48	XXh	
06C31h		Area for storing DTC transfer vector 49	XXh	
06C32h		Area for storing DTC transfer vector 50	XXh	
06C33h		Area for storing DTC transfer vector 51	XXh	
06C34h		Area for storing DTC transfer vector 52	XXh	
06C35h				
06C36h				
06C37h				
06C38h				
06C39h				
06C3Ah				
06C3Bh				
06C3Ch				
06C3Dh				
06C3Eh				
06C3Fh				
06C40h	DTCCR0	DTC Control Register 0	XXh	
06C41h	DTBLS0	DTC Block Size Register 0	XXh	
06C42h	DTCCT0	DTC Transfer Count Register 0	XXh	
06C43h	DTRLD0	DTC Transfer Count Reload Register 0	XXh	
06C44h	DTSAR0	DTC Source Address Register 0	XXXXh	
06C45h				
06C46h	DTDAR0	DTC Destination Address Register 0	XXXXh	
06C47h				
06C48h	DTCCR1	DTC Control Register 1	XXh	
06C49h	DTBLS1	DTC Block Size Register 1	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.15 SFR Information (15) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C4Ah	DTCCT1	DTC Transfer Count Register 1	XXh	
06C4Bh	DTRLD1	DTC Transfer Count Reload Register 1	XXh	
06C4Ch	DTSAR1	DTC Source Address Register 1	XXXXh	
06C4Dh				
06C4Eh	DTDAR1	DTC Destination Address Register 1	XXXXh	
06C4Fh				
06C50h	DTCCR2	DTC Control Register 2	XXh	
06C51h	DTBLS2	DTC Block Size Register 2	XXh	
06C52h	DTCCT2	DTC Transfer Count Register 2	XXh	
06C53h	DTRLD2	DTC Transfer Count Reload Register 2	XXh	
06C54h	DTSAR2	DTC Source Address Register 2	XXXXh	
06C55h				
06C56h	DTDAR2	DTC Destination Address Register 2	XXXXh	
06C57h				
06C58h	DTCCR3	DTC Control Register 3	XXh	
06C59h	DTBLS3	DTC Block Size Register 3	XXh	
06C5Ah	DTCCT3	DTC Transfer Count Register 3	XXh	
06C5Bh	DTRLD3	DTC Transfer Count Reload Register 3	XXh	
06C5Ch	DTSAR3	DTC Source Address Register 3	XXXXh	
06C5Dh				
06C5Eh	DTDAR3	DTC Destination Address Register 3	XXXXh	
06C5Fh				
06C60h	DTCCR4	DTC Control Register 4	XXh	
06C61h	DTBLS4	DTC Block Size Register 4	XXh	
06C62h	DTCCT4	DTC Transfer Count Register 4	XXh	
06C63h	DTRLD4	DTC Transfer Count Reload Register 4	XXh	
06C64h	DTSAR4	DTC Source Address Register 4	XXXXh	
06C65h				
06C66h	DTDAR4	DTC Destination Address Register 4	XXXXh	
06C67h				
06C68h	DTCCR5	DTC Control Register 5	XXh	
06C69h	DTBLS5	DTC Block Size Register 5	XXh	
06C6Ah	DTCCT5	DTC Transfer Count Register 5	XXh	
06C6Bh	DTRLD5	DTC Transfer Count Reload Register 5	XXh	
06C6Ch	DTSAR5	DTC Source Address Register 5	XXXXh	
06C6Dh				
06C6Eh	DTDAR5	DTC Destination Address Register 5	XXXXh	
06C6Fh				
06C70h	DTCCR6	DTC Control Register 6	XXh	
06C71h	DTBLS6	DTC Block Size Register 6	XXh	
06C72h	DTCCT6	DTC Transfer Count Register 6	XXh	
06C73h	DTRLD6	DTC Transfer Count Reload Register 6	XXh	
06C74h	DTSAR6	DTC Source Address Register 6	XXXXh	
06C75h				
06C76h	DTDAR6	DTC Destination Address Register 6	XXXXh	
06C77h				
06C78h	DTCCR7	DTC Control Register 7	XXh	
06C79h	DTBLS7	DTC Block Size Register 7	XXh	
06C7Ah	DTCCT7	DTC Transfer Count Register 7	XXh	
06C7Bh	DTRLD7	DTC Transfer Count Reload Register 7	XXh	
06C7Ch	DTSAR7	DTC Source Address Register 7	XXXXh	
06C7Dh				
06C7Eh	DTDAR7	DTC Destination Address Register 7	XXXXh	
06C7Fh				
06C80h	DTCCR8	DTC Control Register 8	XXh	
06C81h	DTBLS8	DTC Block Size Register 8	XXh	
06C82h	DTCCT8	DTC Transfer Count Register 8	XXh	
06C83h	DTRLD8	DTC Transfer Count Reload Register 8	XXh	
06C84h	DTSAR8	DTC Source Address Register 8	XXXXh	
06C85h				
06C86h	DTDAR8	DTC Destination Address Register 8	XXXXh	
06C87h				
06C88h	DTCCR9	DTC Control Register 9	XXh	
06C89h	DTBLS9	DTC Block Size Register 9	XXh	
06C8Ah	DTCCT9	DTC Transfer Count Register 9	XXh	
06C8Bh	DTRLD9	DTC Transfer Count Reload Register 9	XXh	
06C8Ch	DTSAR9	DTC Source Address Register 9	XXXXh	
06C8Dh				
06C8Eh	DTDAR9	DTC Destination Address Register 9	XXXXh	
06C8Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.16 SFR Information (16) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C90h	DTCCR10	DTC Control Register 10	XXh	
06C91h	DTBLS10	DTC Block Size Register 10	XXh	
06C92h	DTCCT10	DTC Transfer Count Register 10	XXh	
06C93h	DTRLD10	DTC Transfer Count Reload Register 10	XXh	
06C94h	DTSAR10	DTC Source Address Register 10	XXXXh	
06C95h				
06C96h	DTDAR10	DTC Destination Address Register 10	XXXXh	
06C97h				
06C98h	DTCCR11	DTC Control Register 11	XXh	
06C99h	DTBLS11	DTC Block Size Register 11	XXh	
06C9Ah	DTCCT11	DTC Transfer Count Register 11	XXh	
06C9Bh	DTRLD11	DTC Transfer Count Reload Register 11	XXh	
06C9Ch	DTSAR11	DTC Source Address Register 11	XXXXh	
06C9Dh				
06C9Eh	DTDAR11	DTC Destination Address Register 11	XXXXh	
06C9Fh				
06CA0h	DTCCR12	DTC Control Register 12	XXh	
06CA1h	DTBLS12	DTC Block Size Register 12	XXh	
06CA2h	DTCCT12	DTC Transfer Count Register 12	XXh	
06CA3h	DTRLD12	DTC Transfer Count Reload Register 12	XXh	
06CA4h	DTSAR12	DTC Source Address Register 12	XXXXh	
06CA5h				
06CA6h	DTDAR12	DTC Destination Address Register 12	XXXXh	
06CA7h				
06CA8h	DTCCR13	DTC Control Register 13	XXh	
06CA9h	DTBLS13	DTC Block Size Register 13	XXh	
06CAAh	DTCCT13	DTC Transfer Count Register 13	XXh	
06CABh	DTRLD13	DTC Transfer Count Reload Register 13	XXh	
06CACh	DTSAR13	DTC Source Address Register 13	XXXXh	
06CADh				
06CAEh	DTDAR13	DTC Destination Address Register 13	XXXXh	
06CAFh				
06CB0h	DTCCR14	DTC Control Register 14	XXh	
06CB1h	DTBLS14	DTC Block Size Register 14	XXh	
06CB2h	DTCCT14	DTC Transfer Count Register 14	XXh	
06CB3h	DTRLD14	DTC Transfer Count Reload Register 14	XXh	
06CB4h	DTSAR14	DTC Source Address Register 14	XXXXh	
06CB5h				
06CB6h	DTDAR14	DTC Destination Address Register 14	XXXXh	
06CB7h				
06CB8h	DTCCR15	DTC Control Register 15	XXh	
06CB9h	DTBLS15	DTC Block Size Register 15	XXh	
06CBAh	DTCCT15	DTC Transfer Count Register 15	XXh	
06CBBh	DTRLD15	DTC Transfer Count Reload Register 15	XXh	
06CBCh	DTSAR15	DTC Source Address Register 15	XXXXh	
06CBDh				
06CBEh	DTDAR15	DTC Destination Address Register 15	XXXXh	
06CBFh				
06CC0h	DTCCR16	DTC Control Register 16	XXh	
06CC1h	DTBLS16	DTC Block Size Register 16	XXh	
06CC2h	DTCCT16	DTC Transfer Count Register 16	XXh	
06CC3h	DTRLD16	DTC Transfer Count Reload Register 16	XXh	
06CC4h	DTSAR16	DTC Source Address Register 16	XXXXh	
06CC5h				
06CC6h	DTDAR16	DTC Destination Address Register 16	XXXXh	
06CC7h				
06CC8h	DTCCR17	DTC Control Register 17	XXh	
06CC9h	DTBLS17	DTC Block Size Register 17	XXh	
06CCAh	DTCCT17	DTC Transfer Count Register 17	XXh	
06CCBh	DTRLD17	DTC Transfer Count Reload Register 17	XXh	
06CCCh	DTSAR17	DTC Source Address Register 17	XXXXh	
06CCDh				
06CCEh	DTDAR17	DTC Destination Address Register 17	XXXXh	
06CCFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.17 SFR Information (17) (1)

Address	Symbol	Register Name	After Reset	Remarks
06CD0h	DTCCR18	DTC Control Register 18	XXh	
06CD1h	DTBLS18	DTC Block Size Register 18	XXh	
06CD2h	DTCCT18	DTC Transfer Count Register 18	XXh	
06CD3h	DTRLD18	DTC Transfer Count Reload Register 18	XXh	
06CD4h	DTSAR18	DTC Source Address Register 18	XXXXh	
06CD5h				
06CD6h	DTDAR18	DTC Destination Address Register 18	XXXXh	
06CD7h				
06CD8h	DTCCR19	DTC Control Register 19	XXh	
06CD9h	DTBLS19	DTC Block Size Register 19	XXh	
06CDAh	DTCCT19	DTC Transfer Count Register 19	XXh	
06CDBh	DTRLD19	DTC Transfer Count Reload Register 19	XXh	
06CDCh	DTSAR19	DTC Source Address Register 19	XXXXh	
06CDDh				
06CDEh	DTDAR19	DTC Destination Address Register 19	XXXXh	
06CDFh				
06CE0h	DTCCR20	DTC Control Register 20	XXh	
06CE1h	DTBLS20	DTC Block Size Register 20	XXh	
06CE2h	DTCCT20	DTC Transfer Count Register 20	XXh	
06CE3h	DTRLD20	DTC Transfer Count Reload Register 20	XXh	
06CE4h	DTSAR20	DTC Source Address Register 20	XXXXh	
06CE5h				
06CE6h	DTDAR20	DTC Destination Address Register 20	XXXXh	
06CE7h				
06CE8h	DTCCR21	DTC Control Register 21	XXh	
06CE9h	DTBLS21	DTC Block Size Register 21	XXh	
06CEAh	DTCCT21	DTC Transfer Count Register 21	XXh	
06CEBh	DTRLD21	DTC Transfer Count Reload Register 21	XXh	
06CECh	DTSAR21	DTC Source Address Register 21	XXXXh	
06CEDh				
06CEEh	DTDAR21	DTC Destination Address Register 21	XXXXh	
06CEFh				
06CF0h	DTCCR22	DTC Control Register 22	XXh	
06CF1h	DTBLS22	DTC Block Size Register 22	XXh	
06CF2h	DTCCT22	DTC Transfer Count Register 22	XXh	
06CF3h	DTRLD22	DTC Transfer Count Reload Register 22	XXh	
06CF4h	DTSAR22	DTC Source Address Register 22	XXXXh	
06CF5h				
06CF6h	DTDAR22	DTC Destination Address Register 22	XXXXh	
06CF7h				
06CF8h	DTCCR23	DTC Control Register 23	XXh	
06CF9h	DTBLS23	DTC Block Size Register 23	XXh	
06CFAh	DTCCT23	DTC Transfer Count Register 23	XXh	
06CFBh	DTRLD23	DTC Transfer Count Reload Register 23	XXh	
06CFCh	DTSAR23	DTC Source Address Register 23	XXXXh	
06CFDh				
06CFEh	DTDAR23	DTC Destination Address Register 23	XXXXh	
06CFFh				
06D00h to 06DFFh				
06E00h	CMB0_0	CAN_0 Mailbox 0	XXh	
06E01h			XXh	
06E02h			XXh	
06E03h			XXh	
06E04h			XXh	
06E05h			XXh	
06E06h			XXh	
06E07h			XXh	
06E08h			XXh	
06E09h			XXh	
06E0Ah			XXh	
06E0Bh			XXh	
06E0Ch			XXh	
06E0Dh			XXh	
06E0Eh			XXh	
06E0Fh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.18 SFR Information (18) (1)

Address	Symbol	Register Name	After Reset	Remarks
06E10h	CMB1_0	CAN_0 Mailbox 1	XXh	
06E11h			XXh	
06E12h			XXh	
06E13h			XXh	
06E14h			XXh	
06E15h			XXh	
06E16h			XXh	
06E17h			XXh	
06E18h			XXh	
06E19h			XXh	
06E1Ah			XXh	
06E1Bh			XXh	
06E1Ch			XXh	
06E1Dh			XXh	
06E1Eh			XXh	
06E1Fh			XXh	
06E20h	CMB2_0	CAN_0 Mailbox 2	XXh	
06E21h			XXh	
06E22h			XXh	
06E23h			XXh	
06E24h			XXh	
06E25h			XXh	
06E26h			XXh	
06E27h			XXh	
06E28h			XXh	
06E29h			XXh	
06E2Ah			XXh	
06E2Bh			XXh	
06E2Ch			XXh	
06E2Dh			XXh	
06E2Eh			XXh	
06E2Fh			XXh	
06E30h	CMB3_0	CAN_0 Mailbox 3	XXh	
06E31h			XXh	
06E32h			XXh	
06E33h			XXh	
06E34h			XXh	
06E35h			XXh	
06E36h			XXh	
06E37h			XXh	
06E38h			XXh	
06E39h			XXh	
06E3Ah			XXh	
06E3Bh			XXh	
06E3Ch			XXh	
06E3Dh			XXh	
06E3Eh			XXh	
06E3Fh			XXh	
06E40h	CMB4_0	CAN_0 Mailbox 4	XXh	
06E41h			XXh	
06E42h			XXh	
06E43h			XXh	
06E44h			XXh	
06E45h			XXh	
06E46h			XXh	
06E47h			XXh	
06E48h			XXh	
06E49h			XXh	
06E4Ah			XXh	
06E4Bh			XXh	
06E4Ch			XXh	
06E4Dh			XXh	
06E4Eh			XXh	
06E4Fh			XXh	

X: Undefined
Note:
1. The blank areas are reserved. No access is allowed.

Table 3.19 SFR Information (19) (1)

Address	Symbol	Register Name	After Reset	Remarks
06E50h	CMB5_0	CAN_0 Mailbox 5	XXh	
06E51h			XXh	
06E52h			XXh	
06E53h			XXh	
06E54h			XXh	
06E55h			XXh	
06E56h			XXh	
06E57h			XXh	
06E58h			XXh	
06E59h			XXh	
06E5Ah			XXh	
06E5Bh			XXh	
06E5Ch			XXh	
06E5Dh			XXh	
06E5Eh			XXh	
06E5Fh			XXh	
06E60h	CMB6_0	CAN_0 Mailbox 6	XXh	
06E61h			XXh	
06E62h			XXh	
06E63h			XXh	
06E64h			XXh	
06E65h			XXh	
06E66h			XXh	
06E67h			XXh	
06E68h			XXh	
06E69h			XXh	
06E6Ah			XXh	
06E6Bh			XXh	
06E6Ch			XXh	
06E6Dh			XXh	
06E6Eh			XXh	
06E6Fh			XXh	
06E70h	CMB7_0	CAN_0 Mailbox 7	XXh	
06E71h			XXh	
06E72h			XXh	
06E73h			XXh	
06E74h			XXh	
06E75h			XXh	
06E76h			XXh	
06E77h			XXh	
06E78h			XXh	
06E79h			XXh	
06E7Ah			XXh	
06E7Bh			XXh	
06E7Ch			XXh	
06E7Dh			XXh	
06E7Eh			XXh	
06E7Fh			XXh	
06E80h	CMB8_0	CAN_0 Mailbox 8	XXh	
06E81h			XXh	
06E82h			XXh	
06E83h			XXh	
06E84h			XXh	
06E85h			XXh	
06E86h			XXh	
06E87h			XXh	
06E88h			XXh	
06E89h			XXh	
06E8Ah			XXh	
06E8Bh			XXh	
06E8Ch			XXh	
06E8Dh			XXh	
06E8Eh			XXh	
06E8Fh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.20 SFR Information (20) (1)

Address	Symbol	Register Name	After Reset	Remarks
06E90h	CMB9_0	CAN_0 Mailbox 9	XXh	
06E91h			XXh	
06E92h			XXh	
06E93h			XXh	
06E94h			XXh	
06E95h			XXh	
06E96h			XXh	
06E97h			XXh	
06E98h			XXh	
06E99h			XXh	
06E9Ah			XXh	
06E9Bh			XXh	
06E9Ch			XXh	
06E9Dh			XXh	
06E9Eh			XXh	
06E9Fh			XXh	
06EA0h	CMB10_0	CAN_0 Mailbox 10	XXh	
06EA1h			XXh	
06EA2h			XXh	
06EA3h			XXh	
06EA4h			XXh	
06EA5h			XXh	
06EA6h			XXh	
06EA7h			XXh	
06EA8h			XXh	
06EA9h			XXh	
06EAAh			XXh	
06EABh			XXh	
06EACh			XXh	
06EADh			XXh	
06EAEh			XXh	
06EAFh			XXh	
06EB0h	CMB11_0	CAN_0 Mailbox 11	XXh	
06EB1h			XXh	
06EB2h			XXh	
06EB3h			XXh	
06EB4h			XXh	
06EB5h			XXh	
06EB6h			XXh	
06EB7h			XXh	
06EB8h			XXh	
06EB9h			XXh	
06EBAh			XXh	
06EBBh			XXh	
06EBCh			XXh	
06EBDh			XXh	
06EBEh			XXh	
06EBFh			XXh	
06EC0h	CMB12_0	CAN_0 Mailbox 12	XXh	
06EC1h			XXh	
06EC2h			XXh	
06EC3h			XXh	
06EC4h			XXh	
06EC5h			XXh	
06EC6h			XXh	
06EC7h			XXh	
06EC8h			XXh	
06EC9h			XXh	
06ECAh			XXh	
06ECBh			XXh	
06ECCh			XXh	
06ECDh			XXh	
06ECEh			XXh	
06ECFh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.21 SFR Information (21) (1)

Address	Symbol	Register Name	After Reset	Remarks
06ED0h	CMB13_0	CAN_0 Mailbox 13	XXh	
06ED1h			XXh	
06ED2h			XXh	
06ED3h			XXh	
06ED4h			XXh	
06ED5h			XXh	
06ED6h			XXh	
06ED7h			XXh	
06ED8h			XXh	
06ED9h			XXh	
06EDAh			XXh	
06EDBh			XXh	
06EDCh			XXh	
06EDDh			XXh	
06EDEh			XXh	
06EDFh			XXh	
06EE0h	CMB14_0	CAN_0 Mailbox 14	XXh	
06EE1h			XXh	
06EE2h			XXh	
06EE3h			XXh	
06EE4h			XXh	
06EE5h			XXh	
06EE6h			XXh	
06EE7h			XXh	
06EE8h			XXh	
06EE9h			XXh	
06EEAh			XXh	
06EEBh			XXh	
06EECh			XXh	
06EEDh			XXh	
06EEEh			XXh	
06EEFh			XXh	
06EF0h	CMB15_0	CAN_0 Mailbox 15	XXh	
06EF1h			XXh	
06EF2h			XXh	
06EF3h			XXh	
06EF4h			XXh	
06EF5h			XXh	
06EF6h			XXh	
06EF7h			XXh	
06EF8h			XXh	
06EF9h			XXh	
06EFAh			XXh	
06EFBh			XXh	
06EFCh			XXh	
06EFDh			XXh	
06EFEh			XXh	
06EFFh			XXh	
06F00h				
06F01h				
06F02h				
06F03h				
06F04h				
06F05h				
06F06h				
06F07h				
06F08h				
06F09h				
06F0Ah				
06F0Bh				
06F0Ch				
06F0Dh				
06F0Eh				
06F0Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.22 SFR Information (22) (1)

Address	Symbol	Register Name	After Reset	Remarks
06F10h	CMKR0_0	CAN_0 Mask Register 0	XXh	
06F11h			XXh	
06F12h			XXh	
06F13h			XXh	
06F14h	CMKR1_0	CAN_0 Mask Register 1	XXh	
06F15h			XXh	
06F16h			XXh	
06F17h			XXh	
06F18h	CMKR2_0	CAN_0 Mask Register 2	XXh	
06F19h			XXh	
06F1Ah			XXh	
06F1Bh			XXh	
06F1Ch	CMKR3_0	CAN_0 Mask Register 3	XXh	
06F1Dh			XXh	
06F1Eh			XXh	
06F1Fh			XXh	
06F20h	CFIDCR0_0	CAN_0 FIFO Received ID Compare Register 0	XXh	
06F21h			XXh	
06F22h			XXh	
06F23h			XXh	
06F24h	CFIDCR1_0	CAN_0 FIFO Received ID Compare Register 1	XXh	
06F25h			XXh	
06F26h			XXh	
06F27h			XXh	
06F28h				
06F29h				
06F2Ah	CMKIVLR_0	CAN_0 Mask Invalid Register	XXh	
06F2Bh			XXh	
06F2Ch				
06F2Dh				
06F2Eh	CMIER_0	CAN_0 Mailbox Interrupt Enable Register	XXh	
06F2Fh			XXh	
06F30h	CMCTL0_0	CAN_0 Message Control Register 0	00h	
06F31h	CMCTL1_0	CAN_0 Message Control Register 1	00h	
06F32h	CMCTL2_0	CAN_0 Message Control Register 2	00h	
06F33h	CMCTL3_0	CAN_0 Message Control Register 3	00h	
06F34h	CMCTL4_0	CAN_0 Message Control Register 4	00h	
06F35h	CMCTL5_0	CAN_0 Message Control Register 5	00h	
06F36h	CMCTL6_0	CAN_0 Message Control Register 6	00h	
06F37h	CMCTL7_0	CAN_0 Message Control Register 7	00h	
06F38h	CMCTL8_0	CAN_0 Message Control Register 8	00h	
06F39h	CMCTL9_0	CAN_0 Message Control Register 9	00h	
06F3Ah	CMCTL10_0	CAN_0 Message Control Register 10	00h	
06F3Bh	CMCTL11_0	CAN_0 Message Control Register 11	00h	
06F3Ch	CMCTL12_0	CAN_0 Message Control Register 12	00h	
06F3Dh	CMCTL13_0	CAN_0 Message Control Register 13	00h	
06F3Eh	CMCTL14_0	CAN_0 Message Control Register 14	00h	
06F3Fh	CMCTL15_0	CAN_0 Message Control Register 15	00h	
06F40h	CCTLR_0	CAN_0 Control Register	00000101b	
06F41h			00h	
06F42h	CSTR_0	CAN_0 Status Register	00000101b	
06F43h			00h	
06F44h	CBCR_0	CAN_0 Bit Configuration Register	00h	
06F45h			00h	
06F46h			00h	
06F47h	CCLKR_0	CAN_0 Clock Select Register	00h	
06F48h	CRFCR_0	CAN_0 Receive FIFO Control Register	10000000b	
06F49h	CRFPCR_0	CAN_0 Receive FIFO Pointer Control Register	XXh	
06F4Ah	CTFCR_0	CAN_0 Transmit FIFO Control Register	10000000b	
06F4Bh	CTFPCR_0	CAN_0 Transmit FIFO Pointer Control Register	XXh	
06F4Ch	CEIER_0	CAN_0 Error Interrupt Enable Register	00h	
06F4Dh	CEIFR_0	CAN_0 Error Interrupt Factor Judge Register	00h	
06F4Eh	CRECR_0	CAN_0 Receive Error Count Register	00h	
06F4Fh	CTECR_0	CAN_0 Transmit Error Count Register	00h	

X: Undefined
Note:
1. The blank areas are reserved. No access is allowed.

Table 3.23 SFR Information (23) (1)

Address	Symbol	Register Name	After Reset	Remarks
06F50h	CECSR_0	CAN_0 Error Code Store Register	00h	
06F51h	CCSSR_0	CAN_0 Channel Search Support Register	XXh	
06F52h	CMSSR_0	CAN_0 Mailbox Search Status Register	10000000b	
06F53h	CMSMR_0	CAN_0 Mailbox Search Mode Register	00h	
06F54h	CTSR_0	CAN_0 Time Stamp Register	0000h	
06F55h				
06F56h	CAFSR_0	CAN_0 Acceptance Filter Support Register	XXh	
06F57h			XXh	
06F58h	CTCR_0	CAN_0 Test Control Register	00h	
06F59h				
06F5Ah				
06F5Bh				
06F5Ch				
06F5Dh				
06F5Eh				
06F5Fh				
06F60h				
06F61h				
06F62h				
06F63h				
06F64h				
06F65h				
06F66h				
06F67h				
06F68h				
06F69h				
06F6Ah				
06F6Bh				
06F6Ch				
06F6Dh				
06F6Eh				
06F6Fh				
06F70h				
06F71h				
06F72h				
06F73h				
06F74h				
06F75h				
06F76h				
06F77h				
06F78h				
06F79h				
06F7Ah				
06F7Bh				
06F7Ch				
06F7Dh				
06F7Eh	CANISR_0	CAN_0 Interrupt Status Register	00h	
06F7Fh	CANIE_0	CAN_0 Interrupt Control Register	00h	
06F80h to 06FFFh				

X: Undefined
Note:
1. The blank areas are reserved. No access is allowed.

Table 3.24 ID code Area, Option Function Select Area

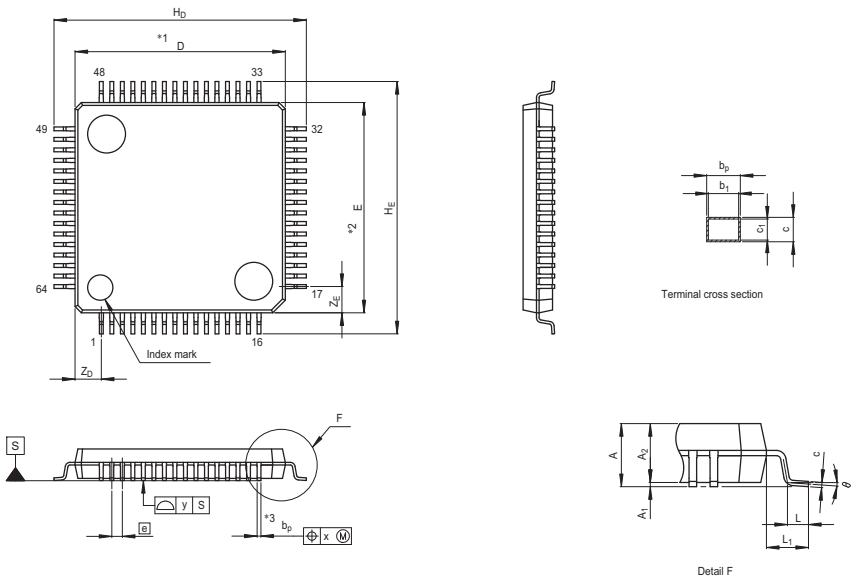
Address	Symbol	Area Name	After Reset	Address size
:				
0FFDBh	OFS2	Option Function Select Register 2		
:				
0FFFFh	OFS	Option Function Select Register		

Note:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not perform any additional writes to the option function select area. Erasure of the block including the option function select area will cause the option function select area to be set to FFh.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	R8C/56E Group, R8C/56F Group, R8C/56G Group, R8C/56H Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Dec 17, 2010	—	First Edition issued
0.10	Mar 15, 2011	1 to 27	1. Overview R8C/56F Group, R8C/56G Group, and R8C/56H Group added
		32 to 34	3.2, 3.3, and 3.4 added
		46	Table 3.12 Port register symbol revised

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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