RAiO

RA8870

Character/Graphic

TFT LCD Controller

Specification

Version 1.1

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1. Description

RA8870 is a TFT LCD controller which supports the character and graphic mixed display. It is designed to meet the requirement of middle size TFT module up to 640x480 pixels with characters or 2D graphic application. With internal RAM, RA8870 can supports 65K color for 320x240 dots TFT Panel, 4K color for 640x240/320x480 display , or 4K color for 320x240 dots with 2-Layers. With external RAM, it supports up to 65K color for 640x480 panel.

The embedded CGROM is capable to display the alphaset of international standard ISO 8859-1/2/3/4. It includes 256x4 characters and can satisfiies almost English or Eurpean language family countries. For graphic usage, RA8870 supports a 2D Block Transfer Engine(BTE) that is compatible with 2D BitBLT function for processing the mass data transfer function. The geometric speed-up engine provides user an easy way to draw the programmable geometric shape by hardware, like line, square and circle. Besides, many powerful functions are combined with RA8870, such as screen rotation function, scroll function, graphic pattern, 2-layer mixed display and font enlargement function. These functions will save user a large of software effort during developement period.

RA8870 is a powerful and cheap choice for color application. To reduce the system cost, RA8870 proivde low cost 8080/6800 MCU I/F, a flexible 4/5-wires Touch Panel controller, PWM for adjusting panel back-light and some GPIOs. With the RA8870 design-in, user can achieve an easy-to-use, low-cost and high performace system compared with the other solution.

2. Feature

- Support Text/Graphic Mixed Display Mode.
- Clock Source: External X'tal Clock Input with Internal PLL.
- Color Depth TFT: 256/4K/65K Colors.
- Supporting MCU Interface: 8080/6800 with 8/16 Data Bus Width.
- Internal DDRAM Size: 230KB
- Embedded 10KB Character ROM with Font Size 8x16 Dots and Supporting Character Set of ISO8859-1/2/3/4.
- Support GB-2312 and BIG-5 Encoding with External Font ROM of Font Size 16x16 Dots.
- External DDRAM up to 512Kbyte*16.
- Font Enlargement X1, X2, X3, X4 for Horizontal or Vertical Direction.
- Support TFT 8/12/16-Bits Generic RGB Interface and Analog TFT Panel Interface.
- Flexible TCON Block Compatible with Most Analog Panel.
- Screen Display Rotation 90°, 180° and 270° for Different Panel Type.
- Support Font Vertical Rotation.
- Support Block Scroll for Vertical or Horizontal Direction.
- Embedded Block Transfer Engine (BTE) with 2D Function.
- Embedded Geometric Speed-up Engine.
- Text Cursor for Character Writing.
- 32X32 Pixel Graphic Cursor Function.
- Supporting TFT Panel Resolution:
  - 2 Layers : Up to 320x240 Pixels with Internal DDRAM.
  - 1 Layer : Up to 640x480 Pixels.
- Support 256 User-defined 8x16 Characters.
- Support 32 User-defined Patterns of 8x8 Pixels.
- 2 programmable PWM for Back-Light Adjusting or Other's Application.
- Embedded 4 or 5-Wires Touch Panel Controller.
- 6 Sets of Programmable GPIO (GPIO0~5).
- Sleep Mode with Low Power Consumption.
- Operation Voltage: 3.0V~3.6V
- Package: TQFP-128pin.

3. Block Diagram

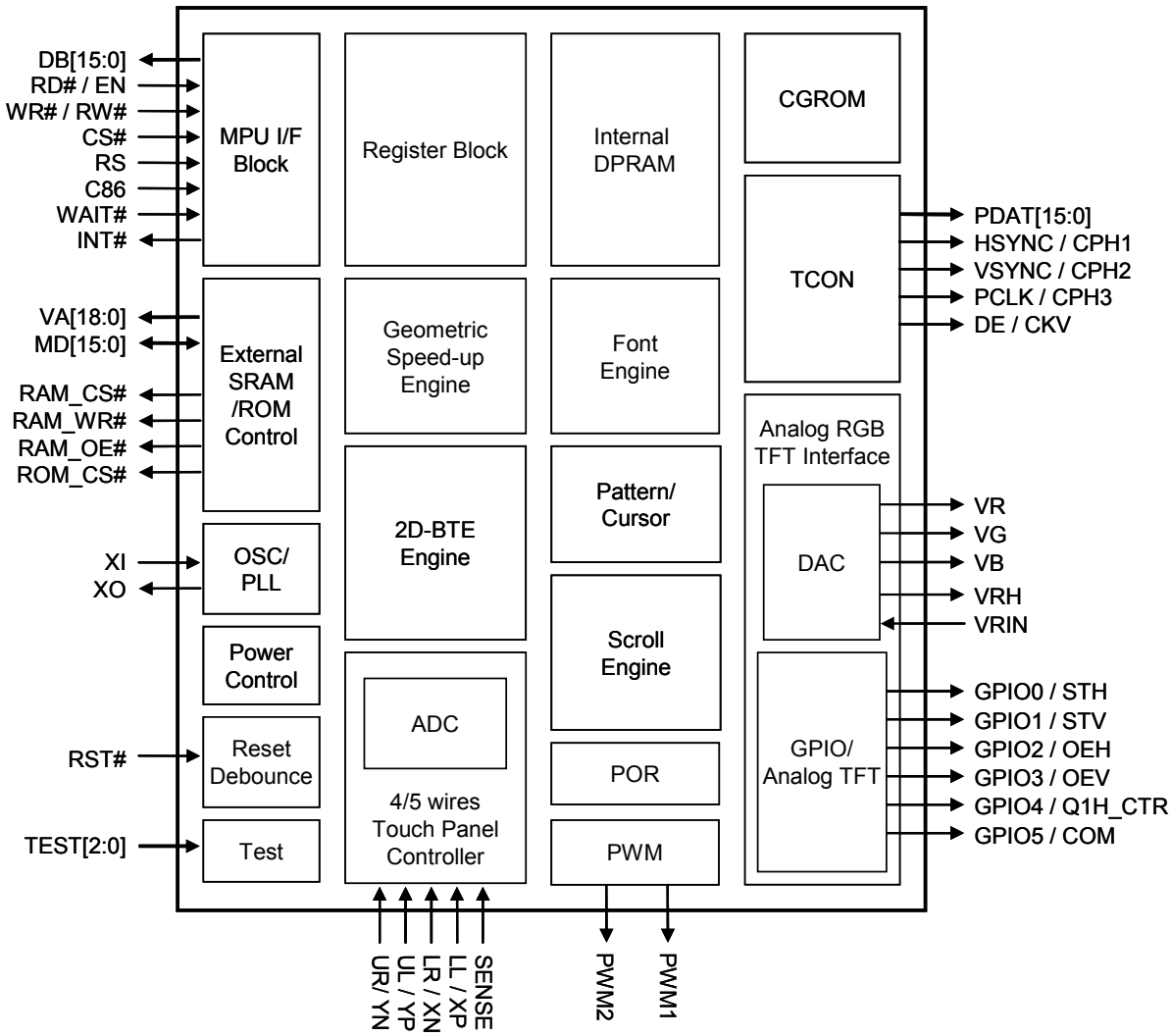


Figure 3-1 : Internal Block Diagram

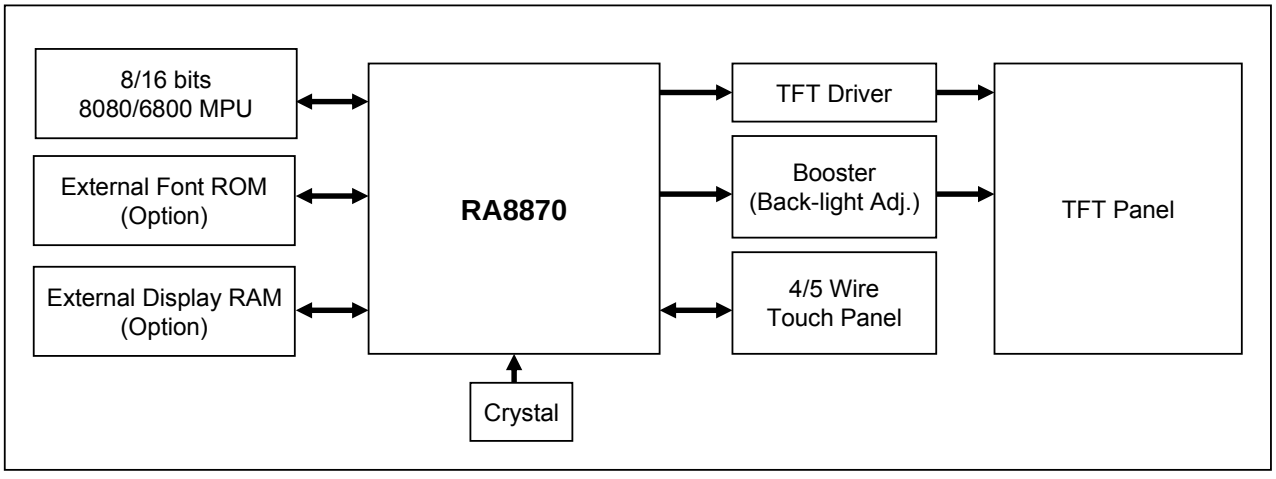


Figure 3-2 : System Block Diagram

4. Pin Definition

4-1 MCU Interface

Pin Name	I/O	Pin#	Pin Description
DB[15:0]	IO	109, 110, 114~ 127	**Data Bus** These are data bus for data transfer between MCU and RA8870. The DB[15:8] is input and should be pulled to GND or VDD when 8-bit data bus mode is used.
RD# / EN	I	104	**Enable/Read Enable** When MCU interface (I/F) is 8080 series, this pin is used as data read (RD#), active low. When MCU I/F is 6800 series, this pin is used as Enable (EN), active high.
WR# / RW#	I	105	**Write/Read-Write** When MCU I/F is 8080 series, this pin is used as data write (WR#), active low. When MCU I/F is 6800 series, this pin is used as data read/write control (RW#). Active high for read and active low for write.
CS#	I	106	**Chip Select Input** Low active chip select pin.
RS	I	107	**Command / Data Select Input** The pin is used to select command/data cycle. RS = 0, data Read/Write cycle is selected. RS = 1, status read/command write cycle is selected. In 8080 interface, usually it connects to “A0” address pin.

RS	WR#	Access Cycle
0	0	Data Write
0	1	Data Read
1	0	CMD Write
1	1	Status Read

C86	I	108	**MCU Interface Select** 0 : 8080 interface is selected. 1 : 6800 interface is selected.
INT#	O	11	**Interrupt Signal Output** The interrupt output for MCU to indicate the status of RA8870.
WAIT#	O	10	**Wait Signal Output** This is a WAIT output to indicate the RA8870 is in busy state. The RA8870 can’t access MCU cycle when WAIT# pin is active. It is active low and could be used for MCU to poll busy status by connecting it to I/O port.

4-2 LCD Panel Interface

Pin Name	I/O	Pin#	Pin Description
PDAT[15:0]	O	78~93	**LCD Panel Data Bus** Data bus output for TFT LCD panel driver IC. This data bus must be connected to the corresponding bus of TFT-LCD panel.
HSYNC / CPH1	O	74	**HSYNC Pulse / CPH1** When generic TFT is selected, the signal is used as HSYNC. When analog TFT is selected, the signal is used as CPH1.
VSYNC / CPH2	O	75	**VSYNC Pulse / CPH2** When generic TFT is selected, the signal is used as VSYNC. When analog TFT is selected, the signal is used as CPH2.
PCLK / CPH3	O	76	**Pixel Clock / CPH3** When generic TFT is selected, the signal is used as PCLK. When analog TFT is selected, the signal is used as CPH3.
DE/ CKV	O	77	**Data Enable / CKV** When generic TFT is selected, the signal is used as DE. When analog TFT is selected, the signal is used as CKV.
GPIO0 / STH	IO	58	**General Purpose I/O 0 / STH** When generic TFT is selected, the signal is used as GPIO signal; user can program it by register. When analog TFT is selected, the signal is used as STH.
GPIO1 / STV	IO	59	**General Purpose I/O 1 / STV** When generic TFT is selected, the signal is used as GPIO signal; user can program it by register. When analog TFT is selected, the signal is used as STV.
GPIO2 / OEH	IO	60	**General Purpose I/O 2/OEH** When generic TFT is selected, the signal is used as GPIO signal; user can program it by register. When analog TFT is selected, the signal is used as OEH.
GPIO3 / OEV	IO	61	**General Purpose I/O 3/OEV** When generic TFT is selected, the signal is used as GPIO signal; user can program it by register. When analog TFT is selected, the signal is used as OEV.
GPIO4 / Q1H_CTR	IO	62	**General Purpose I/O 4 / Q1H_CTR** When generic TFT is selected, the signal is used as GPIO signal; user can program it by register. When analog TFT is selected, the signal is used as Q1H_CTR. It is the control signal for Q1H.
GPIO5 / COM	IO	63	**General Purpose I/O 5 / COM** When generic TFT is selected, the signal is used as GPIO signal; user can program it by register. When analog TFT is selected, the signal is used as COM. It is the control signal of VCOM.

Pin Name	I/O	Pin#	Pin Description
VR	O	69	**Analog R Output** The analog output for analog TFT driver red data denotation.
VG	O	68	**Analog G Output** The analog output for analog TFT driver green data denotation.
VB	O	67	**Analog B Output** The analog output for analog TFT driver blue data denotation.

4-3 Touch Panel and PWM Interface

Pin Name	I/O	Pin#	Pin Description
UR / YN	A	102	**UR/YN Signal for Touch Panel** Touch Panel control signal. When 5-wires TP is selected, it is used as UR output signal. When 4-wires TP is selected, it is used as YN switch signal.
UL / YP	A	101	**UL/YP Signal for Touch Panel** Touch Panel control signal. When 5-wires TP is selected, it is used as UL output signal. When 4-wires TP is selected, it is used as YP switch signal. This pin must be connected a 100KΩ pull-up resistor when the Touch Panel function is enable.
LR / XN	A	99	**LR/XN Signal for Touch Panel** Touch Panel control signal. When 5-wires TP is selected, it is used as LR output signal. When 4-wires TP is selected, it is used as XN switch signal.
LL / XP	A	103	**LL/XP Signal for Touch Panel** Touch Panel control signal. When 5-wires TP is selected, it is used as LL output signal. When 4-wires TP is selected, it is used as XP switch signal.
SENSE	A	100	**SENSE Signal for 5-wire Touch Panel** When 5-wires TP is selected, it is used as SENSE analog input signal. When 4-wires TP is selected, it is not used as should be floating.
PWM1 **PWM2**	O	7, 8	**PWM Output 1** PWM output pin. The duty could be programmed by register setting.

4-4 External Memory

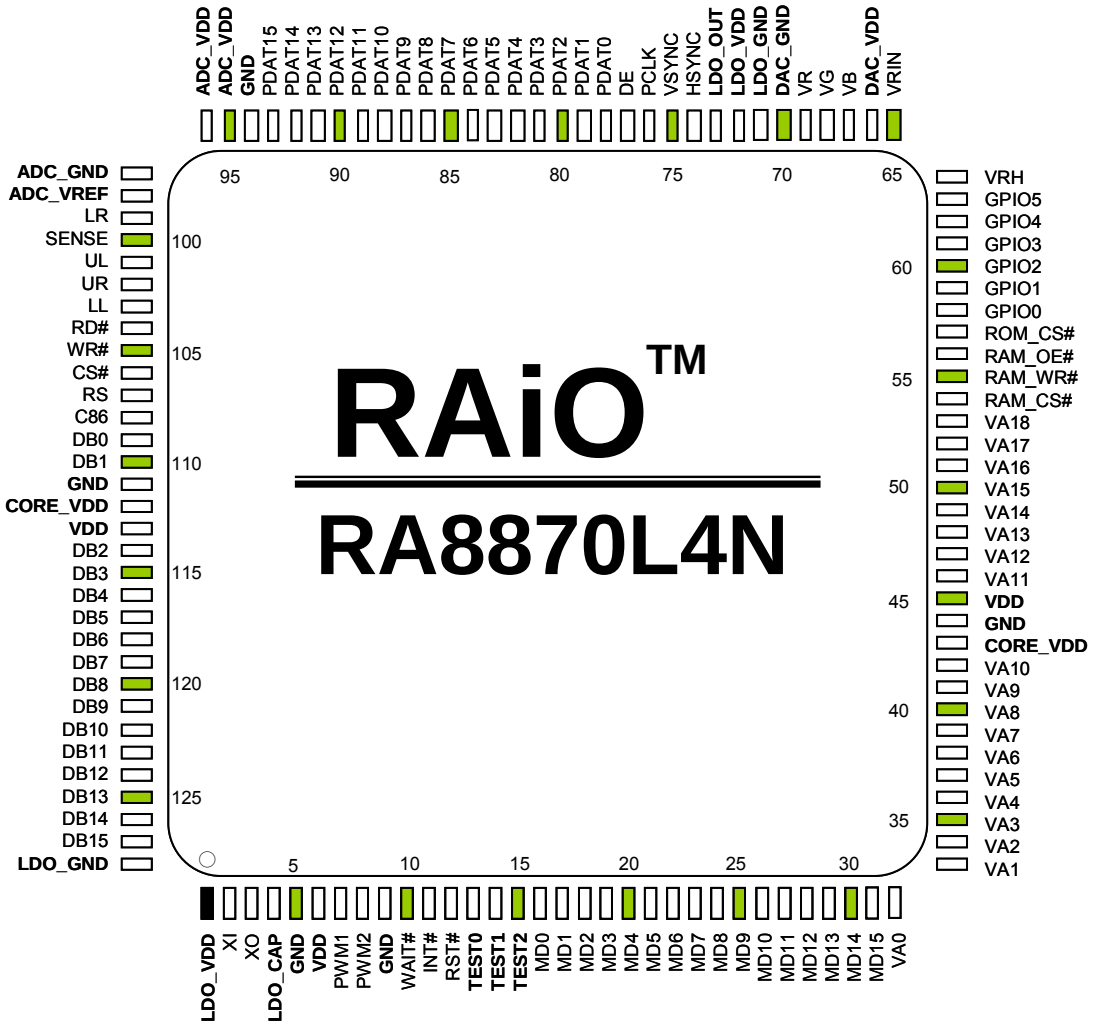
Pin Name	I/O	Pin#	Pin Description
VA[18:0]	O	32~42, 46~53	**External RAM/ROM Address Bus** When external Font ROM is used, VA[18:0] is used as external 512KB Font ROM address bus. When external DDRAM is used, VA[18:0] are also used as RAM address bus. When internal DDRAM is used with no external Font ROM, VA[18:0] should be kept as floating.
MD[15:0]	IO	16~31	**External RAM/ROM Data Bus** When external Font ROM is used, them are used as data bus input signal, only MD[7:0] is used. When external DDRAM is used, them are also used as RAM R/W data bus. 8-bit or 16-bit interface will be selected by register setting. When internal DDRAM is used with no external Font ROM, MD[15:0] are suggested to connected to VDD for preventing the IO leakage.
RAM_OE#	O	56	**RAM Data Output Enable Signal** Data output enable signal for external DDRAM.
RAM_WR#	O	55	**RAM Write Enable Signal** Write strobe signal for external DDRAM.
RAM_CS#	O	54	**RAM Chip Selection Signal** Chip select signal for external DDRAM.
ROM_CS#	O	57	**ROM Chip Selection Signal** Chip select signal for external font ROM.

4-5 Clock and Power Interface

Pin Name	I/O	Pin#	Pin Description
XI	I	2	**Crystal Input Pin** Input pin for internal crystal circuit. It should be connected to external crystal to generate the source of PLL circuit. That will generate the system clock for RA8870.
XO	O	3	**Crystal Output Pin** Output pin for internal crystal circuit.
RST#	I	12	**Reset Signal Input** This active-low input performs a hardware reset on the RA8870. It is a Schmitt-trigger input for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.
TEST[2:0]	I	13~15	**Test Mode Input** For chip test function, should be connected to GND for normal operation.
VRIN	A	65	**DAC Reference Voltage Input** This is a reference voltage input to create VRH signal. For normal operation, it only need add a 0.1uF capacitor to ground.

Pin Name	I/O	Pin#	Pin Description
VRH	A	64	**DAC Reference Voltage Output** This is a reference voltage output of DAC. For normal operation, it only need add a 0.2uF capacitor to ground.
ADC_VREF	A	98	**ADC Reference Voltage** This pin is the reference voltage input of ADC. The reference voltage could be generated by RA8870 or from external circuit.
VDD	P	6, 45, 113	**IO VDD** 3.3V IO power input.
LDO_VDD	P	1, 72	**LDO VDD** 3.3V power source for LDO. The internal LDO will generate the 1.8V power output.
LDO_GND	P	71, 128	**LDO GND** Ground signal for internal LDO.
LDO_OUT	P	73	**LDO Output** 1.8V power generated by internal LDO. It must connect bypass capacities to prevent power noise.
LDO_CAP	P	4	**LDO Capacitor Input** It must connect 1uF bypass capacities to prevent power noise.
CORE_VDD	P	43, 112	**CORE VDD** Core VDD is 1.8V.The core power input that connect to LDO_OUT. It must connect 1uF bypass capacities to prevent power noise.
ADC_VDD	P	95, 96	**ADC VDD** ADC 3.3V power signals. Please connect this signal to 3.3V.
ADC_GND	P	97	**ADC GND** ADC ground signal. Please connect this signal to ground.
DAC_VDD	P	66	**DAC VDD** DAC 3.3V power signal. Please connect this signal to 3.3V.
DAC_GND	P	70	**DAC GND** DAC ground signal. Please connect this signal to ground.
GND	P	5, 9, 44, 94, 111	**GND** IO Cell/Core ground signals.

5. Package


ADC_VDD
ADC_VDD
GND
PDAT15
PDAT14
PDAT13
PDAT12
PDAT11
PDAT10
PDAT9
PDAT8
PDAT7
PDAT6
PDAT5
PDAT4
PDAT3
PDAT2
PDAT1
PDAT0
DE
PCLK
VSYNC
HSYNC
LDO_OUT
LDO_VDD
LDO_GND
DAC_GND
VR
VG
VB
DAC_VDD
VRIN
ADC_GND
ADC_VREF
LR
SENSE
UL
UR
LL
RD#
WR#
CS#
RS
C86
DB0
DB1
GND
CORE_VDD
VDD
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
LDO_GND
VRH
GPIO5
GPIO4
GPIO3
GPIO2
GPIO1
GPIO0
ROM_CS#
RAM_OE#
RAM_WR#
RAM_CS#
VA18
VA17
VA16
VA15
VA14
VA13
VA12
VA11
VDD
GND
CORE_VDD
VA10
VA9
VA8
VA7
VA6
VA5
VA4
VA3
VA2
VA1
LDO_VDD
XI
XO
LDO_CAP
GND
VDD
PWM1
PWM2
GND
WAIT#
INT#
RST#
TEST0
TEST1
TEST2
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
VA0
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