

To all our customers

---

## **Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.**

---

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

## Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

Hitachi SuperH™ RISC engine

SH-2

SH7052 F-ZTAT™

SH7053 F-ZTAT™

SH7054 F-ZTAT™

Hardware Manual

**RENESAS**

ADE-602-185B

Rev. 3.0

3/3/03

Hitachi, Ltd.

## Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

# Preface

The SH7052F/SH7053F/SH7054F is a single-chip RISC (reduced instruction set computer) microcomputer that has an original Hitachi RISC type CPU as its core, and also includes peripheral functions necessary for system configuration.

The CPU of the SH7052F/SH7053F/SH7054F has a RISC type instruction set, with basic instructions executed in one system clock cycle, for a higher instruction execution speed. It employs an internal 32-bit configuration, and offers enhanced data processing performance. The CPU of the SH7052F/SH7053F/SH7054F makes it possible to create high-performance, high-functionality systems at low cost, even for applications requiring high speed such as real-time control, which could not be realized with conventional microcomputers.

The SH7052F/SH7053F/SH7054F is also equipped with on-chip peripheral functions necessary for system configuration, including large-capacity ROM and RAM, a direct memory access controller (DMAC), timers, a serial communication interface (SCI), Hitachi controller area network (HCAN), A/D converter, interrupt controller (INTC), and I/O ports.

In addition, an external memory access support function allows direct connection of ROM and SRAM, enabling system costs to be greatly reduced.

The SH7052F/SH7053F/SH7054F is an F-ZTAT™ (Flexible Zero Turn-Around Time) version with flash memory as its on-chip ROM. Flash memory programs can be written with a programmer that supports SH7052F/SH7053F/SH7054F programming, and the flash memory can also be programmed and erased by software. This allows reprogramming to be carried out by the user with the chip mounted on a board.

This Hardware Manual describes the hardware of the SH7052F/SH7053F/SH7054F. Details of instructions can be found in the Programming Manual.

## Related Manual

Covering SH7052F/SH7053F/SH7054F execution instructions:  
SH-1/SH-2/SH-DSP Programming Manual

Please consult your Hitachi sales representative for details of the development environment system.



# Main Revisions and Additions in this Edition

Page	Item	Revisions (See Manual for Details)
8	1.3.1 Pin Arrangement	Name of 155 th pin amended (PK11/TO8L)
61	5.1.1 Types of Exception Processing and Priority	Table 5.1 Types of Exception Processing and Priority Order Compare match timer (CMT1), A/D converter channel 1 (A/D1) added Module abbreviations amended: CMT0, A/D0
160	9.3.5 Dual Address Mode	Figure 9.5 Dual Address Mode and Indirect Address Operation (16-Bit-Width External Memory Space) Description of 1st and 2nd bus cycles amended If the data bus is 16 bits wide when the external memory space is accessed, two bus cycles are necessary.
217	10.2.3 Timer Control Registers (TCR)	Timer Control Register 9A, 9B, 9C (TCR9A, TCR9B, TCR9C) Description of Bits 1 and 0 amended x=A, C, or E
306	10.2.15 Free-Running Counters (TCNT)	Description of Free-Running Counter 0 added When the bits corresponding to the timer start register 1 (TSTR1) are set to 1, this counter starts to count.
307		Description of Free-Running Counters 1A, 1B, 2A, 2B, 3, 4, 5, 11 added When the bits corresponding to the timer start register 1, 3 (TSTR1, TSTR3) are set to 1, these counters start to count.
335	10.3.1 Overview	Description of Channel 2 amended
337		Description of Channel 10 amended
348	10.3.9 PWM Timer Function	Description amended ..., and H'0002, H'0003, H'0004 (100%), and H'0000 (0%) in BFR6A.
375	10.6 Sample Setup Procedures	Sample Setup Procedure for Channel 0 Input Capture Triggered by Channel 10 Compare-Match Register name amended
399	Writing to ROM Area Immediately after ATU Register Write	Description added

Page	Item	Revisions (See Manual for Details)
400, 401	10.8 ATU-II Registers And Pins	Table 10.4 ATU-II Registers and Pins Register names amended Pin names added and deleted
435	13.4.2 Compare Match Flag Set Timing	Figure 13.4 CMF Set Timing CMCNT timing waveform amended
435	13.4.3 Compare Match Flag Clear Timing	Description deleted
445	14.2.5 Serial Mode Register (SMR)	Description amended
448	14.2.6 Serial Control Register (SCR)	Description amended
456	14.2.8 Bit Rate Register (BRR)	Description amended
463	14.2.9 Serial Direction Control Register (SDCR)	Description amended
497	14.5.3 Break Detection and Processing 14.5.4 Sending a Break Signal	Description added (Asynchronous Mode Only)
504	Table 15.2 HCAN Registers	RFPR register name amended IMR initial value amended
510	15.2.3 Bit Configuration Register (BCR)	BCR setting constraints amended Table note added
517	15.2.11 Interrupt Register (IRR)	Initial value of bits 10 and 9 amended
519		Description of bit 9 amended
520		Description of bit 8 amended
533	15.3.1 Hardware Reset and Software Reset	Description of Hardware Reset amended
537	Table 15.4 BCR Setting Limits	Description amended
541	Figure 15.7 Transmission Flowchart	Description amended
548	Figure 15.9 Reception Flowchart	Description amended
552	Figure 15.11 HCAN Sleep Mode Flowchart	Description amended
554	Figure 15.12 HCAN Halt Mode Flowchart	Description amended
560	16.1.1 Features	Description deleted



Page	Item	Revisions (See Manual for Details)
562	16.1.3 Pin Configuration	Description amended
570	16.2.3 A/D Control Registers 0 and 1 (ADCR0, ADCR1)	Description amended
585	16.4.4 External Triggering of A/D Converter	Description amended
600	17.5.3 ROM Area Writes	New description added
701	20.5.5 RAM Emulation Register (RAMER)	Description of bits 15 to 4 added The write value should always be 0.
713	20.7.3 Erase Mode	Description amended
722	20.10 Note on Flash Memory Programming/Erasing	Description added
763	21.7.3 Erase Mode	Description amended
797	23.3.1 Transition to Hardware Standby Mode	Description added
815 to 819	24.2 DC Characteristics	Table 24.4 DC Characteristics Description amended
837	24.3.9 HCAN Timing	Table 24.14 HCAN Timing Description amended
840	24.3.11 AUD Timing	Table 24.16 AUD Timing Load conditions added
863, 867	Appendix A.1 Address	Table A.1 Address Register abbreviations amended: H'FFFFFF466, H'FFFFFF526
881, 884 to 886	A.2 Register States in Reset and Power-Down States	Table A.2 Register States in Reset and Power-Down States Description amended
891	Appendix D Package Dimensions	Figure D.1 Package Dimensions (FP-208A) Amended



# Contents

Section 1	Overview .....	1
1.1	Features.....	1
1.2	Block Diagram.....	7
1.3	Pin Description .....	8
1.3.1	Pin Arrangement .....	8
1.3.2	Pin Functions.....	9
1.3.3	Pin Assignments .....	16
Section 2	CPU.....	23
2.1	Register Configuration .....	23
2.1.1	General Registers (Rn).....	23
2.1.2	Control Registers.....	24
2.1.3	System Registers .....	25
2.1.4	Initial Values of Registers.....	25
2.2	Data Formats.....	26
2.2.1	Data Format in Registers.....	26
2.2.2	Data Format in Memory .....	26
2.2.3	Immediate Data Format.....	26
2.3	Instruction Features .....	27
2.3.1	RISC-Type Instruction Set .....	27
2.3.2	Addressing Modes.....	30
2.3.3	Instruction Format.....	34
2.4	Instruction Set by Classification.....	37
2.5	Processing States .....	50
2.5.1	State Transitions .....	50
Section 3	Operating Modes .....	53
3.1	Operating Mode Selection .....	53
Section 4	Clock Pulse Generator (CPG).....	55
4.1	Overview.....	55
4.1.1	Block Diagram.....	55
4.1.2	Pin Configuration .....	56
4.2	Frequency Ranges.....	56
4.3	Clock Source.....	57
4.3.1	Connecting a Crystal Oscillator.....	57
4.3.2	External Clock Input Method .....	58
4.4	Usage Notes .....	59

Section 5	Exception Processing .....	61
5.1	Overview.....	61
5.1.1	Types of Exception Processing and Priority .....	61
5.1.2	Exception Processing Operations .....	62
5.1.3	Exception Processing Vector Table.....	63
5.2	Resets.....	65
5.2.1	Types of Reset.....	65
5.2.2	Power-On Reset.....	65
5.2.3	Manual Reset.....	66
5.3	Address Errors .....	67
5.3.1	Address Error Sources.....	67
5.3.2	Address Error Exception Processing .....	68
5.4	Interrupts.....	68
5.4.1	Interrupt Sources .....	68
5.4.2	Interrupt Priority Level.....	69
5.4.3	Interrupt Exception Processing .....	69
5.5	Exceptions Triggered by Instructions.....	70
5.5.1	Types of Exceptions Triggered by Instructions.....	70
5.5.2	Trap Instructions .....	70
5.5.3	Illegal Slot Instructions .....	71
5.5.4	General Illegal Instructions .....	71
5.6	When Exception Sources Are Not Accepted.....	72
5.7	Stack Status after Exception Processing Ends.....	73
5.8	Usage Notes .....	74
5.8.1	Value of Stack Pointer (SP).....	74
5.8.2	Value of Vector Base Register (VBR) .....	74
5.8.3	Address Errors Caused by Stacking of Address Error Exception Processing.....	74
Section 6	Interrupt Controller (INTC).....	75
6.1	Overview.....	75
6.1.1	Features .....	75
6.1.2	Block Diagram.....	76
6.1.3	Pin Configuration .....	77
6.1.4	Register Configuration .....	77
6.2	Interrupt Sources.....	78
6.2.1	NMI Interrupts.....	78
6.2.2	User Break Interrupt .....	78
6.2.3	IRQ Interrupts .....	78
6.2.4	On-Chip Peripheral Module Interrupts .....	79
6.2.5	Interrupt Exception Vectors and Priority Rankings .....	79
6.3	Description of Registers .....	88
6.3.1	Interrupt Priority Registers A, C to L (IPRA, IPRC to IPRL) .....	88
6.3.2	Interrupt Control Register (ICR).....	89

6.3.3	IRQ Status Register (ISR) .....	90
6.4	Interrupt Operation .....	92
6.4.1	Interrupt Sequence .....	92
6.4.2	Stack after Interrupt Exception Processing .....	94
6.5	Interrupt Response Time .....	95
6.6	Data Transfer with Interrupt Request Signals .....	97
6.6.1	Handling CPU Interrupt Sources, but Not DMAC Activating Sources .....	97
6.6.2	Handling DMAC Activating Sources but Not CPU Interrupt Sources .....	97
<b>Section 7</b>	<b>User Break Controller (UBC) .....</b>	<b>99</b>
7.1	Overview .....	99
7.1.1	Features .....	99
7.1.2	Block Diagram .....	100
7.1.3	Register Configuration .....	101
7.2	Register Descriptions .....	101
7.2.1	User Break Address Register (UBAR) .....	101
7.2.2	User Break Address Mask Register (UBAMR) .....	102
7.2.3	User Break Bus Cycle Register (UBBR) .....	104
7.2.4	User Break Control Register (UBCR) .....	106
7.3	Operation .....	107
7.3.1	Flow of the User Break Operation .....	107
7.3.2	Break on On-Chip Memory Instruction Fetch Cycle .....	109
7.3.3	Program Counter (PC) Values Saved .....	109
7.4	Examples of Use .....	110
7.4.1	Break on CPU Instruction Fetch Cycle .....	110
7.4.2	Break on CPU Data Access Cycle .....	111
7.4.3	Break on DMA Cycle .....	111
7.5	Usage Notes .....	112
7.5.1	Simultaneous Fetching of Two Instructions .....	112
7.5.2	Instruction Fetch at Branches .....	112
7.5.3	Contention between User Break and Exception Processing .....	113
7.5.4	Break at Non-Delay Branch Instruction Jump Destination .....	113
7.5.5	User Break Trigger Output .....	113
7.5.6	Module Standby .....	114
<b>Section 8</b>	<b>Bus State Controller (BSC) .....</b>	<b>115</b>
8.1	Overview .....	115
8.1.1	Features .....	115
8.1.2	Block Diagram .....	116
8.1.3	Pin Configuration .....	117
8.1.4	Register Configuration .....	117
8.1.5	Address Map .....	118
8.2	Description of Registers .....	122

8.2.1	Bus Control Register 1 (BCR1).....	122
8.2.2	Bus Control Register 2 (BCR2).....	123
8.2.3	Wait Control Register (WCR).....	126
8.2.4	RAM Emulation Register (RAMER) .....	128
8.3	Accessing External Space.....	130
8.3.1	Basic Timing .....	130
8.3.2	Wait State Control.....	131
8.3.3	$\overline{\text{CS}}$ Assert Period Extension.....	133
8.4	Waits between Access Cycles .....	134
8.4.1	Prevention of Data Bus Conflicts .....	134
8.4.2	Simplification of Bus Cycle Start Detection .....	135
8.5	Bus Arbitration .....	136
8.6	Memory Connection Examples .....	137
<b>Section 9 Direct Memory Access Controller (DMAC).....</b>		<b>139</b>
9.1	Overview.....	139
9.1.1	Features .....	139
9.1.2	Block Diagram.....	140
9.1.3	Register Configuration .....	141
9.2	Register Descriptions.....	142
9.2.1	DMA Source Address Registers 0 to 3 (SAR0 to SAR3) .....	142
9.2.2	DMA Destination Address Registers 0 to 3 (DAR0 to DAR3).....	143
9.2.3	DMA Transfer Count Registers 0 to 3 (DMATCR0 to DMATCR3) .....	144
9.2.4	DMA Channel Control Registers 0 to 3 (CHCR0 to CHCR3) .....	145
9.2.5	DMAC Operation Register (DMAOR) .....	150
9.3	Operation .....	152
9.3.1	DMA Transfer Flow .....	152
9.3.2	DMA Transfer Requests.....	154
9.3.3	Channel Priority.....	157
9.3.4	DMA Transfer Types .....	157
9.3.5	Dual Address Mode.....	157
9.3.6	Bus Modes.....	163
9.3.7	Relationship between Request Modes and Bus Modes by DMA Transfer Category .....	164
9.3.8	Bus Mode and Channel Priorities.....	165
9.3.9	Source Address Reload Function .....	165
9.3.10	DMA Transfer Ending Conditions .....	166
9.3.11	DMAC Access from CPU .....	167
9.4	Examples of Use.....	168
9.4.1	Example of DMA Transfer between On-Chip SCI and External Memory.....	168
9.4.2	Example of DMA Transfer between A/D Converter and On-Chip Memory (Address Reload On).....	168

9.4.3	Example of DMA Transfer between External Memory and SCI1 Transmitting Side (Indirect Address On).....	170
9.5	Usage Notes .....	172
<b>Section 10 Advanced Timer Unit-II (ATU-II).....</b>		
10.1	Overview.....	173
10.1.1	Features .....	173
10.1.2	Pin Configuration .....	178
10.1.3	Register Configuration .....	182
10.1.4	Block Diagrams.....	192
10.1.5	Inter-Channel and Inter-Module Signal Communication Diagram.....	202
10.1.6	Prescaler Diagram .....	203
10.2	Register Descriptions.....	204
10.2.1	Timer Start Registers (TSTR) .....	204
10.2.2	Prescaler Registers (PSCR).....	208
10.2.3	Timer Control Registers (TCR).....	209
10.2.4	Timer I/O Control Registers (TIOR).....	219
10.2.5	Timer Status Registers (TSR) .....	231
10.2.6	Timer Interrupt Enable Registers (TIER).....	260
10.2.7	Interval Interrupt Request Registers (ITVRR) .....	282
10.2.8	Trigger Mode Register (TRGMDR) .....	286
10.2.9	Timer Mode Register (TMDR) .....	286
10.2.10	PWM Mode Register (PMDR).....	288
10.2.11	Down-Count Start Register (DSTR) .....	290
10.2.12	Timer Connection Register (TCNR).....	296
10.2.13	One-Shot Pulse Terminate Register (OTR).....	301
10.2.14	Reload Enable Register (RLDENR) .....	305
10.2.15	Free-Running Counters (TCNT) .....	306
10.2.16	Down-Counters (DCNT).....	308
10.2.17	Event Counters (ECNT) .....	309
10.2.18	Output Compare Registers (OCR).....	310
10.2.19	Input Capture Registers (ICR).....	311
10.2.20	General Registers (GR) .....	312
10.2.21	Offset Base Registers (OSBR) .....	314
10.2.22	Cycle Registers (CYLR) .....	315
10.2.23	Buffer Registers (BFR) .....	316
10.2.24	Duty Registers (DTR) .....	317
10.2.25	Reload Register (RLDR).....	318
10.2.26	Channel 10 Registers.....	318
10.3	Operation .....	333
10.3.1	Overview .....	333
10.3.2	Free-Running Counter Operation and Cyclic Counter Operation.....	339
10.3.3	Compare-Match Function .....	341

10.3.4	Input Capture Function.....	342
10.3.5	One-Shot Pulse Function.....	343
10.3.6	Offset One-Shot Pulse Function and Output Cutoff Function .....	344
10.3.7	Interval Timer Operation.....	345
10.3.8	Twin-Capture Function .....	346
10.3.9	PWM Timer Function .....	347
10.3.10	Channel 3 to 5 PWM Function.....	349
10.3.11	Event Count Function and Event Cycle Measurement.....	350
10.3.12	Channel 10 Functions .....	352
10.4	Interrupts.....	360
10.4.1	Status Flag Setting Timing .....	360
10.4.2	Status Flag Clearing .....	365
10.5	CPU Interface .....	367
10.5.1	Registers Requiring 32-Bit Access .....	367
10.5.2	Registers Permitting 8-Bit, 16-Bit, or 32-Bit Access .....	369
10.5.3	Registers Requiring 16-Bit Access .....	370
10.5.4	8-Bit or 16-Bit Accessible Registers.....	371
10.5.5	Registers Requiring 8-Bit Access .....	372
10.6	Sample Setup Procedures .....	372
10.7	Usage Notes.....	387
10.8	ATU-II Registers And Pins .....	400
<b>Section 11 Advanced Pulse Controller (APC).....</b>		<b>403</b>
11.1	Overview.....	403
11.1.1	Features .....	403
11.1.2	Block Diagram.....	404
11.1.3	Pin Configuration .....	405
11.1.4	Register Configuration .....	405
11.2	Register Descriptions.....	406
11.2.1	Pulse Output Port Control Register (POPCR).....	406
11.3	Operation .....	407
11.3.1	Overview .....	407
11.3.2	Advanced Pulse Controller Output Operation.....	408
11.4	Usage Notes.....	411
<b>Section 12 Watchdog Timer (WDT).....</b>		<b>413</b>
12.1	Overview.....	413
12.1.1	Features .....	413
12.1.2	Block Diagram.....	414
12.1.3	Pin Configuration .....	414
12.1.4	Register Configuration .....	415
12.2	Register Descriptions.....	415
12.2.1	Timer Counter (TCNT).....	415



12.2.2	Timer Control/Status Register (TCSR) .....	416
12.2.3	Reset Control/Status Register (RSTCSR) .....	418
12.2.4	Register Access .....	419
12.3	Operation .....	420
12.3.1	Watchdog Timer Mode .....	420
12.3.2	Interval Timer Mode .....	422
12.3.3	Clearing Software Standby Mode .....	422
12.3.4	Timing of Setting the Overflow Flag (OVF).....	423
12.3.5	Timing of Setting the Watchdog Timer Overflow Flag (WOVF).....	423
12.4	Usage Notes .....	424
12.4.1	TCNT Write and Increment Contention.....	424
12.4.2	Changing CKS2 to CKS0 Bit Values.....	424
12.4.3	Changing between Watchdog Timer/Interval Timer Modes.....	424
12.4.4	System Reset by <u>WDTOVF</u> Signal.....	425
12.4.5	Internal Reset in Watchdog Timer Mode .....	425
12.4.6	Manual Reset in Watchdog Timer.....	425
<b>Section 13 Compare Match Timer (CMT) .....</b>		<b>427</b>
13.1	Overview.....	427
13.1.1	Features .....	427
13.1.2	Block Diagram.....	428
13.1.3	Register Configuration .....	429
13.2	Register Descriptions.....	430
13.2.1	Compare Match Timer Start Register (CMSTR) .....	430
13.2.2	Compare Match Timer Control/Status Register (CMCSR).....	431
13.2.3	Compare Match Timer Counter (CMCNT).....	432
13.2.4	Compare Match Timer Constant Register (CMCOR).....	433
13.3	Operation .....	433
13.3.1	Cyclic Count Operation.....	433
13.3.2	CMCNT Count Timing .....	434
13.4	Interrupts.....	434
13.4.1	Interrupt Sources and DTC Activation.....	434
13.4.2	Compare Match Flag Set Timing .....	434
13.4.3	Compare Match Flag Clear Timing.....	435
13.5	Usage Notes .....	436
13.5.1	Contention between CMCNT Write and Compare Match.....	436
13.5.2	Contention between CMCNT Word Write and Incrementation .....	437
13.5.3	Contention between CMCNT Byte Write and Incrementation .....	438
<b>Section 14 Serial Communication Interface (SCI) .....</b>		<b>439</b>
14.1	Overview.....	439
14.1.1	Features .....	439
14.1.2	Block Diagram.....	440

14.1.3	Pin Configuration .....	441
14.1.4	Register Configuration .....	442
14.2	Register Descriptions.....	443
14.2.1	Receive Shift Register (RSR).....	443
14.2.2	Receive Data Register (RDR) .....	444
14.2.3	Transmit Shift Register (TSR).....	444
14.2.4	Transmit Data Register (TDR) .....	445
14.2.5	Serial Mode Register (SMR).....	445
14.2.6	Serial Control Register (SCR).....	448
14.2.7	Serial Status Register (SSR).....	452
14.2.8	Bit Rate Register (BRR).....	456
14.2.9	Serial Direction Control Register (SDCR).....	463
14.2.10	Inversion of SCK Pin Signal .....	464
14.3	Operation .....	464
14.3.1	Overview .....	464
14.3.2	Operation in Asynchronous Mode.....	466
14.3.3	Multiprocessor Communication .....	476
14.3.4	Synchronous Operation .....	484
14.4	SCI Interrupt Sources and the DMAC.....	495
14.5	Usage Notes .....	496
14.5.1	TDR Write and TDRE Flag.....	496
14.5.2	Simultaneous Multiple Receive Errors .....	496
14.5.3	Break Detection and Processing (Asynchronous Mode Only).....	497
14.5.4	Sending a Break Signal (Asynchronous Mode Only) .....	497
14.5.5	Receive Error Flags and Transmitter Operation (Synchronous Mode Only).....	497
14.5.6	Receive Data Sampling Timing and Receive Margin in Asynchronous Mode....	497
14.5.7	Constraints on DMAC Use .....	499
14.5.8	Cautions on Synchronous External Clock Mode.....	499
14.5.9	Caution on Synchronous Internal Clock Mode .....	499
Section 15 Hitachi Controller Area Network (HCAN) .....		501
15.1	Overview.....	501
15.1.1	Features .....	501
15.1.2	Block Diagram.....	502
15.1.3	Pin Configuration .....	503
15.1.4	Register Configuration .....	504
15.2	Register Descriptions.....	506
15.2.1	Master Control Register (MCR).....	506
15.2.2	General Status Register (GSR).....	507
15.2.3	Bit Configuration Register (BCR).....	508
15.2.4	Mailbox Configuration Register (MBCR).....	512
15.2.5	Transmit Wait Register (TXPR) .....	512
15.2.6	Transmit Wait Cancel Register (TXCR).....	513

15.2.7	Transmit Acknowledge Register (TXACK) .....	514
15.2.8	Abort Acknowledge Register (ABACK).....	515
15.2.9	Receive Complete Register (RXPR).....	516
15.2.10	Remote Request Register (RFPR).....	517
15.2.11	Interrupt Register (IRR) .....	517
15.2.12	Mailbox Interrupt Mask Register (MBIMR).....	521
15.2.13	Interrupt Mask Register (IMR) .....	522
15.2.14	Receive Error Counter (REC) .....	524
15.2.15	Transmit Error Counter (TEC) .....	525
15.2.16	Unread Message Status Register (UMSR) .....	525
15.2.17	Local Acceptance Filter Masks (LAFML, LAFMH) .....	526
15.2.18	Message Control (MC0 to MC15).....	527
15.2.19	Message Data (MD0 to MD15).....	531
15.3	Operation .....	533
15.3.1	Hardware Reset and Software Reset .....	533
15.3.2	Initialization after a Hardware Reset.....	536
15.3.3	Transmit Mode .....	539
15.3.4	Receive Mode .....	546
15.3.5	HCAN Sleep Mode .....	552
15.3.6	HCAN Halt Mode .....	554
15.3.7	Interrupt Interface.....	555
15.3.8	DMAC Interface .....	556
15.4	CAN Bus Interface .....	557
15.5	Usage Notes .....	558
 <b>Section 16 A/D Converter .....</b>		<b>559</b>
16.1	Overview.....	559
16.1.1	Features .....	559
16.1.2	Block Diagram.....	561
16.1.3	Pin Configuration .....	562
16.1.4	Register Configuration .....	564
16.2	Register Descriptions.....	565
16.2.1	A/D Data Registers 0 to 15 (ADDR0 to ADDR15) .....	565
16.2.2	A/D Control/Status Register 0 (ADCSR0).....	566
16.2.3	A/D Control Registers 0 and 1 (ADCR0, ADCR1) .....	570
16.2.4	A/D Control/Status Register 1 (ADCSR1).....	572
16.2.5	A/D Trigger Registers 0 and 1 (ADTRGR0, ADTRGR1).....	575
16.3	CPU Interface .....	576
16.4	Operation .....	577
16.4.1	Single Mode.....	577
16.4.2	Scan Mode.....	579
16.4.3	Analog Input Sampling and A/D Conversion Time .....	583
16.4.4	External Triggering of A/D Converter .....	585

16.4.5	A/D Converter Activation by ATU-II.....	586
16.5	Interrupt Sources and DMA Transfer Requests .....	586
16.6	Usage Notes .....	586
16.6.1	A/D conversion accuracy definitions .....	588
<b>Section 17 Advanced User Debugger (AUD) .....</b>		<b>591</b>
17.1	Overview.....	591
17.1.1	Features .....	591
17.1.2	Block Diagram.....	592
17.2	Pin Configuration .....	592
17.2.1	Pin Descriptions .....	593
17.3	Branch Trace Mode .....	595
17.3.1	Overview .....	595
17.3.2	Operation.....	595
17.4	RAM Monitor Mode.....	597
17.4.1	Overview .....	597
17.4.2	Communication Protocol.....	597
17.4.3	Operation .....	598
17.5	Usage Notes .....	599
17.5.1	Initialization.....	599
17.5.2	Operation in Software Standby Mode.....	599
17.5.3	ROM Area Writes .....	600
<b>Section 18 Pin Function Controller (PFC).....</b>		<b>601</b>
18.1	Overview.....	601
18.2	Register Configuration .....	606
18.3	Register Descriptions.....	607
18.3.1	Port A IO Register (PAIOR) .....	607
18.3.2	Port A Control Registers H and L (PACRH, PACRL) .....	607
18.3.3	Port B IO Register (PBIOR).....	612
18.3.4	Port B Control Registers H and L (PBCRH, PBCRL) .....	612
18.3.5	Port B Invert Register (PBIR) .....	618
18.3.6	Port C IO Register (PCIOR).....	619
18.3.7	Port C Control Register (PCCR) .....	620
18.3.8	Port D IO Register (PDIOR) .....	622
18.3.9	Port D Control Registers H and L (PDCRH, PDCRL) .....	623
18.3.10	Port E IO Register (PEIOR) .....	627
18.3.11	Port E Control Register (PECR).....	628
18.3.12	Port F IO Register (PFIOR).....	633
18.3.13	Port F Control Registers H and L (PFCRH, PFCRL) .....	634
18.3.14	Port G IO Register (PGIOR) .....	640
18.3.15	Port G Control Register (PGCR).....	641
18.3.16	Port H IO Register (PHIOR) .....	643

18.3.17	Port H Control Register (PHCR).....	644
18.3.18	Port J IO Register (PJIOR).....	650
18.3.19	Port J Control Registers H and L (PJCRH, PJCRL).....	651
18.3.20	Port K IO Register (PKIOR).....	655
18.3.21	Port K Control Registers H and L (PKCRH, PKCRL).....	656
18.3.22	Port K Invert Register (PKIR).....	660
Section 19	I/O Ports (I/O).....	661
19.1	Overview.....	661
19.2	Port A.....	662
19.2.1	Register Configuration.....	662
19.2.2	Port A Data Register (PADR).....	663
19.3	Port B.....	664
19.3.1	Register Configuration.....	664
19.3.2	Port B Data Register (PBDR).....	665
19.4	Port C.....	666
19.4.1	Register Configuration.....	666
19.4.2	Port C Data Register (PCDR).....	666
19.5	Port D.....	668
19.5.1	Register Configuration.....	668
19.5.2	Port D Data Register (PDDR).....	669
19.6	Port E.....	670
19.6.1	Register Configuration.....	670
19.6.2	Port E Data Register (PEDR).....	671
19.7	Port F.....	673
19.7.1	Register Configuration.....	673
19.7.2	Port F Data Register (PFDR).....	674
19.8	Port G.....	676
19.8.1	Register Configuration.....	676
19.8.2	Port G Data Register (PGDR).....	676
19.9	Port H.....	678
19.9.1	Register Configuration.....	679
19.9.2	Port H Data Register (PHDR).....	679
19.10	Port J.....	681
19.10.1	Register Configuration.....	681
19.10.2	Port J Data Register (PJDR).....	682
19.11	Port K.....	683
19.11.1	Register Configuration.....	683
19.11.2	Port K Data Register (PKDR).....	684
19.12	POD (Port Output Disable) Control.....	685
Section 20	ROM (SH7052F/SH7053F).....	687
20.1	Features.....	687

20.2	Overview.....	688
20.2.1	Block Diagram.....	688
20.2.2	Mode Transitions.....	689
20.2.3	On-Board Programming Modes.....	690
20.2.4	Flash Memory Emulation in RAM.....	692
20.2.5	Differences between Boot Mode and User Program Mode.....	693
20.2.6	Block Configuration.....	694
20.3	Pin Configuration.....	694
20.4	Register Configuration.....	695
20.5	Register Descriptions.....	696
20.5.1	Flash Memory Control Register 1 (FLMCR1).....	696
20.5.2	Flash Memory Control Register 2 (FLMCR2).....	698
20.5.3	Erase Block Register 1 (EBR1).....	699
20.5.4	Erase Block Register 2 (EBR2).....	699
20.5.5	RAM Emulation Register (RAMER).....	701
20.6	On-Board Programming Modes.....	703
20.6.1	Boot Mode.....	703
20.6.2	User Program Mode.....	708
20.7	Programming/Erasing Flash Memory.....	708
20.7.1	Program Mode.....	709
20.7.2	Program-Verify Mode.....	710
20.7.3	Erase Mode.....	713
20.7.4	Erase-Verify Mode.....	714
20.8	Protection.....	717
20.8.1	Hardware Protection.....	717
20.8.2	Software Protection.....	718
20.8.3	Error Protection.....	718
20.9	Flash Memory Emulation in RAM.....	720
20.10	Note on Flash Memory Programming/Erasing.....	722
20.11	Flash Memory Programmer Mode.....	722
20.11.1	Socket Adapter Pin Correspondence Diagram.....	723
20.11.2	Programmer Mode Operation.....	725
20.11.3	Memory Read Mode.....	726
20.11.4	Auto-Program Mode.....	729
20.11.5	Auto-Erase Mode.....	731
20.11.6	Status Read Mode.....	733
20.11.7	Status Polling.....	734
20.11.8	Programmer Mode Transition Time.....	734
20.11.9	Notes on Memory Programming.....	735
Section 21 ROM (SH7054F).....		737
21.1	Features.....	737
21.2	Overview.....	738

21.2.1	Block Diagram.....	738
21.2.2	Mode Transitions.....	739
21.2.3	On-Board Programming Modes .....	740
21.2.4	Flash Memory Emulation in RAM.....	742
21.2.5	Differences between Boot Mode and User Program Mode.....	743
21.2.6	Block Configuration .....	744
21.3	Pin Configuration .....	744
21.4	Register Configuration .....	745
21.5	Register Descriptions.....	746
21.5.1	Flash Memory Control Register 1 (FLMCR1).....	746
21.5.2	Flash Memory Control Register 2 (FLMCR2).....	748
21.5.3	Erase Block Register 1 (EBR1).....	749
21.5.4	Erase Block Register 2 (EBR2).....	749
21.5.5	RAM Emulation Register (RAMER) .....	751
21.6	On-Board Programming Modes .....	753
21.6.1	Boot Mode.....	753
21.6.2	User Program Mode .....	758
21.7	Programming/Erasing Flash Memory.....	759
21.7.1	Program Mode.....	759
21.7.2	Program-Verify Mode .....	760
21.7.3	Erase Mode.....	763
21.7.4	Erase-Verify Mode .....	764
21.8	Protection.....	767
21.8.1	Hardware Protection .....	767
21.8.2	Software Protection .....	768
21.8.3	Error Protection .....	768
21.9	Flash Memory Emulation in RAM.....	770
21.10	Note on Flash Memory Programming/Erasing.....	772
21.11	Flash Memory Programmer Mode .....	772
21.11.1	Socket Adapter Pin Correspondence Diagram .....	773
21.11.2	Programmer Mode Operation.....	775
21.11.3	Memory Read Mode.....	776
21.11.4	Auto-Program Mode .....	779
21.11.5	Auto-Erase Mode.....	781
21.11.6	Status Read Mode.....	783
21.11.7	Status Polling.....	784
21.11.8	Programmer Mode Transition Time.....	784
21.11.9	Notes on Memory Programming.....	785
	<b>Section 22 RAM.....</b>	<b>787</b>
22.1	Overview.....	787
22.2	Operation .....	789

Section 23	Power-Down State.....	791
23.1	Overview.....	791
23.1.1	Power-Down States .....	791
23.1.2	Pin Configuration .....	793
23.1.3	Related Registers .....	793
23.2	Register Descriptions.....	794
23.2.1	Standby Control Register (SBYCR) .....	794
23.2.2	System Control Register (SYSCR) .....	795
23.2.3	Module Standby Control Register (MSTCR).....	796
23.2.4	Notes on Register Access .....	797
23.3	Hardware Standby Mode .....	797
23.3.1	Transition to Hardware Standby Mode .....	797
23.3.2	Canceling Hardware Standby Mode .....	797
23.3.3	Hardware Standby Mode Timing .....	798
23.4	Software Standby Mode .....	798
23.4.1	Transition to Software Standby Mode.....	798
23.4.2	Canceling Software Standby Mode.....	800
23.4.3	Software Standby Mode Application Example .....	801
23.5	Sleep Mode.....	802
23.5.1	Transition to Sleep Mode .....	802
23.5.2	Canceling Sleep Mode.....	802
Section 24	Electrical Characteristics .....	803
24.1	Absolute Maximum Ratings.....	803
24.2	DC Characteristics .....	804
24.3	AC Characteristics .....	821
24.3.1	Power-On/Off Timing .....	821
24.3.2	Clock Timing.....	822
24.3.3	Control Signal Timing.....	824
24.3.4	Bus Timing .....	827
24.3.5	Advanced Timer Unit Timing and Advance Pulse Controller Timing .....	831
24.3.6	I/O Port Timing .....	833
24.3.7	Watchdog Timer Timing.....	834
24.3.8	Serial Communication Interface Timing.....	835
24.3.9	HCAN Timing.....	837
24.3.10	A/D Converter Timing .....	838
24.3.11	AUD Timing .....	840
24.3.12	UBC Trigger Timing .....	842
24.3.13	Measuring Conditions for AC Characteristics .....	843
24.4	A/D Converter Characteristics .....	844



Appendix A	On-Chip Supporting Module Registers.....	845
A.1	Address.....	845
A.2	Register States in Reset and Power-Down States.....	881
Appendix B	Pin States.....	887
Appendix C	Product Code Lineup.....	890
Appendix D	Package Dimensions.....	891



# Section 1 Overview

## 1.1 Features

The SH7052F/SH7053F/SH7054F is a single-chip RISC microcontroller that integrates a RISC CPU core using an original Hitachi architecture with peripheral functions required for system configuration.

The CPU has a RISC-type instruction set. Basic instructions can be executed in one state (one system clock cycle), which greatly improves instruction execution speed. In addition, the 32-bit internal architecture enhances data processing power. With this CPU, it has become possible to assemble low-cost, high-performance/high-functionality systems even for applications such as real-time control, which could not previously be handled by microcontrollers because of their high-speed processing requirements.

In addition, the SH7052F/SH7053F/SH7054F includes on-chip peripheral functions necessary for system configuration, such as ROM, RAM, a direct memory access controller (DMAC), timers, a serial communication interface (SCI), Hitachi controller area network (HCAN), A/D converter, interrupt controller (INTC), and I/O ports.

ROM and SRAM can be directly connected by means of an external memory access support function, greatly reducing system cost.

On-chip ROM is available as flash memory in the F-ZTAT™\* (Flexible Zero Turn Around Time) version. The flash memory can be programmed with a programmer that supports SH7052F/SH7053F/SH7054F programming, and can also be programmed and erased by software. This enables the chip to be programmed at the user site while mounted on a board.

The features of the SH7052F/SH7053F/SH7054F are summarized in table 1.1.

Note: \* F-ZTAT is a trademark of Hitachi, Ltd.

**Table 1.1 SH7052F/SH7053F/SH7054F Features**

<b>Item</b>	<b>Features</b>
CPU	<ul style="list-style-type: none"><li>• Maximum operating frequency: 40 MHz</li><li>• Original Hitachi SH-2 CPU</li><li>• 32-bit internal architecture</li><li>• General register machine<ul style="list-style-type: none"><li>— Sixteen 32-bit general registers</li><li>— Three 32-bit control registers</li><li>— Four 32-bit system registers</li></ul></li><li>• Instruction execution time: Basic instructions execute in one state (25 ns/instruction at 40 MHz operation)</li><li>• Address space: Architecture supports 4 Gbytes</li><li>• Five-stage pipeline</li></ul>
Operating states	<ul style="list-style-type: none"><li>• Operating modes<ul style="list-style-type: none"><li>— Single-chip mode</li><li>— 8/16-bit bus expanded mode<ul style="list-style-type: none"><li>• Mode with on-chip ROM</li><li>• Mode with no on-chip ROM</li></ul></li></ul></li><li>• Processing states<ul style="list-style-type: none"><li>— Reset state</li><li>— Program execution state</li><li>— Exception handling state</li><li>— Bus-released state</li><li>— Power-down state</li></ul></li><li>• Power-down state<ul style="list-style-type: none"><li>— Sleep mode</li><li>— Software standby mode</li><li>— Hardware standby mode</li><li>— Module standby</li></ul></li></ul>
Multiplier	<ul style="list-style-type: none"><li>• <math>32 \times 32 \rightarrow 64</math> multiply operations executed in two to four cycles</li><li>• <math>32 \times 32 + 64 \rightarrow 64</math> multiply-and-accumulate operations executed in two to four cycles</li></ul>

**Table 1.1 SH7052F/SH7053F/SH7054F Features (cont)**

<b>Item</b>	<b>Features</b>
Clock pulse generator (CPG/PLL)	<ul style="list-style-type: none"><li>• On-chip clock pulse generator (maximum operating frequency: 40 MHz)</li><li>• Independent generation of CPU system clock and peripheral clock for peripheral modules</li><li>• On-chip clock-multiplication PLL circuit (<math>\times 4</math>) Internal clock frequency range: 5 to 10 MHz</li></ul>
Interrupt controller (INTC)	<ul style="list-style-type: none"><li>• Five external interrupt pins (NMI, <math>\overline{\text{IRQ0}}</math> to <math>\overline{\text{IRQ3}}</math>)</li><li>• 109 internal interrupt sources (ATU-II <math>\times 75</math>, SCI <math>\times 20</math>, DMAC <math>\times 4</math>, A/D <math>\times 2</math>, WDT <math>\times 1</math>, UBC <math>\times 1</math>, CMT <math>\times 2</math>, HCAN <math>\times 4</math>)</li><li>• 16 programmable priority levels</li></ul>
User break controller (UBC)	<ul style="list-style-type: none"><li>• Requests an interrupt when the CPU or DMAC generates a bus cycle with specified conditions (interrupt can also be masked)</li><li>• Trigger pulse output (<math>\overline{\text{UBCTR}}\overline{\text{G}}</math>) on break condition — Selection of trigger pulse width (<math>\phi \times 1, \times 4, \times 8, \times 16</math>)</li><li>• Simplifies configuration of an on-chip debugger</li></ul>
Bus state controller (BSC)	<ul style="list-style-type: none"><li>• Supports external memory access (SRAM and ROM directly connectable) — 8/16-bit bus space</li><li>• 3.3 V bus interface</li><li>• 16 MB address space divided into four areas, with the following parameters settable for each area:<ul style="list-style-type: none"><li>— Bus size (8 or 16 bits)</li><li>— Number of wait cycles</li><li>— Chip select signals (<math>\overline{\text{CS0}}</math> to <math>\overline{\text{CS3}}</math>) output for each area</li></ul></li><li>• Wait cycles can be inserted using an external <math>\overline{\text{WAIT}}</math> signal</li><li>• External access in minimum of two cycles</li><li>• Provision for idle cycle insertion to prevent bus collisions</li></ul>

**Table 1.1 SH7052F/SH7053F/SH7054F Features (cont)**

<b>Item</b>	<b>Features</b>
Direct memory access controller (DMAC) (4 channels)	<ul style="list-style-type: none"><li>• DMA transfer possible for the following devices:<ul style="list-style-type: none"><li>— External memory, on-chip memory, on-chip peripheral modules (excluding DMAC, UBC, BSC)</li></ul></li><li>• DMA transfer requests by on-chip modules<ul style="list-style-type: none"><li>— SCI, A/D converter, ATU-II, HCAN</li></ul></li><li>• Cycle steal or burst mode transfer</li><li>• Dual address mode<ul style="list-style-type: none"><li>— Direct transfer mode</li><li>— Indirect transfer mode (channel 3 only)</li></ul></li><li>• Address reload function (channel 2 only)</li><li>• Transfer data width: Byte/word/longword</li></ul>
Advanced timer unit-II (ATU-II)	<ul style="list-style-type: none"><li>• Maximum 63 inputs or outputs can be processed<ul style="list-style-type: none"><li>— Four 32-bit input capture inputs</li><li>— Twenty-eight 16-bit input capture inputs/output compare outputs</li><li>— Sixteen 16-bit one-shot pulse outputs</li><li>— Eight 16-bit PWM outputs</li><li>— Six 8-bit event counters</li><li>— One gap detection function</li></ul></li><li>• I/O pin output inversion function</li></ul>
Advanced pulse controller (APC)	<ul style="list-style-type: none"><li>• Maximum eight pulse outputs on reception of ATU-II (channel 11) compare-match signal</li></ul>
Watchdog timer (WDT) (1 channel)	<ul style="list-style-type: none"><li>• Can be switched between watchdog timer and interval timer function</li><li>• Internal reset, external signal, or interrupt generated by counter overflow</li><li>• Two kinds of internal reset<ul style="list-style-type: none"><li>— Power-on reset</li><li>— Manual reset</li></ul></li></ul>
Compare-match timer (CMT) (2 channels)	<ul style="list-style-type: none"><li>• Selection of 4 counter input clocks</li><li>• A compare-match interrupt can be requested independently for each channel</li></ul>

**Table 1.1 SH7052F/SH7053F/SH7054F Features (cont)**

<b>Item</b>	<b>Features</b>
Serial communication interface (SCI) (5 channels)	<ul style="list-style-type: none"> <li>• Selection of asynchronous or synchronous mode</li> <li>• Simultaneous transmission/reception (full-duplex) capability</li> <li>• Serial data communication possible between multiple processors (asynchronous mode)</li> <li>• Clock inversion function</li> <li>• LSB-/MSB-first selection function for transmission</li> </ul>
Hitachi controller area network (HCAN) (1 channel)	<ul style="list-style-type: none"> <li>• CAN version: Bosch 2.0B active compatible</li> <li>• Buffer size (per channel): Transmit/receive × 15, receive-only × 1</li> <li>• Receive message filtering capability</li> </ul>
A/D converter	<ul style="list-style-type: none"> <li>• Sixteen channels</li> <li>• Two sample-and-hold circuits <ul style="list-style-type: none"> <li>— Independent operation of 12 channels × 1 and 4 channels × 1</li> </ul> </li> <li>• Selection of two conversion modes <ul style="list-style-type: none"> <li>— Single conversion mode</li> <li>— Scan mode <ul style="list-style-type: none"> <li>• Continuous scan mode</li> <li>• Single-cycle scan mode</li> </ul> </li> </ul> </li> <li>• Can be activated by external trigger or ATU-II compare-match</li> <li>• 10-bit resolution</li> <li>• Accuracy: ±2 LSB</li> </ul>
Advanced user debugger (AUD)	<ul style="list-style-type: none"> <li>• Eight dedicated pins</li> <li>• RAM monitor mode <ul style="list-style-type: none"> <li>— Data input/output frequency: <math>\phi/4</math> or less</li> <li>— Possible to read/write to a module connected to the internal/external bus</li> </ul> </li> <li>• Branch address output mode</li> </ul>
I/O ports (including timer I/O pins, address and data buses)	<ul style="list-style-type: none"> <li>• Dual-function input/output pins: 135</li> <li>• Schmitt input pins: <math>\overline{\text{NMI}}</math>, <math>\overline{\text{IRQ}}</math>, <math>\overline{\text{RES}}</math>, <math>\overline{\text{HSTBY}}</math>, FWE, TCLK, IC, IC/OC, SCK, <math>\overline{\text{ADTRG}}</math></li> <li>• Input port protection</li> </ul>

**Table 1.1 SH7052F/SH7053F/SH7054F Features (cont)**

<b>Item</b>	<b>Features</b>	<b>Product</b>		
		<b>SH7052F</b>	<b>SH7053F</b>	<b>SH7054F</b>
On-chip memory	<b>Memory</b>			
	Flash memory	256 kB	256 kB	384 kB
	RAM	12 kB	16 kB	16 kB



# 1.2 Block Diagram

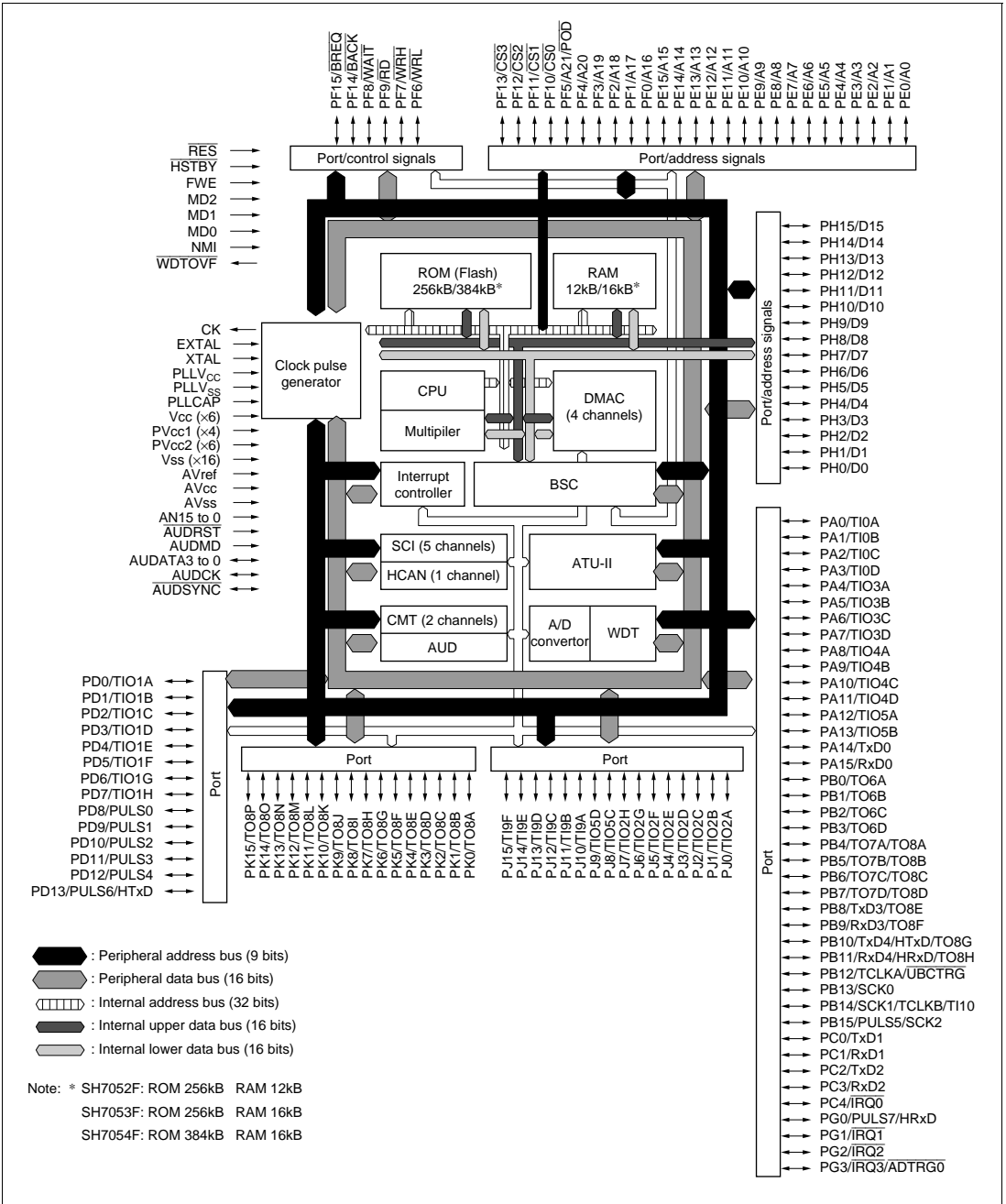


Figure 1.1 Block Diagram

# 1.3 Pin Description

## 1.3.1 Pin Arrangement

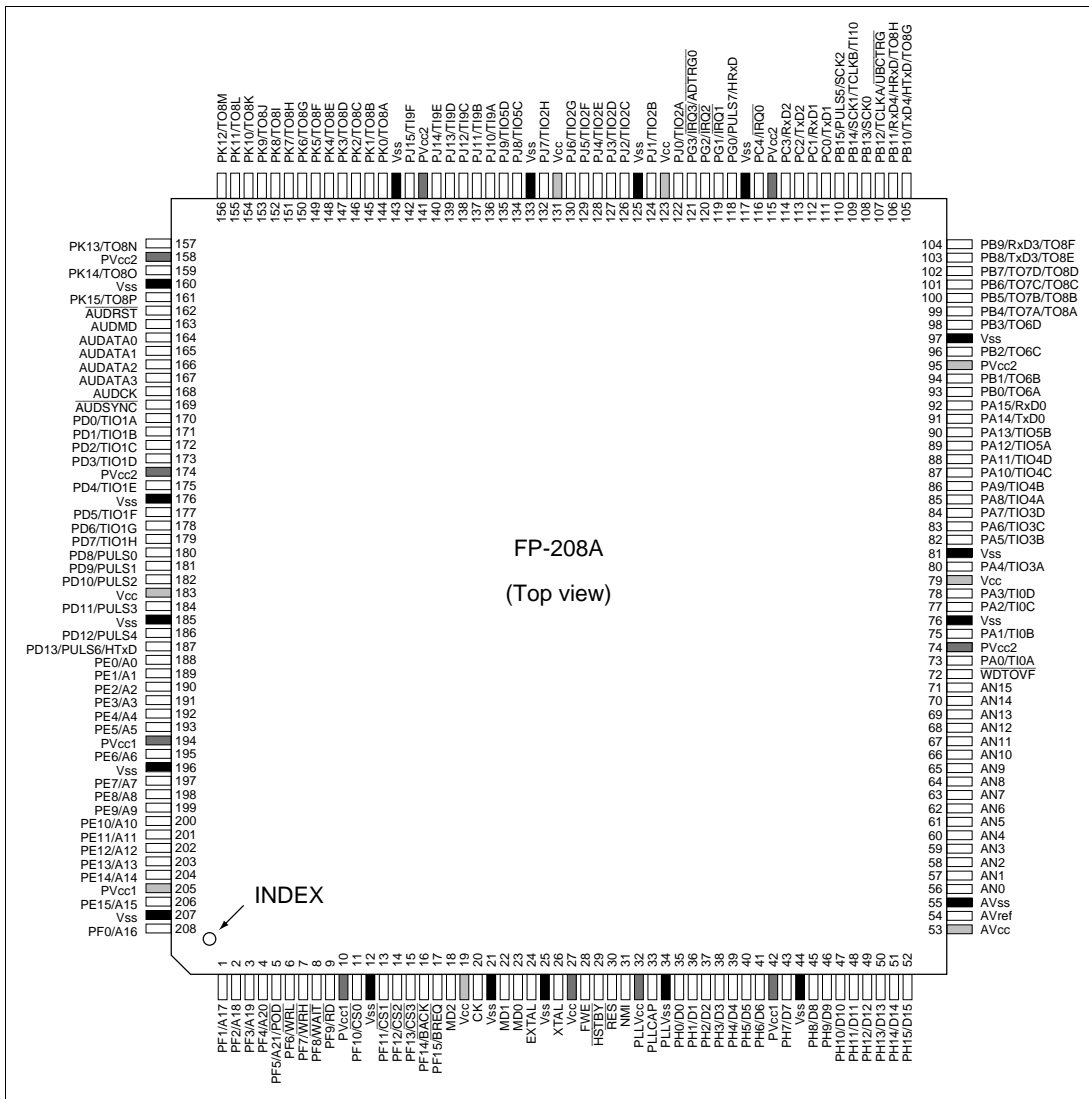


Figure 1.2 Pin Arrangement

### 1.3.2 Pin Functions

Table 1.2 summarizes the pin functions.

**Table 1.2 Pin Functions**

Type	Symbol	Pin No.	I/O	Name	Function
Power supply	$V_{CC}$	19, 27, 79, 123, 131, 183	Input	Power supply	Power supply for chip-internal and system ports (RES, MD2 to MD0, FWE, HSTBY, NMI, CK, EXTAL, XTAL). Connect all $V_{CC}$ pins to the system power supply. The chip will not operate if there are any open pins.
	$PV_{CC1}$	10, 42, 194, 205	Input	Port power supply 1	Power supply for bus ports (ports E, F, and H). Connect all $PV_{CC1}$ pins to the system bus power supply. The chip will not operate if there are any open pins.
	$PV_{CC2}$	74, 95, 115, 141, 158, 174	Input	Port power supply 2	Power supply for peripheral module ports (ports A, B, C, D, G, J, K, the AUD, and WDTOVF). Connect all $PV_{CC2}$ pins to the system peripheral module power supply. The chip will not operate if there are any open pins.
	$V_{SS}$	12, 21, 25, 44, 76, 81, 97, 117, 125, 133, 143, 160, 176, 185, 196, 207	Input	Ground	For connection to ground. Connect all $V_{SS}$ pins to the system ground. The chip will not operate if there are any open pins.
Flash memory	FWE	28	Input	Flash write enable	Connected to ground in normal operation. Apply $V_{CC}$ during on-board programming.

**Table 1.2 Pin Functions (cont)**

Type	Symbol	Pin No.	I/O	Name	Function
Clock	PLL <sub>CC</sub>	32	Input	PLL power supply	On-chip PLL oscillator power supply. For power supply connection, see section 4, Clock Pulse Generator.
	PLL <sub>SS</sub>	34	Input	PLL ground	On-chip PLL oscillator ground. For power supply connection, see section 4, Clock Pulse Generator.
	PLLCAP	33	Input	PLL capacitance	On-chip PLL oscillator external capacitance connection pin. For external capacitance connection, see section 4, Clock Pulse Generator.
	EXTAL	24	Input	External clock	For connection to a crystal resonator. An external clock source can also be connected to the EXTAL pin.
	XTAL	26	Input	Crystal	For connection to a crystal resonator.
	CK	20	Output	System clock	Supplies the system clock to peripheral devices.
System control	$\overline{\text{RES}}$	30	Input	Power-on reset	Executes a power-on reset when driven low.
	$\overline{\text{WDTOVF}}$	72	Output	Watchdog timer overflow	WDT overflow output signal.
	$\overline{\text{BREQ}}$	17	Input	Bus request	Driven low when an external device requests the bus.
	$\overline{\text{BACK}}$	16	Output	Bus request acknowledge	Indicates that the bus has been granted to an external device. The device that output the $\overline{\text{BREQ}}$ signal recognizes that the bus has been acquired when it receives the $\overline{\text{BACK}}$ signal.

**Table 1.2 Pin Functions (cont)**

Type	Symbol	Pin No.	I/O	Name	Function
Operating mode control	MD0 to MD2	18, 22, 23	Input	Mode setting	These pins determine the operating mode. Do not change the input values during operation.
	$\overline{\text{HSTBY}}$	29	Input	Hardware standby	When driven low, this pin forces a transition to hardware standby mode.
Interrupts	NMI	31	Input	Nonmaskable interrupt	Nonmaskable interrupt request pin. Acceptance on the rising edge or falling edge can be selected.
	$\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$	116, 119, 120, 121	Input	Interrupt requests 0 to 3	Maskable interrupt request pins. Level input or edge input can be selected.
Address bus	A0 to A21	1 to 5, 188 to 193, 195, 197 to 204, 206, 208	Output	Address bus	Address output pins.
Data bus	D0 to D15	35 to 41, 43, 45 to 52	Input/output	Data bus	16-bit bidirectional data bus pins.
Bus control	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	11, 13 to 15	Output	Chip select 0 to 3	Chip select signals for external memory or devices.
	$\overline{\text{RD}}$	9	Output	Read	Indicates reading from an external device.
	$\overline{\text{WRH}}$	7	Output	Upper write	Indicates writing of the upper 8 bits of external data.
	$\overline{\text{WRL}}$	6	Output	Lower write	Indicates writing of the lower 8 bits of external data.
	$\overline{\text{WAIT}}$	8	Input	Wait	Input for wait cycle insertion in bus cycles during external space access.

**Table 1.2 Pin Functions (cont)**

Type	Symbol	Pin No.	I/O	Name	Function
Advanced timer unit-II (ATU-II)	TCLKA TCLKB	107, 109	Input	ATU-II timer clock input	ATU-II counter external clock Input pins.
	TIOA to TIOD	73, 75, 77, 78	Input	ATU-II input capture (channel 0)	Channel 0 input capture input pins.
	TIO1A to TIO1H	170 to 173, 175, 177 to 179	Input/output	ATU-II input capture/output compare (channel 1)	Channel 1 input capture input/output compare output pins.
	TIO2A to TIO2H	122, 124, 126 to 130, 132	Input/output	ATU-II input capture/output compare (channel 2)	Channel 2 input capture input/output compare output pins.
	TIO3A to TIO3D	80, 82 to 84	Input/output	ATU-II input capture/output compare/PWM output (channel 3)	Channel 3 input capture input/output compare/PWM output pins.
	TIO4A to TIO4D	85 to 88	Input/output	ATU-II input capture/output compare/PWM output (channel 4)	Channel 4 input capture input/output compare/PWM output pins.
	TIO5A to TIO5D	89, 90, 134, 135	Input/output	ATU-II input capture/output compare/PWM output (channel 5)	Channel 5 input capture input/output compare/PWM output pins.
	TO6A to TO6D	93, 94, 96, 98	Output	ATU-II PWM output (channel 6)	Channel 6 PWM output pins.
	TO7A to TO7D	99 to 102	Output	ATU-II PWM output (channel 7)	Channel 7 PWM output pins.
TO8A to TO8P	99 to 106, 144 to 157, 159, 161	Output	ATU-II one-shot pulse (channel 8)	Channel 8 down-counter one-shot pulse output pins.	

**Table 1.2 Pin Functions (cont)**

Type	Symbol	Pin No.	I/O	Name	Function
Advanced timer unit-II (ATU-II)	TI9A to TI9F	136 to 140, 142	Input	ATU-II event input (channel 9)	Channel 9 event counter input pins.
	TI10	109	Input	ATU-II multiplied clock generation (channel 10)	Channel 10 external clock input pin.
Advanced pulse controller (APC)	PULS0 to PULS7	110, 118, 180 to 182, 184, 186, 187	Output	APC pulse outputs 0 to 7	APC pulse output pins.
Serial communication interface (SCI)	TxD0 to TxD4	91, 103, 105, 111, 113	Output	Transmit data (channels 0 to 4)	SCI0 to SCI4 transmit data output pins.
	RxD0 to RxD4	92, 104, 106, 112, 114	Input	Receive data (channels 0 to 4)	SCI0 to SCI4 receive data input pins.
	SCK0 to SCK2	108, 109, 110	Input/output	Serial clock (channels 0 to 2)	SCI0 to SCI2 clock input/output pins.
Hitachi controller area network (HCAN)	HTxD	105, 187	Output	Transmit data	CAN bus transmit data output pins.
	HRxD	106, 118	input	Receive data	CAN bus receive data input pins.
A/D converter	AV <sub>CC</sub>	53	Input	Analog power supply	A/D converter power supply.
	AV <sub>SS</sub>	55	Input	Analog ground	A/D converter power supply.
	AV <sub>ref</sub>	54	Input	Analog reference power supply	Analog reference power supply input pins.
	AN0 to AN15	56 to 71	Input	Analog input	Analog signal input pins.
	ADTRG0	121	Input	A/D conversion trigger input	External trigger input pins for starting A/D conversion.

**Table 1.2 Pin Functions (cont)**

Type	Symbol	Pin No.	I/O	Name	Function
User break controller (UBC)	$\overline{\text{UBCTR}}\overline{\text{G}}$	107	Output	User break trigger output	UBC condition match trigger output pin.
Advanced user debugger (AUD)	AUDATA0 to AUDATA3	164 to 167	Input/output	AUD data	Realtime trace mode: Branch destination address output pins. RAM monitor mode: Monitor address input / data input/output pins.
	$\overline{\text{AUDRST}}$	162	Input	AUD reset	Reset signal input pin.
	AUDMD	163	Input	AUD mode	Mode select signal input pin. Realtime trace mode: Low RAM monitor mode: High
	AUDCK	168	Input/output	AUD clock	Realtime trace mode: Serial clock output pin. RAM monitor mode: Serial clock input pin.
	$\overline{\text{AUDSYNC}}$	169	Input/output	AUD synchronization signal	Realtime trace mode: Data start position identification signal output pin. RAM monitor mode: Data start position identification signal input pin.
I/O ports	$\overline{\text{POD}}$	5	Input	Port output disable	Input pin for port pin drive control when general port is set for output.
	PA0 to PA15	73, 75, 77, 78, 80, 82 to 92	Input/output	Port A	General input/output port pins. Input or output can be specified bit by bit.



**Table 1.2 Pin Functions (cont)**

<b>Type</b>	<b>Symbol</b>	<b>Pin No.</b>	<b>I/O</b>	<b>Name</b>	<b>Function</b>
I/O ports	PB0 to PB15	93, 94, 96, 98 to 110	Input/ output	Port B	General input/output port pins. Input or output can be specified bit by bit.
	PC0 to PC4	111 to 114, 116	Input/ output	Port C	General input/output port pins. Input or output can be specified bit by bit.
	PD0 to PD13	170 to 173, 175, 177 to 182, 184, 186, 187	Input/ output	Port D	General input/output port pins. Input or output can be specified bit by bit.
	PE0 to PE15	188 to 193, 195, 197 to 204, 206	Input/ output	Port E	General input/output port pins. Input or output can be specified bit by bit.
	PF0 to PF15	1 to 9, 11, 13 to 17, 208	Input/ output	Port F	General input/output port pins. Input or output can be specified bit by bit.
	PG0 to PG3	118 to 121	Input/ output	Port G	General input/output port pins. Input or output can be specified bit by bit.
	PH0 to PH15	35 to 41, 43, 45 to 52	Input/ output	Port H	General input/output port pins. Input or output can be specified bit by bit.
	PJ0 to PJ15	122, 124, 126 to 130, 132, 134 to 140, 142	Input/ output	Port J	General input/output port pins. Input or output can be specified bit by bit.
	PK0 to PK15	144 to 157, 159, 161	Input/ output	Port K	General input/output port pins. Input or output can be specified bit by bit.

### 1.3.3 Pin Assignments

**Table 1.3 Pin Assignments**

Pin No.	MCU Mode	Programmer Mode
1	PF1/A17	A17
2	PF2/A18	A18
3	PF3/A19	N.C
4	PF4/A20	N.C
5	PF5/A21/ $\overline{\text{POD}}$	N.C
6	PF6/ $\overline{\text{WRL}}$	N.C
7	PF7/ $\overline{\text{WRH}}$	N.C.
8	PF8/ $\overline{\text{WAIT}}$	N.C.
9	PF9/ $\overline{\text{RD}}$	N.C.
10	PVcc1	Vcc
11	PF10/ $\overline{\text{CS0}}$	N.C.
12	Vss	Vss
13	PF11/ $\overline{\text{CS1}}$	Vcc
14	PF12/ $\overline{\text{CS2}}$	Vcc
15	PF13/ $\overline{\text{CS3}}$	Vss
16	PF14/ $\overline{\text{BACK}}$	N.C.
17	PF15/ $\overline{\text{BREQ}}$	Vcc
18	MD2	Vss
19	Vcc	Vcc
20	CK	N.C.
21	Vss	Vss
22	MD1	Vcc
23	MD0	Vcc
24	EXTAL	EXTAL
25	Vss	Vss
26	XTAL	XTAL
27	Vcc	Vcc
28	FWE	FWE
29	$\overline{\text{HSTBY}}$	Vcc
30	$\overline{\text{RES}}$	$\overline{\text{RES}}$

**Table 1.3 Pin Assignments (cont)**

<b>Pin No.</b>	<b>MCU Mode</b>	<b>Programmer Mode</b>
31	NMI	Vss
32	PLLVcc	PLLVcc
33	PLLCAP	PLLCAP
34	PLLVss	PLLVss
35	PH0/D0	D0
36	PH1/D1	D1
37	PH2/D2	D2
38	PH3/D3	D3
39	PH4/D4	D4
40	PH5/D5	D5
41	PH6/D6	D6
42	PVcc1	Vcc
43	PH7/D7	D7
44	Vss	Vss
45	PH8/D8	N.C.
46	PH9/D9	N.C.
47	PH10/D10	N.C.
48	PH11/D11	N.C.
49	PH12/D12	N.C.
50	PH13/D13	N.C.
51	PH14/D14	N.C.
52	PH15/D15	N.C.
53	AVcc	Vcc
54	AVref	Vcc
55	AVss	Vss
56	AN0	N.C.
57	AN1	N.C.
58	AN2	N.C.
59	AN3	N.C.
60	AN4	N.C.
61	AN5	N.C.

**Table 1.3 Pin Assignments (cont)**

<b>Pin No.</b>	<b>MCU Mode</b>	<b>Programmer Mode</b>
62	AN6	N.C.
63	AN7	N.C.
64	AN8	N.C.
65	AN9	N.C.
66	AN10	N.C.
67	AN11	N.C.
68	AN12	N.C.
69	AN13	N.C.
70	AN14	N.C.
71	AN15	N.C.
72	WDTOVF	N.C.
73	PA0/TIOA	N.C.
74	PVcc2	Vcc
75	PA1/TIOB	N.C.
76	Vss	Vss
77	PA2/TIOC	N.C.
78	PA3/TIOD	N.C.
79	Vcc	Vcc
80	PA4/TIO3A	N.C.
81	Vss	Vss
82	PA5/TIO3B	N.C.
83	PA6/TIO3C	N.C.
84	PA7/TIO3D	N.C.
85	PA8/TIO4A	N.C.
86	PA9/TIO4B	N.C.
87	PA10/TIO4C	N.C.
88	PA11/TIO4D	N.C.
89	PA12/TIO5A	N.C.
90	PA13/TIO5B	N.C.
91	PA14/TxD0	N.C.
92	PA15/RxD0	N.C.

**Table 1.3 Pin Assignments (cont)**

<b>Pin No.</b>	<b>MCU Mode</b>	<b>Programmer Mode</b>
93	PB0/TO6A	N.C.
94	PB1/TO6B	N.C.
95	PVcc2	Vcc
96	PB2/TO6C	N.C.
97	Vss	Vss
98	PB3/TO6D	N.C.
99	PB4/TO7A/TO8A	N.C.
100	PB5/TO7B/TO8B	N.C.
101	PB6/TO7C/TO8C	N.C.
102	PB7/TO7D/TO8D	N.C.
103	PB8/TxD3/TO8E	N.C.
104	PB9/RxD3/TO8F	N.C.
105	PB10/TxD4/HTxD/TO8G	N.C.
106	PB11/RxD4/HRxD/TO8H	N.C.
107	PB12/TCLKA/UBCTRG	N.C.
108	PB13/SCK0	N.C.
109	PB14/SCK1/TCLKB/TI10	N.C.
110	PB15/PULS5/SCK2	N.C.
111	PC0/TxD1	N.C.
112	PC1/RxD1	N.C.
113	PC2/TxD2	N.C.
114	PC3/RxD2	N.C.
115	PVcc2	Vcc
116	PC4/IRQ0	N.C.
117	Vss	Vss
118	PG0/PULS7/HRxD	N.C.
119	PG1/IRQ1	CE
120	PG2/IRQ2	WE
121	PG3/IRQ3/ADTRG0	OE
122	PJ0/TIO2A	N.C.
123	Vcc	Vcc

**Table 1.3 Pin Assignments (cont)**

<b>Pin No.</b>	<b>MCU Mode</b>	<b>Programmer Mode</b>
124	PJ1/TIO2B	N.C.
125	Vss	Vss
126	PJ2/TIO2C	N.C.
127	PJ3/TIO2D	N.C.
128	PJ4/TIO2E	N.C.
129	PJ5/TIO2F	N.C.
130	PJ6/TIO2G	N.C.
131	Vcc	Vcc
132	PJ7/TIO2H	N.C.
133	Vss	Vss
134	PJ8/TIO5C	N.C.
135	PJ9/TIO5D	N.C.
136	PJ10/TI9A	N.C.
137	PJ11/TI9B	N.C.
138	PJ12/TI9C	N.C.
139	PJ13/TI9D	N.C.
140	PJ14/TI9E	N.C.
141	PVcc2	Vcc
142	PJ15/TI9F	N.C.
143	Vss	Vss
144	PK0/TO8A	N.C.
145	PK1/TO8B	N.C.
146	PK2/TO8C	N.C.
147	PK3/TO8D	N.C.
148	PK4/TO8E	N.C.
149	PK5/TO8F	N.C.
150	PK6/TO8G	N.C.
151	PK7/TO8H	N.C.
152	PK8/TO8I	N.C.
153	PK9/TO8J	N.C.
154	PK10/TO8K	N.C.

**Table 1.3 Pin Assignments (cont)**

<b>Pin No.</b>	<b>MCU Mode</b>	<b>Programmer Mode</b>
155	PK11/TO8L	N.C.
156	PK12/TO8M	N.C.
157	PK13/TO8N	N.C.
158	PVcc2	Vcc
159	PK14/TO8O	N.C.
160	Vss	Vss
161	PK15/TO8P	N.C.
162	$\overline{\text{AUDRST}}$	N.C.
163	AUDMD	N.C.
164	AUDATA0	N.C.
165	AUDATA1	N.C.
166	AUDATA2	N.C.
167	AUDATA3	N.C.
168	AUDCK	N.C.
169	$\overline{\text{AUDSYNC}}$	N.C.
170	PD0/TIO1A	N.C.
171	PD1/TIO1B	N.C.
172	PD2/TIO1C	N.C.
173	PD3/TIO1D	N.C.
174	PVcc2	Vcc
175	PD4/TIO1E	N.C.
176	Vss	Vss
177	PD5/TIO1F	N.C.
178	PD6/TIO1G	N.C.
179	PD7/TIO1H	N.C.
180	PD8/PULS0	N.C.
181	PD9/PULS1	N.C.
182	PD10/PULS2	N.C.
183	Vcc	Vcc
184	PD11/PULS3	N.C.
185	Vss	Vss

**Table 1.3 Pin Assignments (cont)**

<b>Pin No.</b>	<b>MCU Mode</b>	<b>Programmer Mode</b>
186	PD12/PULS4	N.C.
187	PD13/PULS6/HTxD	N.C.
188	PE0/A0	A0
189	PE1/A1	A1
190	PE2/A2	A2
191	PE3/A3	A3
192	PE4/A4	A4
193	PE5/A5	A5
194	PVcc1	Vcc
195	PE6/A6	A6
196	Vss	Vss
197	PE7/A7	A7
198	PE8/A8	A8
199	PE9/A9	A9
200	PE10/A10	A10
201	PE11/A11	A11
202	PE12/A12	A12
203	PE13/A13	A13
204	PE14/A14	A14
205	PVcc1	Vcc
206	PE15/A15	A15
207	Vss	Vss
208	PF0/A16	A16



# Section 2 CPU

## 2.1 Register Configuration

The register set consists of sixteen 32-bit general registers, three 32-bit control registers and four 32-bit system registers.

### 2.1.1 General Registers (Rn)

The sixteen 32-bit general registers (Rn) are numbered R0 to R15. General registers are used for data processing and address calculation. R0 is also used as an index register. Several instructions have R0 fixed as their only usable register. R15 is used as the hardware stack pointer (SP). Saving and recovering the status register (SR) and program counter (PC) in exception processing is accomplished by referencing the stack using R15. Figure 2.1 shows the general registers.

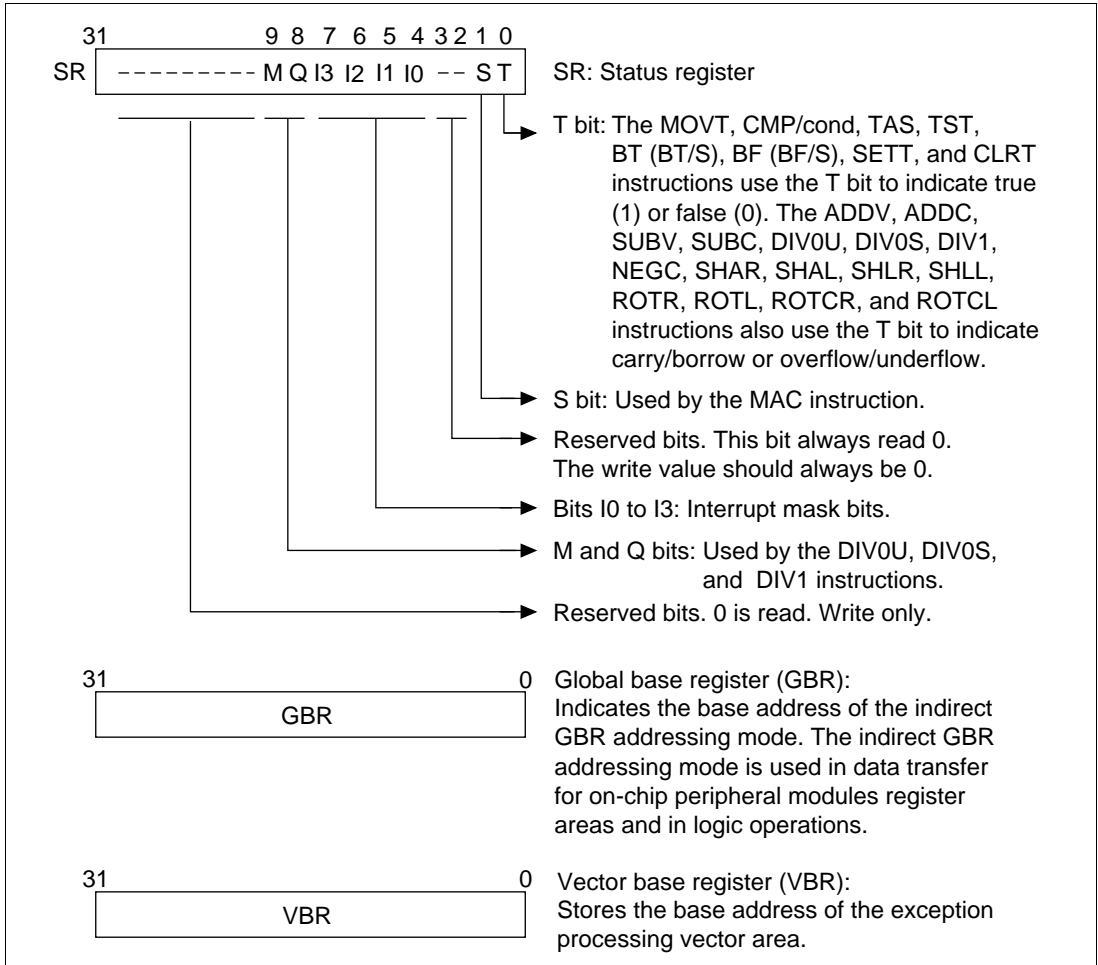
31		0
	R0*1	
	R1	
	R2	
	R3	
	R4	
	R5	
	R6	
	R7	
	R8	
	R9	
	R10	
	R11	
	R12	
	R13	
	R14	
	R15, SP (hardware stack pointer)*2	

- Notes:
1. R0 functions as an index register in the indirect indexed register addressing mode and indirect indexed GBR addressing mode. In some instructions, R0 functions as a fixed source register or destination register.
  2. R15 functions as a hardware stack pointer (SP) during exception processing.

**Figure 2.1 General Registers**

## 2.1.2 Control Registers

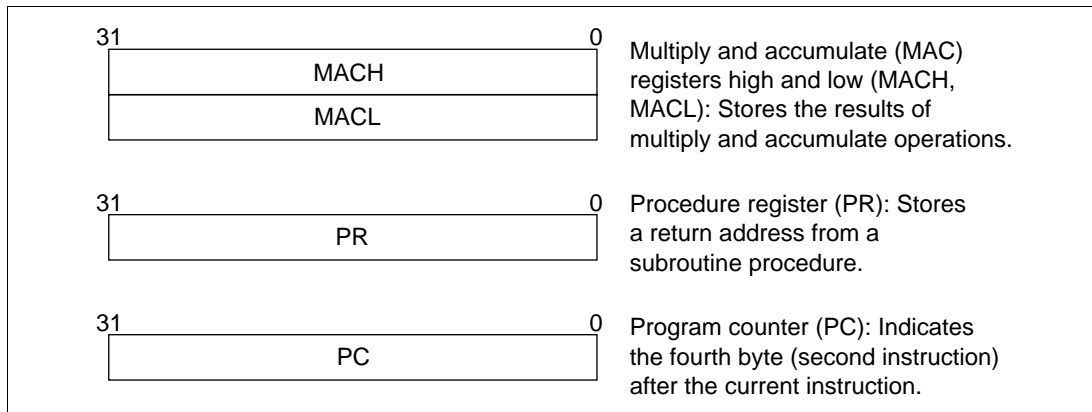
The 32-bit control registers consist of the 32-bit status register (SR), global base register (GBR), and vector base register (VBR). The status register indicates processing states. The global base register functions as a base address for the indirect GBR addressing mode to transfer data to the registers of on-chip peripheral modules. The vector base register functions as the base address of the exception processing vector area (including interrupts). Figure 2.2 shows a control register.



**Figure 2.2 Control Registers**

### 2.1.3 System Registers

System registers consist of four 32-bit registers: high and low multiply and accumulate registers (MACH and MACL), the procedure register (PR), and the program counter (PC). The multiply and accumulate registers store the results of multiply and accumulate operations. The procedure register stores the return address from the subroutine procedure. The program counter stores program addresses to control the flow of the processing. Figure 2.3 shows a system register.



**Figure 2.3 System Registers**

### 2.1.4 Initial Values of Registers

Table 2.1 lists the values of the registers after reset.

**Table 2.1 Initial Values of Registers**

Classification	Register	Initial Value
General registers	R0 to R14	Undefined
	R15 (SP)	Value of the stack pointer in the vector address table
Control registers	SR	Bits I3 to I0 are 1111 (H'F), reserved bits are 0, and other bits are undefined
	GBR	Undefined
	VBR	H'00000000
System registers	MACH, MACL, PR	Undefined
	PC	Value of the program counter in the vector address table

## 2.2 Data Formats

### 2.2.1 Data Format in Registers

Register operands are always longwords (32 bits). When the memory operand is only a byte (8 bits) or a word (16 bits), it is sign-extended into a longword when loaded into a register (figure 2.4).

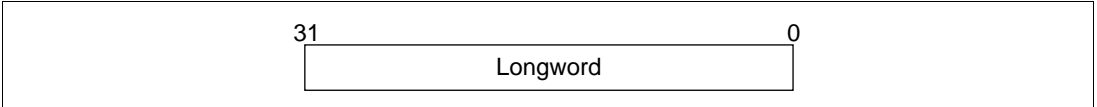


Figure 2.4 Longword Operand

### 2.2.2 Data Format in Memory

Memory data formats are classified into bytes, words, and longwords. Byte data can be located at any address, but word data must begin at address  $2n$  and longword data at address  $4n$ . An address error will occur if access is attempted beginning at an address other than these boundaries. In such cases, the data accessed cannot be guaranteed. The hardware stack area, referred to by the hardware stack pointer (SP, R15), uses only longword data starting from address  $4n$  because this area holds the program counter and status register (figure 2.5).

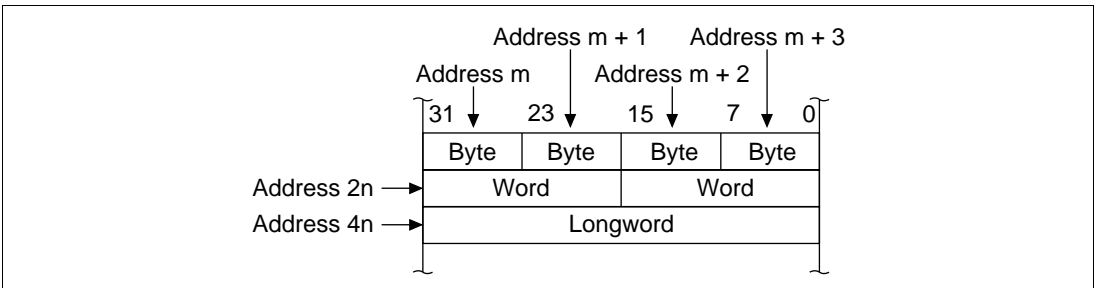


Figure 2.5 Byte, Word, and Longword Alignment

### 2.2.3 Immediate Data Format

Byte (8-bit) immediate data resides in an instruction code. Immediate data accessed by the MOV, ADD, and CMP/EQ instructions is sign-extended and handled in registers as longword data. Immediate data accessed by the TST, AND, OR, and XOR instructions is zero-extended and handled as longword data. Consequently, AND instructions with immediate data always clear the upper 24 bits of the destination register.

Word or longword immediate data is not located in the instruction code, but instead is stored in a memory table. An immediate data transfer instruction (MOV) accesses the memory table using the PC relative addressing mode with displacement.

## 2.3 Instruction Features

### 2.3.1 RISC-Type Instruction Set

All instructions are RISC type. This section details their functions.

**16-Bit Fixed Length:** All instructions are 16 bits long, increasing program code efficiency.

**One Instruction per Cycle:** The microprocessor can execute basic instructions in one cycle using the pipeline system. Instructions are executed in 25 ns at 40 MHz.

**Data Length:** Longword is the standard data length for all operations. Memory can be accessed in bytes, words, or longwords. Byte or word data accessed from memory is sign-extended and handled as longword data. Immediate data is sign-extended for arithmetic operations or zero-extended for logic operations. It also is handled as longword data (table 2.2).

**Table 2.2 Sign Extension of Word Data**

SH7052F/SH7053F/SH7054F CPU		Description	Example of Conventional CPU
MOV.W	@(disp,PC),R1	Data is sign-extended to 32 bits, and R1 becomes H'00001234. It is next operated upon by an ADD instruction.	ADD.W #H'1234,R0
ADD	R1,R0 .....		
.DATA.W	H'1234		

Note: @(disp, PC) accesses the immediate data.

**Load-Store Architecture:** Basic operations are executed between registers. For operations that involve memory access, data is loaded to the registers and executed (load-store architecture). Instructions such as AND that manipulate bits, however, are executed directly in memory.

**Delayed Branch Instructions:** Unconditional branch instructions are delayed branch instructions. With a delayed branch instruction, the branch is taken after execution of the instruction following the delayed branch instruction (table 2.3). This reduces pipeline disruption when branching. There are two types of conditional branch instructions: delayed branch instructions and ordinary branch instructions.

**Table 2.3 Delayed Branch Instructions****SH7052F/SH7053F/SH7054F**

CPU		Description	Example of Conventional CPU	
BRA	TRGET	Executes an ADD before branching to TRGET	ADD.W	R1,R0
ADD	R1,R0		BRA	TRGET

**Multiplication/Accumulation Operation:** 16-bit  $\times$  16-bit  $\rightarrow$  32-bit multiplication operations are executed in one to two cycles. 16-bit  $\times$  16-bit + 64-bit  $\rightarrow$  64-bit multiplication/accumulation operations are executed in two to three cycles. 32-bit  $\times$  32-bit  $\rightarrow$  64-bit and 32-bit  $\times$  32-bit + 64bit  $\rightarrow$  64-bit multiplication/accumulation operations are executed in two to four cycles.

**T Bit:** The T bit in the status register reflects the result of the comparison, and its value is the condition (true/false) that determines whether the program will branch. The number of instructions that change the T bit is kept to a minimum to improve the processing speed.

**Table 2.4 T Bit****SH7052F/SH7053F/  
SH7054F CPU**

CPU		Description	Example of Conventional CPU	
CMP/GE	R1,R0	T bit is set when $R0 \geq R1$ . The program branches to TRGET0 when $R0 \geq R1$ and to TRGET1 when $R0 < R1$ .	CMP.W	R1,R0
BT	TRGET0		BGE	TRGET0
BF	TRGET1		BLT	TRGET1
ADD	#1,R0	T bit is not changed by ADD. T bit is set when $R0 = 0$ . The program branches if $R0 = 0$ .	SUB.W	#1,R0
CMP/EQ	#0,R0		BEQ	TRGET
BT	TRGET			

**Immediate Data:** Byte (8-bit) immediate data resides in instruction code. Word or longword immediate data is not input via instruction codes but is stored in a memory table. An immediate data transfer instruction (MOV) accesses the memory table using the PC relative addressing mode with displacement (table 2.5).

**Table 2.5 Immediate Data Accessing**

Classification	SH7052F/SH7053F/SH7054F CPU		Example of Conventional CPU
8-bit immediate	MOV	#H' 12 ,R0	MOV.B #H' 12 ,R0
16-bit immediate	MOV.W	@(disp,PC) ,R0	MOV.W #H' 1234 ,R0
	.DATA.W	H' 1234	
32-bit immediate	MOV.L	@(disp,PC) ,R0	MOV.L #H' 12345678 ,R0
	.DATA.L	H' 12345678	

Note: @(disp, PC) accesses the immediate data.

**Absolute Address:** When data is accessed by absolute address, the value already in the absolute address is placed in the memory table. Loading the immediate data when the instruction is executed transfers that value to the register and the data is accessed in the indirect register addressing mode (table 2.6).

**Table 2.6 Absolute Address Accessing**

Classification	SH7052F/SH7053F/SH7054F CPU		Example of Conventional CPU
Absolute address	MOV.L	@(disp,PC) ,R1	MOV.B @H' 12345678 ,R0
	MOV.B	@R1 ,R0	
	.DATA.L	H' 12345678	

Note: @(disp,PC) accesses the immediate data.

**16-Bit/32-Bit Displacement:** When data is accessed by 16-bit or 32-bit displacement, the pre-existing displacement value is placed in the memory table. Loading the immediate data when the instruction is executed transfers that value to the register and the data is accessed in the indirect indexed register addressing mode (table 2.7).

**Table 2.7 Displacement Accessing**

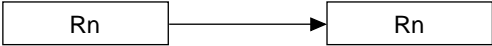
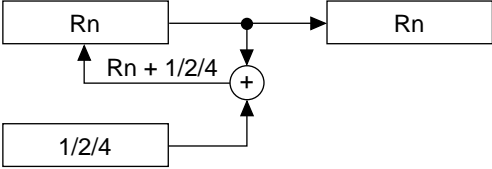
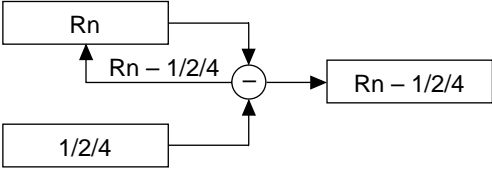
Classification	SH7052F/SH7053F/SH7054F CPU		Example of Conventional CPU
16-bit displacement	MOV.W	@(disp,PC) ,R0	MOV.W @(H' 1234 ,R1) ,R2
	MOV.W	@(R0 ,R1) ,R2	
	.DATA.W	H' 1234	

Note: @(disp,PC) accesses the immediate data.

## 2.3.2 Addressing Modes

Table 2.8 describes addressing modes and effective address calculation.

**Table 2.8 Addressing Modes and Effective Addresses**

Addressing Mode	Instruction Format	Effective Addresses Calculation	Equation
Direct register addressing	Rn	The effective address is register Rn. (The operand is the contents of register Rn.)	—
Indirect register addressing	@Rn	The effective address is the content of register Rn. 	Rn
Post-increment indirect register addressing	@Rn+	The effective address is the content of register Rn. A constant is added to the content of Rn after the instruction is executed. 1 is added for a byte operation, 2 for a word operation, and 4 for a longword operation. 	Rn (After the instruction executes) Byte: $Rn + 1 \rightarrow Rn$ Word: $Rn + 2 \rightarrow Rn$ Longword: $Rn + 4 \rightarrow Rn$
Pre-decrement indirect register addressing	@-Rn	The effective address is the value obtained by subtracting a constant from Rn. 1 is subtracted for a byte operation, 2 for a word operation, and 4 for a longword operation. 	Byte: $Rn - 1 \rightarrow Rn$ Word: $Rn - 2 \rightarrow Rn$ Longword: $Rn - 4 \rightarrow Rn$ (Instruction executed with Rn after calculation)



**Table 2.8 Addressing Modes and Effective Addresses (cont)**

Addressing Mode	Instruction Format	Effective Addresses Calculation	Equation
Indirect register addressing with displacement	@(disp:4, Rn)	The effective address is Rn plus a 4-bit displacement (disp). The value of disp is zero-extended, and remains the same for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation.	Byte: $Rn + disp$ Word: $Rn + disp \times 2$ Longword: $Rn + disp \times 4$
Indirect indexed register addressing	@(R0, Rn)	The effective address is the Rn value plus R0.	$Rn + R0$
Indirect GBR addressing with displacement	@(disp:8, GBR)	The effective address is the GBR value plus an 8-bit displacement (disp). The value of disp is zero-extended, and remains the same for a byte operation, is doubled for a word operation, and is quadrupled for a longword operation.	Byte: $GBR + disp$ Word: $GBR + disp \times 2$ Longword: $GBR + disp \times 4$

**Table 2.8 Addressing Modes and Effective Addresses (cont)**

Addressing Mode	Instruction Format	Effective Addresses Calculation	Equation
Indirect indexed GBR addressing	@(R0, GBR)	The effective address is the GBR value plus the R0.	$GBR + R0$
PC relative addressing with displacement	@(disp:8, PC)	The effective address is the PC value plus an 8-bit displacement (disp). The value of disp is zero-extended, and is doubled for a word operation, and quadrupled for a longword operation. For a longword operation, the lowest two bits of the PC value are masked.	Word: $PC + disp \times 2$ Longword: $PC \& H'FFFFFFC + disp \times 4$

**Table 2.8 Addressing Modes and Effective Addresses (cont)**

Addressing Mode	Instruction Format	Effective Addresses Calculation	Equation
PC relative addressing	disp:8	The effective address is the PC value sign-extended with an 8-bit displacement (disp), doubled, and added to the PC value.	$PC + disp \times 2$
	disp:12	The effective address is the PC value sign-extended with a 12-bit displacement (disp), doubled, and added to the PC value.	$PC + disp \times 2$
Rn		The effective address is the register PC value plus Rn.	$PC + Rn$
Immediate addressing	#imm:8	The 8-bit immediate data (imm) for the TST, AND, OR, and XOR instructions are zero-extended.	—
	#imm:8	The 8-bit immediate data (imm) for the MOV, ADD, and CMP/EQ instructions are sign-extended.	—
	#imm:8	The 8-bit immediate data (imm) for the TRAPA instruction is zero-extended and is quadrupled.	—

### 2.3.3 Instruction Format

Table 2.9 lists the instruction formats for the source operand and the destination operand. The meaning of the operand depends on the instruction code. The symbols are used as follows:

- xxxx: Instruction code
- mmmm: Source register
- nnnn: Destination register
- iiiii: Immediate data
- dddd: Displacement

**Table 2.9 Instruction Formats**

Instruction Formats	Source Operand	Destination Operand	Example
0 format <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 5px auto;"> <span style="float: left;">15</span> <span style="float: right;">0</span> <div style="display: flex; justify-content: space-around; width: 100%;"> <span>xxxx</span> <span>xxxx</span> <span>xxxx</span> <span>xxxx</span> </div> </div>	—	—	NOP
n format <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 5px auto;"> <span style="float: left;">15</span> <span style="float: right;">0</span> <div style="display: flex; justify-content: space-around; width: 100%;"> <span>xxxx</span> <span>nnnn</span> <span>xxxx</span> <span>xxxx</span> </div> </div>	—	nnnn: Direct register	MOVT Rn
	Control register or system register	nnnn: Direct register	STS MACH, Rn
	Control register or system register	nnnn: Indirect pre-decrement register	STC.L SR, @-Rn
m format <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 5px auto;"> <span style="float: left;">15</span> <span style="float: right;">0</span> <div style="display: flex; justify-content: space-around; width: 100%;"> <span>xxxx</span> <span>mmmm</span> <span>xxxx</span> <span>xxxx</span> </div> </div>	mmmm: Direct register	Control register or system register	LDC Rm, SR
	mmmm: Indirect post-increment register	Control register or system register	LDC.L @Rm+, SR
	mmmm: Direct register	—	JMP @Rm
	mmmm: PC relative using Rm	—	BRAF Rm

**Table 2.9 Instruction Formats (cont)**

Instruction Formats	Source Operand	Destination Operand	Example				
nm format	mmmm: Direct register	nnnn: Direct register	ADD Rm, Rn				
15 <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="width: 25px; text-align: center;">xxxx</td> <td style="width: 25px; text-align: center;">nnnn</td> <td style="width: 25px; text-align: center;">mmmm</td> <td style="width: 25px; text-align: center;">xxxx</td> </tr> </table> 0	xxxx	nnnn	mmmm	xxxx	mmmm: Direct register	nnnn: Indirect register	MOV.L Rm, @Rn
xxxx	nnnn	mmmm	xxxx				
	mmmm: Indirect post-increment register (multiply/accumulate) nnnn*: Indirect post-increment register (multiply/accumulate)	MACH, MACL	MAC.W @Rm+, @Rn+				
	mmmm: Indirect post-increment register	nnnn: Direct register	MOV.L @Rm+, Rn				
	mmmm: Direct register	nnnn: Indirect pre-decrement register	MOV.L Rm, @-Rn				
	mmmm: Direct register	nnnn: Indirect indexed register	MOV.L Rm, @(R0, Rn)				
md format	mmmmddd: indirect register with displacement	R0 (Direct register)	MOV.B @(disp, Rm), R0				
15 <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="width: 25px; text-align: center;">xxxx</td> <td style="width: 25px; text-align: center;">xxxx</td> <td style="width: 25px; text-align: center;">mmmm</td> <td style="width: 25px; text-align: center;">ddd</td> </tr> </table> 0	xxxx	xxxx	mmmm	ddd	R0 (Direct register)	nnnnddd: Indirect register with displacement	MOV.B R0, @(disp, Rn)
xxxx	xxxx	mmmm	ddd				
nd4 format							
15 <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="width: 25px; text-align: center;">xxxx</td> <td style="width: 25px; text-align: center;">xxxx</td> <td style="width: 25px; text-align: center;">nnnn</td> <td style="width: 25px; text-align: center;">ddd</td> </tr> </table> 0	xxxx	xxxx	nnnn	ddd			
xxxx	xxxx	nnnn	ddd				
nmd format	mmmm: Direct register	nnnnddd: Indirect register with displacement	MOV.L Rm, @(disp, Rn)				
15 <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="width: 25px; text-align: center;">xxxx</td> <td style="width: 25px; text-align: center;">nnnn</td> <td style="width: 25px; text-align: center;">mmmm</td> <td style="width: 25px; text-align: center;">ddd</td> </tr> </table> 0	xxxx	nnnn	mmmm	ddd	mmmmddd: Indirect register with displacement	nnnn: Direct register	MOV.L @(disp, Rm), Rn
xxxx	nnnn	mmmm	ddd				

Note: \* In multiply/accumulate instructions, nnnn is the source register.

**Table 2.9 Instruction Formats (cont)**

Instruction Formats	Source Operand	Destination Operand	Example				
<p>d format</p> <p>15 <span style="float: right;">0</span></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">dddd</td> <td style="width: 25%; text-align: center;">dddd</td> </tr> </table>	xxxx	xxxx	dddd	dddd	<p>ddddddd: Indirect GBR with displacement</p>	<p>R0 (Direct register)</p>	<p>MOV.L @(disp,GBR),R0</p>
xxxx	xxxx	dddd	dddd				
	<p>R0(Direct register)</p>	<p>ddddddd: Indirect GBR with displacement</p>	<p>MOV.L R0,@(disp,GBR)</p>				
	<p>ddddddd: PC relative with displacement</p>	<p>R0 (Direct register)</p>	<p>MOVA @(disp,PC),R0</p>				
	<p>ddddddd: PC relative</p>	<p>—</p>	<p>BF label</p>				
<p>d12 format</p> <p>15 <span style="float: right;">0</span></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">dddd</td> <td style="width: 25%; text-align: center;">dddd</td> <td style="width: 25%; text-align: center;">dddd</td> </tr> </table>	xxxx	dddd	dddd	dddd	<p>ddddddddddd: PC relative</p>	<p>—</p>	<p>BRA label (label = disp + PC)</p>
xxxx	dddd	dddd	dddd				
<p>nd8 format</p> <p>15 <span style="float: right;">0</span></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">nnnn</td> <td style="width: 25%; text-align: center;">dddd</td> <td style="width: 25%; text-align: center;">dddd</td> </tr> </table>	xxxx	nnnn	dddd	dddd	<p>ddddddd: PC relative with displacement</p>	<p>nnnn: Direct register</p>	<p>MOV.L @(disp,PC),Rn</p>
xxxx	nnnn	dddd	dddd				
<p>i format</p> <p>15 <span style="float: right;">0</span></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">iii</td> <td style="width: 25%; text-align: center;">iii</td> </tr> </table>	xxxx	xxxx	iii	iii	<p>iiiiiii: Immediate</p>	<p>Indirect indexed GBR</p>	<p>AND.B #imm,@(R0,GBR)</p>
xxxx	xxxx	iii	iii				
	<p>iiiiiii: Immediate</p>	<p>R0 (Direct register)</p>	<p>AND #imm,R0</p>				
	<p>iiiiiii: Immediate</p>	<p>—</p>	<p>TRAPA #imm</p>				
<p>ni format</p> <p>15 <span style="float: right;">0</span></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%; text-align: center;">xxxx</td> <td style="width: 25%; text-align: center;">nnnn</td> <td style="width: 25%; text-align: center;">iii</td> <td style="width: 25%; text-align: center;">iii</td> </tr> </table>	xxxx	nnnn	iii	iii	<p>iiiiiii: Immediate</p>	<p>nnnn: Direct register</p>	<p>ADD #imm,Rn</p>
xxxx	nnnn	iii	iii				

## 2.4 Instruction Set by Classification

**Table 2.10 Classification of Instructions**

Classification	Types	Operation		No. of Instructions
		Code	Function	
Data transfer	5	MOV	Data transfer, immediate data transfer, peripheral module data transfer, structure data transfer	39
		MOVA	Effective address transfer	
		MOVT	T bit transfer	
		SWAP	Swap of upper and lower bytes	
		XTRCT	Extraction of the middle of registers connected	
Arithmetic operations	21	ADD	Binary addition	33
		ADDC	Binary addition with carry	
		ADDV	Binary addition with overflow check	
		CMP/cond	Comparison	
		DIV1	Division	
		DIV0S	Initialization of signed division	
		DIV0U	Initialization of unsigned division	
		DMULS	Signed double-length multiplication	
		DMULU	Unsigned double-length multiplication	
		DT	Decrement and test	
		EXTS	Sign extension	
		EXTU	Zero extension	
		MAC	Multiply/accumulate, double-length multiply/accumulate operation	
		MUL	Double-length multiply operation	
		MULS	Signed multiplication	
		MULU	Unsigned multiplication	
		NEG	Negation	
		NEGC	Negation with borrow	
		SUB	Binary subtraction	
		SUBC	Binary subtraction with borrow	
SUBV	Binary subtraction with underflow			

**Table 2.10 Classification of Instructions (cont)**

Classification	Types	Operation		No. of Instructions
		Code	Function	
Logic operations	6	AND	Logical AND	14
		NOT	Bit inversion	
		OR	Logical OR	
		TAS	Memory test and bit set	
		TST	Logical AND and T bit set	
		XOR	Exclusive OR	
Shift	10	ROTL	One-bit left rotation	14
		ROTR	One-bit right rotation	
		ROTCL	One-bit left rotation with T bit	
		ROTCR	One-bit right rotation with T bit	
		SHAL	One-bit arithmetic left shift	
		SHAR	One-bit arithmetic right shift	
		SHLL	One-bit logical left shift	
		SHLLn	n-bit logical left shift	
		SHLR	One-bit logical right shift	
		SHLRn	n-bit logical right shift	
Branch	9	BF	Conditional branch, conditional branch with delay (Branch when T = 0)	11
		BT	Conditional branch, conditional branch with delay (Branch when T = 1)	
		BRA	Unconditional branch	
		BRAF	Unconditional branch	
		BSR	Branch to subroutine procedure	
		BSRF	Branch to subroutine procedure	
		JMP	Unconditional branch	
		JSR	Branch to subroutine procedure	
		RTS	Return from subroutine procedure	



**Table 2.10 Classification of Instructions (cont)**

Classification	Types	Operation		No. of Instructions
		Code	Function	
System control	11	CLRT	T bit clear	31
		CLRMAC	MAC register clear	
		LDC	Load to control register	
		LDS	Load to system register	
		NOP	No operation	
		RTE	Return from exception processing	
		SETT	T bit set	
		SLEEP	Shift into power-down mode	
		STC	Storing control register data	
		STS	Storing system register data	
		TRAPA	Trap exception handling	
Total:		62		142

Table 2.11 shows the format used in tables 2.12 to 2.17, which list instruction codes, operation, and execution states in order by classification.

**Table 2.11 Instruction Code Format**

Item	Format	Explanation
Instruction	OP, Sz SRC, DEST	OP: Operation code Sz: Size (B: byte, W: word, or L: longword) SRC: Source DEST: Destination Rm: Source register Rn: Destination register imm: Immediate data disp: Displacement* <sup>1</sup>
Instruction code	MSB ↔ LSB	mmmm: Source register nnnn: Destination register 0000: R0 0001: R1 . . . 1111: R15 iiii: Immediate data dddd: Displacement
Operation	→, ←	Direction of transfer
	(xx)	Memory operand
	M/Q/T	Flag bits in the SR
	&	Logical AND of each bit
		Logical OR of each bit
	^	Exclusive OR of each bit
	~	Logical NOT of each bit
	<<n	n-bit left shift
	>>n	n-bit right shift
Execution cycles	—	Value when no wait states are inserted* <sup>2</sup>
T bit	—	Value of T bit after instruction is executed. An em-dash (—) in the column means no change.

Notes: 1. Depending on the operand size, displacement is scaled  $\times 1$ ,  $\times 2$ , or  $\times 4$ . For details, see the *SH-1/SH-2/SH-DSP Programming Manual*.

2. Instruction execution cycles: The execution cycles shown in the table are minimums. The actual number of cycles may be increased when (1) contention occurs between instruction fetches and data access, or (2) when the destination register of the load instruction (memory → register) and the register used by the next instruction are the same.

**Table 2.12 Data Transfer Instructions**

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
MOV	#imm,Rn	1110nnnniiiiiiii	#imm → Sign extension → Rn	1	—
MOV.W	@(disp,PC),Rn	1001nnnnndddddddd	(disp × 2 + PC) → Sign extension → Rn	1	—
MOV.L	@(disp,PC),Rn	1101nnnnndddddddd	(disp × 4 + PC) → Rn	1	—
MOV	Rm,Rn	0110nnnnnnmmmm0011	Rm → Rn	1	—
MOV.B	Rm,@Rn	0010nnnnnnmmmm0000	Rm → (Rn)	1	—
MOV.W	Rm,@Rn	0010nnnnnnmmmm0001	Rm → (Rn)	1	—
MOV.L	Rm,@Rn	0010nnnnnnmmmm0010	Rm → (Rn)	1	—
MOV.B	@Rm,Rn	0110nnnnnnmmmm0000	(Rm) → Sign extension → Rn	1	—
MOV.W	@Rm,Rn	0110nnnnnnmmmm0001	(Rm) → Sign extension → Rn	1	—
MOV.L	@Rm,Rn	0110nnnnnnmmmm0010	(Rm) → Rn	1	—
MOV.B	Rm,@-Rn	0010nnnnnnmmmm0100	Rn-1 → Rn, Rm → (Rn)	1	—
MOV.W	Rm,@-Rn	0010nnnnnnmmmm0101	Rn-2 → Rn, Rm → (Rn)	1	—
MOV.L	Rm,@-Rn	0010nnnnnnmmmm0110	Rn-4 → Rn, Rm → (Rn)	1	—
MOV.B	@Rm+,Rn	0110nnnnnnmmmm0100	(Rm) → Sign extension → Rn, Rm + 1 → Rm	1	—
MOV.W	@Rm+,Rn	0110nnnnnnmmmm0101	(Rm) → Sign extension → Rn, Rm + 2 → Rm	1	—
MOV.L	@Rm+,Rn	0110nnnnnnmmmm0110	(Rm) → Rn, Rm + 4 → Rm	1	—
MOV.B	R0,@(disp,Rn)	10000000nnnnndddd	R0 → (disp + Rn)	1	—
MOV.W	R0,@(disp,Rn)	10000001nnnnndddd	R0 → (disp × 2 + Rn)	1	—
MOV.L	Rm,@(disp,Rn)	0001nnnnnnmmmmndddd	Rm → (disp × 4 + Rn)	1	—
MOV.B	@(disp,Rm),R0	10000100nnnnndddd	(disp + Rm) → Sign extension → R0	1	—
MOV.W	@(disp,Rm),R0	10000101nnnnndddd	(disp × 2 + Rm) → Sign extension → R0	1	—
MOV.L	@(disp,Rm),Rn	0101nnnnnnmmmmndddd	(disp × 4 + Rm) → Rn	1	—
MOV.B	Rm,@(R0,Rn)	0000nnnnnnmmmm0100	Rm → (R0 + Rn)	1	—

**Table 2.12 Data Transfer Instructions (cont)**

<b>Instruction</b>	<b>Instruction Code</b>	<b>Operation</b>	<b>Execution Cycles</b>	<b>T Bit</b>
MOV.W Rm,@(R0,Rn)	0000nnnnmmmm0101	Rm → (R0 + Rn)	1	—
MOV.L Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B @(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W @(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L @(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B @(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W @(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L @(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA @(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B Rm,Rn	0110nnnnmmmm1000	Rm → Swap the bottom two bytes → Rn	1	—
SWAP.W Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT Rm,Rn	0010nnnnmmmm1101	Rm: Middle 32 bits of Rn → Rn	1	—

**Table 2.13 Arithmetic Operation Instructions**

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
ADD	Rn, Rn	0011nnnnnnmm1100	$Rn + Rm \rightarrow Rn$	1	—
ADD	#imm, Rn	0111nnnniiiiiiii	$Rn + imm \rightarrow Rn$	1	—
ADDC	Rn, Rn	0011nnnnnnmm1110	$Rn + Rm + T \rightarrow Rn$ , Carry $\rightarrow T$	1	Carry
ADDV	Rn, Rn	0011nnnnnnmm1111	$Rn + Rm \rightarrow Rn$ , Overflow $\rightarrow T$	1	Overflow
CMP/EQ	#imm, R0	10001000iiiiiiii	If $R0 = imm$ , $1 \rightarrow T$	1	Comparison result
CMP/EQ	Rn, Rn	0011nnnnnnmm0000	If $Rn = Rm$ , $1 \rightarrow T$	1	Comparison result
CMP/HS	Rn, Rn	0011nnnnnnmm0010	If $Rn \geq Rm$ with unsigned data, $1 \rightarrow T$	1	Comparison result
CMP/GE	Rn, Rn	0011nnnnnnmm0011	If $Rn \geq Rm$ with signed data, $1 \rightarrow T$	1	Comparison result
CMP/HI	Rn, Rn	0011nnnnnnmm0110	If $Rn > Rm$ with unsigned data, $1 \rightarrow T$	1	Comparison result
CMP/GT	Rn, Rn	0011nnnnnnmm0111	If $Rn > Rm$ with signed data, $1 \rightarrow T$	1	Comparison result
CMP/PL	Rn	0100nnnn00010101	If $Rn > 0$ , $1 \rightarrow T$	1	Comparison result
CMP/PZ	Rn	0100nnnn00010001	If $Rn \geq 0$ , $1 \rightarrow T$	1	Comparison result
CMP/STR	Rm, Rn	0010nnnnnnmm1100	If Rn and Rm have an equivalent byte, $1 \rightarrow T$	1	Comparison result
DIV1	Rn, Rn	0011nnnnnnmm0100	Single-step division (Rn/Rm)	1	Calculation result
DIV0S	Rm, Rn	0010nnnnnnmm0111	MSB of Rn $\rightarrow Q$ , MSB of Rm $\rightarrow M$ , $M \wedge Q \rightarrow T$	1	Calculation result
DIV0U		000000000011001	$0 \rightarrow M/Q/T$	1	0

**Table 2.13 Arithmetic Operation Instructions (cont)**

Instruction	Instruction Code	Operation	Execution Cycles	T Bit
DMULS.L Rm, Rn	0011nnnnnnmmmm1101	Signed operation of $Rn \times Rm \rightarrow MACH, MACL$ $32 \times 32 \rightarrow 64$ bit	2 to 4*	—
DMULU.L Rm, Rn	0011nnnnnnmmmm0101	Unsigned operation of $Rn \times Rm \rightarrow MACH, MACL$ $32 \times 32 \rightarrow 64$ bit	2 to 4*	—
DT Rn	0100nnnn00010000	$Rn - 1 \rightarrow Rn$ , when Rn is 0, $1 \rightarrow T$ . When Rn is nonzero, $0 \rightarrow T$	1	Comparison result
EXTS.B Rm, Rn	0110nnnnnnmmmm1110	A byte in Rm is sign-extended $\rightarrow Rn$	1	—
EXTS.W Rm, Rn	0110nnnnnnmmmm1111	A word in Rm is sign-extended $\rightarrow Rn$	1	—
EXTU.B Rm, Rn	0110nnnnnnmmmm1100	A byte in Rm is zero-extended $\rightarrow Rn$	1	—
EXTU.W Rm, Rn	0110nnnnnnmmmm1101	A word in Rm is zero-extended $\rightarrow Rn$	1	—
MAC.L @Rm+, @Rn+	0000nnnnnnmmmm1111	Signed operation of $(Rn) \times (Rm) + MAC \rightarrow MAC$ $32 \times 32 \rightarrow 64$ bit	3/(2 to 4)*	—
MAC.W @Rm+, @Rn+	0100nnnnnnmmmm1111	Signed operation of $(Rn) \times (Rm) + MAC \rightarrow MAC$ $16 \times 16 + 64 \rightarrow 64$ bit	3/(2)*	—
MUL.L Rm, Rn	0000nnnnnnmmmm0111	$Rn \times Rm \rightarrow MACL, 32 \times 32 \rightarrow 32$ bit	2 to 4*	—
MULS.W Rm, Rn	0010nnnnnnmmmm1111	Signed operation of $Rn \times Rm \rightarrow MAC$ $16 \times 16 \rightarrow 32$ bit	1 to 3*	—
MULU.W Rm, Rn	0010nnnnnnmmmm1110	Unsigned operation of $Rn \times Rm \rightarrow MAC$ $16 \times 16 \rightarrow 32$ bit	1 to 3*	—
NEG Rm, Rn	0110nnnnnnmmmm1011	$0 - Rm \rightarrow Rn$	1	—
NEGC Rm, Rn	0110nnnnnnmmmm1010	$0 - Rm - T \rightarrow Rn$ , Borrow $\rightarrow T$	1	Borrow

**Table 2.13 Arithmetic Operation Instructions (cont)**

<b>Instruction</b>		<b>Instruction Code</b>	<b>Operation</b>	<b>Execution Cycles</b>	<b>T Bit</b>
SUB	Rn, Rn	0011nnnnnnmm1000	Rn-Rm → Rn	1	—
SUBC	Rn, Rn	0011nnnnnnmm1010	Rn-Rm-T → Rn, Borrow → T	1	Borrow
SUBV	Rn, Rn	0011nnnnnnmm1011	Rn-Rm → Rn, Underflow → T	1	Overflow

Note: \* The normal minimum number of execution cycles. (The number in parentheses is the number of cycles when there is contention with following instructions.)

**Table 2.14 Logic Operation Instructions**

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
AND	Rn, Rn	0010nnnnmmmm1001	$Rn \& Rn \rightarrow Rn$	1	—
AND	#imm, R0	11001001iiiiiii	$R0 \& imm \rightarrow R0$	1	—
AND.B	#imm, @(R0, GBR)	11001101iiiiiii	$(R0 + GBR) \& imm \rightarrow (R0 + GBR)$	3	—
NOT	Rn, Rn	0110nnnnmmmm0111	$\sim Rn \rightarrow Rn$	1	—
OR	Rn, Rn	0010nnnnmmmm1011	$Rn   Rn \rightarrow Rn$	1	—
OR	#imm, R0	11001011iiiiiii	$R0   imm \rightarrow R0$	1	—
OR.B	#imm, @(R0, GBR)	11001111iiiiiii	$(R0 + GBR)   imm \rightarrow (R0 + GBR)$	3	—
TAS.B	@Rn	0100nmmn00011011	If (Rn) is 0, $1 \rightarrow T$ ; $1 \rightarrow$ MSB of (Rn)	4	Test result
TST	Rn, Rn	0010nnnnmmmm1000	$Rn \& Rn$ ; if the result is 0, $1 \rightarrow T$	1	Test result
TST	#imm, R0	11001000iiiiiii	$R0 \& imm$ ; if the result is 0, $1 \rightarrow T$	1	Test result
TST.B	#imm, @(R0, GBR)	11001100iiiiiii	$(R0 + GBR) \& imm$ ; if the result is 0, $1 \rightarrow T$	3	Test result
XOR	Rn, Rn	0010nnnnmmmm1010	$Rn \wedge Rn \rightarrow Rn$	1	—
XOR	#imm, R0	11001010iiiiiii	$R0 \wedge imm \rightarrow R0$	1	—
XOR.B	#imm, @(R0, GBR)	11001110iiiiiii	$(R0 + GBR) \wedge imm \rightarrow (R0 + GBR)$	3	—



**Table 2.15 Shift Instructions**

Instruction		Instruction Code	Operation	Execution Cycles	T Bit
ROTL	Rn	0100nnnn00000100	$T \leftarrow Rn \leftarrow \text{MSB}$	1	MSB
ROTR	Rn	0100nnnn00000101	$\text{LSB} \rightarrow Rn \rightarrow T$	1	LSB
ROTCL	Rn	0100nnnn00100100	$T \leftarrow Rn \leftarrow T$	1	MSB
ROTCR	Rn	0100nnnn00100101	$T \rightarrow Rn \rightarrow T$	1	LSB
SHAL	Rn	0100nnnn00100000	$T \leftarrow Rn \leftarrow 0$	1	MSB
SHAR	Rn	0100nnnn00100001	$\text{MSB} \rightarrow Rn \rightarrow T$	1	LSB
SHLL	Rn	0100nnnn00000000	$T \leftarrow Rn \leftarrow 0$	1	MSB
SHLR	Rn	0100nnnn00000001	$0 \rightarrow Rn \rightarrow T$	1	LSB
SHLL2	Rn	0100nnnn00001000	$Rn \ll 2 \rightarrow Rn$	1	—
SHLR2	Rn	0100nnnn00001001	$Rn \gg 2 \rightarrow Rn$	1	—
SHLL8	Rn	0100nnnn00011000	$Rn \ll 8 \rightarrow Rn$	1	—
SHLR8	Rn	0100nnnn00011001	$Rn \gg 8 \rightarrow Rn$	1	—
SHLL16	Rn	0100nnnn00101000	$Rn \ll 16 \rightarrow Rn$	1	—
SHLR16	Rn	0100nnnn00101001	$Rn \gg 16 \rightarrow Rn$	1	—

**Table 2.16 Branch Instructions**

Instruction		Instruction Code	Operation	Exec. Cycles	T Bit
BF	label	10001011dddddddd	If T = 0, disp × 2 + PC → PC; if T = 1, nop	3/1*	—
BF/S	label	10001111dddddddd	Delayed branch, if T = 0, disp × 2 + PC → PC; if T = 1, nop	3/1*	—
BT	label	10001001dddddddd	If T = 1, disp × 2 + PC → PC; if T = 0, nop	3/1*	—
BT/S	label	10001101dddddddd	Delayed branch, if T = 1, disp × 2 + PC → PC; if T = 0, nop	2/1*	—
BRA	label	1010dddddddddddd	Delayed branch, disp × 2 + PC → PC	2	—
BRAF	Rm	0000mmmm00100011	Delayed branch, Rm + PC → PC	2	—
BSR	label	1011dddddddddddd	Delayed branch, PC → PR, disp × 2 + PC → PC	2	—
BSRF	Rm	0000mmmm00000011	Delayed branch, PC → PR, Rm + PC → PC	2	—
JMP	@Rm	0100mmmm00101011	Delayed branch, Rm → PC	2	—
JSR	@Rm	0100mmmm00001011	Delayed branch, PC → PR, Rm → PC	2	—
RTS		000000000001011	Delayed branch, PR → PC	2	—

Note: \* One state when it does not branch.

**Table 2.17 System Control Instructions**

Instruction	Instruction Code	Operation	Exec. Cycles	T Bit
CLRT	000000000001000	0 → T	1	0
CLRMACH	000000000101000	0 → MACH, MACL	1	—
LDC Rm, SR	0100mmmm00001110	Rm → SR	1	LSB
LDC Rm, GBR	0100mmmm00011110	Rm → GBR	1	—
LDC Rm, VBR	0100mmmm00101110	Rm → VBR	1	—
LDC.L @Rm+, SR	0100mmmm00000111	(Rm) → SR, Rm + 4 → Rm	3	LSB
LDC.L @Rm+, GBR	0100mmmm00010111	(Rm) → GBR, Rm + 4 → Rm	3	—
LDC.L @Rm+, VBR	0100mmmm00100111	(Rm) → VBR, Rm + 4 → Rm	3	—
LDS Rm, MACH	0100mmmm00001010	Rm → MACH	1	—
LDS Rm, MACL	0100mmmm00011010	Rm → MACL	1	—
LDS Rm, PR	0100mmmm00101010	Rm → PR	1	—
LDS.L @Rm+, MACH	0100mmmm00000110	(Rm) → MACH, Rm + 4 → Rm	1	—
LDS.L @Rm+, MACL	0100mmmm00010110	(Rm) → MACL, Rm + 4 → Rm	1	—
LDS.L @Rm+, PR	0100mmmm00100110	(Rm) → PR, Rm + 4 → Rm	1	—
NOP	000000000001001	No operation	1	—
RTE	000000000101011	Delayed branch, stack area → PC/SR	4	—
SETT	000000000011000	1 → T	1	1
SLEEP	000000000011011	Sleep	3*	—
STC SR, Rn	0000nnnn00000010	SR → Rn	1	—
STC GBR, Rn	0000nnnn00010010	GBR → Rn	1	—
STC VBR, Rn	0000nnnn00100010	VBR → Rn	1	—
STC.L SR, @-Rn	0100nnnn00000011	Rn-4 → Rn, SR → (Rn)	2	—
STC.L GBR, @-Rn	0100nnnn00010011	Rn-4 → Rn, GBR → (Rn)	2	—
STC.L VBR, @-Rn	0100nnnn00100011	Rn-4 → Rn, BR → (Rn)	2	—
STS MACH, Rn	0000nnnn00001010	MACH → Rn	1	—
STS MACL, Rn	0000nnnn00011010	MACL → Rn	1	—
STS PR, Rn	0000nnnn00101010	PR → Rn	1	—

**Table 2.17 System Control Instructions (cont)**

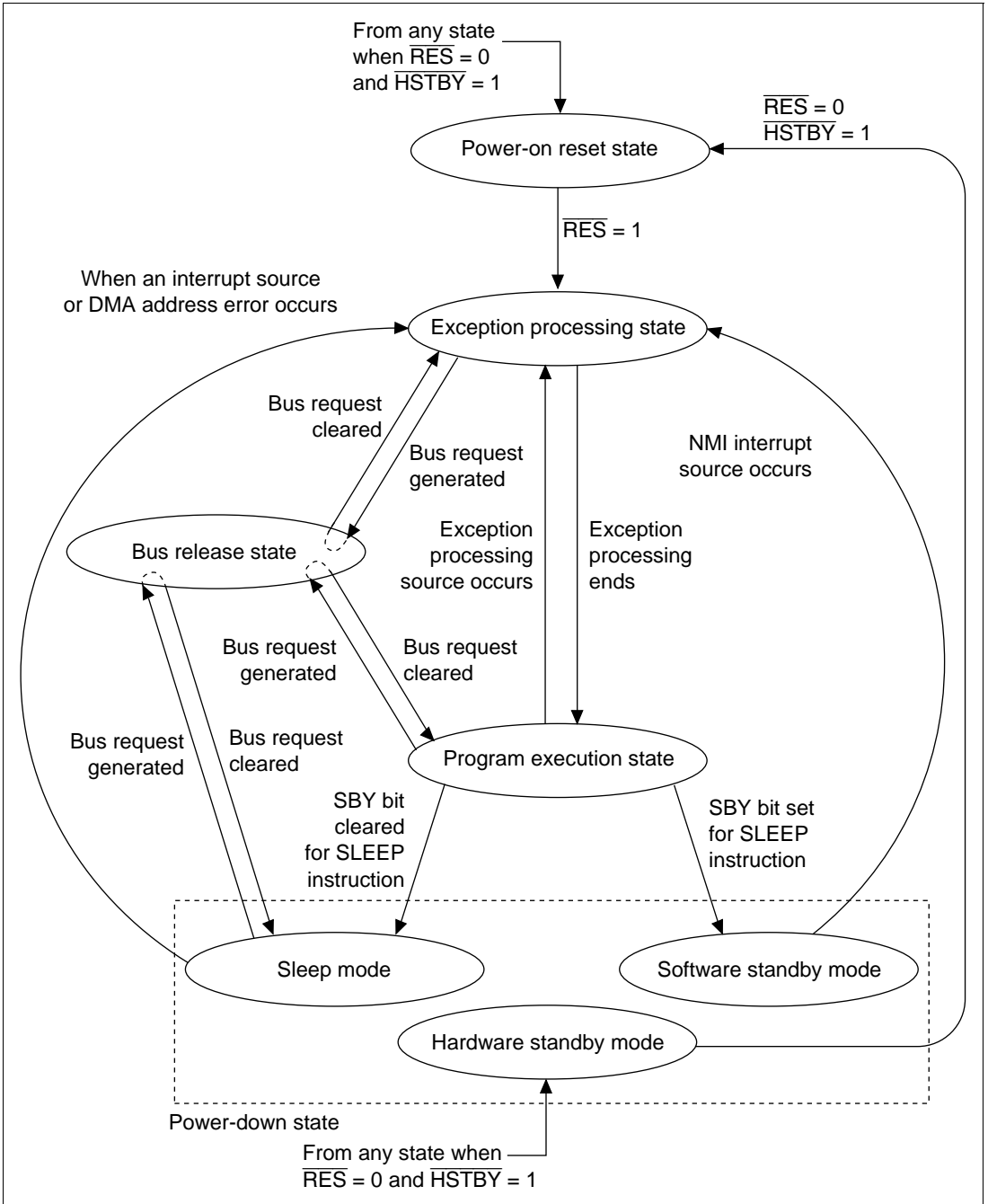
<b>Instruction</b>	<b>Instruction Code</b>	<b>Operation</b>	<b>Exec. Cycles</b>	<b>T Bit</b>
STS.L MACH,@-Rn	0100nnnn00000010	Rn-4 → Rn, MACH → (Rn)	1	—
STS.L MACL,@-Rn	0100nnnn00010010	Rn-4 → Rn, MACL → (Rn)	1	—
STS.L PR,@-Rn	0100nnnn00100010	Rn-4 → Rn, PR → (Rn)	1	—
TRAPA #imm	11000011iiiiiiii	PC/SR → stack area, (imm × 4 + VBR) → PC	8	—

Note: \* The number of execution cycles before the chip enters sleep mode: The execution cycles shown in the table are minimums. The actual number of cycles may be increased when (1) contention occurs between instruction fetches and data access, or (2) when the destination register of the load instruction (memory → register) and the register used by the next instruction are the same.

## 2.5 Processing States

### 2.5.1 State Transitions

The CPU has five processing states: reset, exception processing, bus release, program execution and power-down. Figure 2.6 shows the transitions between the states.



**Figure 2.6 Transitions between Processing States**

**Reset State:** The CPU resets in the reset state. When the  $\overline{\text{RES}}$  pin level goes low, a power-on reset results. When the  $\overline{\text{RES}}$  pin is high and MRES is low, a manual reset will occur.

**Exception Processing State:** The exception processing state is a transient state that occurs when exception processing sources such as resets or interrupts alter the CPU's processing state flow.

For a reset, the initial values of the program counter (PC) (execution start address) and stack pointer (SP) are fetched from the exception processing vector table and stored; the CPU then branches to the execution start address and execution of the program begins.

For an interrupt, the stack pointer (SP) is accessed and the program counter (PC) and status register (SR) are saved to the stack area. The exception service routine start address is fetched from the exception processing vector table; the CPU then branches to that address and the program starts executing, thereby entering the program execution state.

**Program Execution State:** In the program execution state, the CPU sequentially executes the program.

**Power-Down State:** In the power-down state, the CPU operation halts and power consumption declines. The SLEEP instruction places the CPU in the power-down state. This state has two modes: sleep mode and standby mode. In addition, driving the  $\overline{\text{HSTBY}}$  pin low while the  $\overline{\text{RES}}$  pin is low causes a transition to hardware standby mode.

**Bus Release State:** In the bus release state, the CPU releases access rights to the bus to the device that has requested them.

# Section 3 Operating Modes

## 3.1 Operating Mode Selection

The SH7052F/SH7053F/SH7054F has five operating modes that are selected by pins MD2 to MD0 and FWE. The mode setting pins should not be changed during operation of the SH7052F/SH7053F/SH7054F, and only the setting combinations shown in Table 3.1 should be used. The  $PV_{CC1}$  power supply voltage must be within the range shown in table 3.1.

**Table 3.1 Operating Mode Selection**

Operating Mode No.	Pin Settings				Mode Name	On-Chip ROM	Area 0 Bus	
	FWE	MD2	MD1	MD0			Width	$PV_{CC1}$ Voltage
Mode 0	0	1	0	0	MCU expanded mode	Disabled	8 bits	3.3 V $\pm$ 0.3 V
Mode 1	0	1	0	1			16 bits	
Mode 2	0	1	1	0		Enabled	Set by BCR1	
Mode 3	0	1	1	1	MCU single-chip mode	Enabled	—	5.0 V $\pm$ 0.5 V
Mode 4	1	1	0	0	Boot mode	Enabled	Set by BCR1	3.3 V $\pm$ 0.3 V
Mode 5	1	1	0	1			—	5.0 V $\pm$ 0.5 V
Mode 6	1	1	1	0			User program mode	Enabled
Mode 7	1	1	1	1	Programmer mode	—	—	5.0 V $\pm$ 0.5 V
—	0/1	0	1	1			—	—

There are two MCU operating modes: MCU single-chip mode and MCU expanded mode.

Modes in which the flash memory can be programmed are boot mode and user program mode (the two on-board programming modes) and programmer mode in which programming is performed with an EPROM programmer (a type which supports programming of this device).

For details, see section 20, ROM (SH7052F/SH7053F) and section 21, ROM (SH7054F).

**Caution:** In the SH7052F/SH7053F/SH7054F expanded modes (modes 0, 1, and 2), the guaranteed operating range of bus port power supply (port power supply 1:  $PV_{CC1}$ ) in the MCU expanded modes is 3.3 V  $\pm$ 0.3 V.

Since operation is not guaranteed in the MCU expanded modes on a voltage outside this range, a voltage within this range must be used.





# Section 4 Clock Pulse Generator (CPG)

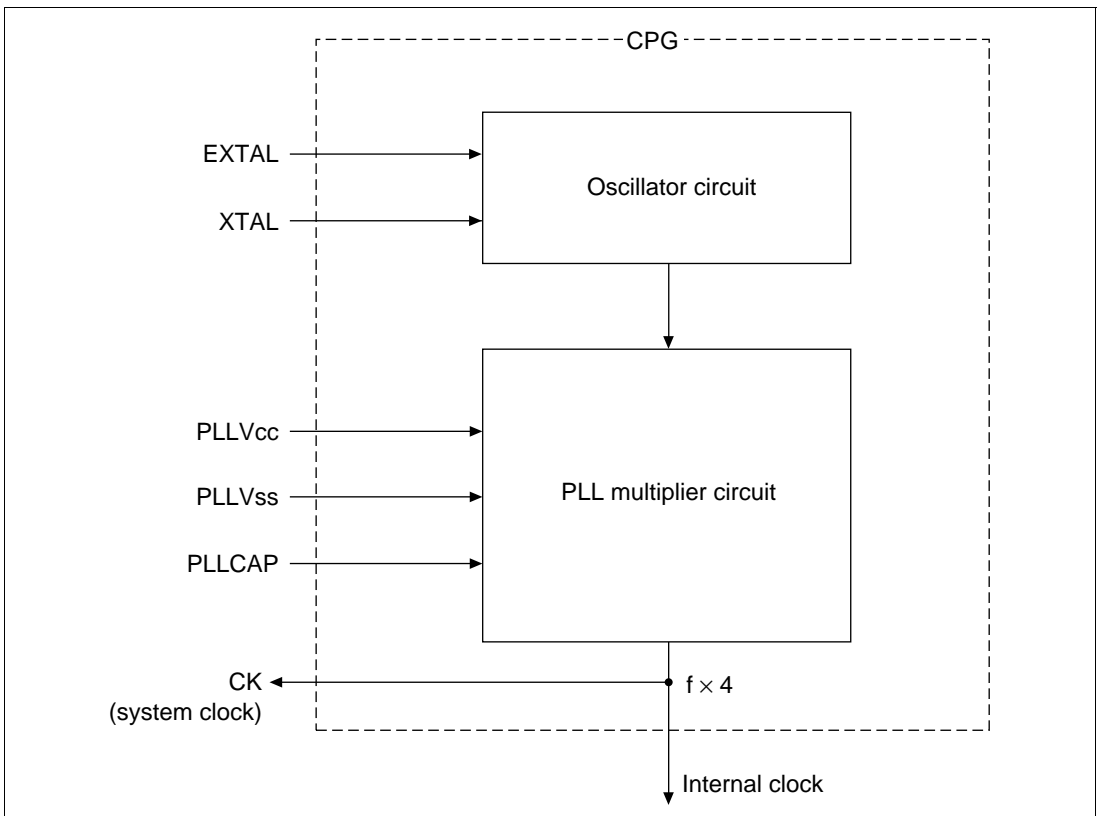
## 4.1 Overview

The clock pulse generator (CPG) supplies clock pulses inside the SH7052F/SH7053F/SH7054F chip and to external devices. The SH7052F/SH7053F/SH7054F CPG consists of an oscillator circuit and a PLL multiplier circuit. There are two methods of generating a clock with the CPG: by connecting a crystal resonator, or by inputting an external clock. The oscillator circuit oscillates at the same frequency as the input clock. A chip operating frequency of 4 times the oscillator frequency is generated by the PLL multiplier circuit.

The CPG is halted in software standby mode and hardware standby mode.

### 4.1.1 Block Diagram

A block diagram of the clock pulse generator is shown in figure 4.1.



**Figure 4.1 Block Diagram of Clock Pulse Generator**

## 4.1.2 Pin Configuration

The pins relating to the clock pulse generator are shown in table 4.1.

**Table 4.1 CPG Pins**

Pin Name	Abbreviation	I/O	Description
External clock	EXTAL	Input	Crystal resonator or external clock input
Crystal	XTAL	Input	Crystal resonator connection
System clock	CK	Output	System clock output
PLL power supply	PLL <sub>V<sub>cc</sub></sub>	Input	PLL multiplier circuit power supply
PLL ground	PLL <sub>V<sub>ss</sub></sub>	Input	PLL multiplier circuit ground
PLL capacitance	PLLCAP	Input	PLL multiplier circuit oscillation external capacitance pin

## 4.2 Frequency Ranges

The input frequency and operating frequency ranges are shown in table 4.2.

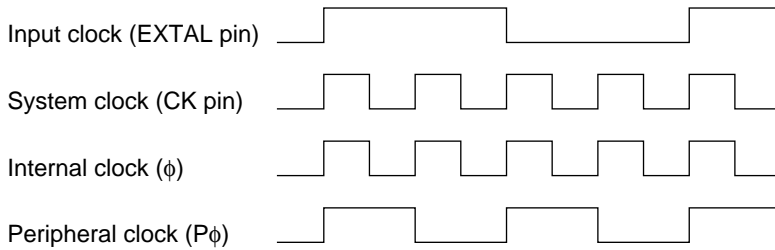
**Table 4.2 Input Frequency and Operating Frequency**

Input Frequency Range (MHz)	PLL Multiplication Factor	Operating Frequency Range (MHz)
5 to 10	×4	20 to 40

Note: Crystal resonator and external clock input

For the chip operating frequency, a frequency of 4 times the input frequency (EXTAL pin) is generated as the internal clock ( $\phi$ ) by the on-chip PLL circuit. The system clock (CK pin) output frequency is the same as that of the internal clock ( $\phi$ ).

Some on-chip peripheral modules operate on a peripheral clock ( $P\phi$ ) obtained by dividing the internal clock ( $\phi$ ) by 2. Figure 4.2 shows the relationship between the various clocks. As regards the system clock, since the input clock is multiplied by the PLL multiplier circuit, the phases of both clocks are not determined uniformly.



**Figure 4.2 Input Clock and System Clock**

## 4.3 Clock Source

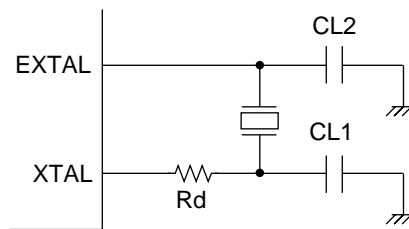
Clock pulses can be supplied from a connected crystal resonator or an external clock.

### 4.3.1 Connecting a Crystal Oscillator

**Circuit Configuration:** Figure 4.3 shows an example of connecting a crystal resonator. Use the damping resistance ( $R_d$ ) shown in table 4.3. An AT-cut parallel-resonance type crystal resonator should be used. Load capacitors ( $CL1$ ,  $CL2$ ) must be connected as shown in the figure.

The clock pulses generated by the crystal resonator and internal oscillator are sent to the PLL multiplier circuit, where a multiplied frequency is selected and supplied inside the SH7052F/SH7053F/SH7054F chip and to external devices.

The crystal oscillator manufacturer should be consulted concerning the compatibility between the crystal oscillator and the chip.



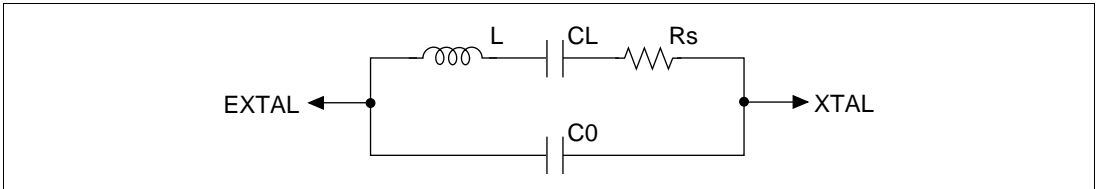
$CL1 = CL2 = 18$  to  $22$  pF (recommended value)

**Figure 4.3 Connection of Crystal Oscillator (Example)**

**Table 4.3 Damping Resistance Values (Recommended Values)**

Parameter	Frequency (MHz)	
	5	10
Rd ( $\Omega$ )	500	0

**Crystal Oscillator:** Figure 4.4 shows an equivalent circuit of the crystal oscillator. Use a crystal oscillator with the characteristics listed in table 4.4.

**Figure 4.4 Crystal Oscillator Equivalent Circuit****Table 4.4 Crystal Oscillator Parameters (Recommended Values)**

Parameter	Frequency (MHz)	
	5	10
Rs max ( $\Omega$ )	100	50
C0 max (pF)	7	7

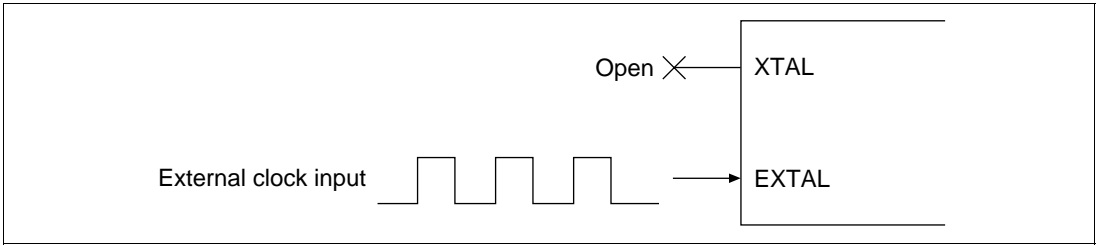
The crystal oscillator manufacturer should be consulted concerning the compatibility between the crystal oscillator and the chip.

### 4.3.2 External Clock Input Method

An example of external clock input connection is shown in figure 4.5.

When the XTAL pin is placed in the open state, the parasitic capacitance should be 10 pF or less.

Even when an external clock is input, provide for a wait of at least the oscillation settling time when powering on or exiting standby mode in order to secure the PLL settling time.



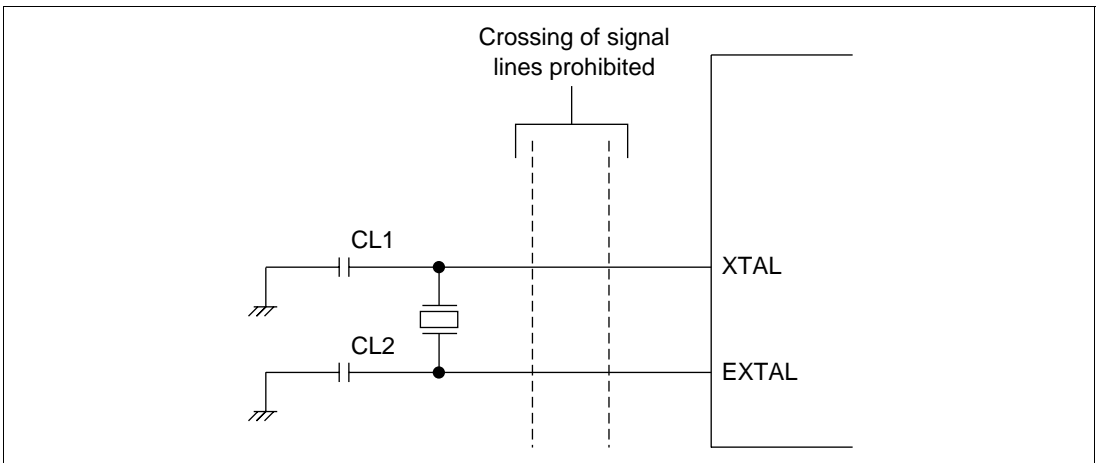
**Figure 4.5 External Clock Input Method (Example)**

## 4.4 Usage Notes

**Notes on Board Design:** When connecting a crystal oscillator, observe the following precautions:

- To prevent induction from interfering with correct oscillation, do not route any signal lines near the oscillator circuitry (figure 4.6).
- When designing the board, place the crystal oscillator and its load capacitors as close as possible to the XTAL and EXTAL pins.

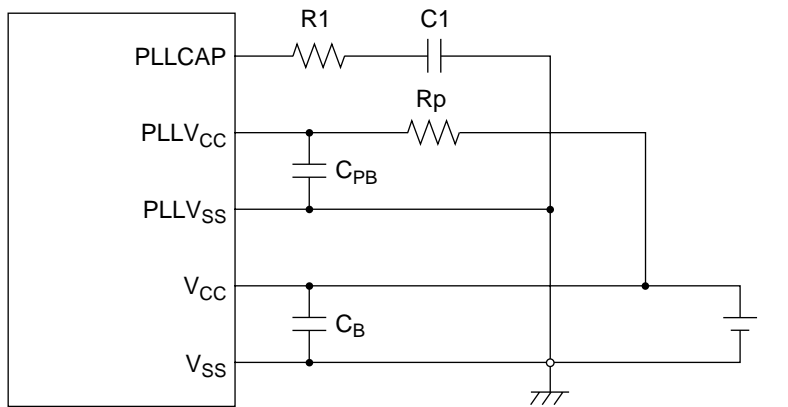
Figure 4.6 shows the precautions regarding oscillator circuit system board design.



**Figure 4.6 Precautions for Oscillator Circuit System Board Design**

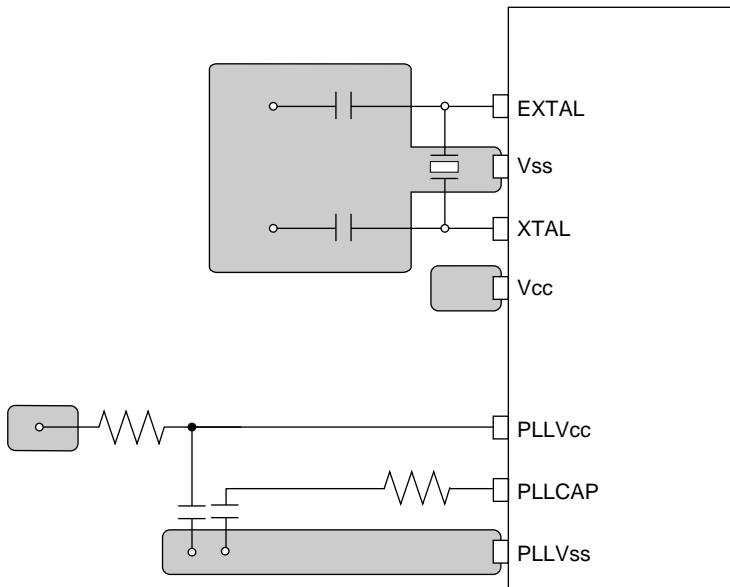
**PLL Oscillation Power Supply:** Place oscillation capacitor C1 and resistor R1 close to the PLL CAP pin, and ensure that no other signal lines cross this line. Supply the C1 ground from PLLV<sub>SS</sub>.

Separate PLLV<sub>CC</sub> and PLLV<sub>SS</sub> from the other V<sub>CC</sub> and V<sub>SS</sub> lines at the board power supply source, and be sure to insert bypass capacitors C<sub>PB</sub> and C<sub>B</sub> close to the pins.



Recommended values  
 $C_{PB}, C_B: 0.1 \mu F$   
 $R_p: 200 \Omega$   
 $R_1: 3 k\Omega$   
 $C_1: 470 pF$  (laminated ceramic)

**Figure 4.7 Points for Caution in PLL Power Supply Connection**



**Figure 4.8 Actual Example of Board Design**

# Section 5 Exception Processing

## 5.1 Overview

### 5.1.1 Types of Exception Processing and Priority

Exception processing is started by four sources: resets, address errors, interrupts and instructions and have the priority shown in table 5.1. When several exception processing sources occur at once, they are processed according to the priority shown.

**Table 5.1 Types of Exception Processing and Priority Order**

Exception	Source	Priority	
Reset	Power-on reset		
	Manual reset		
Address error	CPU address error		
	DMAC address error		
Interrupt	NMI		
	User break		
	IRQ		
	On-chip peripheral modules:		<ul style="list-style-type: none"> <li>• Direct memory access controller (DMAC)</li> <li>• Advanced timer unit-II (ATU-II)</li> <li>• Compare match timer 0 (CMT0)</li> <li>• A/D converter channel 0 (A/D0)</li> <li>• Compare match timer (CMT1)</li> <li>• A/D converter channel 1 (A/D1)</li> <li>• Serial communication interface (SCI)</li> <li>• Hitachi controller area network (HCAN)</li> <li>• Watchdog timer (WDT)</li> </ul>
Instructions	Trap instruction (TRAPA instruction)		
	General illegal instructions (undefined code)		
	Illegal slot instructions (undefined code placed directly after a delay branch instruction* <sup>1</sup> or instructions that rewrite the PC* <sup>2</sup> )	Low	

- Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, BRAF.  
 2. Instructions that rewrite the PC: JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, TRAPA, BF/S, BT/S, BSRF, BRAF.

## 5.1.2 Exception Processing Operations

The exception processing sources are detected and begin processing according to the timing shown in table 5.2.

**Table 5.2 Timing of Exception Source Detection and Start of Exception Processing**

Exception	Source	Timing of Source Detection and Start of Processing
Reset	Power-on reset	Starts when the $\overline{\text{RES}}$ pin changes from low to high or when the WDT overflows.
	Manual reset	Starts when the WDT overflows.
Address error		Detected when instruction is decoded and starts when the previous executing instruction finishes executing.
Interrupts		Detected when instruction is decoded and starts when the previous executing instruction finishes executing.
Instructions	Trap instruction	Starts from the execution of a TRAPA instruction.
	General illegal instructions	Starts from the decoding of undefined code anytime except after a delayed branch instruction (delay slot).
	Illegal slot instructions	Starts from the decoding of undefined code placed in a delayed branch instruction (delay slot) or of instructions that rewrite the PC.

When exception processing starts, the CPU operates as follows:

1. Exception processing triggered by reset:

The initial values of the program counter (PC) and stack pointer (SP) are fetched from the exception processing vector table (PC and SP are respectively the H'00000000 and H'00000004 addresses for power-on resets and the H'00000008 and H'0000000C addresses for manual resets). See section 5.1.3, Exception Processing Vector Table, for more information. H'00000000 is then written to the vector base register (VBR) and H'F (1111) is written to the interrupt mask bits (I3 to I0) of the status register (SR). The program begins running from the PC address fetched from the exception processing vector table.

2. Exception processing triggered by address errors, interrupts and instructions:

SR and PC are saved to the stack indicated by R15. For interrupt exception processing, the interrupt priority level is written to the SR's interrupt mask bits (I3 to I0). For address error and instruction exception processing, the I3 to I0 bits are not affected. The start address is then fetched from the exception processing vector table and the program begins running from that address.



### 5.1.3 Exception Processing Vector Table

Before exception processing begins running, the exception processing vector table must be set in memory. The exception processing vector table stores the start addresses of exception service routines. (The reset exception processing table holds the initial values of PC and SP.)

All exception sources are given different vector numbers and vector table address offsets, from which the vector table addresses are calculated. During exception processing, the start addresses of the exception service routines are fetched from the exception processing vector table, which is indicated by this vector table address.

Table 5.3 shows the vector numbers and vector table address offsets. Table 5.4 shows how vector table addresses are calculated.

**Table 5.3 Exception Processing Vector Table**

Exception Sources		Vector Numbers	Vector Table Address Offset
Power-on reset	PC	0	H'00000000 to H'00000003
	SP	1	H'00000004 to H'00000007
Manual reset	PC	2	H'00000008 to H'0000000B
	SP	3	H'0000000C to H'0000000F
General illegal instruction		4	H'00000010 to H'00000013
(Reserved by system)		5	H'00000014 to H'00000017
Slot illegal instruction		6	H'00000018 to H'0000001B
(Reserved by system)		7	H'0000001C to H'0000001F
		8	H'00000020 to H'00000023
CPU address error		9	H'00000024 to H'00000027
DMAC address error		10	H'00000028 to H'0000002B
Interrupts	NMI	11	H'0000002C to H'0000002F
	User break	12	H'00000030 to H'00000033
(Reserved by system)		13	H'00000034 to H'00000037
		:	:
		31	H'0000007C to H'0000007F

**Table 5.3 Exception Processing Vector Table (cont)**

Exception Sources		Vector Numbers	Vector Table Address Offset
Trap instruction (user vector)		32	H'00000080 to H'00000083
		:	:
		63	H'000000FC to H'000000FF
Interrupts	IRQ0	64	H'00000100 to H'00000103
	IRQ1	65	H'00000104 to H'00000107
	IRQ2	66	H'00000108 to H'0000010B
	IRQ3	67	H'0000010C to H'0000010F
Reserved by system		68 to 71	H'00000110 to H'0000011F
On-chip peripheral module*		72	H'00000120 to H'00000124
		:	:
		255	H'000003FC to H'000003FF

Note: \* The vector numbers and vector table address offsets for each on-chip peripheral module interrupt are given in table 6.3, Interrupt Exception Processing Vectors and Priorities, in section 6, Interrupt Controller.

**Table 5.4 Calculating Exception Processing Vector Table Addresses**

Exception Source	Vector Table Address Calculation
Resets	Vector table address = (vector table address offset) = (vector number) × 4
Address errors, interrupts, instructions	Vector table address = VBR + (vector table address offset) = VBR + (vector number) × 4

- Notes: 1. VBR: Vector base register  
2. Vector table address offset: See table 5.3.  
3. Vector number: See table 5.3.

## 5.2 Resets

### 5.2.1 Types of Reset

A reset is the highest-priority exception processing source. There are two kinds of reset, power-on and manual. As shown in table 5.5, the CPU state is initialized in both a power-on reset and a manual reset. On-chip peripheral module registers are also initialized by a power-on reset, but not by a manual reset.

**Table 5.5 Exception Source Detection and Exception Processing Start Timing**

Type	Conditions for Transition to Reset State		Internal States		
	RES	WDT Overflow	CPU/MULT/ FPU/INTC	On-Chip Peripheral Modules	PFC, IO Port
Power-on reset	Low	—	Initialized	Initialized	Initialized
	High	Power-on reset	Initialized	Initialized	Not initialized
Manual reset	High	Manual reset	Initialized	Not initialized	Not initialized

### 5.2.2 Power-On Reset

**Power-On Reset by Means of  $\overline{\text{RES}}$  Pin:** When the  $\overline{\text{RES}}$  pin is driven low, the chip enters the power-on reset state. To reliably reset the chip, the  $\overline{\text{RES}}$  pin should be kept at the low level for at least the duration of the oscillation settling time at power-on or when in standby mode (when the clock is halted), or at least  $20 t_{\text{cyc}}$  when the clock is running. In the power-on reset state, the CPU's internal state and all the on-chip peripheral module registers are initialized. See Appendix B, Pin States, for the state of individual pins in the power-on reset state.

In the power-on reset state, power-on reset exception processing starts when the  $\overline{\text{RES}}$  pin is first driven low for a set period of time and then returned to high. The CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception processing vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception processing vector table.
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (I3 to I0) of the status register (SR) are set to H'F (1111).
4. The values fetched from the exception processing vector table are set in the PC and SP, and the program begins executing.

Be certain to always perform power-on reset processing when turning the system power on.

**Power-On Reset Initiated by WDT:** When a setting is made for a power-on reset to be generated in the WDT's watchdog timer mode, and the WDT's TCNT overflows, the chip enters the power-on reset state.

The pin function controller (PFC) registers and I/O port registers are not initialized by the reset signal generated by the WDT (these registers are only initialized by a power-on reset from off-chip).

If reset caused by the input signal at the  $\overline{\text{RES}}$  pin and a reset caused by WDT overflow occur simultaneously, the  $\overline{\text{RES}}$  pin reset has priority, and the WOVF bit in RSTCSR is cleared to 0. When WDT-initiated power-on reset processing is started, the CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception processing vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception processing vector table.
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (I3-I0) of the status register (SR) are set to H'F (1111).
4. The values fetched from the exception processing vector table are set in the PC and SP, and the program begins executing.

### 5.2.3 Manual Reset

When a setting is made for a manual reset to be generated in the WDT's watchdog timer mode, and the WDT's TCNT overflows, the chip enters the power-on reset state.

When WDT-initiated manual reset processing is started, the CPU operates as follows:

1. The initial value (execution start address) of the program counter (PC) is fetched from the exception processing vector table.
2. The initial value of the stack pointer (SP) is fetched from the exception processing vector table.
3. The vector base register (VBR) is cleared to H'00000000 and the interrupt mask bits (I3-I0) of the status register (SR) are set to H'F (1111).
4. The values fetched from the exception processing vector table are set in the PC and SP, and the program begins executing.

In a manual reset the bus cycle is retained, but if a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception processing will be deferred until the CPU acquires the bus. However, if the interval from generation of the manual reset until the end of the bus cycle is equal to or longer than the internal manual reset interval of 512 cycles, the internal manual reset source is ignored instead of being deferred, and manual reset exception processing is not executed.

## 5.3 Address Errors

### 5.3.1 Address Error Sources

Address errors occur when instructions are fetched or data read or written, as shown in table 5.6.

**Table 5.6 Bus Cycles and Address Errors**

<b>Bus Cycle</b>			
<b>Type</b>	<b>Bus Master</b>	<b>Bus Cycle Description</b>	<b>Address Errors</b>
Instruction fetch	CPU	Instruction fetched from even address	None (normal)
		Instruction fetched from odd address	Address error occurs
		Instruction fetched from other than on-chip peripheral module space*	None (normal)
		Instruction fetched from on-chip peripheral module space*	Address error occurs
		Instruction fetched from external memory space when in single chip mode	Address error occurs
Data read/write	CPU or DMAC	Word data accessed from even address	None (normal)
		Word data accessed from odd address	Address error occurs
		Longword data accessed from a longword boundary	None (normal)
		Longword data accessed from other than a long-word boundary	Address error occurs
		Byte or word data accessed in on-chip peripheral module space*	None (normal)
		Longword data accessed in 16-bit on-chip peripheral module space*	None (normal)
		Longword data accessed in 8-bit on-chip peripheral module space*	Address error occurs
		External memory space accessed when in single chip mode	Address error occurs

Note: \* See section 8, Bus State Controller, for details of the on-chip peripheral module space.

## 5.3.2 Address Error Exception Processing

When an address error occurs, the bus cycle in which the address error occurred ends. When the executing instruction then finishes, address error exception processing starts up. The CPU operates as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the last executed instruction.
3. The exception service routine start address is fetched from the exception processing vector table that corresponds to the address error that occurred and the program starts executing from that address. The jump that occurs is not a delayed branch.

## 5.4 Interrupts

### 5.4.1 Interrupt Sources

Table 5.7 shows the sources that start up interrupt exception processing. These are divided into NMI, user breaks, IRQ and on-chip peripheral modules.

**Table 5.7** Interrupt Sources

Type	Request Source	Number of Sources
NMI	NMI pin (external input)	1
User break	User break controller	1
IRQ	$\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$ (external input)	4
On-chip peripheral module	Direct memory access controller (DMAC)	4
	Advanced timer unit-II (ATU-II)	75
	Compare match timer (CMT)	2
	A/D converter (A/D)	2
	Serial communication interface (SCI)	20
	Watchdog timer (WDT)	1
	Hitachi controller area network (HCAN)	4

Each interrupt source is allocated a different vector number and vector table offset. See table 6.3, Interrupt Exception Processing Vectors and Priorities, in section 6, Interrupt Controller, for more information on vector numbers and vector table address offsets.

## 5.4.2 Interrupt Priority Level

The interrupt priority order is predetermined. When multiple interrupts occur simultaneously (overlap), the interrupt controller (INTC) determines their relative priorities and starts up processing according to the results.

The priority order of interrupts is expressed as priority levels 0 to 16, with priority 0 the lowest and priority 16 the highest. The NMI interrupt has priority 16 and cannot be masked, so it is always accepted. The user break interrupt and H-UDI interrupt priority level is 15. IRQ interrupts and on-chip peripheral module interrupt priority levels can be set freely using the INTC's interrupt priority registers A, C to L (IPRA, IPRC to IPRL) as shown in table 5.8. The priority levels that can be set are 0 to 15. Level 16 cannot be set. See section 6.3.1, Interrupt Priority Registers A, C to L (IPRA, IPRC to IPRL), for details of the interrupt priority registers.

**Table 5.8 Interrupt Priority Order**

Type	Priority Level	Comment
NMI	16	Fixed priority level. Cannot be masked.
User break	15	Fixed priority level.
IRQ	0 to 15	Set with interrupt priority level setting registers A and C through L (IPRA, IPRC to IPRL).
On-chip peripheral module	0 to 15	Set with interrupt priority level setting registers A and C through L (IPRA, IPRC to IPRL).

## 5.4.3 Interrupt Exception Processing

When an interrupt occurs, its priority level is ascertained by the interrupt controller (INTC). NMI is always accepted, but other interrupts are only accepted if they have a priority level higher than the priority level set in the interrupt mask bits (I3 to I0) of the status register (SR).

When an interrupt is accepted, exception processing begins. In interrupt exception processing, the CPU saves SR and the program counter (PC) to the stack. The priority level value of the accepted interrupt is written to SR bits I3 to I0. For NMI, however, the priority level is 16, but the value set in I3 to I0 is H'F (level 15). Next, the start address of the exception service routine is fetched from the exception processing vector table for the accepted interrupt, that address is jumped to and execution begins. See section 6.4, Interrupt Operation, for further details.

## 5.5 Exceptions Triggered by Instructions

### 5.5.1 Types of Exceptions Triggered by Instructions

Exception processing can be triggered by trap instructions, general illegal instructions, and illegal slot instructions, as shown in table 5.9.

**Table 5.9** Types of Exceptions Triggered by Instructions

Type	Source Instruction	Comment
Trap instructions	TRAPA	
Illegal slot instructions	Undefined code placed immediately after a delayed branch instruction (delay slot) and instructions that rewrite the PC	Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, BRAF Instructions that rewrite the PC: JMP, JSR, BRA, BSR, RTS, RTE, BT, BF, TRAPA, BF/S, BT/S, BSRF, BRAF
General illegal instructions	Undefined code anywhere besides in a delay slot	

### 5.5.2 Trap Instructions

When a TRAPA instruction is executed, trap instruction exception processing starts up. The CPU operates as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the TRAPA instruction.
3. The exception service routine start address is fetched from the exception processing vector table that corresponds to the vector number specified in the TRAPA instruction. That address is jumped to and the program starts executing. The jump that occurs is not a delayed branch.



### 5.5.3 Illegal Slot Instructions

An instruction placed immediately after a delayed branch instruction is said to be placed in a delay slot. When the instruction placed in the delay slot is undefined code, illegal slot exception processing starts up when that undefined code is decoded. Illegal slot exception processing also starts up when an instruction that rewrites the program counter (PC) is placed in a delay slot. The processing starts when the instruction is decoded. The CPU handles an illegal slot instruction as follows:

1. The status register (SR) is saved to the stack.
2. The program counter (PC) is saved to the stack. The PC value saved is the jump address of the delayed branch instruction immediately before the undefined code or the instruction that rewrites the PC.
3. The exception service routine start address is fetched from the exception processing vector table that corresponds to the exception that occurred. That address is jumped to and the program starts executing. The jump that occurs is not a delayed branch.

### 5.5.4 General Illegal Instructions

When undefined code placed anywhere other than immediately after a delayed branch instruction (i.e., in a delay slot) is decoded, general illegal instruction exception processing starts up. The CPU handles general illegal instructions in the same way as illegal slot instructions. Unlike processing of illegal slot instructions, however, the program counter value stored is the start address of the undefined code.

## 5.6 When Exception Sources Are Not Accepted

When an address error or interrupt is generated after a delayed branch instruction or interrupt-disabled instruction, it is sometimes not accepted immediately but stored instead, as shown in table 5.10. When this happens, it will be accepted when an instruction that can accept the exception is decoded.

**Table 5.10 Generation of Exception Sources Immediately after a Delayed Branch Instruction or Interrupt-Disabled Instruction**

Point of Occurrence	Exception Source		
	Bus Error	Interrupt	FPU Exception
Immediately after a delayed branch instruction* <sup>1</sup>	Not accepted	Not accepted	Not accepted
Immediately after an interrupt-disabled instruction* <sup>2</sup>	Not accepted* <sup>3</sup>	Not accepted	Accepted

Notes: 1. Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, BRAF  
2. Interrupt-disabled instructions: LDC, LDC.L, STC, STC.L, LDS, LDS.L, STS, STS.L  
3. In the SH-2 a bus error is accepted.

## 5.7 Stack Status after Exception Processing Ends

The status of the stack after exception processing ends is as shown in table 5.11.

**Table 5.11 Stack Status After Exception Processing Ends**

Exception Type	Stack Status
Address error	<p>SP → Address of instruction after executed instruction 32 bits</p> <p>SR 32 bits</p>
Trap instruction	<p>SP → Address of instruction after TRAPA instruction 32 bits</p> <p>SR 32 bits</p>
General illegal instruction	<p>SP → Start address of illegal instruction 32 bits</p> <p>SR 32 bits</p>
Interrupt	<p>SP → Address of instruction after executed instruction 32 bits</p> <p>SR 32 bits</p>
Illegal slot instruction	<p>SP → Jump destination address of delay branch instruction 32 bits</p> <p>SR 32 bits</p>

## **5.8 Usage Notes**

### **5.8.1 Value of Stack Pointer (SP)**

The value of the stack pointer must always be a multiple of four. If it is not, an address error will occur when the stack is accessed during exception processing.

### **5.8.2 Value of Vector Base Register (VBR)**

The value of the vector base register must always be a multiple of four. If it is not, an address error will occur when the stack is accessed during exception processing.

### **5.8.3 Address Errors Caused by Stacking of Address Error Exception Processing**

When the stack pointer is not a multiple of four, an address error will occur during stacking of the exception processing (interrupts, etc.) and address error exception processing will start up as soon as the first exception processing is ended. Address errors will then also occur in the stacking for this address error exception processing. To ensure that address error exception processing does not go into an endless loop, no address errors are accepted at that point. This allows program control to be shifted to the address error exception service routine and enables error processing.

When an address error occurs during exception processing stacking, the stacking bus cycle (write) is executed. During stacking of the status register (SR) and program counter (PC), the SP is decremented by 4 for both, so the value of SP will not be a multiple of four after the stacking either. The address value output during stacking is the SP value, so the address where the error occurred is itself output. This means the write data stacked will be undefined.

# Section 6 Interrupt Controller (INTC)

## 6.1 Overview

The interrupt controller (INTC) ascertains the priority of interrupt sources and controls interrupt requests to the CPU. The INTC has registers for setting the priority of each interrupt which can be used by the user to order the priorities in which the interrupt requests are processed.

### 6.1.1 Features

The INTC has the following features:

- 16 levels of interrupt priority  
By setting the twelve interrupt-priority level registers, the priorities of IRQ interrupts and on-chip peripheral module interrupts can be set in 16 levels for different request sources.
- NMI noise canceler function  
NMI input level bits indicate the NMI pin status. By reading these bits with the interrupt exception service routine, the pin status can be confirmed, enabling it to be used as a noise canceler.

## 6.1.2 Block Diagram

Figure 6.1 is a block diagram of the INTC.

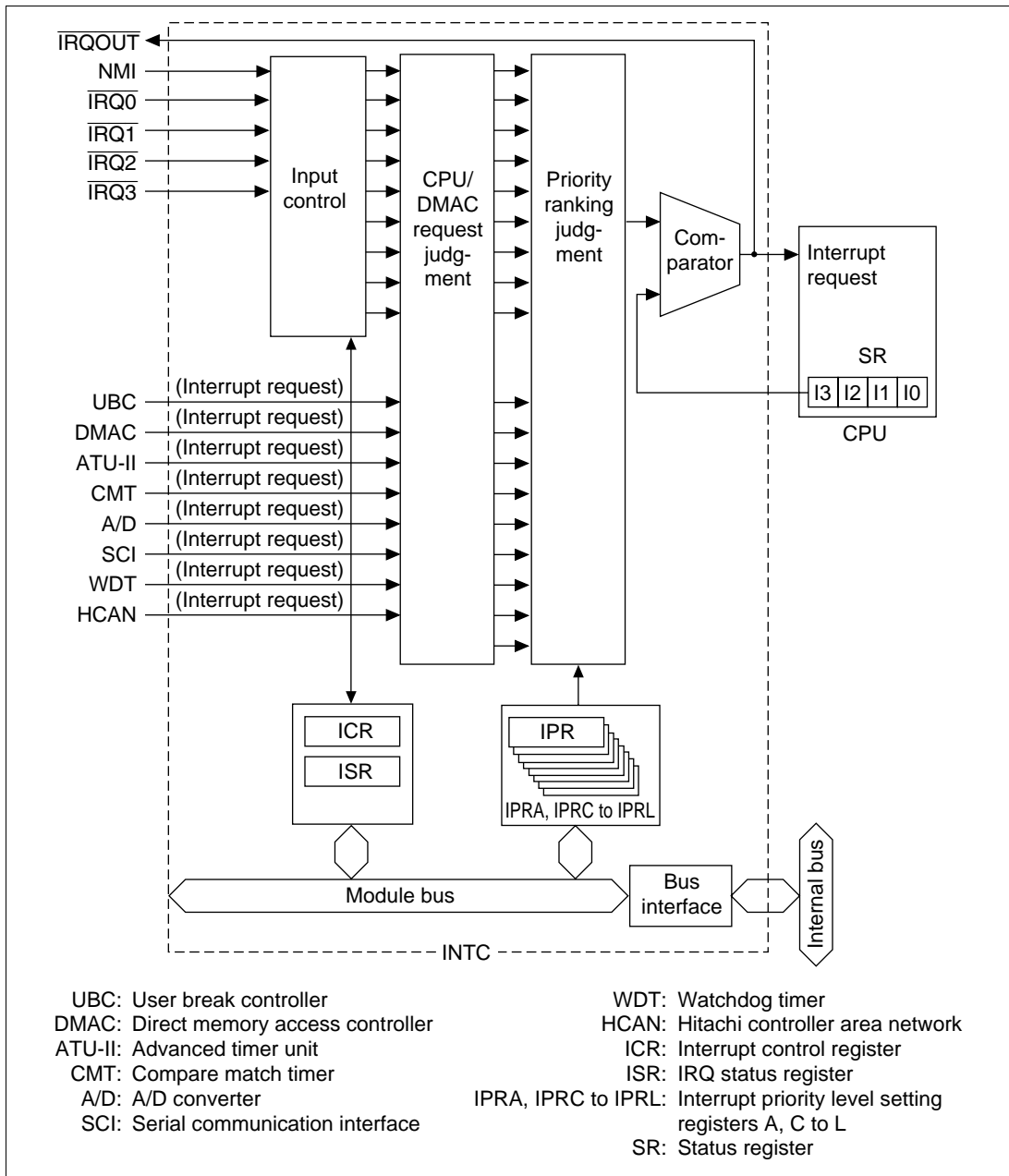


Figure 6.1 INTC Block Diagram

### 6.1.3 Pin Configuration

Table 6.1 shows the INTC pin configuration.

**Table 6.1 Pin Configuration**

Name	Abbreviation	I/O	Function
Non-maskable interrupt input pin	NMI	I	Input of non-maskable interrupt request signal
Interrupt request input pins	$\overline{IRQ0}$ to $\overline{IRQ3}$	I	Input of maskable interrupt request signals

### 6.1.4 Register Configuration

The INTC has the 14 registers shown in table 6.2. These registers set the priority of the interrupts and control external interrupt input signal detection.

**Table 6.2 Register Configuration**

Name	Abbr.	R/W	Initial Value	Address	Access Sizes
Interrupt priority register A	IPRA	R/W	H'0000	H'FFFF ED00	8, 16, 32
Interrupt priority register C	IPRC	R/W	H'0000	H'FFFF ED04	8, 16, 32
Interrupt priority register D	IPRD	R/W	H'0000	H'FFFF ED06	8, 16, 32
Interrupt priority register E	IPRE	R/W	H'0000	H'FFFF ED08	8, 16, 32
Interrupt priority register F	IPRF	R/W	H'0000	H'FFFF ED0A	8, 16, 32
Interrupt priority register G	IPRG	R/W	H'0000	H'FFFF ED0C	8, 16, 32
Interrupt priority register H	IPRH	R/W	H'0000	H'FFFF ED0E	8, 16, 32
Interrupt priority register I	IPRI	R/W	H'0000	H'FFFF ED10	8, 16, 32
Interrupt priority register J	IPRJ	R/W	H'0000	H'FFFF ED12	8, 16, 32
Interrupt priority register K	IPRK	R/W	H'0000	H'FFFF ED14	8, 16, 32
Interrupt priority register L	IPRL	R/W	H'0000	H'FFFF ED16	8, 16, 32
Interrupt control register	ICR	R/W	*1	H'FFFF ED18	8, 16, 32
IRQ status register	ISR	R(W)*2	H'0000	H'FFFF ED1A	8, 16, 32

Notes: Three access cycles are required for byte access and word access, and six cycles for longword access.

1. The value when the NMI pin is high is H'8000; when the NMI pin is low, it is H'0000.
2. Only 0 can be written, in order to clear flags.

## 6.2 Interrupt Sources

There are five types of interrupt sources: NMI, user breaks, H-UDI, IRQ, and on-chip peripheral modules. Each interrupt has a priority expressed as a priority level (0 to 16, with 0 the lowest and 16 the highest). Giving an interrupt a priority level of 0 masks it.

### 6.2.1 NMI Interrupts

The NMI interrupt has priority 16 and is always accepted. Input at the NMI pin is detected by edge. Use the NMI edge select bit (NMIE) in the interrupt control register (ICR) to select either the rising or falling edge. NMI interrupt exception processing sets the interrupt mask level bits (I3 to I0) in the status register (SR) to level 15.

### 6.2.2 User Break Interrupt

A user break interrupt has a priority of level 15, and occurs when the break condition set in the user break controller (UBC) is satisfied. User break interrupt requests are detected by edge and are held until accepted. User break interrupt exception processing sets the interrupt mask level bits (I3 to I0) in the status register (SR) to level 15. For more information about the user break interrupt, see section 7, User Break Controller.

### 6.2.3 IRQ Interrupts

IRQ interrupts are requested by input from pins  $\overline{\text{IRQ0}}$  to  $\overline{\text{IRQ3}}$ . Set the IRQ sense select bits (IRQ0S to IRQ3S) of the interrupt control register (ICR) to select low level detection or falling edge detection for each pin. The priority level can be set from 0 to 15 for each pin using interrupt priority registers A and B (IPRA to IPRB).

When IRQ interrupts are set to low level detection, an interrupt request signal is sent to the INTC during the period the IRQ pin is low. Interrupt request signals are not sent to the INTC when the IRQ pin becomes high. Interrupt request levels can be confirmed by reading the IRQ flags (IRQ0F to IRQ3F) of the IRQ status register (ISR).

When IRQ interrupts are set to falling edge detection, interrupt request signals are sent to the INTC upon detecting a change on the IRQ pin from high to low level. IRQ interrupt request detection results are maintained until the interrupt request is accepted. Confirmation that IRQ interrupt requests have been detected is possible by reading the IRQ flags (IRQ0F to IRQ3F) of the IRQ status register (ISR), and by writing a 0 after reading a 1, IRQ interrupt request detection results can be withdrawn.

In IRQ interrupt exception processing, the interrupt mask bits (I3 to I0) of the status register (SR) are set to the priority level value of the accepted IRQ interrupt.



## 6.2.4 On-Chip Peripheral Module Interrupts

On-chip peripheral module interrupts are interrupts generated by the following on-chip peripheral modules:

- Direct memory access controller (DMAC)
- Advanced timer unit (ATU-II)
- Compare match timer (CMT)
- A/D converter (A/D)
- Serial communication interface (SCI)
- Watchdog timer (WDT)
- Hitachi controller area network (HCAN)

A different interrupt vector is assigned to each interrupt source, so the exception service routine does not have to decide which interrupt has occurred. Priority levels between 0 and 15 can be assigned to individual on-chip peripheral modules in interrupt priority registers C to L (IPRC to IPRL).

On-chip peripheral module interrupt exception processing sets the interrupt mask level bits (I3 to I0) in the status register (SR) to the priority level value of the on-chip peripheral module interrupt that was accepted.

## 6.2.5 Interrupt Exception Vectors and Priority Rankings

Table 6.3 lists interrupt sources and their vector numbers, vector table address offsets and interrupt priorities.

Each interrupt source is allocated a different vector number and vector table address offset. Vector table addresses are calculated from vector numbers and address offsets. In interrupt exception processing, the exception service routine start address is fetched from the vector table indicated by the vector table address. See table 5.4, Calculating Exception Processing Vector Table Addresses, in section 5, Exception Processing.

IRQ interrupts and on-chip peripheral module interrupt priorities can be set freely between 0 and 15 for each pin or module by setting interrupt priority registers A and C to L (IPRA, IPRC to IPRL). The ranking of interrupt sources for IPRC to IPRL, however, must be the order listed under Priority within IPR Setting Range in table 6.3 and cannot be changed. A power-on reset assigns priority level 0 to IRQ interrupts and on-chip peripheral module interrupts. If the same priority level is assigned to two or more interrupt sources and interrupts from those sources occur simultaneously, their priority order is the default priority order indicated at the right in table 6.3.

**Table 6.3 Interrupt Exception Processing Vectors and Priorities**

Interrupt Source	Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR		Default Priority
	Vector No.	Vector Table Address Offset			Setting Range		
NMI	11	H'0000002C to H'0000002F	16	—	—	—	High
UBC	12	H'00000030 to H'00000033	15	—	—	—	
IRQ0	64	H'00000100 to H'00000103	0 to 15 (0)	IPRA (15 to 12)	—	—	
IRQ1	65	H'00000104 to H'00000107	0 to 15 (0)	IPRA (11 to 8)	—	—	
IRQ2	66	H'00000108 to H'0000010B	0 to 15 (0)	IPRA (7 to 4)	—	—	
IRQ3	67	H'0000010C to H'0000010F	0 to 15 (0)	IPRA (3 to 0)	—	—	
DMAC0	DEI0	72	H'00000120 to H'00000123	0 to 15 (0)	IPRC (15 to 12)	↑ 1	
DMAC1	DEI1	74	H'00000128 to H'0000012B	0 to 15 (0)		↓ 2	
DMAC2	DEI2	76	H'00000130 to H'00000133	0 to 15 (0)	IPRC (11 to 8)	↑ 1	
DMAC3	DEI3	78	H'00000138 to H'0000013B	0 to 15 (0)		↓ 2	
ATU0	ATU01	ITV1 ITV2A ITV2B	80	H'00000140 to H'00000143	0 to 15 (0)	IPRC (7 to 4)	
	ATU02	ICI0A	84	H'00000150 to H'00000153	0 to 15 (0)		↑ 1
		ICI0B	86	H'00000158 to H'0000015B		↓ 2	
ATU03	ICI0C	88	H'00000160 to H'00000163	0 to 15 (0)	IPRD (15 to 12)	↑ 1	
	ICI0D	90	H'00000168 to H'0000016B			↓ 2	
ATU04	OVI0	92	H'00000170 to H'00000173	0 to 15 (0)	IPRD (11 to 8)	—	Low

**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range		Default Priority
		Vector No.	Vector Address Offset					
ATU1	ATU11	IMI1A/CMI1	96	H'00000180 to H'00000183	0 to 15 (0)	IPRD (7 to 4)	↑ 1	High ↑ ↓ Low
		IMI1B	97	H'00000184 to H'00000187			2	
		IMI1C	98	H'00000188 to H'0000018B			3	
		IMI1D	99	H'0000018C to H'0000018F			↓ 4	
	ATU12	IMI1E	100	H'00000190 to H'00000193	0 to 15 (0)	IPRD (3 to 0)	↑ 1	
		IMI1F	101	H'00000194 to H'00000197			2	
		IMI1G	102	H'00000198 to H'0000019B			3	
		IMI1H	103	H'0000019C to H'0000019F			↓ 4	
ATU13	OVI1A/OVI1B	104	H'000001A0 to H'000001A3	0 to 15 (0)	IPRE (15 to 12)		Low	

**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR		Default Priority	
		Vector No.	Vector Table Address Offset			Setting Range			
ATU2	ATU21	IMI2A/ CMI2A	108	H'000001B0 to H'000001B3	0 to 15 (0)	IPRE (11 to 8)	↑	1	High ↑
		IMI2B/ CMI2B	109	H'000001B4 to H'000001B7			2		
		IMI2C/ CMI2C	110	H'000001B8 to H'000001BB			3		
		IMI2D/ CMI2D	111	H'000001BC to H'000001BF			↓	4	
ATU22	ATU22	IMI2E/ CMI2E	112	H'000001C0 to H'000001C3	0 to 15 (0)	IPRE (7 to 4)	↑	1	↑
		IMI2F/ CMI2F	113	H'000001C4 to H'000001C7			2		
		IMI2G/ CMI2G	114	H'000001C8 to H'000001CB			3		
		IMI2H/ CMI2H	115	H'000001CC to H'000001CF			↓	4	
ATU23	OVI2A/ OVI2B	116	H'000001D0 to H'000001D3	0 to 15 (0)	IPRE (3 to 0)				
ATU3	ATU31	IMI3A	120	H'000001E0 to H'000001E3	0 to 15 (0)	IPRF (15 to 12)	↑	1	↑
		IMI3B	121	H'000001E4 to H'000001E7			2		
		IMI3C	122	H'000001E8 to H'000001EB			3		
		IMI3D	123	H'000001EC to H'000001EF			↓	4	
ATU32	OVI3	124	H'000001F0 to H'000001F3	0 to 15 (0)	IPRF (11 to 8)			Low ↓	

**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range		Default Priority
		Vector No.	Vector Address Offset					
ATU4	ATU41	IMI4A	128	H'00000200 to H'00000203	0 to 15 (0)	IPRF (7 to 4)	↑ 1	High
		IMI4B	129	H'00000204 to H'00000207			2	
		IMI4C	130	H'00000208 to H'0000020B			3	
		IMI4D	131	H'0000020C to H'0000020F			↓ 4	
ATU42	OVI4	132	H'00000210 to H'00000213	0 to 15 (0)	IPRF (3 to 0)			
ATU5	ATU51	IMI5A	136	H'00000220 to H'00000223	0 to 15 (0)	IPRG (15 to 12)	↑ 1	
		IMI5B	137	H'00000224 to H'00000227			2	
		IMI5C	138	H'00000228 to H'0000022B			3	
		IMI5D	139	H'0000022C to H'0000022F			↓ 4	
ATU52	OVI5	140	H'00000230 to H'00000233	0 to 15 (0)	IPRG (11 to 8)			
ATU6		CMI6A	144	H'00000240 to H'00000243	0 to 15 (0)	IPRG (7 to 4)	↑ 1	
		CMI6B	145	H'00000244 to H'00000247			2	
		CMI6C	146	H'00000248 to H'0000024B			3	
		CMI6D	147	H'0000024C to H'0000024F			↓ 4	

**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source	Interrupt Vector			Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR		Default Priority	
	Vector No.	Vector Address Offset	Table Address Offset			Setting Range			
ATU7	CMI7A	148	H'00000250 to H'00000253	0 to 15 (0)	IPRG (3 to 0)	↑	1	High	
	CMI7B	149	H'00000254 to H'00000257			2			
	CMI7C	150	H'00000258 to H'0000025B			3			
	CMI7D	151	H'0000025C to H'0000025F			↓	4		
ATU8	ATU81	OSI8A	152	H'00000260 to H'00000263	0 to 15 (0)	IPRH (15 to 12)	↑	1	↑
		OSI8B	153	H'00000264 to H'00000267			2		
		OSI8C	154	H'00000268 to H'0000026B			3		
		OSI8D	155	H'0000026C to H'0000026F			↓	4	
	ATU82	OSI8E	156	H'00000270 to H'00000273	0 to 15 (0)	IPRH (11 to 8)	↑	1	
		OSI8F	157	H'00000274 to H'00000277			2		
		OSI8G	158	H'00000278 to H'0000027B			3		
		OSI8H	159	H'0000027C to H'0000027F			↓	4	
	ATU83	OSI8I	160	H'00000280 to H'00000283	0 to 15 (0)	IPRH (7 to 4)	↑	1	
		OSI8J	161	H'00000284 to H'00000287			2		
		OSI8K	162	H'00000288 to H'0000028B			3		
		OSI8L	163	H'0000028C to H'0000028F			↓	4	

**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range		Default Priority	
		Vector No.	Vector Address Offset						
ATU8	ATU84	OSI8M	164	H'00000290 to H'00000293	0 to 15 (0)	IPRH (3 to 0)	↑ 1	High	
		OSI8N	165	H'00000294 to H'00000297			2		
		OSI8O	166	H'00000298 to H'0000029B			3		
		OSI8P	167	H'0000029C to H'0000029F			↓ 4		
ATU9	ATU91	CMI9A	168	H'000002A0 to H'000002A3	0 to 15 (0)	IPRI (15 to 12)	↑ 1	↑ High       ↓ Low	
		CMI9B	169	H'000002A4 to H'000002A7			2		
		CMI9C	170	H'000002A8 to H'000002AB			3		
		CMI9D	171	H'000002AC to H'000002AF			↓ 4		
	ATU92	CMI9E	172	H'000002B0 to H'000002B3	0 to 15 (0)	IPRI (11 to 8)	↑ 1		
		CMI9F	174	H'000002B8 to H'000002BB			↓ 2		
	ATU10	ATU101	CMI10A	176	H'000002C0 to H'000002C3	0 to 15 (0)	IPRI (7 to 4)		↑ 1
			CMI10B	178	H'000002C8 to H'000002CB				↓ 2
ATU102		ICI10A/ CMI10G	180	H'000002D0 to H'000002D3	0 to 15(0)	IPRI (3 to 0)			
ATU11	IMI11A	184	H'000002E0 to H'000002E3	0 to 15 (0)	IPRJ (15 to 12)	↑ 1			
		186	H'000002E8 to H'000002EB			2			
	OVI11	187	H'000002EC to H'000002EF			↓ 3	Low		

**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source	Vector No.	Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range		Default Priority
		Vector Address	Table Offset			Setting	Range	
CMT0	CMTI0	188	H'000002F0 to H'000002F3	0 to 15 (0)	I PRJ (11 to 8)	↑	1	High ↑ ↓ Low
A/D0	ADI0	190	H'000002F8 to H'000002FB			↓	2	
CMT1	CMTI1	192	H'00000300 to H'00000303	0 to 15 (0)	IPRJ (7 to 4)	↑	1	
A/D1	ADI1	194	H'00000308 to H'0000030B			↓	2	
SCIO	ERI0	200	H'00000320 to H'00000323	0 to 15 (0)	IPRK (15 to 12)	↑	1	
	RXI0	201	H'00000324 to H'00000327			2		
	TXI0	202	H'00000328 to H'0000032B			3		
	TEI0	203	H'0000032C to H'0000032F			↓	4	
SCI1	ERI1	204	H'00000330 to H'00000333	0 to 15 (0)	IPRK (11 to 8)	↑	1	
	RXI1	205	H'00000334 to H'00000337			2		
	TXI1	206	H'00000338 to H'0000033B			3		
	TEI1	207	H'0000033C to H'0000033F			↓	4	
SCI2	ERI2	208	H'00000340 to H'00000343	0 to 15 (0)	IPRK (7 to 4)	↑	1	
	RXI2	209	H'00000344 to H'00000347			2		
	TXI2	210	H'00000348 to H'0000034B			3		
	TEI2	211	H'0000034C to H'0000034F			↓	4	



**Table 6.3 Interrupt Exception Processing Vectors and Priorities (cont)**

Interrupt Source	Vector No.	Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range		Default Priority
		Vector Address	Offset			Setting	Range	
SCI3	ERI3	212	H'00000350 to H'00000353	0 to 15 (0)	IPRK (3 to 0)	↑	1	High
	RXI3	213	H'00000354 to H'00000357			2		
	TXI3	214	H'00000358 to H'0000035B			3		
	TEI3	215	H'0000035C to H'0000035F			↓	4	
SCI4	ERI4	216	H'00000360 to H'00000363	0 to 15 (0)	IPRL (15 to 12)	↑	1	↑
	RXI4	217	H'00000364 to H'00000367			2		
	TXI4	218	H'00000368 to H'0000036B			3		
	TEI4	219	H'0000036C to H'0000036F			↓	4	
HCAN	ERS	220	H'00000370 to H'00000373	0 to 15 (0)	IPRL (11 to 8)	↑	1	↓
	OVR	221	H'00000374 to H'00000377			2		
	RM	222	H'00000378 to H'0000037B			3		
	SLE	223	H'0000037C to H'0000037F			↓	4	
WDT	ITI	224	H'00000380 to H'00000383	0 to 15 (0)	IPRL (7 to 4)			Low

## 6.3 Description of Registers

### 6.3.1 Interrupt Priority Registers A, C to L (IPRA, IPRC to IPRL)

Interrupt priority registers A, C to L (IPRA, IPRC to IPRL) are 16-bit readable/writable registers that set priority levels from 0 to 15 for IRQ interrupts and on-chip peripheral module interrupts. Correspondence between interrupt request sources and each of the IPRA, IPRC to IPRL bits is shown in table 6.4.

Bit:	15	14	13	12	11	10	9	8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 6.4** Interrupt Request Sources and IPRA, IPRC to IPRL

Register	Bits			
	15 to 12	11 to 8	7 to 4	3 to 0
Interrupt priority register A	IRQ0	IRQ1	IRQ2	IRQ3
Interrupt priority register C	DMAC0, 1	DMAC2, 3	ATU01	ATU02
Interrupt priority register D	ATU03	ATU04	ATU11	ATU12
Interrupt priority register E	ATU13	ATU21	ATU22	ATU23
Interrupt priority register F	ATU31	ATU32	ATU41	ATU42
Interrupt priority register G	ATU51	ATU52	ATU6	ATU7
Interrupt priority register H	ATU81	ATU82	ATU83	ATU84
Interrupt priority register I	ATU91	ATU92	ATU101	ATU102
Interrupt priority register J	ATU11	CMT0, A/D0	CMT1, A/D1	—
Interrupt priority register K	SCI0	SCI1	SCI2	SCI3
Interrupt priority register L	SCI4	HCAN	WDT	—

As indicated in table 6.4, four  $\overline{\text{IRQ}}$  pins or groups of 4 on-chip peripheral modules are allocated to each register. Each of the corresponding interrupt priority ranks are established by setting a value from H'0 (0000) to H'F (1111) in each of the four-bit groups 15 to 12, 11 to 8, 7 to 4 and 3 to 0. Interrupt priority rank becomes level 0 (lowest) by setting H'0, and level 15 (highest) by setting H'F. If multiple on-chip peripheral modules are assigned to the same bit (DMAC0 and DMAC1, DMAC2 and DMAC3, CMT0 and A/D0, and CMT1 and A/D1), those multiple modules are set to the same priority rank.

IPRA, IPRC to IPRL are initialized to H'0000 by a reset and in hardware standby mode. They are not initialized in software standby mode.

### 6.3.2 Interrupt Control Register (ICR)

ICR is a 16-bit register that sets the input signal detection mode of the external interrupt input pin NMI and  $\overline{\text{IRQ0}}$  to  $\overline{\text{IRQ3}}$  and indicates the input signal level at the NMI pin. A reset and hardware standby mode initialize ICR but the software standby mode does not.

Bit:	15	14	13	12	11	10	9	8
	NMIL	—	—	—	—	—	—	NMIE
Initial value:	*	0	0	0	0	0	0	0
R/W:	R	—	—	—	—	—	—	R/W
Bit:	7	6	5	4	3	2	1	0
	$\overline{\text{IRQ0S}}$	$\overline{\text{IRQ1S}}$	$\overline{\text{IRQ2S}}$	$\overline{\text{IRQ3S}}$	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	—	—	—	—

Note: \* When NMI input is high: 1; when NMI input is low: 0

- Bit 15—NMI Input Level (NMIL): Sets the level of the signal input at the NMI pin. This bit can be read to determine the NMI pin level. This bit cannot be modified.

Bit 15: NMIL	Description
0	NMI input level is low
1	NMI input level is high

- Bits 14 to 9—Reserved: These bits always read 0. The write value should always be 0.

- Bit 8—NMI Edge Select (NMIE)

Bit 8: NMIE	Description
0	Interrupt request is detected on falling edge of NMI input (Initial value)
1	Interrupt request is detected on rising edge of NMI input

- Bits 7 to 4—IRQ0 to IRQ3 Sense Select (IRQ0S to IRQ3S): These bits set the IRQ0 to IRQ3 interrupt request detection mode.

Bits 7 to 4: IRQ0S to IRQ3S	Description
0	Interrupt request is detected on low level of IRQ input (Initial value)
1	Interrupt request is detected on falling edge of IRQ input

- Bits 3 to 0—Reserved: These bits always read 0. The write value should always be 0.

### 6.3.3 IRQ Status Register (ISR)

ISR is a 16-bit register that indicates the interrupt request status of the external interrupt input pins  $\overline{\text{IRQ0}}$  to  $\overline{\text{IRQ3}}$ . When IRQ interrupts are set to edge detection, held interrupt requests can be withdrawn by writing 0 to  $\text{IRQnF}$  after reading  $\text{IRQnF} = 1$ .

A reset and hardware standby mode initialize ISR but software standby mode does not.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	IRQ0F	IRQ1F	IRQ2F	IRQ3F	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R

- Bits 15 to 8—Reserved: These bits always read 0. The write value should always be 0.

- Bits 7 to 4—IRQ0 to IRQ3 Flags (IRQ0F to IRQ3F): These bits display the IRQ0 to IRQ3 interrupt request status.

**Bits 7 to 4:**

IRQ0F to IRQ3F	Detection Setting	Description
0	Level detection	No IRQn interrupt request exists [Clearing condition] When $\overline{\text{IRQn}}$ input is high
	Edge detection	No IRQn interrupt request was detected (Initial value) [Clearing conditions] <ul style="list-style-type: none"> <li>• When 0 is written after reading <math>\text{IRQnF} = 1</math></li> <li>• When IRQn interrupt exception processing has been executed</li> </ul>
1	Level detection	An IRQn interrupt request exists [Setting condition] When $\overline{\text{IRQn}}$ input is low
	Edge detection	An IRQn interrupt request was detected [Setting condition] When a falling edge occurs at an $\overline{\text{IRQn}}$ input

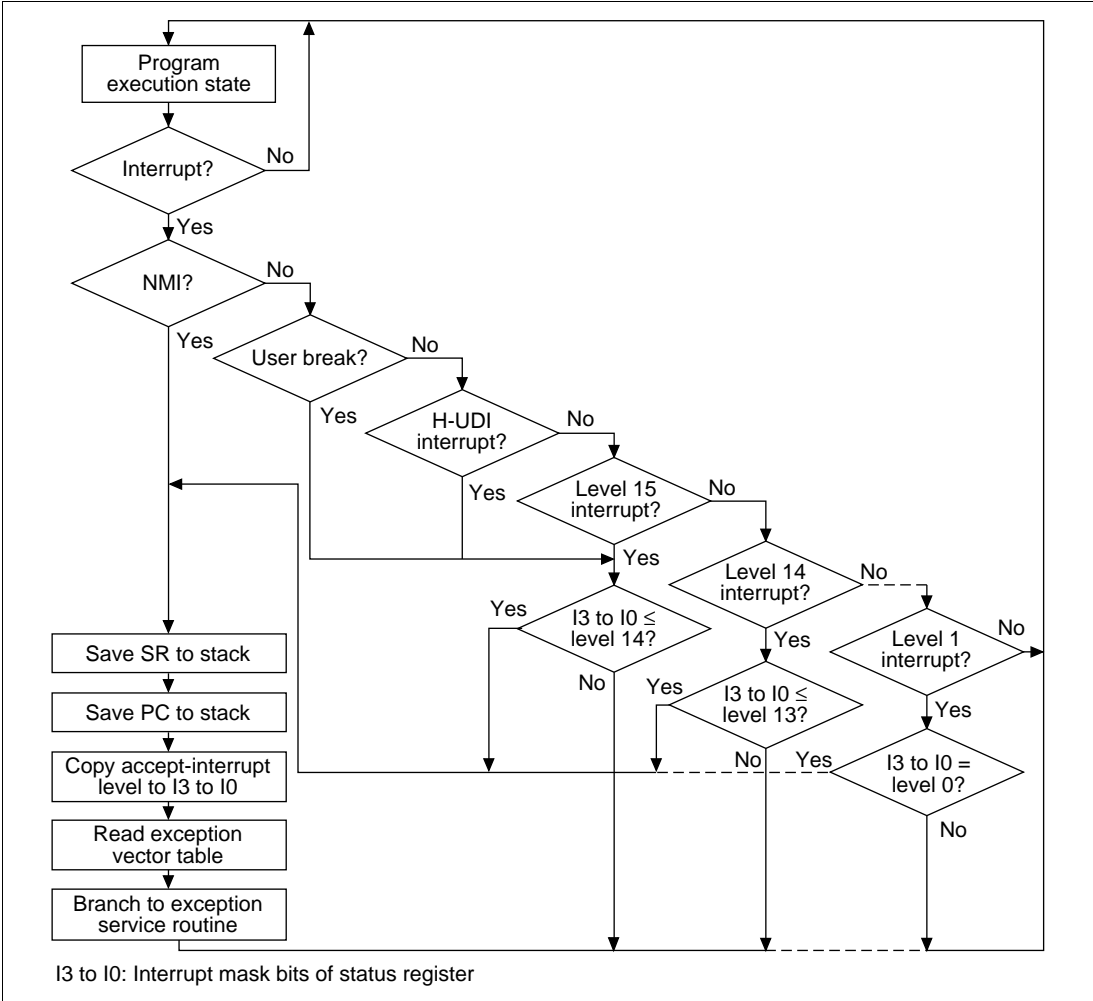
- Bits 3 to 0—Reserved: These bits always read 0. The write value should always be 0.

## 6.4 Interrupt Operation

### 6.4.1 Interrupt Sequence

The sequence of interrupt operations is explained below. Figure 6.2 is a flowchart of the operations.

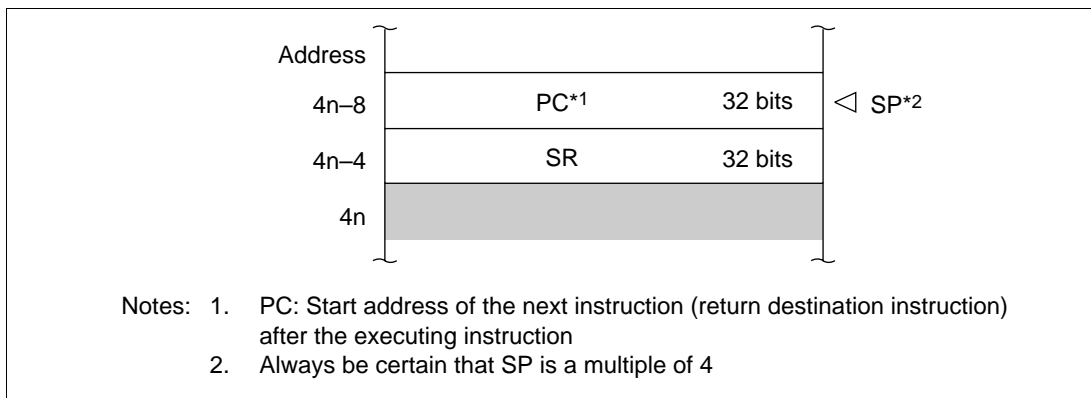
1. The interrupt request sources send interrupt request signals to the interrupt controller.
2. The interrupt controller selects the highest priority interrupt in the interrupt requests sent, following the priority levels set in interrupt priority registers A, C to L (IPRA, IPRC to IPRL). Lower-priority interrupts are ignored. They are held pending until interrupt requests designated as edge-detect type are accepted. For IRQ interrupts, however, withdrawal is possible by accessing the IRQ status register (ISR). See section 6.2.3, IRQ Interrupts, for details. Interrupts held pending due to edge detection are cleared by a power-on reset or a manual reset. If two of these interrupts have the same priority level or if multiple interrupts occur within a single module, the interrupt with the highest default priority or the highest priority within its IPR setting range (as indicated in table 6.3) is selected.
3. The interrupt controller compares the priority level of the selected interrupt request with the interrupt mask bits (I3 to I0) in the CPU's status register (SR). If the request priority level is equal to or less than the level set in I3 to I0, the request is ignored. If the request priority level is higher than the level in bits I3 to I0, the interrupt controller accepts the interrupt and sends an interrupt request signal to the CPU.
4. The CPU detects the interrupt request sent from the interrupt controller when it decodes the next instruction to be executed. Instead of executing the decoded instruction, the CPU starts interrupt exception processing (figure 6.4).
5. SR and PC are saved onto the stack.
6. The priority level of the accepted interrupt is copied to the interrupt mask level bits (I3 to I0) in the status register (SR).
7. The CPU reads the start address of the exception service routine from the exception vector table for the accepted interrupt, jumps to that address, and starts executing the program there. This jump is not a delay branch.



**Figure 6.2 Interrupt Sequence Flowchart**

## 6.4.2 Stack after Interrupt Exception Processing

Figure 6.3 shows the stack after interrupt exception processing.



**Figure 6.3 Stack after Interrupt Exception Processing**



## 6.5 Interrupt Response Time

Table 6.5 indicates the interrupt response time, which is the time from the occurrence of an interrupt request until the interrupt exception processing starts and fetching of the first instruction of the interrupt service routine begins. Figure 6.4 shows an example of pipeline operation when an IRQ interrupt is accepted.

**Table 6.5 Interrupt Response Time**

Item	Number of States		Notes
	NMI, Peripheral Module	IRQ	
DMAC activation judgment	0 or 1	0	1 state required for interrupt signals for which DMAC activation is possible
Compare identified interrupt priority with SR mask level	2	3	
Wait for completion of sequence currently being executed by CPU	$X (\geq 0)$		The longest sequence is for interrupt or address-error exception processing ( $X = 4 + m1 + m2 + m3 + m4$ ). If an interrupt-masking instruction follows, however, the time may be even longer.
Time from start of interrupt exception processing until fetch of first instruction of exception service routine starts	$5 + m1 + m2 + m3$		Performs the PC and SR saves and vector address fetch.
Interrupt response time	Total: $(7 \text{ or } 8) + m1 + m2 + m3 + X$	$8 + m1 + m2 + m3 + X$	
	Minimum: 10	11	0.25 to 0.28 $\mu\text{s}$ at 40 MHz
	Maximum: $12 + 2(m1 + m2 + m3) + m4$	$12 + 2(m1 + m2 + m3) + m4$	0.48 $\mu\text{s}$ at 40 MHz*

Note: \* When  $m1 = m2 = m3 = m4 = 1$

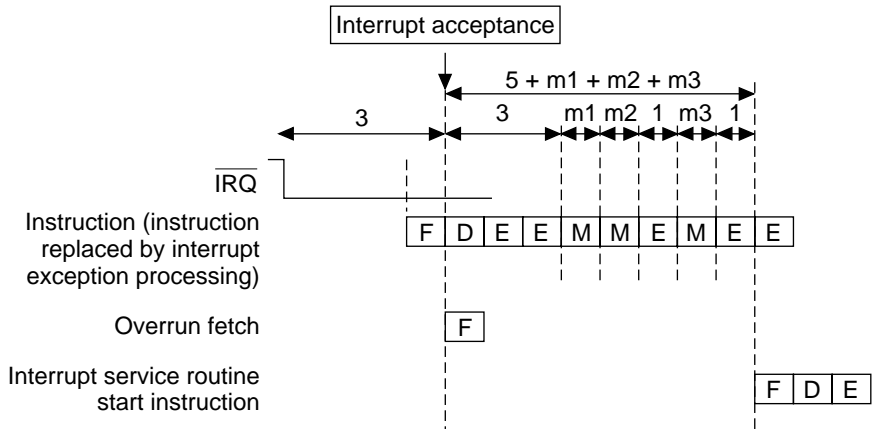
$m1$ – $m4$  are the number of states needed for the following memory accesses.

$m1$ : SR save (longword write)

$m2$ : PC save (longword write)

$m3$ : Vector address read (longword read)

$m4$ : Fetch first instruction of interrupt service routine



- F: Instruction fetch (instruction fetched from memory where program is stored).
- D: Instruction decoding (fetched instruction is decoded).
- E: Instruction execution (data operation and address calculation is performed according to the results of decoding).
- M: Memory access (data in memory is accessed).

**Figure 6.4 Example of Pipeline Operation when an IRQ Interrupt is Accepted**

## 6.6 Data Transfer with Interrupt Request Signals

The following data transfer can be carried out using interrupt request signals:

- Activate DMAC only, without generating CPU interrupt

Among interrupt sources, those designated as DMAC activating sources are masked and not input to the INTC. The masking condition is as follows:

$$\text{Mask condition} = \text{DME} \cdot (\text{DE0} \cdot \text{source selection 0} + \text{DE1} \cdot \text{source selection 1} + \text{DE2} \cdot \text{source selection 2} + \text{DE3} \cdot \text{source selection 3})$$

### 6.6.1 Handling CPU Interrupt Sources, but Not DMAC Activating Sources

1. Either do not select the DMAC as a source, or clear the DME bit to 0.
2. Activating sources are applied to the CPU when interrupts occur.
3. The CPU clears interrupt sources with its interrupt processing routine and performs the necessary processing.

### 6.6.2 Handling DMAC Activating Sources but Not CPU Interrupt Sources

1. Select the DMAC as a source and set the DME bit to 1. CPU interrupt sources are masked regardless of the interrupt priority level register settings.
2. Activating sources are applied to the DMAC when interrupts occur.
3. The DMAC clears activating sources at the time of data transfer.



# Section 7 User Break Controller (UBC)

## 7.1 Overview

The user break controller (UBC) provides functions that simplify program debugging. Break conditions are set in the UBC and a user break interrupt is generated according to the conditions of the bus cycle generated by the CPU or DMAC. This function makes it easy to design an effective self-monitoring debugger, enabling the chip to easily debug programs without using a large in-circuit emulator.

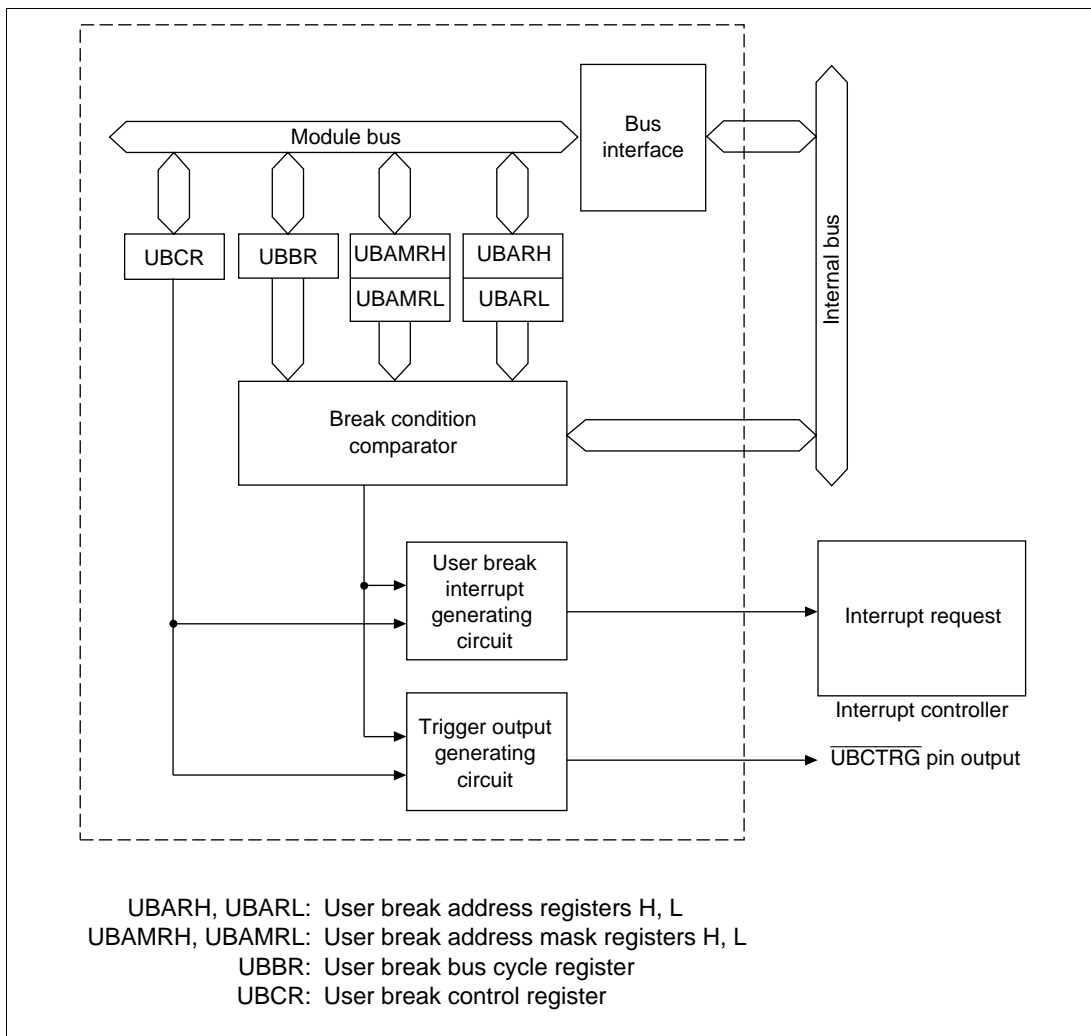
### 7.1.1 Features

The features of the user break controller are:

- The following break compare conditions can be set:
  - Address
  - CPU cycle/DMA cycle
  - Instruction fetch or data access
  - Read or write
  - Operand size: byte/word/longword
- User break interrupt generated upon satisfying break conditions  
A user-designed user break interrupt exception processing routine can be run.
- Select either to break in the CPU instruction fetch cycle before the instruction is executed or after.
- Satisfaction of a break condition can be output to the  $\overline{\text{UBCTRG}}$  pin.

## 7.1.2 Block Diagram

Figure 7.1 shows a block diagram of the UBC.



**Figure 7.1 User Break Controller Block Diagram**

### 7.1.3 Register Configuration

The UBC has the six registers shown in table 7.1. Break conditions are established using these registers.

**Table 7.1 Register Configuration**

Name	Abbr.	R/W	Initial Value	Address*	Access Size
User break address register H	UBARH	R/W	H'0000	H'FFFFFFE00	8, 16, 32
User break address register L	UBARL	R/W	H'0000	H'FFFFFFE02	8, 16, 32
User break address mask register H	UBAMRH	R/W	H'0000	H'FFFFFFE04	8, 16, 32
User break address mask register L	UBAMRL	R/W	H'0000	H'FFFFFFE06	8, 16, 32
User break bus cycle register	UBBR	R/W	H'0000	H'FFFFFFE08	8, 16, 32
User break control register	UBCR	R/W	H'0000	H'FFFFFFE0A	8, 16, 32

Note: \* In register access, three cycles are required for byte access and word access, and six cycles for longword access.

## 7.2 Register Descriptions

### 7.2.1 User Break Address Register (UBAR)

#### UBARH:

Bit:	15	14	13	12	11	10	9	8
	UBA31	UBA30	UBA29	UBA28	UBA27	UBA26	UBA25	UBA24
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	UBA23	UBA22	UBA21	UBA20	UBA19	UBA18	UBA17	UBA16
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## UBARL:

Bit:	15	14	13	12	11	10	9	8
	UBA15	UBA14	UBA13	UBA12	UBA11	UBA10	UBA9	UBA8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	UBA7	UBA6	UBA5	UBA4	UBA3	UBA2	UBA1	UBA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The user break address register (UBAR) consists of user break address register H (UBARH) and user break address register L (UBARL). Both are 16-bit readable/writable registers. UBARH stores the upper bits (bits 31 to 16) of the address of the break condition, while UBARL stores the lower bits (bits 15 to 0). UBARH and UBARL are initialized to H'0000 by a power-on reset and in module standby mode. They are not initialized in software standby mode.

- UBARH Bits 15 to 0—User Break Address 31 to 16 (UBA31 to UBA16): These bits store the upper bit values (bits 31 to 16) of the address of the break condition.
- UBARL Bits 15 to 0—User Break Address 15 to 0 (UBA15 to UBA0): These bits store the lower bit values (bits 15 to 0) of the address of the break condition.

### 7.2.2 User Break Address Mask Register (UBAMR)

#### UBAMRH:

Bit:	15	14	13	12	11	10	9	8
	UBM31	UBM30	UBM29	UBM28	UBM27	UBM26	UBM25	UBM24
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	UBM23	UBM22	UBM21	UBM20	UBM19	UBM18	UBM17	UBM16
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



## UBAMRL:

Bit:	15	14	13	12	11	10	9	8
	UBM15	UBM14	UBM13	UBM12	UBM11	UBM10	UBM9	UBM8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	UBM7	UBM6	UBM5	UBM4	UBM3	UBM2	UBM1	UBM0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The user break address mask register (UBAMR) consists of user break address mask register H (UBAMRH) and user break address mask register L (UBAMRL). Both are 16-bit readable/writable registers. UBAMRH designates whether to mask any of the break address bits established in UBARH, and UBAMRL designates whether to mask any of the break address bits established in UBARL. UBAMRH and UBAMRL are initialized to H'0000 by a power-on reset and in module standby mode. They are not initialized in software standby mode.

- UBAMRH Bits 15 to 0—User Break Address Mask 31 to 16 (UBM31 to UBM16): These bits designate whether to mask the corresponding break address 31 to 16 bits (UBA31 to UBA16) established in UBARH.
- UBAMRL Bits 15 to 0—User Break Address Mask 15 to 0 (UBM15 to UBM0): These bits designate whether to mask the corresponding break address 15 to 0 bits (UBA15 to UBA0) established in UBARL.

Bit 15 to 0: UBMn	Description
0	Break address UBAn is included in the break conditions (Initial value)
1	Break address UBAn is not included in the break conditions

Note: n = 31 to 0

### 7.2.3 User Break Bus Cycle Register (UBBR)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	CP1	CP0	ID1	ID0	RW1	RW0	SZ1	SZ0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The user break bus cycle register (UBBR) is a 16-bit readable/writable register that selects from among the following four break conditions:

1. CPU cycle/DMA cycle
2. Instruction fetch/data access
3. Read/write
4. Operand size (byte, word, longword)

UBBR is initialized to H'0000 by a power on reset and in module standby mode. It is not initialized in software standby mode.

- Bits 15 to 8—Reserved: These bits always read 0. The write value should always be 0.
- Bits 7 and 6—CPU Cycle/DMA Cycle Select (CP1, CP0): These bits designate break conditions for CPU cycles or DMA cycles.

Bit 7: CP1	Bit 6: CP0	Description
0	0	No user break interrupt occurs (Initial value)
	1	Break on CPU cycles
1	0	Break on DMA cycles
	1	Break on both CPU and DMA cycles

- Bits 5 and 4—Instruction Fetch/Data Access Select (ID1, ID0): These bits select whether to break on instruction fetch and/or data access cycles.

Bit 5: ID1	Bit 4: ID0	Description
0	0	No user break interrupt occurs (Initial value)
	1	Break on instruction fetch cycles
1	0	Break on data access cycles
	1	Break on both instruction fetch and data access cycles

- Bits 3 and 2—Read/Write Select (RW1, RW0): These bits select whether to break on read and/or write cycles.

Bit 3: RW1	Bit 2: RW0	Description
0	0	No user break interrupt occurs (Initial value)
	1	Break on read cycles
1	0	Break on write cycles
	1	Break on both read and write cycles

- Bits 1 and 0—Operand Size Select (SZ1, SZ0): These bits select operand size as a break condition.

Bit 1: SZ1	Bit 0: SZ0	Description
0	0	Operand size is not a break condition (Initial value)
	1	Break on byte access
1	0	Break on word access
	1	Break on longword access

Note: When breaking on an instruction fetch, clear the SZ0 bit to 0. All instructions are considered to be word-size accesses (even when there are instructions in on-chip memory and two instruction fetches are performed simultaneously in one bus cycle).

Operand size is word for instructions or determined by the operand size specified for the CPU/DMAC data access. It is not determined by the bus width of the space being accessed.

## 7.2.4 User Break Control Register (UBCR)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	CKS1	CKS0	UBID
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

The user break control register (UBCR) is a 16-bit readable/writable register that (1) enables or disables user break interrupts and (2) sets the pulse width of the  $\overline{\text{UBCTR}}\overline{\text{G}}$  signal output in the event of a break condition match.

UBCR is initialized to H'0000 by a power-on reset and in module standby mode. It is not initialized in software standby mode.

- Bits 15 to 3—Reserved: These bits always read 0. The write value should always be 0.
- Bits 2 and 1—Clock Select 1 and 0 (CKS1, CKS0): These bits specify the pulse width of the  $\overline{\text{UBCTR}}\overline{\text{G}}$  signal output in the event of a condition match.

Bit 2: CKS1	Bit 1: CKS0	Description
0	0	$\overline{\text{UBCTR}}\overline{\text{G}}$ pulse width is $\phi$ (Initial value)
	1	$\overline{\text{UBCTR}}\overline{\text{G}}$ pulse width is $\phi/4$
1	0	$\overline{\text{UBCTR}}\overline{\text{G}}$ pulse width is $\phi/8$
	1	$\overline{\text{UBCTR}}\overline{\text{G}}$ pulse width is $\phi/16$

Note:  $\phi$ : Internal clock

- Bit 0—User Break Disable (UBID): Enables or disables user break interrupt request generation in the event of a user break condition match.

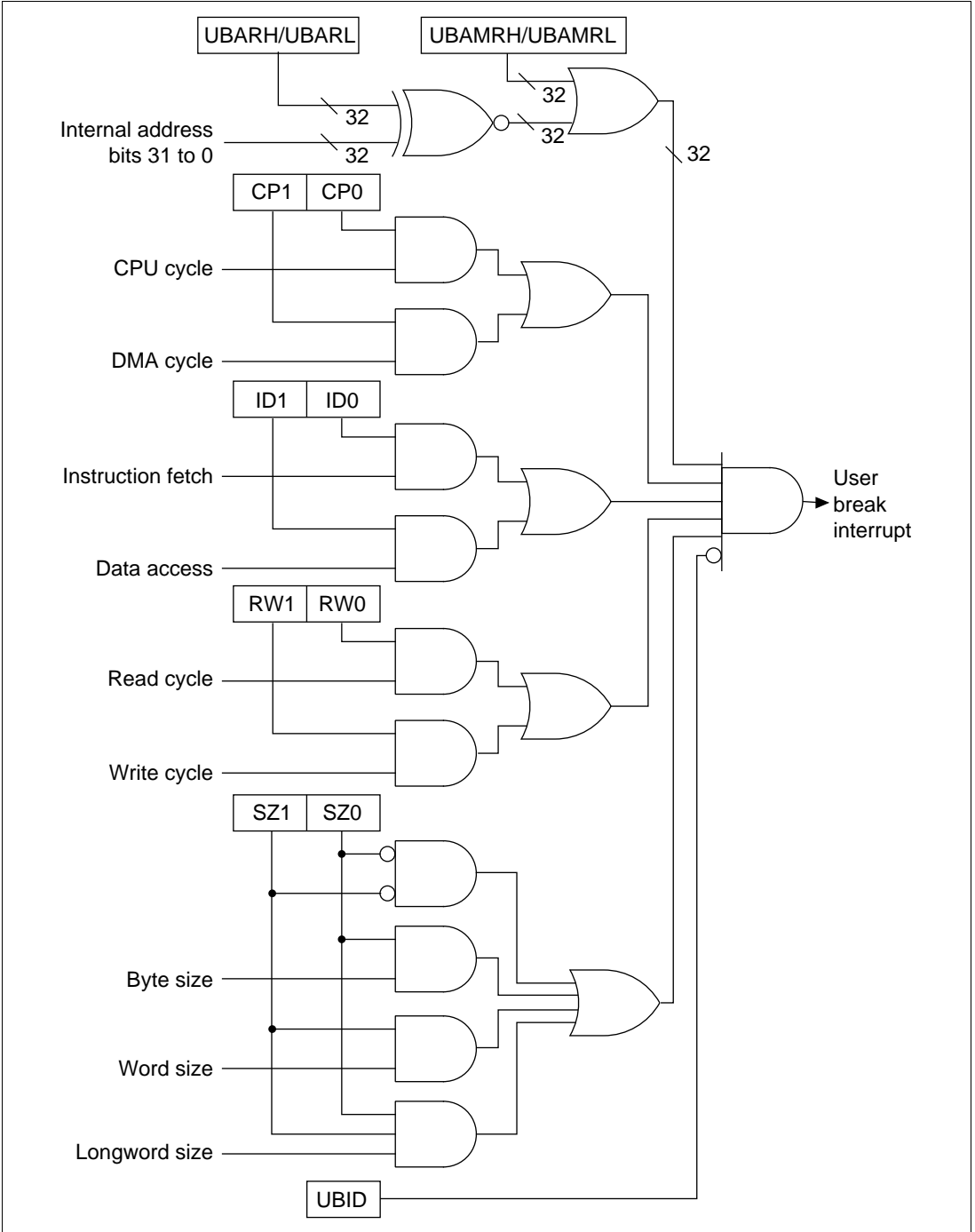
Bit 0: UBID	Description
0	User break interrupt request is enabled (Initial value)
1	User break interrupt request is disabled

## 7.3 Operation

### 7.3.1 Flow of the User Break Operation

The flow from setting of break conditions to user break interrupt exception processing is described below:

1. The user break addresses are set in the user break address register (UBAR), the desired masked bits in the addresses are set in the user break address mask register (UBAMR) and the breaking bus cycle type is set in the user break bus cycle register (UBBR). If even one of the three groups of the UBBR's CPU cycle/DMA cycle select bits (CP1, CP0), instruction fetch/data access select bits (ID1, ID0), and read/write select bits (RW1, RW0) is set to 00 (no user break generated), no user break interrupt will be generated even if all other conditions are in agreement. When using user break interrupts, always be certain to establish bit conditions for all of these three groups.
2. The UBC uses the method shown in figure 7.2 to judge whether set conditions have been fulfilled. When the set conditions are satisfied, the UBC sends a user break interrupt request signal to the interrupt controller (INTC). At the same time, a condition match signal is output at the  $\overline{\text{UBCTR}}\overline{\text{G}}$  pin with the pulse width set in bits CKS1 and CKS0.
3. The interrupt controller checks the accepted user break interrupt request signal's priority level. The user break interrupt has priority level 15, so it is accepted only if the interrupt mask level in bits I3 to I0 in the status register (SR) is 14 or lower. When the I3 to I0 bit level is 15, the user break interrupt cannot be accepted but it is held pending until user break interrupt exception processing can be carried out. Consequently, user break interrupts within NMI exception service routines cannot be accepted, since the I3 to I0 bit level is 15. However, if the I3 to I0 bit level is changed to 14 or lower at the start of the NMI exception service routine, user break interrupts become acceptable thereafter. Section 6, Interrupt Controller, describes the handling of priority levels in greater detail.
4. The INTC sends the user break interrupt request signal to the CPU, which begins user break interrupt exception processing upon receipt. See Section 6.4, Interrupt Operation, for details on interrupt exception processing.



**Figure 7.2 Break Condition Judgment Method**

### 7.3.2 Break on On-Chip Memory Instruction Fetch Cycle

On-chip memory (on-chip ROM and/or RAM) is always accessed as 32 bits in one bus cycle. Therefore, two instructions can be retrieved in one bus cycle when fetching instructions from on-chip memory. At such times, only one bus cycle is generated, but by setting the start addresses of both instructions in the user break address register (UBAR) it is possible to cause independent breaks. In other words, when wanting to effect a break using the latter of two addresses retrieved in one bus cycle, set the start address of that instruction in UBAR. The break will occur after execution of the former instruction.

### 7.3.3 Program Counter (PC) Values Saved

**Break on Instruction Fetch:** The program counter (PC) value saved to the stack in user break interrupt exception processing is the address that matches the break condition. The user break interrupt is generated before the fetched instruction is executed. If a break condition is set in an instruction fetch cycle placed immediately after a delayed branch instruction (delay slot), or on an instruction that follows an interrupt-disabled instruction, however, the user break interrupt is not accepted immediately, but the break condition establishing instruction is executed. The user break interrupt is accepted after execution of the instruction that has accepted the interrupt. In this case, the PC value saved is the start address of the instruction that will be executed after the instruction that has accepted the interrupt.

**Break on Data Access (CPU/DMA):** The program counter (PC) value is the top address of the next instruction after the last instruction executed before the user break exception processing started. When data access (CPU/DMA) is set as a break condition, the place where the break will occur cannot be specified exactly. The break will occur at the instruction fetched close to where the data access that is to receive the break occurs.

## 7.4 Examples of Use

### 7.4.1 Break on CPU Instruction Fetch Cycle

1. Register settings:      UBARH = H'0000  
                              UBARL = H'0404  
                              UBBR = H'0054  
                              UBCR = H'0000  
  
Conditions set:            Address: H'00000404  
                              Bus cycle: CPU, instruction fetch, read  
                              (operand size not included in conditions)  
                              Interrupt requests enabled

A user break interrupt will occur before the instruction at address H'00000404. If it is possible for the instruction at H'00000402 to accept an interrupt, the user break exception processing will be executed after execution of that instruction. The instruction at H'00000404 is not executed. The PC value saved is H'00000404.

2. Register settings:      UBARH = H'0015  
                              UBARL = H'389C  
                              UBBR = H'0058  
                              UBCR = H'0000  
  
Conditions set:            Address: H'0015389C  
                              Bus cycle: CPU, instruction fetch, write  
                              (operand size not included in conditions)  
                              Interrupt requests enabled

A user break interrupt does not occur because the instruction fetch cycle is not a write cycle.

3. Register settings:      UBARH = H'0003  
                              UBARL = H'0147  
                              UBBR = H'0054  
                              UBCR = H'0000  
  
Conditions set:            Address: H'00030147  
                              Bus cycle: CPU, instruction fetch, read  
                              (operand size not included in conditions)  
                              Interrupt requests enabled

A user break interrupt does not occur because the instruction fetch was performed for an even address. However, if the first instruction fetch address after the branch is an odd address set by these conditions, user break interrupt exception processing will be carried out after address error exception processing.



## 7.4.2 Break on CPU Data Access Cycle

1. Register settings:      UBARH = H'0012  
                              UBARL = H'3456  
                              UBBR = H'006A  
                              UBCR = H'0000

Conditions set:          Address: H'00123456  
                              Bus cycle: CPU, data access, write, word  
                              Interrupt requests enabled

A user break interrupt occurs when word data is written into address H'00123456.

2. Register settings:      UBARH = H'00A8  
                              UBARL = H'0391  
                              UBBR = H'0066  
                              UBCR = H'0000

Conditions set:          Address: H'00A80391  
                              Bus cycle: CPU, data access, read, word  
                              Interrupt requests enabled

A user break interrupt does not occur because the word access was performed on an even address.

## 7.4.3 Break on DMA Cycle

1. Register settings:      UBARH = H'0076  
                              UBARL = H'BCDC  
                              UBBR = H'00A7  
                              UBCR = H'0000

Conditions set:          Address: H'0076BCDC  
                              Bus cycle: DMA, data access, read, longword  
                              Interrupt requests enabled

A user break interrupt occurs when longword data is read from address H'0076BCDC.

2. Register settings:      UBARH = H'0023  
                              UBARL = H'45C8  
                              UBBR = H'0094  
                              UBCR = H'0000

Conditions set:          Address: H'002345C8  
                              Bus cycle: DMA, instruction fetch, read  
                              (operand size not included in conditions)  
                              Interrupt requests enabled

A user break interrupt does not occur because no instruction fetch is performed in the DMA cycle.

## 7.5 Usage Notes

### 7.5.1 Simultaneous Fetching of Two Instructions

Two instructions may be simultaneously fetched from on-chip memory. If a break condition is set on the second of these two instructions but the contents of the UBC break condition registers are changed so as to alter the break condition immediately after the first of the two instructions is fetched, a user break interrupt will still occur when the second instruction is fetched.

### 7.5.2 Instruction Fetch at Branches

When a conditional branch instruction or TRAPA instruction causes a branch, instructions are fetched and executed as follows:

1. Conditional branch instruction, branch taken: BT, BF

TRAPA instruction, branch taken: TRAPA

Instruction fetch order: Branch instruction fetch → next instruction overrun fetch → overrun fetch of instruction after next → branch destination instruction fetch

Instruction execution order: Branch instruction execution → branch destination instruction execution

2. When branching with a delayed conditional instruction: BT/S and BF/S instructions

Instruction fetch order: Branch instruction fetch → next instruction fetch (delay slot) → overrun fetch of instruction after next → branch destination instruction fetch

Instruction execution order: Branch instruction execution → delay slot instruction execution → branch destination instruction execution

When a conditional branch instruction or TRAPA instruction causes a branch, the branch destination will be fetched after the next instruction or the one after that performs an overrun fetch. However, because the instruction that is the object of the break first breaks after a definite instruction fetch and execution, the kind of overrun fetch instructions noted above do not become objects of a break. If data access breaks are also included with instruction fetch breaks as break conditions, a break occurs because the instruction overrun fetch is also regarded as becoming a data break.

### 7.5.3 Contention between User Break and Exception Processing

If a user break is set for the fetch of a particular instruction, and exception processing with higher priority than a user break is in contention and is accepted in the decode stage for that instruction (or the next instruction), user break exception processing may not be performed after completion of the higher-priority exception service routine (on return by RTE).

Thus, if a user break condition is applied to the branch destination instruction fetch after a branch (BRA, BRAF, BT, BF, BT/S, BF/S, BSR, BSRF, JMP, JSR, RTS, RTE, exception processing), and that branch instruction accepts exception processing with higher priority than a user break interrupt, user break exception processing is not performed after completion of the higher-priority exception service routine.

Therefore, a user break condition should not be set for the fetch of the branch destination instruction after a branch.

### 7.5.4 Break at Non-Delay Branch Instruction Jump Destination

When a branch instruction with no delay slot (including exception processing) jumps to the jump destination instruction on execution of the branch, a user break will not be generated even if a user break condition has been set for the first jump destination instruction fetch.

### 7.5.5 User Break Trigger Output

Information on internal bus condition matches monitored by the UBC is output as  $\overline{\text{UBCTR}}\overline{\text{G}}$ . The trigger width can be set with clock select bits 1 and 0 (CKS1, CKS0) in the user break control register (UBCR).

If a condition matches occurs again during trigger output, the  $\overline{\text{UBCTR}}\overline{\text{G}}$  pin continues to output a low level, and outputs a pulse of the length set in bits CKS1 and CKS0 from the cycle in which the last condition match occurs.

The trigger output conditions differ from those in the case of a user break interrupt when a CPU instruction fetch condition is satisfied. When a condition occurs in an overrun fetch instruction as described in section 7.5.2, Instruction Fetch at Branches, a user break interrupt is not requested but a trigger is output from the  $\overline{\text{UBCTR}}\overline{\text{G}}$  pin.

In other CPU data accesses and DMAC bus cycles, pulse output is performed under conditions similar to user break interrupt conditions.

Setting the user break interrupt disable (UBID) bit to 1 in UBCR enables trigger output to be monitored externally without requesting a user break interrupt.

## 7.5.6 Module Standby

After a power-on reset the UBC is in the module standby state, in which the clock supply is halted. When using the UBC, the module standby state must be cleared before making UBC register settings. Module standby is controlled by the module standby control register (MSTCR). See section 23.2.3, Module Standby Control Register, for further details.

# Section 8 Bus State Controller (BSC)

## 8.1 Overview

The bus state controller (BSC) divides up the address spaces and outputs control for various types of memory. This enables memories like SRAM and ROM to be linked directly to the chip without external circuitry, simplifying system design and enabling high-speed data transfer to be achieved in a compact system.

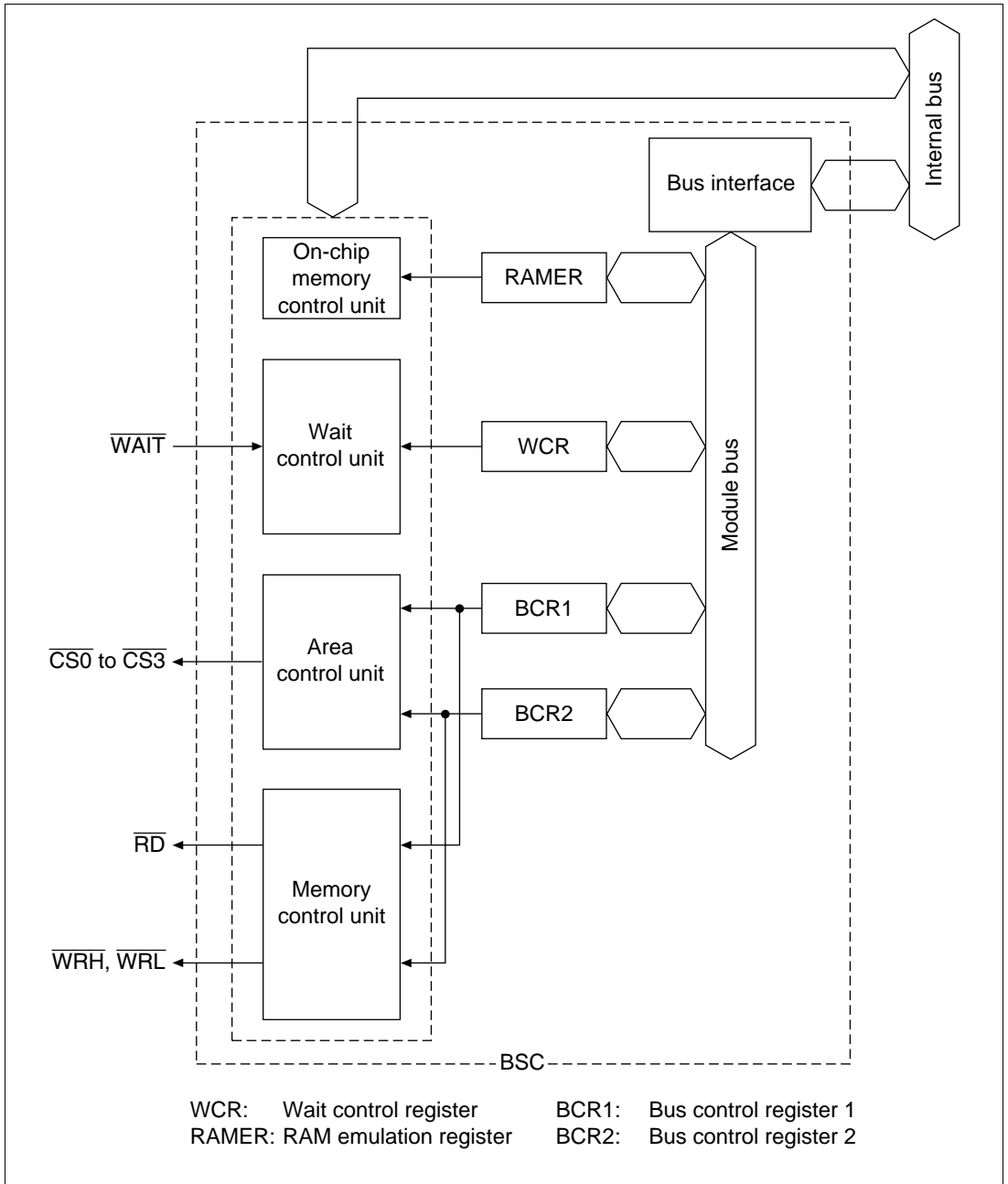
### 8.1.1 Features

The BSC has the following features:

- Address space is divided into four spaces
  - A maximum linear 2 Mbytes for on-chip ROM effective mode, and a maximum 4 Mbytes for on-chip ROM disabled mode, for address space CS0
  - A maximum linear 4 Mbytes for each of address spaces CS1 to CS3
  - Bus width can be selected for each space (8 or 16 bits)
  - Wait states can be inserted by software for each space
  - Wait state insertion with  $\overline{\text{WAIT}}$  pin in external memory space access
  - Outputs control signals for each space according to the type of memory connected
- On-chip ROM and RAM interfaces
  - On-chip ROM and RAM access of 32 bits in 1 state

## 8.1.2 Block Diagram

Figure 8.1 shows the BSC block diagram.



**Figure 8.1 BSC Block Diagram**

### 8.1.3 Pin Configuration

Table 8.1 shows the bus state controller pin configuration.

**Table 8.1 Pin Configuration**

Name	Abbr.	I/O	Description
Address bus	A21 to A0	O	Address output
Data bus	D15 to D0	I/O	16-bit data bus
Chip select	$\overline{CS0}$ to $\overline{CS3}$	O	Chip select signals indicating the area being accessed
Read	$\overline{RD}$	O	Strobe that indicates the read cycle for ordinary space/multiplex I/O
Upper write	$\overline{WRH}$	O	Strobe that indicates a write cycle to the upper 8 bits (D15 to D8)
Lower write	$\overline{WRL}$	O	Strobe that indicates a write cycle to the lower 8 bits (D7 to D0)
Wait	$\overline{WAIT}$	I	Wait state request signal
Bus request	$\overline{BREQ}$	I	Bus release request input
Bus acknowledge	$\overline{BACK}$	O	Bus use enable output

Note: When an 8-bit bus width is selected for external space,  $\overline{WRL}$  is enabled.

When a 16-bit bus width is selected for external space,  $\overline{WRH}$  and  $\overline{WRL}$  are enabled.

### 8.1.4 Register Configuration

The BSC has four registers. These registers are used to control wait states, bus width, and interfaces with memories like ROM and SRAM, as well as refresh control. The register configurations are listed in table 8.2.

All registers are 16 bits. All BSC registers are all initialized by a power-on reset and in hardware standby mode. Values are retained in a manual reset and in software standby mode.

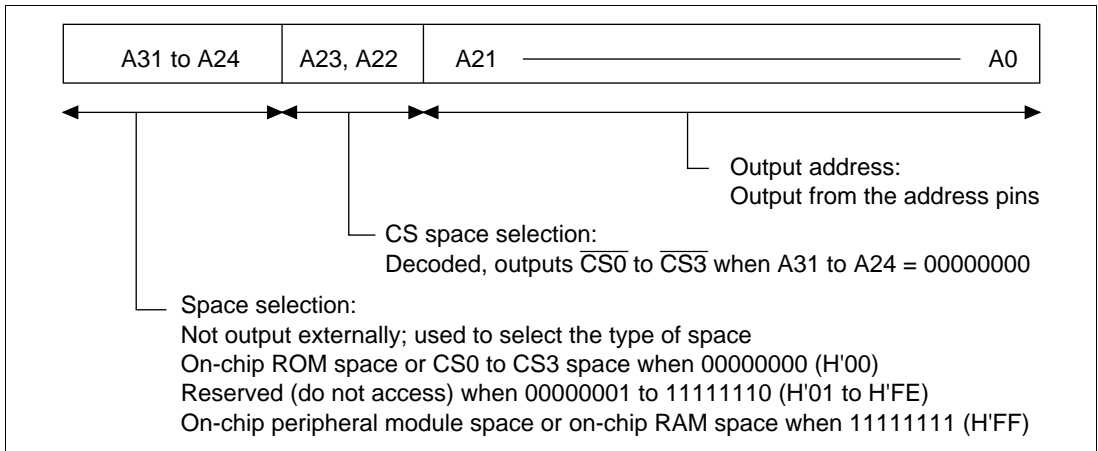
**Table 8.2 Register Configuration**

Name	Abbr.	R/W	Initial Value	Address	Access Size
Bus control register 1	BCR1	R/W	H'000F	H'FFFFFFEC20	8, 16, 32
Bus control register 2	BCR2	R/W	H'FFFF	H'FFFFFFEC22	8, 16, 32
Wait state control register	WCR	R/W	H'FFFF	H'FFFFFFEC24	8, 16, 32
RAM emulation register	RAMER	R/W	H'0000	H'FFFFFFEC26	8, 16, 32

Note: In register access, three cycles are required for byte access and word access, and six cycles for longword access.

### 8.1.5 Address Map

Figure 8.2 shows the address format used by the SH7052F/SH7053F/SH7054F.



**Figure 8.2 Address Format**

This chip uses 32-bit addresses:

- Bits A31 to A24 are used to select the type of space and are not output externally.
- Bits A23 and A22 are decoded and output as chip select signals ( $\overline{CS0}$  to  $\overline{CS3}$ ) for the corresponding areas when bits A31 to A24 are 00000000.
- A21 to A0 are output externally.



Tables 8.3, 8.4 and 8.5 show the address map.

**Table 8.3 Address Map**

- On-chip ROM enabled mode (SH7052F)

Address	Space	Memory	Size	Bus Width
H'0000 0000 to H'0003 FFFF	On-chip ROM	On-chip ROM	256 kB	32 bits
H'0004 0000 to H'001F FFFF	Reserved	Reserved		
H'0020 0000 to H'003F FFFF	CS0 space	External space	2 MB	8, 16 bits *1
H'0040 0000 to H'007F FFFF	CS1 space	External space	4 MB	8, 16 bits *1
H'0080 0000 to H'00BF FFFF	CS2 space	External space	4 MB	8, 16 bits *1
H'00C0 0000 to H'00FF FFFF	CS3 space	External space	4 MB	8, 16 bits *1
H'0100 0000 to H'FFFF 7FFF	Reserved	Reserved		
H'FFFF 8000 to H'FFFF AFFF	On-chip RAM	On-chip RAM	12 kB	32 bits
H'FFFF B000 to H'FFFF DFFF	Reserved	Reserved		
H'FFFF E000 to H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module	8 kB	8, 16 bits

- On-chip ROM disabled mode (SH7052F)

Address	Space	Memory	Size	Bus Width
H'0000 0000 to H'003F FFFF	CS0 space	External space	4 MB	8, 16 bits *2
H'0040 0000 to H'007F FFFF	CS1 space	External space	4 MB	8, 16 bits *1
H'0080 0000 to H'00BF FFFF	CS2 space	External space	4 MB	8, 16 bits *1
H'00C0 0000 to H'00FF FFFF	CS3 space	External space	4 MB	8, 16 bits *1
H'0100 0000 to H'FFFF 7FFF	Reserved	Reserved		
H'FFFF 8000 to H'FFFF AFFF	On-chip RAM	On-chip RAM	12 kB	32 bits
H'FFFF B000 to H'FFFF DFFF	Reserved	Reserved		
H'FFFF E000 to H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module	8 kB	8, 16 bits

Notes: Do not access reserved spaces. Operation cannot be guaranteed if they are accessed.

- Selected by on-chip register (BCR1) settings.
- Selected by the mode pin.

**Table 8.4 Address Map**

- On-chip ROM enabled mode (SH7053F)

Address	Space	Memory	Size	Bus Width
H'0000 0000 to H'0003 FFFF	On-chip ROM	On-chip ROM	256 kB	32 bits
H'0004 0000 to H'001F FFFF	Reserved	Reserved		
H'0020 0000 to H'003F FFFF	CS0 space	External space	2 MB	8, 16 bits * <sup>1</sup>
H'0040 0000 to H'007F FFFF	CS1 space	External space	4 MB	8, 16 bits * <sup>1</sup>
H'0080 0000 to H'00BF FFFF	CS2 space	External space	4 MB	8, 16 bits * <sup>1</sup>
H'00C0 0000 to H'00FF FFFF	CS3 space	External space	4 MB	8, 16 bits * <sup>1</sup>
H'0100 0000 to H'FFFF 7FFF	Reserved	Reserved		
H'FFFF 8000 to H'FFFF BFFF	On-chip RAM	On-chip RAM	12 kB	32 bits
H'FFFF C000 to H'FFFF DFFF	Reserved	Reserved		
H'FFFF E000 to H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module	8 kB	8, 16 bits

- On-chip ROM disabled mode (SH7053F)

Address	Space	Memory	Size	Bus Width
H'0000 0000 to H'003F FFFF	CS0 space	External space	4 MB	8, 16 bits * <sup>2</sup>
H'0040 0000 to H'007F FFFF	CS1 space	External space	4 MB	8, 16 bits * <sup>1</sup>
H'0080 0000 to H'00BF FFFF	CS2 space	External space	4 MB	8, 16 bits * <sup>1</sup>
H'00C0 0000 to H'00FF FFFF	CS3 space	External space	4 MB	8, 16 bits * <sup>1</sup>
H'0100 0000 to H'FFFF 7FFF	Reserved	Reserved		
H'FFFF 8000 to H'FFFF BFFF	On-chip RAM	On-chip RAM	16 kB	32 bits
H'FFFF B000 to H'FFFF DFFF	Reserved	Reserved		
H'FFFF E000 to H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module	8 kB	8, 16 bits

Notes: Do not access reserved spaces. Operation cannot be guaranteed if they are accessed.

- Selected by on-chip register (BCR1) settings.
- Selected by the mode pin.

**Table 8.5 Address Map**

- On-chip ROM enabled mode (SH7054F)

Address	Space	Memory	Size	Bus Width
H'0000 0000 to H'0005 FFFF	On-chip ROM	On-chip ROM	384 kB	32 bits
H'0006 0000 to H'001F FFFF	Reserved	Reserved		
H'0020 0000 to H'003F FFFF	CS0 space	External space	2 MB	8, 16 bits *1
H'0040 0000 to H'007F FFFF	CS1 space	External space	4 MB	8, 16 bits *1
H'0080 0000 to H'00BF FFFF	CS2 space	External space	4 MB	8, 16 bits *1
H'00C0 0000 to H'00FF FFFF	CS3 space	External space	4 MB	8, 16 bits *1
H'0100 0000 to H'FFFF 7FFF	Reserved	Reserved		
H'FFFF 8000 to H'FFFF BFFF	On-chip RAM	On-chip RAM	16 kB	32 bits
H'FFFF C000 to H'FFFF DFFF	Reserved	Reserved		
H'FFFF E000 to H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module	8 kB	8, 16 bits

- On-chip ROM disabled mode (SH7054F)

Address	Space	Memory	Size	Bus Width
H'0000 0000 to H'003F FFFF	CS0 space	External space	4 MB	8, 16 bits *2
H'0040 0000 to H'007F FFFF	CS1 space	External space	4 MB	8, 16 bits *1
H'0080 0000 to H'00BF FFFF	CS2 space	External space	4 MB	8, 16 bits *1
H'00C0 0000 to H'00FF FFFF	CS3 space	External space	4 MB	8, 16 bits *1
H'0100 0000 to H'FFFF 7FFF	Reserved	Reserved		
H'FFFF 8000 to H'FFFF BFFF	On-chip RAM	On-chip RAM	16 kB	32 bits
H'FFFF C000 to H'FFFF DFFF	Reserved	Reserved		
H'FFFF E000 to H'FFFF FFFF	On-chip peripheral module	On-chip peripheral module	8 kB	8, 16 bits

Notes: Do not access reserved spaces. Operation cannot be guaranteed if they are accessed.

- Selected by on-chip register (BCR1) settings.
- Selected by the mode pin.

## 8.2 Description of Registers

### 8.2.1 Bus Control Register 1 (BCR1)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	A3SZ	A2SZ	A1SZ	A0SZ
Initial value:	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

BCR1 is a 16-bit readable/writable register that specifies the bus size of the CS spaces.

Write bits 15 to 0 of BCR1 during the initialization stage after a power-on reset, and do not change the values thereafter. In on-chip ROM enabled mode, do not access any of the CS spaces until after completion of register initialization. In on-chip ROM disabled mode, do not access any CS space other than CS0 until after completion of register initialization.

BCR1 is initialized to H'000F by a power-on reset and in hardware standby mode. It is not initialized by a manual reset or in software standby mode.

- Bits 15 to 4—Reserved: These bits always read 0. Operation cannot be guaranteed if 1 is written to these bits.
- Bit 3—CS3 Space Size Specification (A3SZ): Specifies the CS3 space bus size. A 0 setting specifies byte (8-bit) size, and a 1 setting specifies word (16-bit) size.

Bit 3: A3SZ	Description
0	Byte (8-bit) size
1	Word (16-bit) size (Initial value)

- Bit 2—CS2 Space Size Specification (A2SZ): Specifies the CS2 space bus size. A 0 setting specifies byte (8-bit) size, and a 1 setting specifies word (16-bit) size.

Bit 2: A2SZ	Description
0	Byte (8-bit) size
1	Word (16-bit) size (Initial value)

- Bit 1—CS1 Space Size Specification (A1SZ): Specifies the CS1 space bus size. A 0 setting specifies byte (8-bit) size, and a 1 setting specifies word (16-bit) size.

Bit 1: A1SZ	Description
0	Byte (8-bit) size
1	Word (16-bit) size (Initial value)

- Bit 0—CS0 Space Size Specification (A0SZ): Specifies the CS0 space bus size. A 0 setting specifies byte (8-bit) size, and a 1 setting specifies word (16-bit) size.

Bit 0: A0SZ	Description
0	Byte (8-bit) size
1	Word (16-bit) size (Initial value)

Note: A0SZ is valid only in on-chip ROM enabled mode. In on-chip ROM disabled mode, the CS0 space bus size is specified by the mode pin.

## 8.2.2 Bus Control Register 2 (BCR2)

Bit:	15	14	13	12	11	10	9	8
	IW31	IW30	IW21	IW20	IW11	IW10	IW01	IW00
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	CW3	CW2	CW1	CW0	SW3	SW2	SW1	SW0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCR2 is a 16-bit readable/writable register that specifies the number of idle cycles and  $\overline{\text{CS}}$  signal assert extension of each CS space.

BCR2 is initialized to H'FFFF by a power-on reset and in hardware standby mode. It is not initialized by a manual reset or in software standby mode.

- Bits 15 to 8—Idles between Cycles (IW31, IW30, IW21, IW20, IW11, IW10, IW01, IW00): These bits specify idle cycles inserted between consecutive accesses when the second one is to a different CS area after a read. Idles are used to prevent data conflict between ROM (and other memories, which are slow to turn the read data buffer off), fast memories, and I/O interfaces. Even when access is to the same area, idle cycles must be inserted when a read access is followed immediately by a write access. The idle cycles to be inserted comply with

the area specification of the previous access. Refer to section 8.4, Waits between Access Cycles, for details.

IW31 and IW30 specify the idle between cycles for CS3 space; IW21 and IW20 specify the idle between cycles for CS2 space; IW11 and IW10 specify the idle between cycles for CS1 space and IW01 and IW00 specify the idle between cycles for CS0 space.

Bit 15: IW31	Bit 14: IW30	Description
0	0	No CS3 space idle cycle
	1	Inserts one idle cycle
1	0	Inserts two idle cycles
	1	Inserts three idle cycles (Initial value)

Bit 13: IW21	Bit 12: IW20	Description
0	0	No CS2 space idle cycle
	1	Inserts one idle cycle
1	0	Inserts two idle cycles
	1	Inserts three idle cycles (Initial value)

Bit 11: IW11	Bit 10: IW10	Description
0	0	No CS1 space idle cycle
	1	Inserts one idle cycle
1	0	Inserts two idle cycles
	1	Inserts three idle cycles (Initial value)

Bit 9: IW01	Bit 8: IW00	Description
0	0	No CS0 space idle cycle
	1	Inserts one idle cycle
1	0	Inserts two idle cycles
	1	Inserts three idle cycles (Initial value)

- Bits 7 to 4—Idle Specification for Continuous Access (CW3, CW2, CW1, CW0): The continuous access idle specification makes insertions to clearly delineate the bus intervals by once negating the  $\overline{CS}_n$  signal when performing consecutive accesses to the same CS space. When a write immediately follows a read, the number of idle cycles inserted is the larger of the two values specified by IW and CW. Refer to section 8.4, Waits between Access Cycles, for details.

CW3 specifies the continuous access idles for CS3 space; CW2 specifies the continuous access idles for CS2 space; CW1 specifies the continuous access idles for CS1 space and CW0 specifies the continuous access idles for CS0 space.

Bit 7: CW3	Description
0	No CS3 space continuous access idle cycles
1	One CS3 space continuous access idle cycle (Initial value)

Bit 6: CW2	Description
0	No CS2 space continuous access idle cycles
1	One CS2 space continuous access idle cycle (Initial value)

Bit 5: CW1	Description
0	No CS1 space continuous access idle cycles
1	One CS1 space continuous access idle cycle (Initial value)

Bit 4: CW0	Description
0	No CS0 space continuous access idle cycles
1	One CS0 space continuous access idle cycle (Initial value)

- Bits 3 to 0— $\overline{\text{CS}}$  Assert Extension Specification (SW3, SW2, SW1, SW0): The  $\overline{\text{CS}}$  assert cycle extension specification is for making insertions to prevent extension of the  $\overline{\text{RD}}$  signal,  $\overline{\text{WRH}}$  signal, or  $\overline{\text{WRL}}$  signal assert period beyond the length of the  $\overline{\text{CS}}_n$  signal assert period. Extended cycles insert one cycle before and after each bus cycle, which simplifies interfaces with external devices and also has the effect of extending the write data hold time. Refer to section 8.3.3,  $\overline{\text{CS}}$  Assert Period Extension, for details.

SW3 specifies the  $\overline{\text{CS}}$  assert extension for CS3 space access; SW2 specifies the  $\overline{\text{CS}}$  assert extension for CS2 space access; SW1 specifies the  $\overline{\text{CS}}$  assert extension for CS1 space access and SW0 specifies the  $\overline{\text{CS}}$  assert extension for CS0 space access.

Bit 3: SW3	Description
0	No CS3 space $\overline{\text{CS}}$ assert extension
1	CS3 space $\overline{\text{CS}}$ assert extension (Initial value)

Bit 2: SW2	Description
0	No CS2 space $\overline{\text{CS}}$ assert extension
1	CS2 space $\overline{\text{CS}}$ assert extension (Initial value)

Bit 1: SW1	Description
0	No CS1 space $\overline{CS}$ assert extension
1	CS1 space $\overline{CS}$ assert extension (Initial value)

Bit 0: SW0	Description
0	No CS0 space $\overline{CS}$ assert extension
1	CS0 space $\overline{CS}$ assert extension (Initial value)

### 8.2.3 Wait Control Register (WCR)

Bit:	15	14	13	12	11	10	9	8
	W33	W32	W31	W30	W23	W22	W21	W20
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	W13	W12	W11	W10	W03	W02	W01	W00
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WCR is a 16-bit readable/writable register that specifies the number of wait cycles for each CS space.

WCR1 is initialized to H'FFFF by a power-on reset and in hardware standby mode. It is not initialized by a manual reset or in software standby mode.

- Bits 15 to 12—CS3 Space Wait Specification (W33, W32, W31, W30): These bits specify the number of waits for CS3 space access.

Bit 15: W33	Bit 14: W32	Bit 13: W31	Bit 12: W30	Description
0	0	0	0	No wait (external wait input disabled)
0	0	0	1	1 wait external wait input enabled
...				
1	1	1	1	15 wait external wait input enabled (Initial value)



- Bits 11 to 8—CS2 Space Wait Specification (W23, W22, W21, W20): These bits specify the number of waits for CS2 space access.

Bit 11: W23	Bit 10: W22	Bit 9: W21	Bit 8: W20	Description
0	0	0	0	No wait (external wait input disabled)
0	0	0	1	1 wait external wait input enabled
...				
1	1	1	1	15 wait external wait input enabled (Initial value)

- Bits 7 to 4—CS1 Space Wait Specification (W13, W12, W11, W10): These bits specify the number of waits for CS1 space access.

Bit 7: W13	Bit 6: W12	Bit 5: W11	Bit 4: W10	Description
0	0	0	0	No wait (external wait input disabled)
0	0	0	1	1 wait external wait input enabled
...				
1	1	1	1	15 wait external wait input enabled (Initial value)

- Bits 3 to 0—CS0 Space Wait Specification (W03, W02, W01, W00): These bits specify the number of waits for CS0 space access.

Bit 3: W03	Bit 2: W02	Bit 1: W01	Bit 0: W00	Description
0	0	0	0	No wait (external wait input disabled)
0	0	0	1	1 wait external wait input enabled
...				
1	1	1	1	15 wait external wait input enabled (Initial value)

## 8.2.4 RAM Emulation Register (RAMER)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

The RAM emulation register (RAMER) is a 16-bit readable/writable register that selects the RAM area to be used when emulating realtime programming of flash memory.

RAMER is initialized to H'0000 by a power-on reset and in hardware standby mode. It is not initialized by a manual reset or in software standby mode.

**Note:** To ensure correct operation of the RAM emulation function, the ROM for which RAM emulation is performed should not be accessed immediately after this register has been modified. Operation cannot be guaranteed if such an access is made.

- Bits 15 to 4—Reserved: Only 0 should be written to these bits. Operation cannot be guaranteed if 1 is written.
- Bit 3—RAM Select (RAMS): Used together with bits 2 to 0 to select or deselect flash memory emulation by RAM (table 8.6).  
When 1 is written to this bit, all flash memory blocks are write/erase-protected.  
This bit is ignored in modes with on-chip ROM disabled.
- Bits 2 to 0—RAM Area Specification (RAM2 to RAM0): These bits are used together with the RAMS bit to designate the flash memory area to be overlapped onto RAM (table 8.6).

**Table 8.6 RAM Area Setting Method**

<b>RAM Area</b>	<b>Bit 3: RAMS</b>	<b>Bit 2: RAM2</b>	<b>Bit 1: RAM1</b>	<b>Bit 0: RAM0</b>
H'FFFF8000 to H'FFFF8FFF	0	*	*	*
H'00000000 to H'00000FFF	1	0	0	0
H'00001000 to H'00001FFF	1	0	0	1
H'00002000 to H'00002FFF	1	0	1	0
H'00003000 to H'00003FFF	1	0	1	1
H'00004000 to H'00004FFF	1	1	0	0
H'00005000 to H'00005FFF	1	1	0	1
H'00006000 to H'00006FFF	1	1	1	0
H'00007000 to H'00007FFF	1	1	1	1

\*: Don't care

## 8.3 Accessing External Space

A strobe signal is output in external space accesses to provide primarily for SRAM or ROM direct connections.

### 8.3.1 Basic Timing

Figure 8.3 shows the basic timing of external space access. External access bus cycles are performed in 2 states.

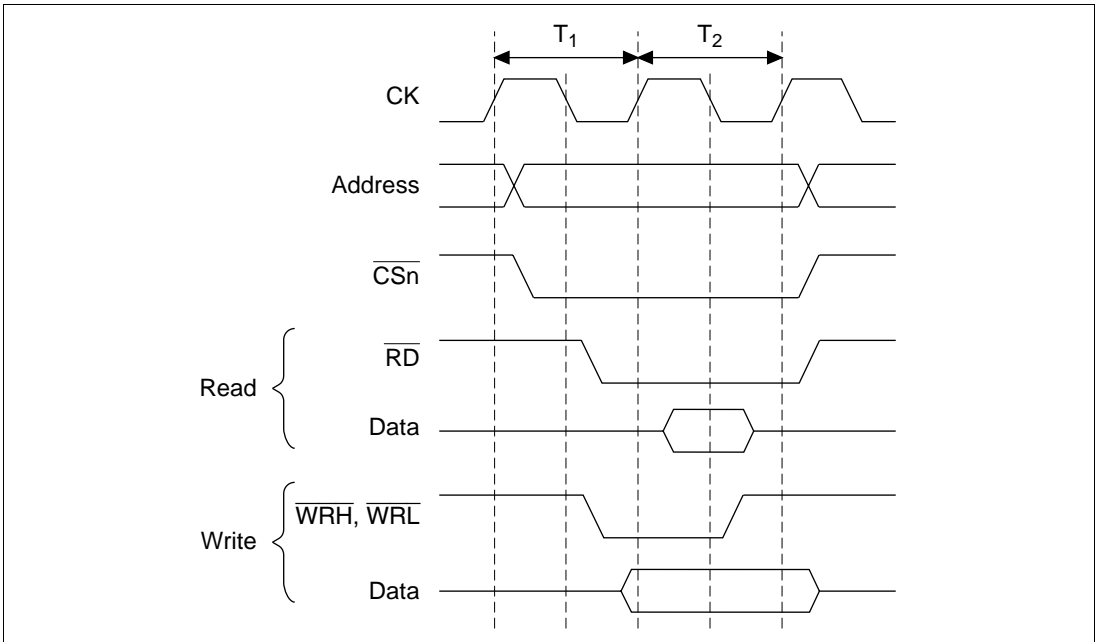
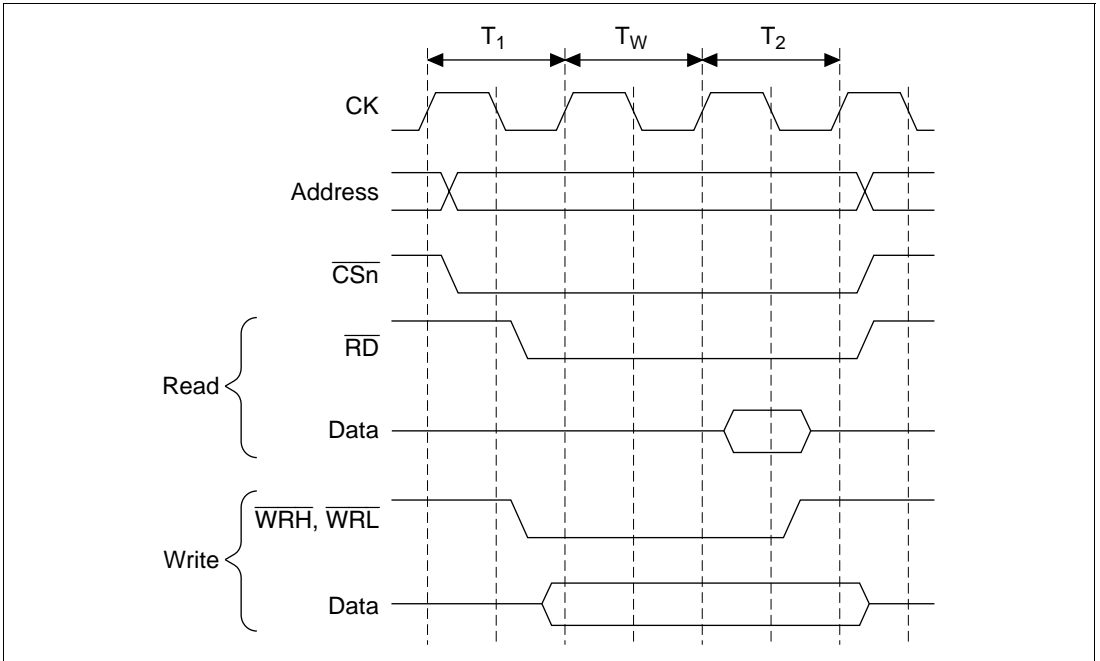


Figure 8.3 Basic Timing of External Space Access

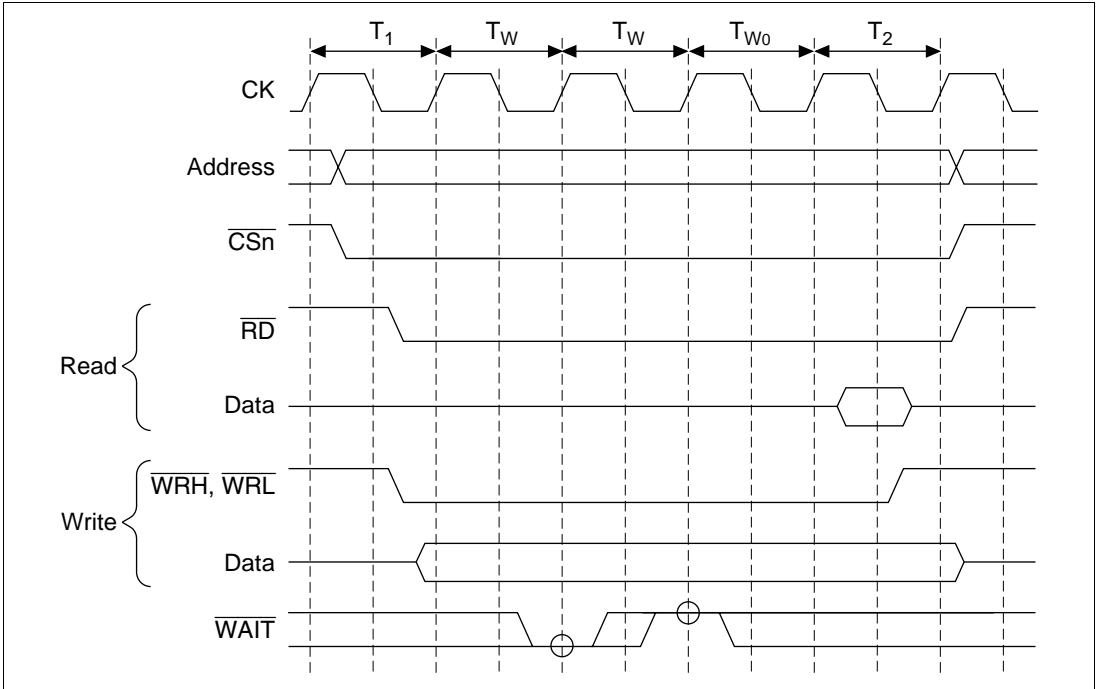
### 8.3.2 Wait State Control

The number of wait states inserted into external space access states can be controlled using the WCR settings (figure 8.4). The specified number of  $T_w$  cycles are inserted as software cycles at the timing shown in figure 8.4.



**Figure 8.4 Wait State Timing of External Space Access (Software Wait Only)**

When the wait is specified by software using WCR, the wait input  $\overline{\text{WAIT}}$  signal from outside is sampled. Figure 8.5 shows the  $\overline{\text{WAIT}}$  signal sampling. The  $\overline{\text{WAIT}}$  signal is sampled at the clock rise one cycle before the clock rise when the  $T_w$  state shifts to the  $T_2$  state. When using external waits, use a WCR setting of 1 state or more when extending  $\overline{\text{CS}}$  assertion, and 2 states or more otherwise.



**Figure 8.5 Wait State Timing of External Space Access (Two Software Wait States +  $\overline{\text{WAIT}}$  Signal Wait State)**

### 8.3.3 $\overline{\text{CS}}$ Assert Period Extension

Idle cycles can be inserted to prevent extension of the  $\overline{\text{RD}}$ ,  $\overline{\text{WRH}}$ , or  $\overline{\text{WRL}}$  signal assert period beyond the length of the  $\overline{\text{CSn}}$  signal assert period by setting the SW3 to SW0 bits of BCR2. This allows for flexible interfaces with external circuitry. The timing is shown in figure 8.6.  $T_h$  and  $T_f$  cycles are added respectively before and after the ordinary cycle. Only  $\overline{\text{CSn}}$  is asserted in these cycles;  $\overline{\text{RD}}$ ,  $\overline{\text{WRH}}$ , and  $\overline{\text{WRL}}$  signals are not. Further, data is extended up to the  $T_f$  cycle, which is effective for gate arrays and the like, which have slower write operations.

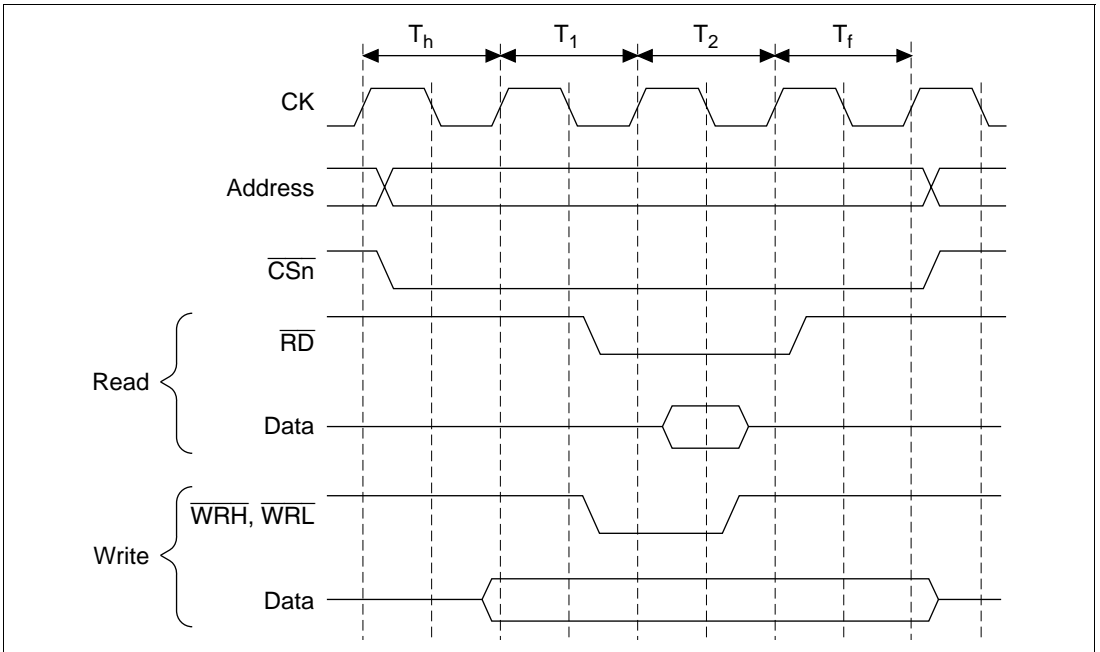


Figure 8.6  $\overline{\text{CS}}$  Assert Period Extension Function

## 8.4 Waits between Access Cycles

When a read from a slow device is completed, data buffers may not go off in time to prevent data conflicts with the next access. If there is a data conflict during memory access, the problem can be solved by inserting a wait in the access cycle.

To enable detection of bus cycle starts, waits can be inserted between access cycles during continuous accesses of the same CS space by negating the  $\overline{CSn}$  signal once.

### 8.4.1 Prevention of Data Bus Conflicts

For the two cases of write cycles after read cycles, and read cycles for a different area after read cycles, waits are inserted so that the number of idle cycles specified by the IW31 to IW00 bits of BCR2 occur. When idle cycles already exist between access cycles, only the number of empty cycles remaining beyond the specified number of idle cycles are inserted.

Figure 8.7 shows an example of idles between cycles. In this example, one idle between CSn space cycles has been specified, so when a CSm space write immediately follows a CSn space read cycle, one idle cycle is inserted.

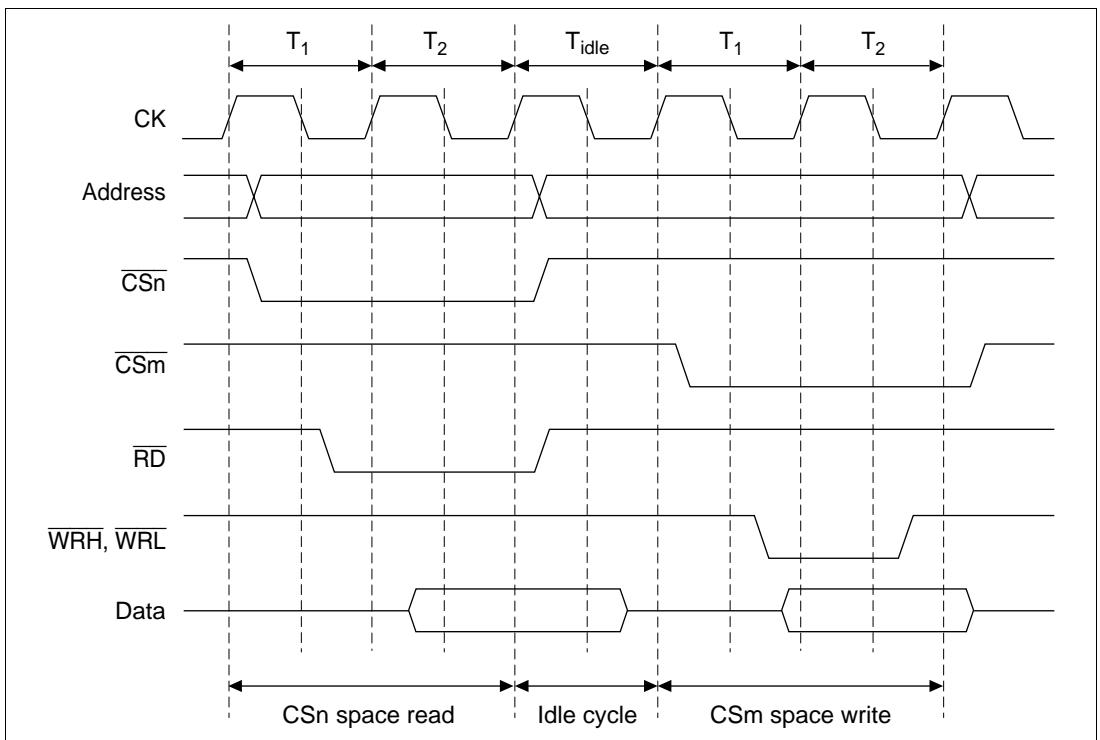


Figure 8.7 Idle Cycle Insertion Example



IW31 and IW30 specify the number of idle cycles required after a CS3 space read either to read other external spaces, or for this chip, to perform write accesses. In the same manner, IW21 and IW20 specify the number of idle cycles after a CS2 space read, IW11 and IW10, the number after a CS1 space read, and IW01 and IW00, the number after a CS0 space read. 0 to 3 idle cycles can be specified.

#### 8.4.2 Simplification of Bus Cycle Start Detection

For consecutive accesses of the same CS space, waits are inserted so that the number of idle cycles designated by the CW3 to CW0 bits of BCR2 occur. However, for write cycles after reads, the number of idle cycles inserted will be the larger of the two values defined by the IW and CW bits. When idle cycles already exist between access cycles, waits are not inserted. Figure 8.8 shows an example. A continuous access idle is specified for CSn space, and CSn space is consecutively write-accessed.

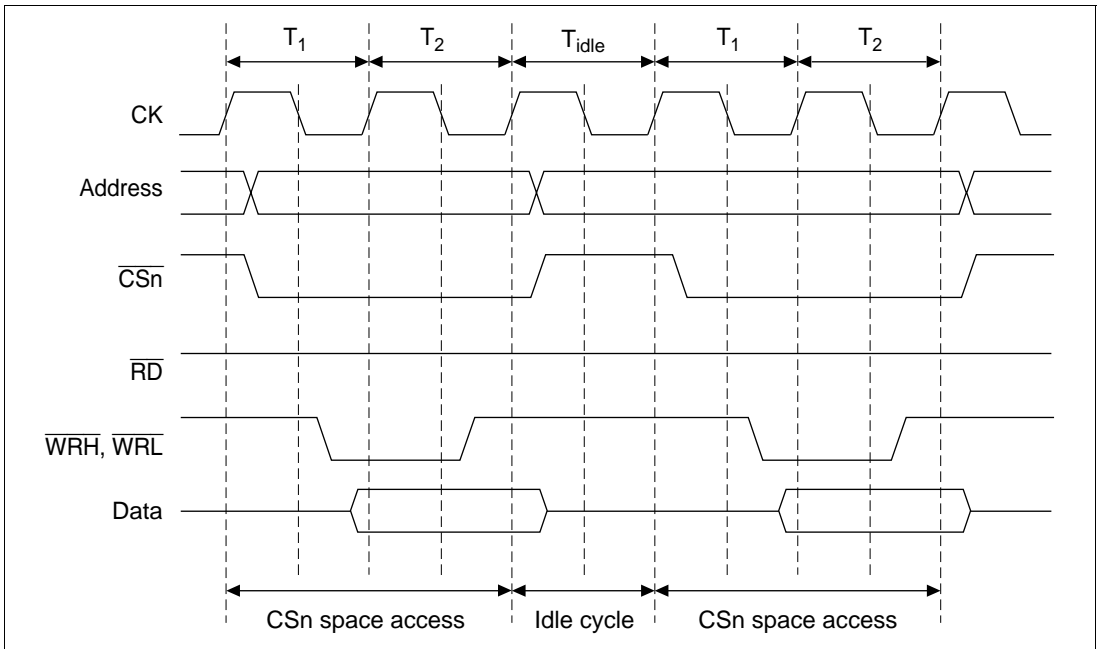


Figure 8.8 Same Space Consecutive Access Idle Cycle Insertion Example

## 8.5 Bus Arbitration

The SH7052F/SH7053F/SH7054F has a bus arbitration function that, when a bus release request is received from an external device, releases the bus to that device. The SH7052F/SH7053F/SH7054F also has three internal bus masters, the CPU, DMAC, and AUD. The priority ranking for determining bus right transfer between these bus masters is:

Bus right request from external device > AUD > DMAC > CPU

Therefore, an external device that generates a bus request is given priority even if the request is made during a DMAC burst transfer.

The AUD does not acquire the bus during DMAC burst transfer, but at the end of the transfer. When the CPU has possession of the bus, the AUD has higher priority than the DMAC for bus acquisition.

A bus request by an external device should be input at the  $\overline{\text{BREQ}}$  pin. The signal indicating that the bus has been released is output from the  $\overline{\text{BACK}}$  pin.

Figure 8.9 shows the bus right release procedure.

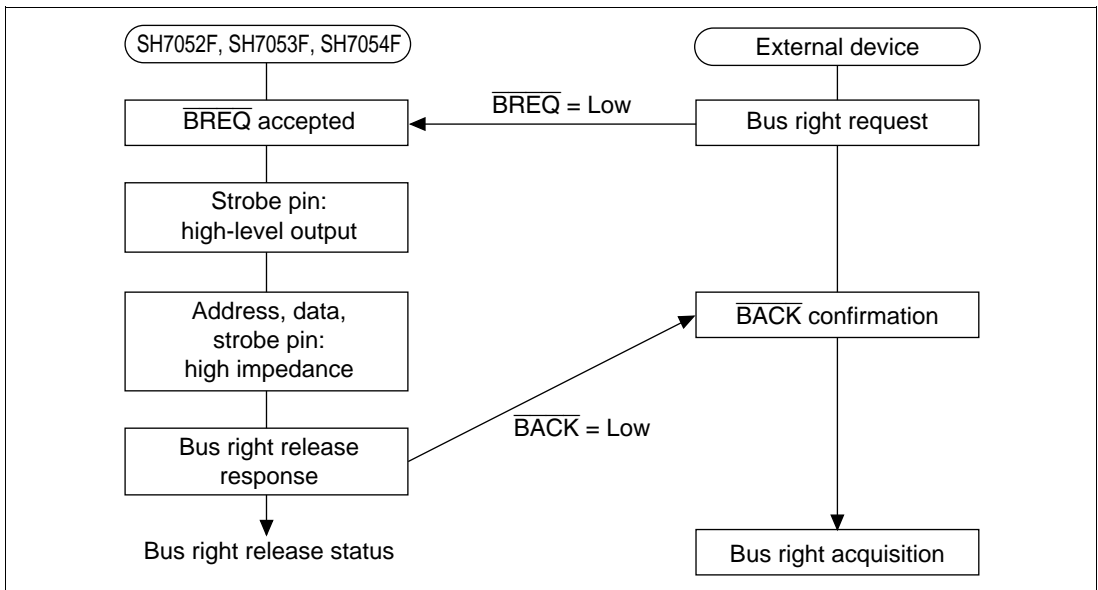
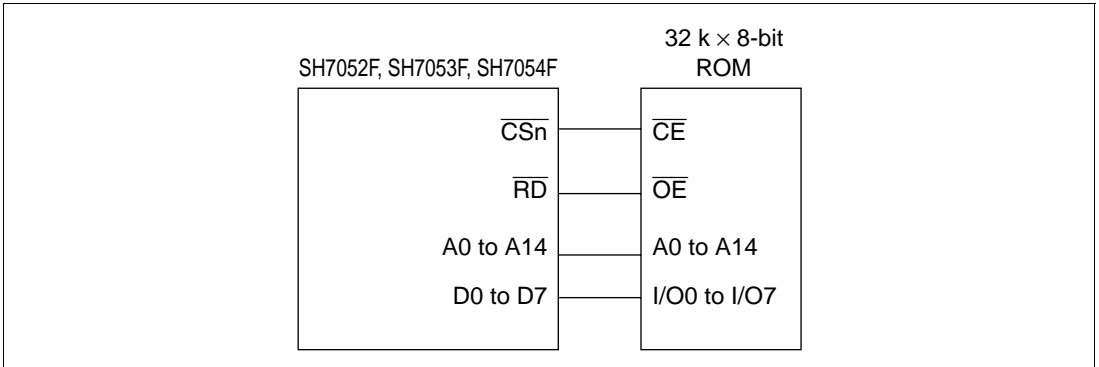


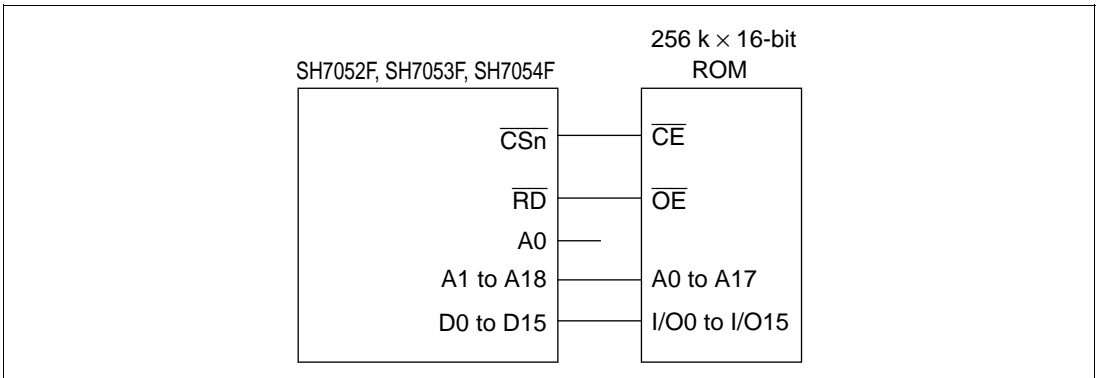
Figure 8.9 Bus Right Release Procedure

## 8.6 Memory Connection Examples

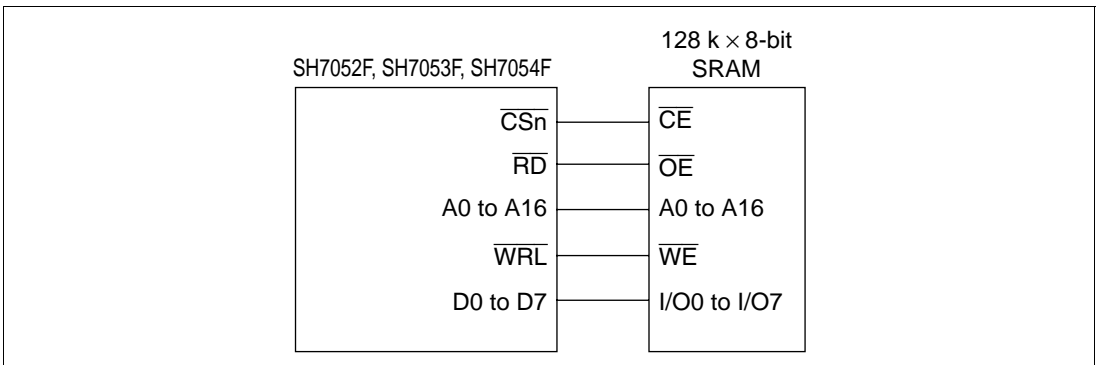
Figures 8.10 to 8.13 show examples of the memory connections.



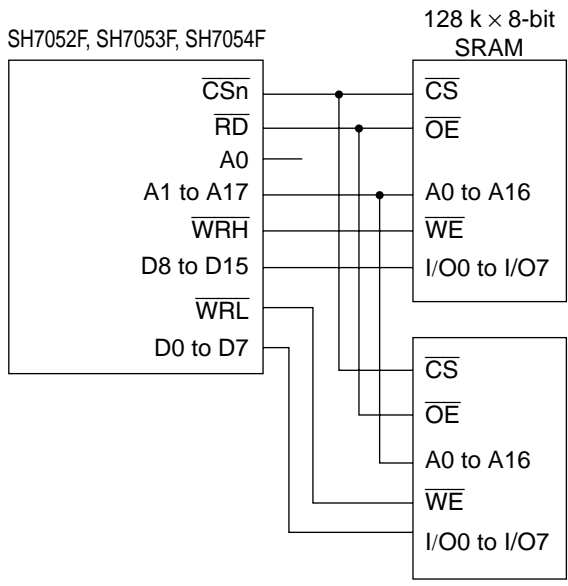
**Figure 8.10 Example of 8-Bit Data Bus Width ROM Connection**



**Figure 8.11 Example of 16-Bit Data Bus Width ROM Connection**



**Figure 8.12 Example of 8-Bit Data Bus Width SRAM Connection**



**Figure 8.13 Example of 16-Bit Data Bus Width SRAM Connection**

# Section 9 Direct Memory Access Controller (DMAC)

## 9.1 Overview

The SH7052F/SH7053F/SH7054F includes an on-chip four-channel direct memory access controller (DMAC). The DMAC can be used in place of the CPU to perform high-speed data transfers among external memories, memory-mapped external devices, and on-chip peripheral modules (except for the DMAC, BSC, and UBC). Using the DMAC reduces the burden on the CPU and increases the operating efficiency of the chip as a whole.

### 9.1.1 Features

The DMAC has the following features:

- Four channels
- 4-Gbyte address space in the architecture
- 8-, 16-, or 32-bit selectable data transfer length
- Maximum of 16 M (6,777,216) transfers
- Address modes

Both the transfer source and transfer destination are accessed by address. There are two transfer modes: direct address and indirect address.

— Direct address transfer mode: Values set in a DMAC internal register indicate the accessed address for both the transfer source and transfer destination. Two bus cycles are required for one data transfer.

— Indirect address transfer mode: The value stored at the location pointed to by the address set in the DMAC internal transfer source register is used as the address. Operation is otherwise the same as for direct access. This function can only be set for channel 3. Four bus cycles are required for one data transfer.

- Channel function: Dual address mode is supported on all channels.

Channel 2 has a source address reload function that reloads the source address every fourth transfer. Direct address transfer mode or indirect address transfer mode can be specified for channel 3.

- Reload function

Enables automatic reloading of the value set in the first source address register every fourth DMA transfer. This function can be executed on channel 2 only.

- Transfer requests

There are two DMAC transfer activation requests, as indicated below.

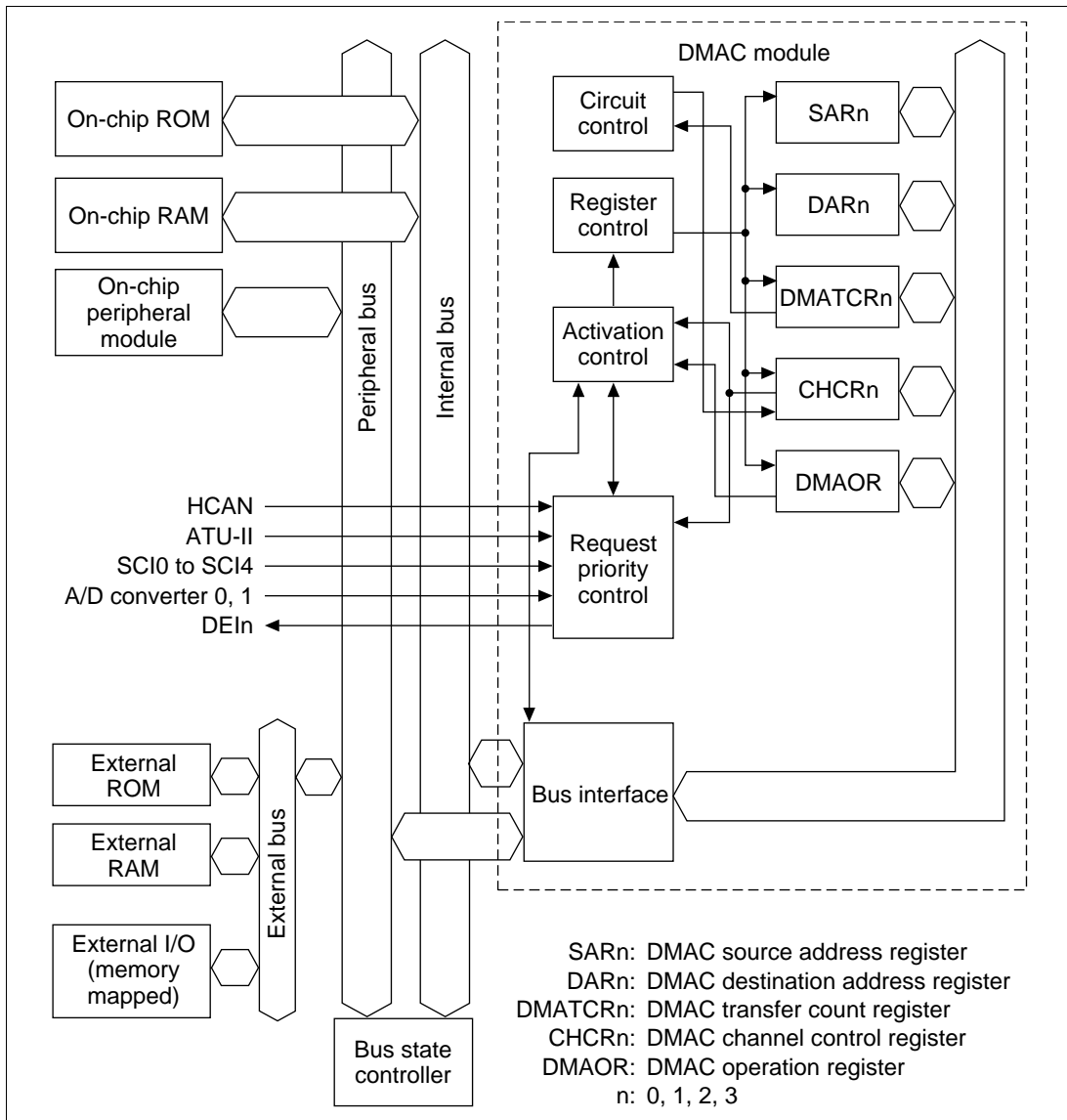
— Requests from on-chip peripheral modules: Transfer requests from on-chip modules such as the SCI or A/D. These can be received by all channels.

— Auto-request: The transfer request is generated automatically within the DMAC.

- Selectable bus modes: Cycle-steal mode or burst mode
- Fixed DMAC channel priority ranking
- CPU can be interrupted when the specified number of data transfers are complete.

### 9.1.2 Block Diagram

Figure 9.1 is a block diagram of the DMAC.



**Figure 9.1 DMAC Block Diagram**

### 9.1.3 Register Configuration

Table 9.1 summarizes the DMAC registers. The DMAC has a total of 17 registers. Each channel has four registers, and one overall DMAC control register is shared by all channels.

**Table 9.1 DMAC Registers**

Channel	Name	Abbr.	R/W	Initial Value	Address	Register Size	Access Size
0	DMA source address register 0	SAR0	R/W	Undefined	H'FFFFFFECC0	32 bits	16, 32 <sup>*2</sup>
	DMA destination address register 0	DAR0	R/W	Undefined	H'FFFFFFECC4	32 bits	16, 32 <sup>*2</sup>
	DMA transfer count register 0	DMATCR0	R/W	Undefined	H'FFFFFFECC8	32 bits	16, 32 <sup>*2</sup>
	DMA channel control register 0	CHCR0	R/W <sup>*1</sup>	H'00000000	H'FFFFFFECCC	32 bits	16, 32 <sup>*2</sup>
1	DMA source address register 1	SAR1	R/W	Undefined	H'FFFFFFECD0	32 bits	16, 32 <sup>*2</sup>
	DMA destination address register 1	DAR1	R/W	Undefined	H'FFFFFFECD4	32 bits	16, 32 <sup>*2</sup>
	DMA transfer count register 1	DMATCR1	R/W	Undefined	H'FFFFFFECD8	32 bits	16, 32 <sup>*3</sup>
	DMA channel control register 1	CHCR1	R/W <sup>*1</sup>	H'00000000	H'FFFFFFECCD	32 bits	16, 32 <sup>*2</sup>
2	DMA source address register 2	SAR2	R/W	Undefined	H'FFFFFFECE0	32 bits	16, 32 <sup>*2</sup>
	DMA destination address register 2	DAR2	R/W	Undefined	H'FFFFFFECE4	32 bits	16, 32 <sup>*2</sup>
	DMA transfer count register 2	DMATCR2	R/W	Undefined	H'FFFFFFECE8	32 bits	16, 32 <sup>*3</sup>
	DMA channel control register 2	CHCR2	R/W <sup>*1</sup>	H'00000000	H'FFFFFFECEC	32 bits	16, 32 <sup>*2</sup>

**Table 9.1 DMAC Registers (cont)**

Channel	Name	Abbr.	R/W	Initial Value	Address	Register Size	Access Size
3	DMA source address register 3	SAR3	R/W	Undefined	H'FFFFE0F0	32 bits	16, 32 <sup>*2</sup>
	DMA destination address register 3	DAR3	R/W	Undefined	H'FFFFE0F4	32 bits	16, 32 <sup>*2</sup>
	DMA transfer count register 3	DMATCR3	R/W	Undefined	H'FFFFE0F8	32 bits	16, 32 <sup>*3</sup>
	DMA channel control register 3	CHCR3	R/W <sup>*1</sup>	H'00000000	H'FFFFE0FC	32 bits	16, 32 <sup>*2</sup>
Shared	DMA operation register	DMAOR	R/W <sup>*1</sup>	H'0000	H'FFFFE0B0	16 bits	16 <sup>*4</sup>

Notes: Word access to a register takes 3 cycles, and longword access 6 cycles.

1. Write 0 after reading 1 in bit 1 of CHCR0 to CHCR3 and in bits 1 and 2 of DMAOR to clear flags. No other writes are allowed.
2. For 16-bit access of SAR0 to SAR3, DAR0 to DAR3, and CHCR0 to CHCR3, the 16-bit value on the side not accessed is held.
3. DMATCR has a 24-bit configuration: bits 0 to 23. Writing to the upper 8 bits (bits 24 to 31) is invalid, and these bits always read 0.
4. Do not use 32-bit access on DMAOR.
5. Do not attempt to access an empty address, as operation cannot be guaranteed if this is done.

## 9.2 Register Descriptions

### 9.2.1 DMA Source Address Registers 0 to 3 (SAR0 to SAR3)

DMA source address registers 0 to 3 (SAR0 to SAR3) are 32-bit readable/writable registers that specify the source address of a DMA transfer. These registers have a count function, and during a DMA transfer, they indicate the next source address.

Specify a 16-bit boundary when performing 16-bit data transfers, and a 32-bit boundary when performing 32-bit data transfers. Operation cannot be guaranteed if any other addresses are set.

The initial value after a power-on reset and in standby mode is undefined.



Bit:	31	30	29	28	27	26	25	24
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	23	22	21	...	...	2	1	0
				...	...			
Initial value:	—	—	—	...	...	—	—	—
R/W:	R/W	R/W	R/W	...	...	R/W	R/W	R/W

### 9.2.2 DMA Destination Address Registers 0 to 3 (DAR0 to DAR3)

DMA destination address registers 0 to 3 (DAR0 to DAR3) are 32-bit readable/writable registers that specify the destination address of a DMA transfer. These registers have a count function, and during a DMA transfer, they indicate the next destination address.

Specify a 16-bit boundary when performing 16-bit data transfers, and a 32-bit boundary when performing 32-bit data transfers. Operation cannot be guaranteed if any other addresses are set.

The value after a power-on reset and in standby mode is undefined.

Bit:	31	30	29	28	27	26	25	24
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	23	22	21	...	...	2	1	0
				...	...			
Initial value:	—	—	—	...	...	—	—	—
R/W:	R/W	R/W	R/W	...	...	R/W	R/W	R/W

### 9.2.3 DMA Transfer Count Registers 0 to 3 (DMATCR0 to DMATCR3)

DMA transfer count registers 0 to 3 (DMATCR0 to DMATCR3) are 24-bit read/write registers that specify the transfer count for the channel (byte count, word count, or longword count) in bits 23 to 0. Specifying H'000001 gives a transfer count of 1, while H'000000 gives the maximum setting, 16,777,216 transfers. During DMAC operation, these registers indicate the remaining number of transfers.

The upper 8 bits of DMATCR always read 0. The write value, also, should always be 0.

The value after a power-on reset and in standby mode is undefined.

Bit:	31	30	29	28	27	26	25	24
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	23	22	21	20	19	18	17	16
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## 9.2.4 DMA Channel Control Registers 0 to 3 (CHCR0 to CHCR3)

DMA channel control registers 0 to 3 (CHCR0 to CHCR3) are 32-bit readable/writable registers that designate the operation and transmission of each channel. CHCR register bits are initialized to 0 by a power-on reset and in standby mode.

Bit:	31	30	29	28	27	26	25	24
	—	—	—	DI	—	—	—	RO
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W*2	R	R	R	R/W*2
Bit:	23	22	21	20	19	18	17	16
	—	—	—	RS4	RS3	RS2	RS1	RS0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W*1	R/W
Bit:	15	14	13	12	11	10	9	8
	—	—	SM1	SM0	—	—	DM1	DM0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	—	—	TS1	TS0	TM	IE	TE	DE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/(W)*1	R/W

Notes: 1. TE bit: Allows only a 0 write after reading 1.

2. The DI and RO bits may be absent, depending on the channel.

- Bits 31 to 29, 27 to 25, 23 to 21, 15, 14, 11, 10, 7, 6—Reserved: These bits are always read as 0, and should only be written with 0.
- Bit 28—Direct/Indirect Select (DI): Specifies either direct address mode operation or indirect address mode operation for the channel 3 source address. This bit is valid only in CHCR3. It always reads 0 in CHCR0 to CHCR2, and should always be written with 0.

Bit 28: DI	Description	
0	Direct access mode operation for channel 3	(Initial value)
1	Indirect access mode operation for channel 3	

- Bit 24—Source Address Reload (RO): Selects whether to reload the source address initial value during channel 2 transfer. This bit is valid only for channel 2. It always reads 0 in CHCR0, CHCR1, and CHCR3, and should always be written with 0.

Bit 24: RO	Description	
0	Does not reload source address	(Initial value)
1	Reloads source address	

- Bits 20 to 16—Resource Select 4 to 0 (RS4 to RS0): These bits specify the transfer request source.

Bit 20: RS4	Bit 19: RS3	Bit 18: RS2	Bit 17: RS1	Bit 16: RS0	Description	
0	0	0	0	0	No request (Initial value)	
				1	SCI0 transmission	
			1	0	0	SCI0 reception
					1	SCI1 transmission
				1	0	SCI1 reception
					1	SCI2 transmission
	1	0	0	0	SCI2 reception	
				1	SCI3 transmission	
				1	SCI3 reception	
			1	0	0	SCI4 transmission
					1	SCI4 reception
				1	On-chip A/D0	
		1	1	0	0	On-chip A/D1
					1	No request
			1	0	No request	
				1	HCAN (RM)	
1	0	0	0	0	No request	
				1	ATU-II (ICI0A)	
			1	0	0	ATU-II (ICI0B)
					1	ATU-II (ICI0C)
				1	0	ATU-II (ICI0D)
					1	ATU-II (CMI6A)
		1	0	0	0	ATU-II (CMI6B)
					1	ATU-II (CMI6C)
				1	0	ATU-II (CMI6D)
			1		ATU-II (CMI7A)	
			1		ATU-II (CMI7B)	
			1	0	0	0
	1	ATU-II (CMI7D)				
	1	0		No request		
		1		No request		
					1	Auto-request

- Bits 13 and 12—Source Address Mode 1 and 0 (SM1, SM0): These bits specify increment/decrement of the DMA transfer source address.

Bit 13: SM1	Bit 12: SM0	Description
0	0	Source address fixed (Initial value)
0	1	Source address incremented (+1 during 8-bit transfer, +2 during 16-bit transfer, +4 during 32-bit transfer)
1	0	Source address decremented (−1 during 8-bit transfer, −2 during 16-bit transfer, −4 during 32-bit transfer)
1	1	Setting prohibited

When the transfer source is specified at an indirect address, specify in source address register 3 (SAR3) the actual storage address of the data to be transferred as the data storage address (indirect address).

During indirect address mode, SAR3 obeys the SM1/SM0 setting for increment/decrement. In this case, SAR3's increment/decrement is fixed at +4/−4 or 0, irrespective of the transfer data size specified by TS1 and TS0.

- Bits 9 and 8—Destination Address Mode 1 and 0 (DM1, DM0): These bits specify increment/decrement of the DMA transfer source address.

Bit 9: DM1	Bit 8: DM0	Description
0	0	Destination address fixed (Initial value)
0	1	Destination address incremented (+1 during 8-bit transfer, +2 during 16-bit transfer, +4 during 32-bit transfer)
1	0	Destination address decremented (−1 during 8-bit transfer, −2 during 16-bit transfer, −4 during 32-bit transfer)
1	1	Setting prohibited

- Bits 5 and 4—Transfer Size 1 and 0 (TS1, TS0): These bits specify the size of the data for transfer.

Bit 5: TS1	Bit 4: TS0	Description
0	0	Specifies byte size (8 bits) (Initial value)
0	1	Specifies word size (16 bits)
1	0	Specifies longword size (32 bits)
1	1	Setting prohibited

- Bit 3—Transfer Mode (TM): Specifies the bus mode for data transfer.

Bit 3: TM	Description
0	Cycle-steal mode (Initial value)
1	Burst mode

- Bit 2—Interrupt Enable (IE): When this bit is set to 1, interrupt requests are generated after the number of data transfers specified in DMATCR (when TE = 1).

Bit 2: IE	Description
0	Interrupt request not generated on completion of DMATCR-specified number of transfers (Initial value)
1	Interrupt request enabled on completion of DMATCR-specified number of transfers

- Bit 1—Transfer End (TE): This bit is set to 1 after the number of data transfers specified by DMATCR. At this time, if the IE bit is set to 1, an interrupt request is generated.

If data transfer ends before TE is set to 1 (for example, due to an NMI or address error, or clearing of the DE bit or DME bit of DMAOR) TE is not set to 1. With this bit set to 1, data transfer is disabled even if the DE bit is set to 1.

Bit 1: TE	Description
0	DMATCR-specified number of transfers not completed (Initial value) [Clearing condition] 0 write after TE = 1 read, power-on reset, standby mode
1	DMATCR-specified number of transfers completed

- Bit 0—DMAC Enable (DE): DE enables operation in the corresponding channel.

Bit 0: DE	Description
0	Operation of the corresponding channel disabled (Initial value)
1	Operation of the corresponding channel enabled

Transfer is initiated if this bit is set to 1 when auto-request is specified (RS4 to RS0 settings). With an on-chip module request, when a transfer request occurs after this bit is set to 1, transfer is initiated. If this bit is cleared during a data transfer, transfer is suspended.

If the DE bit has been set, but TE = 1, then if the DME bit of DMAOR is 0, and the NMIF or AE bit of DMAOR is 1, the transfer enable state is not entered.

## 9.2.5 DMAC Operation Register (DMAOR)

DMAOR is a 16-bit readable/writable register that controls the overall operation of the DMAC.

Register values are initialized to 0 by a power-on reset and in standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	AE	NMIF	DME
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/(W)*	R/(W)*	R/W

Note: \* A 0 write only is valid after 1 is read at the AE and NMIF bits.

- Bits 15 to 3—Reserved: These bits are always read 0 and should always be written with 0.
- Bit 2—Address Error Flag (AE): Indicates that an address error has occurred during DMA transfer. If this bit is set during a data transfer, transfers on all channels are suspended. The CPU cannot write a 1 to the AE bit. Clearing is effected by a 0 write after a 1 read.

Bit 2: AE	Description
0	No address error, DMA transfer enabled [Clearing condition] Write AE = 0 after reading AE = 1 (Initial value)
1	Address error, DMA transfer disabled [Setting condition] Address error due to DMAC



- Bit 1—NMI Flag (NMIF): Indicates input of an NMI. This bit is set irrespective of whether the DMAC is operating or suspended. If this bit is set during a data transfer, transfers on all channels are suspended. The CPU is unable to write a 1 to the NMIF. Clearing is effected by a 0 write after a 1 read.

Bit 1: NMIF	Description
0	No NMI interrupt, DMA transfer enabled (Initial value) [Clearing condition] Write NMIF = 0 after reading NMIF = 1
1	NMI has occurred, DMC transfer disabled [Setting condition] NMI interrupt occurrence

- Bit 0—DMAC Master Enable (DME): This bit enables activation of the entire DMAC. When the DME bit and DE bit of the CHCR register for the corresponding channel are set to 1, that channel is transfer-enabled. If this bit is cleared during a data transfer, transfers on all channels are suspended.

Even when the DME bit is set, when the TE bit of CHCR is 1, or its DE bit is 0, transfer is disabled if the NMIF or AE bit in DMAOR is set to 1.

Bit 0: DME	Description
0	Operation disabled on all channels (Initial value)
1	Operation enabled on all channels

## 9.3 Operation

When there is a DMA transfer request, the DMAC starts the transfer according to the channel priority order; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto-request and on-chip peripheral module request. Transfer is performed only in dual address mode, and either direct or indirect address transfer mode can be used. The bus mode can be either burst or cycle-steal.

### 9.3.1 DMA Transfer Flow

After the DMA source address registers (SAR), DMA destination address registers (DAR), DMA transfer count register (DMATCR), DMA channel control registers (CHCR), and DMA operation register (DMAOR) are set to the desired transfer conditions, the DMAC transfers data according to the following procedure:

1. The DMAC checks to see if transfer is enabled (DE = 1, DME = 1, TE = 0, NMIF = 0, AE = 0).
2. When a transfer request comes and transfer has been enabled, the DMAC transfers 1 transfer unit of data (determined by the TS0 and TS1 setting). For an auto-request, the transfer begins automatically when the DE bit and DME bit are set to 1. The DMATCR value will be decremented by 1 upon each transfer. The actual transfer flows vary by address mode and bus mode.
3. When the specified number of transfers have been completed (when DMATCR reaches 0), the transfer ends normally. If the IE bit of CHCR is set to 1 at this time, a DEI interrupt is sent to the CPU.
4. When an address error occurs in the DMAC or an NMI interrupt is generated, the transfer is aborted. Transfer is also aborted when the DE bit of CHCR or the DME bit of DMAOR is cleared to 0.

Figure 9.2 is a flowchart of this procedure.

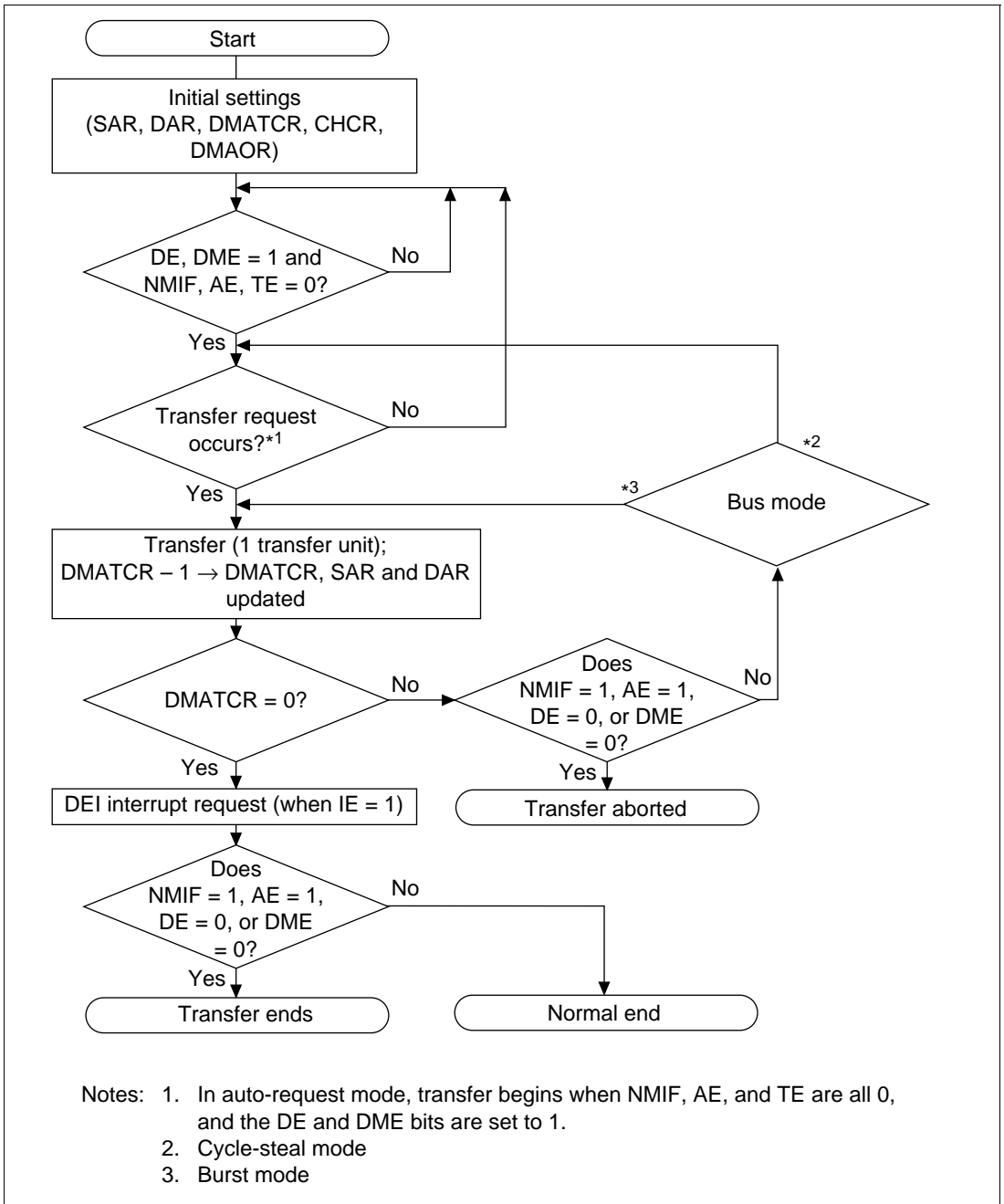


Figure 9.2 DMAC Transfer Flowchart

### 9.3.2 DMA Transfer Requests

DMA transfer requests are generated in either the data transfer source or destination. Transfers can be requested in two modes: auto-request and on-chip peripheral module request. The request mode is selected in the RS4 to RS0 bits of DMA channel control registers 0 to 3 (CHCR0 to CHCR3).

**Auto-Request Mode:** When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, the auto-request mode allows the DMAC to automatically generate a transfer request signal internally. When the DE bits of CHCR0 to CHCR3 and the DME bit of DMAOR are set to 1, the transfer begins (so long as the TE bits of CHCR0 to CHCR3 and the NMIF and AE bits of DMAOR are all 0).

**On-Chip Peripheral Module Request Mode:** In this mode a transfer is performed at the transfer request signal (interrupt request signal) of an on-chip peripheral module. As indicated in table 9.2, there are 26 transfer request signals: 12 from the advanced timer unit (ATU-II), which are compare match or input capture interrupts; the receive data full interrupts (RXI) and transmit data empty interrupts (TXI) of the five serial communication interfaces (SCI); the receive interrupt of HCAN; and the A/D conversion end interrupts (ADI) of the three A/D converters. When DMA transfers are enabled (DE = 1, DME = 1, TE = 0, NMIF = 0, AE = 0), a transfer is performed upon the input of a transfer request signal.

When the transfer request is set to RXI (transfer request because the SCI's receive data register is full), the transfer source must be the SCI's receive data register (RDR). When the transfer request is set to TXI (transfer request because the SCI's transmit data register is empty), the transfer destination must be the SCI's transmit data register (TDR). If the transfer request is set to the A/D converter, the data transfer source must be the A/D converter register; if set to HCAN, the transfer source must be HCAN message data.

**Table 9.2 Selecting On-Chip Peripheral Module Request Modes with the RS Bits**

RS4	RS3	RS2	RS1	RS0	DMAC Transfer Request Source	DMAC Transfer Request Signal	Transfer Source	Transfer Destination	Bus Mode		
0	0	0	0	1	SCI0 transmit block	TXI0 (SCI0 transmit-data-empty transfer request)	Don't care*	TDR0	Burst/cycle-steal		
				1	0	SCI0 receive block	RXI0 (SCI0 receive-data-full transfer request)	RDR0	Don't care*	Burst/cycle-steal	
				1	1	SCI1 transmit block	TXI1 (SCI1 transmit-data-empty transfer request)	Don't care*	TDR1	Burst/cycle-steal	
	1	0	0	0	SCI1 receive block	RXI1 (SCI1 receive-data-full transfer request)	RDR1	Don't care*	Burst/cycle-steal		
				1	1	SCI2 transmit block	TXI2 (SCI2 transmit-data-empty transfer request)	Don't care*	TDR2	Burst/cycle-steal	
				1	0	SCI2 receive block	RXI2 (SCI2 receive-data-full transfer request)	RDR2	Don't care*	Burst/cycle-steal	
		1	0	0	0	SCI3 receive block	RXI3 (SCI3 receive-data-full transfer request)	RDR3	Don't care*	Burst/cycle-steal	
					1	1	SCI4 transmit block	TXI4 (SCI4 transmit-data-empty transfer request)	Don't care*	TDR4	Burst/cycle-steal
					1	0	SCI4 receive block	RXI4 (SCI4 receive-data-full transfer request)	RDR4	Don't care*	Burst/cycle-steal
	1	0	0	0	A/D0	ADI0 (A/D0 conversion end interrupt)	ADDR0 to ADDR11	Don't care*	Burst/cycle-steal		
				1	0	A/D1	ADI1 (A/D1 conversion end interrupt)	ADDR12 to ADDR23	Don't care*	Burst/cycle-steal	
				1	1	Reserved					
1	1	1	1	1	HCAN	RM0 (HCAN receive interrupt)	MD0 to MD15	Don't care*	Burst/cycle-steal		

**Table 9.2 Selecting On-Chip Peripheral Module Request Modes with the RS Bits (cont)**

RS4	RS3	RS2	RS1	RS0	DMAC Transfer Request Source	DMAC Transfer Request Signal	Transfer Source	Transfer Destination	Bus Mode					
1	0	0	0	1	ATU-II	ICI0A (ICR0A input capture generation)	Don't care*	Don't care*	Burst/cycle-steal					
				0	ATU-II	ICI0B (ICR0B input capture generation)	Don't care*	Don't care*	Burst/cycle-steal					
				1	ATU-II	ICI0C (ICR0C input capture generation)	Don't care*	Don't care*	Burst/cycle-steal					
			1	0	0	0	ATU-II	ICI0D (ICR0D input capture generation)	Don't care*	Don't care*	Burst/cycle-steal			
						1	ATU-II	CMI6A (CYLR6A compare-match generation)	Don't care*	Don't care*	Burst/cycle-steal			
					1	0	0	0	ATU-II	CMI6B (CYLR6B compare-match generation)	Don't care*	Don't care*	Burst/cycle-steal	
								1	ATU-II	CMI6C (CYLR6C compare-match generation)	Don't care*	Don't care*	Burst/cycle-steal	
								1	ATU-II	CMI6D (CYLR6D compare-match generation)	Don't care*	Don't care*	Burst/cycle-steal	
					1	0	0	0	0	ATU-II	CMI7A (CYLR7A compare-match generation)	Don't care*	Don't care*	Burst/cycle-steal
									1	ATU-II	CMI7B (CYLR7B compare-match generation)	Don't care*	Don't care*	Burst/cycle-steal
1	ATU-II	CMI7C (CYLR7C compare-match generation)	Don't care*	Don't care*					Burst/cycle-steal					
1	ATU-II	CMI7D (CYLR7D compare-match generation)	Don't care*	Don't care*					Burst/cycle-steal					

**Legend:**

SCIO, SCI1, SCI2, SCI3, SCI4: Serial communication interface channels 0 to 4  
 A/D0, A/D1: A/D converter channels 0, 1  
 HCAN: Hitachi controller area network channel 0  
 ATU-II: Advanced timer unit  
 TDR0, TDR1, TDR2, TDR3, TDR4: SCIO to SCI4 transmit data registers  
 RDR0, RDR1, RDR2, RDR3, RDR4: SCIO to SCI4 receive data registers  
 ADDR0 to ADDR11: A/D0 data registers

ADDR12 to ADDR23:

A/D1 data registers

MD0 to MD15:

HCAN message data

Note: \* External memory, memory-mapped external device, on-chip memory, on-chip peripheral module (excluding DMAC, BSC, and UBC)

### 9.3.3 Channel Priority

When the DMAC receives simultaneous transfer requests on two or more channels, it selects a channel according to the following priority order:

- CH0 > CH1 > CH2 > CH3

### 9.3.4 DMA Transfer Types

The DMAC supports the transfers shown in table 9.3. It operates in dual address mode, in which both the transfer source and destination addresses are output. The dual address mode consists of a direct address mode, in which the output address value is the object of a direct data transfer, and an indirect address mode, in which the output address value is not the object of the data transfer, but the value stored at the output address becomes the transfer object address. The actual transfer operation timing varies with the bus mode. The DMAC has two bus modes: cycle-steal mode and burst mode.

**Table 9.3 Supported DMA Transfers**

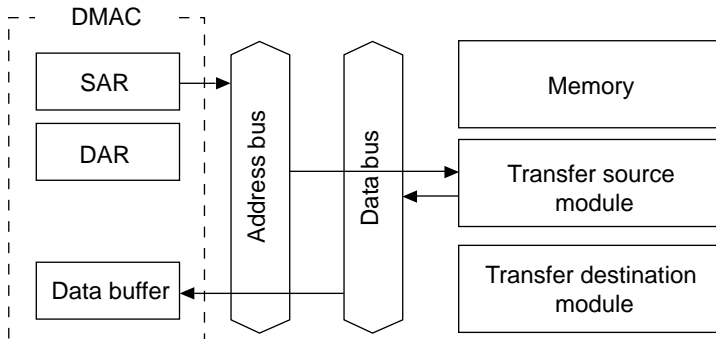
Transfer Source	Transfer Destination			
	External Memory	Memory-Mapped External Device	On-Chip Memory	On-Chip Peripheral Module
External memory	Supported	Supported	Supported	Supported
Memory-mapped external device	Supported	Supported	Supported	Supported
On-chip memory	Supported	Supported	Supported	Supported
On-chip peripheral module	Supported	Supported	Supported	Supported

### 9.3.5 Dual Address Mode

Dual address mode is used for access of both the transfer source and destination by address. Transfer source and destination can be accessed either internally or externally. Dual address mode is subdivided into two other modes: direct address transfer mode and indirect address transfer mode.

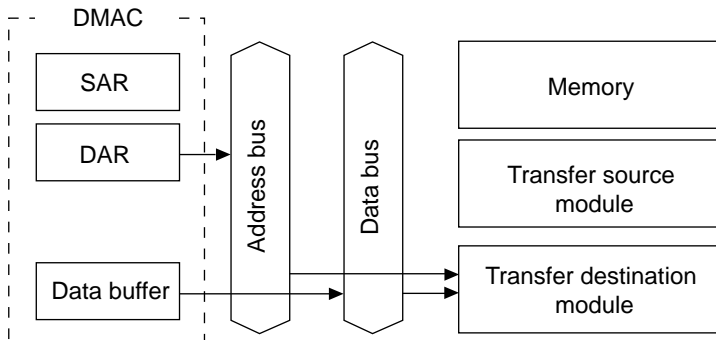
**Direct Address Transfer Mode:** Data is read from the transfer source during the data read cycle, and written to the transfer destination during the write cycle, so transfer is conducted in two bus cycles. At this time, the transfer data is temporarily stored in the DMAC. With the kind of external memory transfer shown in figure 9.3, data is read from one of the memories by the DMAC during a read cycle, then written to the other external memory during the subsequent write cycle. Figure 9.4 shows the timing for this operation.

### 1st bus cycle



The SAR value is taken as the address, and data is read from the transfer source module and stored temporarily in the DMAC.

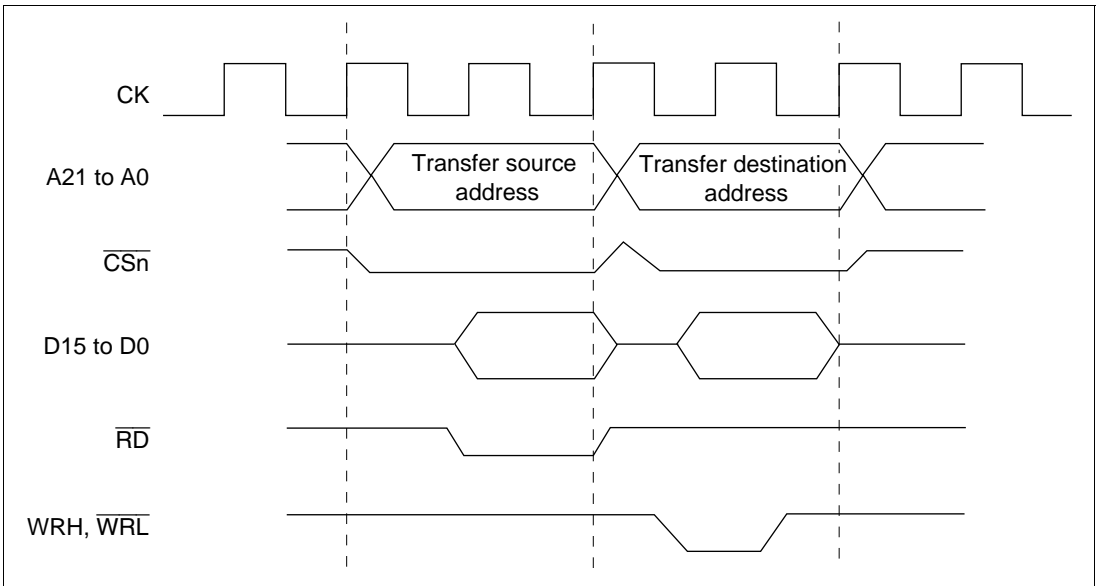
### 2nd bus cycle



The DAR value is taken as the address, and data stored in the DMAC's data buffer is written to the transfer destination module.

**Figure 9.3 Direct Address Operation in Dual Address Mode**





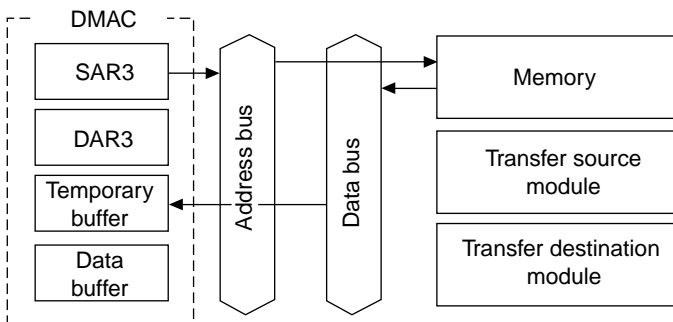
**Figure 9.4 Direct Address Transfer Timing in Dual Address Mode**

**Indirect Address Transfer Mode:** In this mode the memory address storing the data actually to be transferred is specified in the DMAC internal transfer source address register (SAR3). Therefore, in indirect address transfer mode, the DMAC internal transfer source address register value is read first. This value is first stored in the DMAC. Next, the read value is output as the address, and the value stored at that address is again stored in the DMAC. Finally, the subsequent read value is written to the address specified by the transfer destination address register, ending one cycle of DMAC transfer.

In indirect address mode (figure 9.5), the transfer destination, transfer source, and indirect address storage destination are all 16-bit external memory locations, and transfer in this example is conducted in 16-bit or 8-bit units. Timing for this transfer example is shown in figure 9.6.

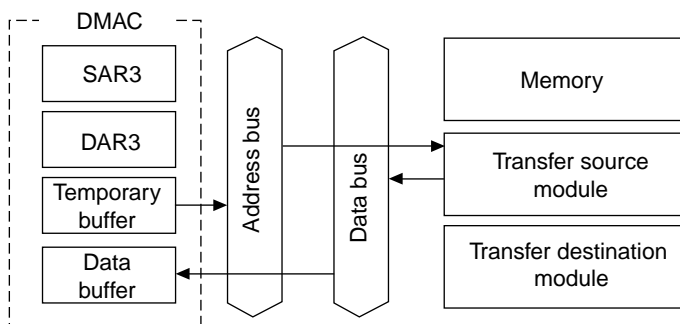
In indirect address mode, one NOP cycle (figure 9.6) is required until the data read as the indirect address is output to the address bus. When transfer data is 32-bit, the third and fourth bus cycles each need to be doubled, giving a required total of six bus cycles and one NOP cycle for the whole operation.

**1st and 2nd bus cycles**



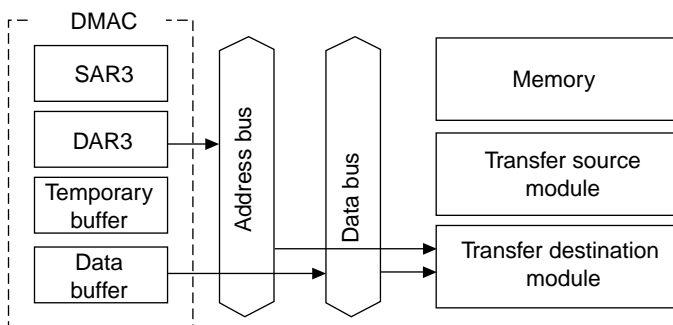
The SAR3 value is taken as the address, memory data is read, and the value is stored in the temporary buffer. Since the value read at this time is used as the address, it must be 32 bits. If the data bus is 16 bits wide when the external memory space is accessed, two bus cycles are necessary.

**3rd bus cycle**



The value in the temporary buffer is taken as the address, and data is read from the transfer source module to the data buffer.

**4th bus cycle**

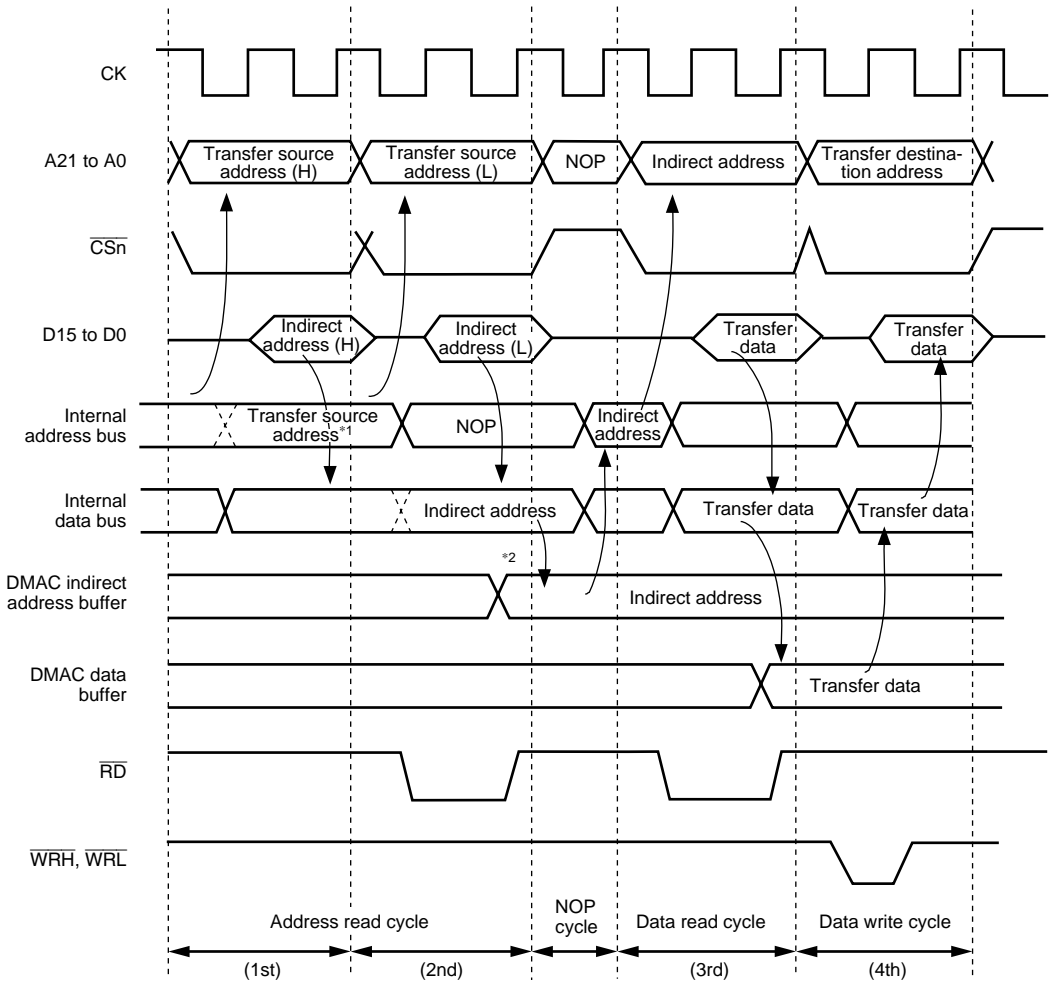


The DAR3 value is taken as the address, and the value in the data buffer is written to the transfer destination module.

Note: Memory, transfer source, and transfer destination modules are shown here. In practice, connection can be made as long as it is within the address space.

**Figure 9.5 Dual Address Mode and Indirect Address Operation (16-Bit-Width External Memory Space)**

**External memory space → External memory space**  
**(External memory space has 16-bit width)**

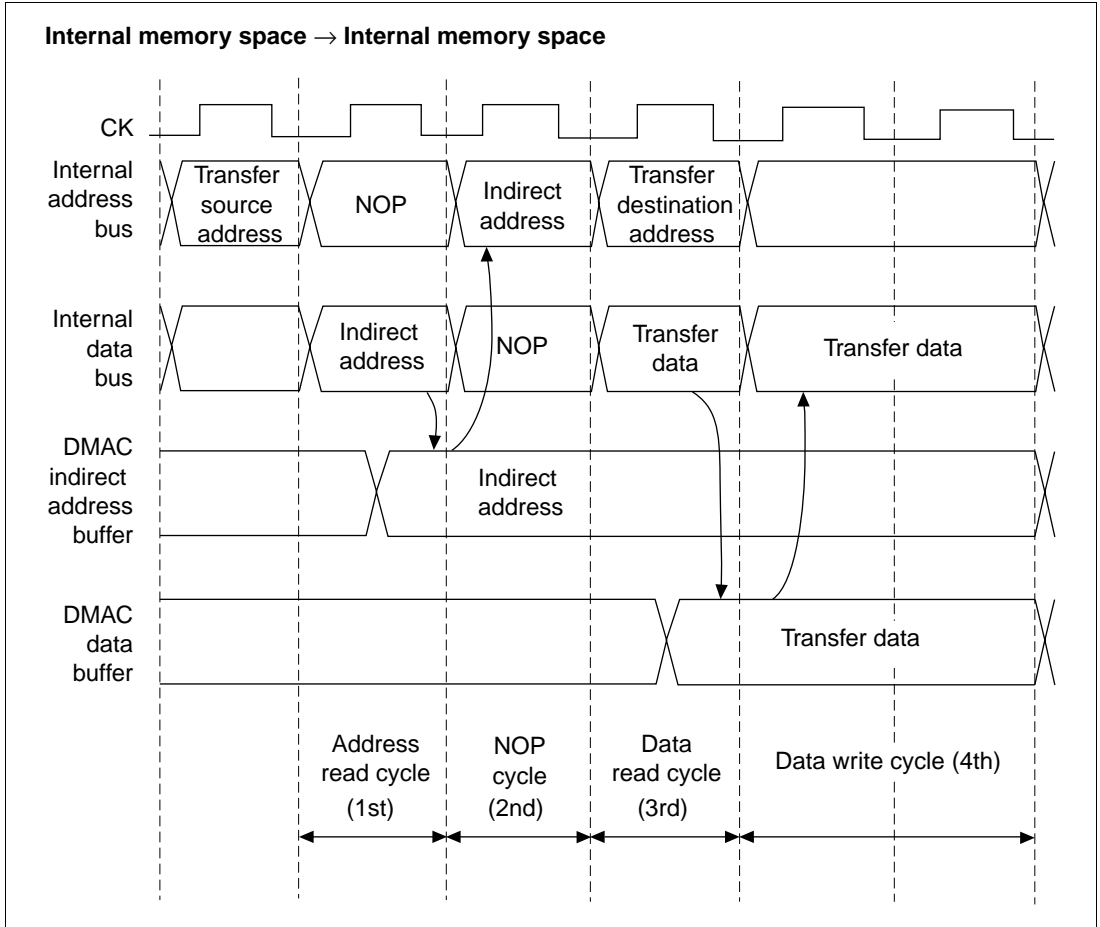


- Notes: 1. The internal address bus is controlled by the port and does not change.  
 2. The DMAC does not latch the value until 32-bit data is read from the internal data bus.

**Figure 9.6 Dual Address Mode and Indirect Address Transfer Timing Example 1**

Figure 9.7 shows an example of timing in indirect address mode when transfer source and indirect address storage locations are in internal memory, the transfer destination is an on-chip peripheral module with 2-cycle access space, and transfer data is 8-bit.

Since the indirect address storage destination and the transfer source are in internal memory, these can be accessed in one cycle. The transfer destination is 2-cycle access space, so two data write cycles are required. One NOP cycle is required until the data read as the indirect address is output to the address bus.



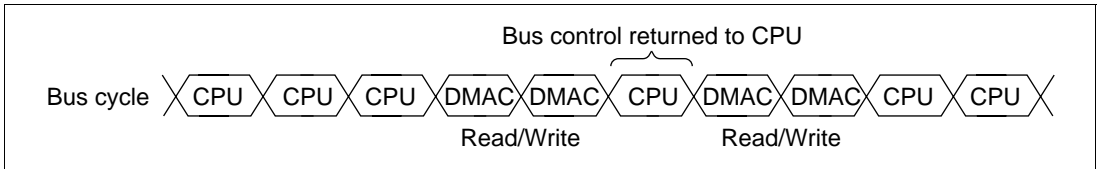
**Figure 9.7 Dual Address Mode and Indirect Address Transfer Timing Example 2**

### 9.3.6 Bus Modes

Select the appropriate bus mode in the TM bits of CHCR0 to CHCR3. There are two bus modes: cycle-steal and burst.

**Cycle-Steal Mode:** In cycle-steal mode, the bus right is given to another bus master after each one-transfer-unit (8-bit, 16-bit, or 32-bit) DMAC transfer. When the next transfer request occurs, the bus right is obtained from the other bus master and a transfer is performed for one transfer unit. When that transfer ends, the bus right is passed to the other bus master. This is repeated until the transfer end conditions are satisfied.

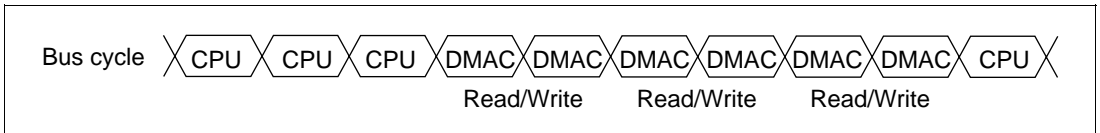
Cycle-steal mode can be used with all categories of transfer destination, transfer source and transfer request. Figure 9.8 shows an example of DMA transfer timing in cycle-steal mode.



**Figure 9.8 DMA Transfer Timing Example in Cycle-Steal Mode**

**Burst Mode:** Once the bus right is obtained, transfer is performed continuously until the transfer end condition is satisfied.

Figure 9.9 shows an example of DMA transfer timing in burst mode.



**Figure 9.9 DMA Transfer Timing Example in Burst Mode**

### 9.3.7 Relationship between Request Modes and Bus Modes by DMA Transfer Category

Table 9.4 shows the relationship between request modes and bus modes by DMA transfer category.

**Table 9.4 Relationship between Request Modes and Bus Modes by DMA Transfer Category**

Address Mode	Transfer Category	Request Mode	Bus* <sup>5</sup> Mode	Transfer Size (Bits)	Usable Channels
Dual	External memory and external memory	Any* <sup>1</sup>	B/C	8/16/32	0 to 3
	External memory and memory-mapped external device	Any* <sup>1</sup>	B/C	8/16/32	0 to 3
	Memory-mapped external device and memory-mapped external device	Any* <sup>1</sup>	B/C	8/16/32	0 to 3
	External memory and on-chip memory	Any* <sup>1</sup>	B/C	8/16/32	0 to 3
	External memory and on-chip peripheral module	Any* <sup>2</sup>	B/C* <sup>3</sup>	8/16/32* <sup>4</sup>	0 to 3
	Memory-mapped external device and on-chip memory	Any* <sup>1</sup>	B/C	8/16/32	0 to 3
	Memory-mapped external device and on-chip peripheral module	Any* <sup>2</sup>	B/C* <sup>3</sup>	8/16/32* <sup>4</sup>	0 to 3
	On-chip memory and on-chip memory	Any* <sup>1</sup>	B/C	8/16/32	0 to 3
	On-chip memory and on-chip peripheral module	Any* <sup>2</sup>	B/C* <sup>3</sup>	8/16/32* <sup>4</sup>	0 to 3
	On-chip peripheral module and on-chip peripheral module	Any* <sup>2</sup>	B/C* <sup>3</sup>	8/16/32* <sup>4</sup>	0 to 3

B: Burst, C: Cycle-steal

- Notes:
1. Auto-request or on-chip peripheral module request enabled. However, in the case of an on-chip peripheral module request, it is not possible to specify the ATU, SCI, HCAN, or A/D converter for the transfer request source.
  2. Auto-request or on-chip peripheral module request possible. However, if the transfer request source is the SCI, HCAN, or A/D converter, the transfer source or transfer destination must be same as the transfer request source.
  3. When the transfer request source is the SCI, only cycle-steal mode is possible.
  4. Access size permitted by the on-chip peripheral module register that is the transfer source or transfer destination.

### 9.3.8 Bus Mode and Channel Priorities

If, for example, a transfer request is issued for channel 0 while transfer is in progress on lower-priority channel 1 in burst mode, transfer is started immediately on channel 0.

In this case, if channel 0 is set to burst mode, channel 1 transfer is continued after completion of all transfers on channel 0. If channel 0 is set to cycle-steal mode, channel 1 transfer is continued only if a channel 0 transfer request has not been issued; if a transfer request is issued, channel 0 transfer is started immediately.

### 9.3.9 Source Address Reload Function

Channel 2 has a source address reload function. This returns to the first value set in the source address register (SAR2) every four transfers by setting the RO bit of CHCR2 to 1. Figure 9.10 illustrates this operation. Figure 9.11 is a timing chart for reload ON mode, with burst mode, auto-request, 16-bit transfer data size, SAR2 increment, and DAR2 fixed.

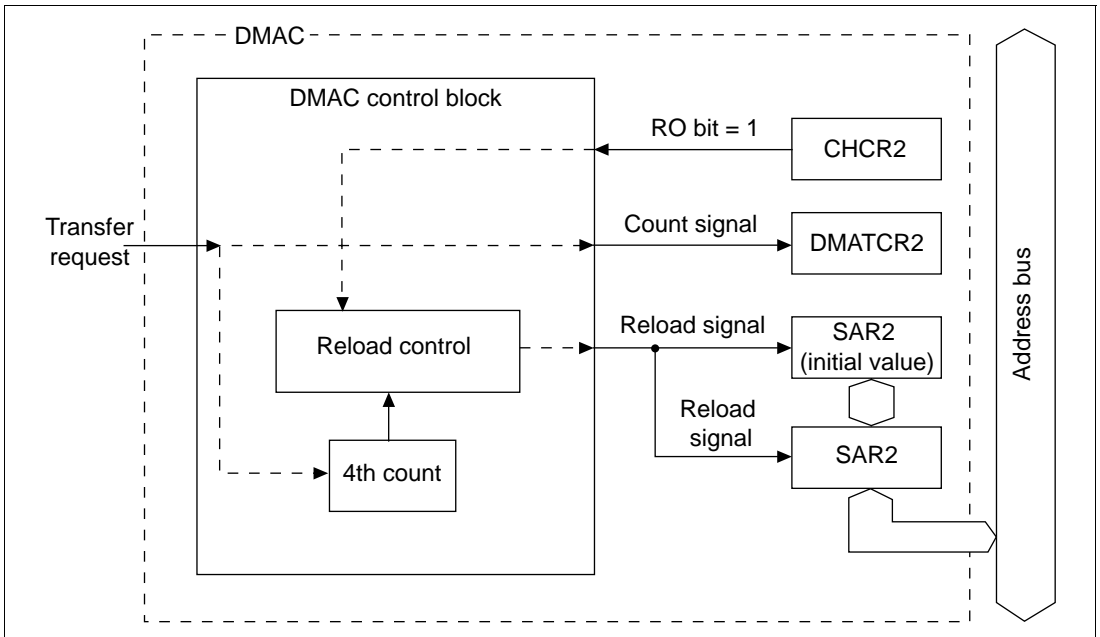
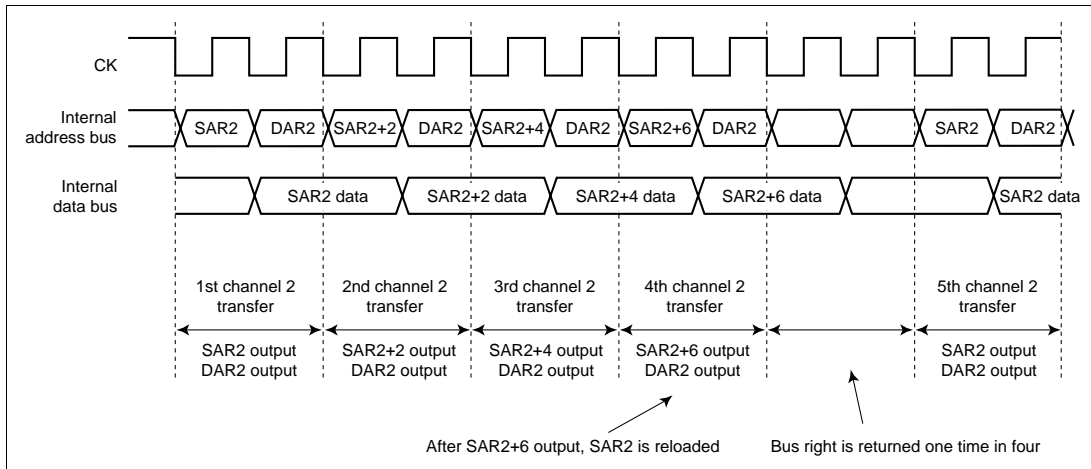


Figure 9.10 Source Address Reload Function



**Figure 9.11 Source Address Reload Function Timing Chart**

The reload function can be executed whether the transfer data size is 8, 16, or 32 bits.

DMATCR2, which specifies the number of transfers, is decremented by 1 at the end of every single-transfer-unit transfer, regardless of whether the reload function is on or off. Therefore, when using the reload function in the on state, a multiple of 4 must be specified in DMATCR2. Operation will not be guaranteed if any other value is set. Also, the counter which counts the occurrence of four transfers for address reloading is reset by clearing of the DME bit in DMAOR or the DE bit in CHCR2, setting of the transfer end flag (the TE bit in CHCR2), NMI input, and setting of the AE flag (address error generation in DMAC transfer), as well as by a reset and in software standby mode, but SAR2, DAR2, DMATCR2, and other registers are not reset. Consequently, when one of these sources occurs, there is a mixture of initialized counters and uninitialized registers in the DMAC, and incorrect operation may result if a restart is executed in this state. Therefore, when one of the above sources, other than TE setting, occurs during use of the address reload function, SAR, DAR2, and DMATCR2 settings must be carried out before re-execution.

### 9.3.10 DMA Transfer Ending Conditions

The DMA transfer ending conditions vary for individual channels ending and for all channels ending together.

**Individual Channel Ending Conditions:** There are two ending conditions. A transfer ends when the value of the channel's DMA transfer count register (DMATCR) is 0, or when the DE bit of the channel's CHCR is cleared to 0.



- When DMATCR is 0: When the DMATCR value becomes 0 and the corresponding channel's DMA transfer ends, the transfer end flag bit (TE) is set in CHCR. If the IE (interrupt enable) bit has been set, a DMAC interrupt (DEI) request is sent to the CPU.
- When DE of CHCR is 0: Software can halt a DMA transfer by clearing the DE bit in the channel's CHCR. The TE bit is not set when this happens.

**Conditions for Ending on All Channels Simultaneously:** Transfers on all channels end when the NMIF (NMI flag) bit or AE (address error flag) bit is set to 1 in DMAOR, or when the DME bit in DMAOR is cleared to 0.

- When the NMIF or AE bit is set to 1 in DMAOR: When an NMI interrupt or DMAC address error occurs, the NMIF or AE bit is set to 1 in DMAOR and all channels stop their transfers. The DMAC obtains the bus right, and if these flags are set to 1 during execution of a transfer, DMAC halts operation when the transfer processing currently being executed ends, and transfers the bus right to the other bus master. Consequently, even if the NMIF or AE bit is set to 1 during a transfer, the DMA source address register (SAR), designation address register (DAR), and transfer count register (DMATCR) are all updated. The TE bit is not set. To resume the transfers after NMI interrupt or address error processing, the NMIF or AE flag must be cleared. To avoid restarting a transfer on a particular channel, clear its DE bit to 0 in CHCR.

When the processing of a one-unit transfer is complete: In a dual address mode direct address transfer, even if an address error occurs or the NMI flag is set during read processing, the transfer will not be halted until after completion of the following write processing. In such a case, SAR, DAR, and DMATCR values are updated. In the same manner, the transfer is not halted in indirect address transfers until after the final write processing has ended.

- When DME is cleared to 0 in DMAOR: Clearing the DME bit to 0 in DMAOR aborts the transfers on all channels. The TE bit is not set.

### 9.3.11 DMAC Access from CPU

The space addressed by the DMAC is 3-cycle space. Therefore, when the CPU becomes the bus master and accesses the DMAC, a minimum of three basic clock cycles are required for one bus cycle. Also, since the DMAC is located in word space, while a word-size access to the DMAC is completed in one bus cycle, a longword-size access is automatically divided into two word accesses, requiring two bus cycles (six basic clock cycles). These two bus cycles are executed consecutively; a different bus cycle is never inserted between the two word accesses. This applies to both write accesses and read accesses.

## 9.4 Examples of Use

### 9.4.1 Example of DMA Transfer between On-Chip SCI and External Memory

In this example, on-chip serial communication interface channel 0 (SCI0) receive data is transferred to external memory using DMAC channel 0.

Table 9.5 indicates the transfer conditions and the set values of each of the registers.

**Table 9.5 Transfer Conditions and Register Set Values for Transfer between On-chip SCI and External Memory**

<b>Transfer Conditions</b>	<b>Register</b>	<b>Value</b>
Transfer source: RDR0 of on-chip SCI0	SAR0	H'FFFFFF05
Transfer destination: external memory	DAR0	H'00400000
Transfer count: 64 times	DMATCR0	H'00000040
Transfer source address: fixed	CHCR0	H'00020105
Transfer destination address: incremented		
Transfer request source: SCI0 (RDR0)		
Bus mode: cycle-steal		
Transfer unit: byte		
Interrupt request generation at end of transfer		
DMAC master enable on	DMAOR	H'0001

### 9.4.2 Example of DMA Transfer between A/D Converter and On-Chip Memory (Address Reload On)

In this example, on-chip A/D converter channel 0 is the transfer source and on-chip memory is the transfer destination, and the address reload function is on.

Table 9.6 indicates the transfer conditions and the set values of each of the registers.

**Table 9.6 Transfer Conditions and Register Set Values for Transfer between A/D Converter and On-Chip Memory**

<b>Transfer Conditions</b>	<b>Register</b>	<b>Value</b>
Transfer source: on-chip A/D converter ch1 (A/D1)	SAR2	H'FFFFFF820
Transfer destination: on-chip memory	DAR2	H'FFFF6000
Transfer count: 128 times (reload count 32 times)	DMATCR2	H'00000080
Transfer source address: incremented	CHCR2	H'010C110D
Transfer destination address: incremented		
Transfer request source: A/D converter ch1 (A/D1)		
Bus mode: burst		
Transfer unit: byte		
Interrupt request generation at end of transfer		
DMAC master enable on	DMAOR	H'0001

When address reload is on, the SAR2 value returns to its initially set value every four transfers. In the above example, when a transfer request is input from the A/D1, the byte-size data is first read in from the H'FFFFFF820 register of on-chip A/D1 and that data is written to internal address H'FFFF6000. Because a byte-size transfer was performed, the SAR2 and DAR2 values at this point are H'FFFFFF821 and H'FFFF6001, respectively. Also, because this is a burst transfer, the bus right remains secured, so continuous data transfer is possible.

When four transfers are completed, if address reload is off, execution continues with the fifth and sixth transfers and the SAR2 value continues to increment from H'FFFFFF824 to H'FFFFFF825 to H'FFFFFF826 and so on. However, when address reload is on, DMAC transfer is halted upon completion of the fourth transfer and the bus right request signal to the CPU is cleared. At this time, the value stored in SAR2 is not H'FFFFFF823 → H'FFFFFF824, but H'FFFFFF823 → H'FFFFFF820, a return to the initially set address. The DAR2 value always continues to be decremented regardless of whether address reload is on or off.

The DMAC internal status, due to the above operation after completion of the fourth transfer, is indicated in table 9.7 for both address reload on and off.

**Table 9.7 DMAC Internal Status**

Item	Address Reload On	Address Reload Off
SAR2	H'FFFFFF820	H'FFFFFF824
DAR2	H'FFFF6004	H'FFFF6004
DMATCR2	H'0000007C	H'0000007C
Bus right	Released	Retained
DMAC operation	Halted	Processing continues
Interrupts	Not issued	Not issued
Transfer request source flag clear	Executed	Not executed

- Notes:
1. Interrupts are executed until the DMATCR2 value becomes 0, and if the IE bit of CHCR2 is set to 1, are issued regardless of whether address reload is on or off.
  2. If transfer request source flag clears are executed until the DMATCR2 value becomes 0, they are executed regardless of whether address reload is on or off.
  3. Designate burst mode when using the address reload function. There are cases where abnormal operation will result if it is used in cycle-steal mode.
  4. Designate a multiple of four for the DMATCR2 value when using the address reload function. There are cases where abnormal operation will result if anything else is designated.

To execute transfers after the fifth transfer when address reload is on, have the transfer request source issue another transfer request signal.

### 9.4.3 Example of DMA Transfer between External Memory and SC11 Transmitting Side (Indirect Address On)

In this example, DMAC channel 3 is used, indirect address designated external memory is the transfer source, and the SC11 transmitting side is the transfer destination.

Table 9.8 indicates the transfer conditions and the set values of each of the registers.

**Table 9.8 Transfer Conditions and Register Set Values for Transfer between External Memory and SCI1 Transmitting Side**

<b>Transfer Conditions</b>	<b>Register</b>	<b>Value</b>
Transfer source: external memory	SAR3	H'00400000
Value stored in address H'00400000	—	H'00450000
Value stored in address H'00450000	—	H'55
Transfer destination: on-chip SCI TDR1	DAR3	H'FFFFFF00B
Transfer count: 10 times	DMATCR3	H'0000000A
Transfer source address: incremented	CHCR3	H'10031001
Transfer destination address: fixed		
Transfer request source: SCI1 (TDR1)		
Bus mode: cycle-steal		
Transfer unit: byte		
Interrupt request not generated at end of transfer		
DMAC master enable on	DMAOR	H'0001

When indirect address mode is on, the data stored in the address set in SAR is not used as the transfer source data. In the case of indirect addressing, the value stored in the SAR address is read, then that value is used as the address and the data read from that address is used as the transfer source data, then that data is stored in the address designated by DAR.

In the table 9.8 example, when a transfer request from TDR1 of SCI1 is generated, a read of the address located at H'00400000, which is the value set in SAR3, is performed first. The data H'00450000 is stored at this H'00400000 address, and the DMAC first reads this H'00450000 value. It then uses this read value of H'00450000 as an address and reads the value of H'55 that is stored in the H'00450000 address. It then writes the value H'55 to address H'FFFFFF00B designated by DAR3 to complete one indirect address transfer.

With indirect addressing, the first executed data read from the address set in SAR3 always results in a longword size transfer regardless of the TS0 and TS1 bit designations for transfer data size. However, the transfer source address fixed and increment or decrement designations are according to the SM0 and SM1 bits. Consequently, despite the fact that the transfer data size designation is byte in this example, the SAR3 value at the end of one transfer is H'00400004. The write operation is exactly the same as an ordinary dual address transfer write operation.

## 9.5 Usage Notes

1. Only word (16-bit) access can be used on the DMA operation register (DMAOR). All other registers can be accessed in word (16-bit) or longword (32-bit) units.
2. When rewriting the RS0 to RS4 bits of CHCR0 to CHCR3, first clear the DE bit to 0 (clear the DE bit to 0 before modifying CHCR).
3. When an NMI interrupt is input, the NMIF bit of DMAOR is set even when the DMAC is not operating.
4. Clear the DME bit of DMAOR to 0 and make certain that any transfer request processing accepted by the DMAC has been completed before entering standby mode.
5. Do not access the DMAC, BSC, or UBC on-chip peripheral modules from the DMAC.
6. When activating the DMAC, make the CHCR settings as the final step. Abnormal operation may result if any other registers are set last.
7. After the DMATCR count becomes 0 and the DMA transfer ends normally, always write 0 to DMATCR, even when executing the maximum number of transfers on the same channel. Abnormal operation may result if this is not done.
8. Designate burst mode as the transfer mode when using the address reload function. Abnormal operation may result in cycle-steal mode.
9. Designate a multiple of four for the DMATCR value when using the address reload function, otherwise abnormal operation may result.
10. Do not access empty DMAC register addresses. Operation cannot be guaranteed when empty addresses are accessed.
11. If DMAC transfer is aborted by NMIF or AE setting, or DME or DE clearing, during DMAC execution with address reload on, the SAR2, DAR2, and DMATCR2 settings should be made before re-executing the transfer. The DMAC may not operate correctly if this is not done.
12. Do not set the DE bit to 1 while bits RS0 to RS4 in CHCR0 to CHCR3 are still set to “no request.”

# Section 10 Advanced Timer Unit-II (ATU-II)

## 10.1 Overview

The SH7052F/SH7053F/SH7054F has an on-chip advanced timer unit-II (ATU-II) with one 32-bit timer channel and eleven 16-bit timer channels.

### 10.1.1 Features

ATU-II features are summarized below.

- Capability to process up to 63 pulse inputs and outputs
- Prescaler
  - Input clock to channels 0 and 10 scaled in 1 stage, input clock to channels 1 to 8 and 11 scaled in 2 stages
  - 1/1 to 1/32 clock scaling possible in initial stage for all channels
  - 1/1, 1/2, 1/4, 1/8, 1/16, or 1/32 scaling possible in second stage for channels 1 to 8 and 11
  - External clock TCLKA, TCLKB selection also possible for channels 1 to 5 and 11
- Channel 0 has four 32-bit input capture lines, allowing the following operations:
  - Rising-edge, falling-edge, or both-edge detection selectable
  - DMAC can be activated at capture timing
  - Channel 10 compare-match signal can be captured as a trigger
  - Interval interrupt generation function generates three interval interrupts as selected. CPU interruption or A/D converter (AD0, 1) activation possible
  - Capture interrupt and counter overflow interrupt can be generated
- Channel 1 has one 16-bit output compare register, eight general registers, and one dedicated input capture register. The output compare register can also be selected for one-shot pulse offset in combination with the channel 8 down-counter.
  - General registers (GR1A to H) can be used as input capture or output compare registers
  - Waveform output by means of compare-match: Selection of 0 output, 1 output, or toggle output
  - Input capture function: Rising-edge, falling-edge, or both-edge detection
  - Channel 0 input signal (TI0A) can be captured as trigger
  - Provision for forcible cutoff of channel 8 down-counters (DCNT8A to H)
  - Compare-match interrupts/capture interrupts and counter overflow interrupts can be generated

- Channel 2 has eight 16-bit output compare registers, eight general registers, and one dedicated input capture register. The output compare registers can also be selected for one-shot pulse offset in combination with the channel 8 down-counter.
  - General registers (GR2A to H) can be used as input capture or output compare registers
  - Waveform output by means of compare-match: Selection of 0 output, 1 output, or toggle output
  - Input capture function: Rising-edge, falling-edge, or both-edge detection
  - Channel 0 input signal (TIOA) can be captured as trigger
  - Provision for forcible cutoff of channel 8 down-counters (DCNT8A to H)
  - Compare-match interrupts/capture interrupts and counter overflow interrupts can be generated
- Channels 3 to 5 each have four general registers, allowing the following operations:
  - Selection of input capture, output compare, PWM mode
  - Waveform output by means of compare-match: Selection of 0 output, 1 output, or toggle output
  - Input capture function: Rising-edge, falling-edge, or both-edge detection
  - Channel 9 compare-match signal can be captured as trigger (channel 3 only)
  - Compare-match interrupts/capture interrupts can be generated
- Channels 6 and 7 have four 16-bit duty registers, four cycle registers, and four buffer registers, allowing the following operations:
  - Any cycle and duty from 0 to 100% can be set
  - Duty buffer register value transferred to duty register every cycle
  - Interrupts can be generated every cycle
  - Complementary PWM output can be set (channel 6 only)
- Channel 8 has sixteen 16-bit down-counters for one-shot pulse output, allowing the following operations:
  - One-shot pulse generation by down-counter
  - Down-counter can be rewritten during count
  - Interrupt can be generated at end of down-count
  - Offset one-shot pulse function available
  - Can be linked to channel 1 and 2 output compare functions
- Channel 9 has six event counters and six output compare registers, allowing the following operations:
  - Event counters can be cleared by compare-match
  - Rising-edge, falling-edge, or both-edge detection available for external input
  - Compare-match signal can be input to channel 3



- Channel 10 has a 32-bit output compare and input capture register, free-running counter, 16-bit free-running counter, output compare/input capture register, reload register, 8-bit event counter, and output compare register, and four 16-bit reload counters, allowing the following operations:
  - Capture on external input pin edge input
  - Reload count possible with 32, 64, 128, or 256 times the captured value
  - Internal clock generated by reload counter underflow can be used as 16-bit free-running counter input
  - Channel 1 and 2 free-running counter clearing capability
- Channel 11 has one 16-bit free-running counter and two 16-bit general registers, allowing the following operations:
  - Two general registers can be used for compare-match
  - Compare-match signal can be output to APC
- High-speed access to internal 16-bit bus
  - High-speed access to 16-bit bus for 16-bit registers: timer counters, compare registers, and capture registers
- 75 interrupt sources
  - Four input capture interrupt requests, one overflow interrupt request, and one interval interrupt request for channel 0
  - Sixteen dual input capture/compare-match interrupt requests and two counter overflow interrupt requests for channels 1 and 2
  - Twelve dual input capture/compare-match interrupt requests and three overflow interrupt requests for channels 3 to 5
  - Eight compare-match interrupts for channels 6 and 7
  - Sixteen one-shot end interrupt requests for channel 8
  - Six compare-match interrupts for channel 9
  - Two compare-match interrupts and one dual-function input capture/compare-match interrupt for channel 10
  - Two dual input capture/compare-match interrupt requests and one overflow interrupt request for channel 11
- Direct memory access controller (DMAC) activation
  - The DMAC can be activated by a channel 0 input capture interrupt (ICI0A to D)
  - The DMAC can be activated by a channel 6 cycle register 6 compare-match interrupt (CMI6A to D)
  - The DMAC can be activated by a channel 7 cycle register 7 compare-match interrupt (CMI7A to D)
- A/D converter activation
  - The A/D converter can be activated by detection of 1 in bits ITVA6 to 13 of the channel 0 interval interrupt request registers (ITVRR1, ITVRR2A, ITVRR2B)

**Table 10.1 ATU-II Functions**

Item	Channel 0	Channel 1	Channel 2	Channels 3 to 5	
Counter configuration	Clock sources	$\phi$ to $\phi/32$	$(\phi \text{ to } \phi/32) \times (1/2n)$ (n = 0 to 5) TCLKA, TCLKB	$(\phi \text{ to } \phi/32) \times (1/2n)$ (n = 0 to 5) TCLKA, TCLKB TCLKA, TCLKB	$(\phi \text{ to } \phi/32) \times (1/2n)$ (n = 0 to 5) TCLKA, TCLKB
	Counters	TCNT0H, TCNT0L	TCNT1A, TCNT1B	TCNT2A, TCNT2B	TCNT3 to 5
	General registers	—	GR1A to H	GR2A to H	GR3A to D, GR4A to D, GR5A to D
	Dedicated input capture	ICR0AH, ICR0AL, ICR0BH, ICR0BL, ICR0CH, ICR0CL, ICR0DH, ICR0DL	OSBR1	OSBR2	—
	Dedicated output compare	—	OCR1	OCR2A to 2H	—
	PWM output	—	—	—	Duty: GR3A to C, GR4A to C, GR5A to C Cycle: GR3D, GR4D, GR5D
Input pins	TIOA to D	—	—	—	
I/O pins	—	TIO1A to H	TIO2A to H	TIO3A to D, TIO4A to D, TIO5A to D	
Output pins	—	—	—	—	
Counter clearing function	—	—	—	O	
Interrupt sources	6 sources	9 sources	9 sources	15 sources	
	Interval $\times$ 1, input capture $\times$ 4, overflow $\times$ 1	Dual input capture/ compare-match $\times$ 8, overflow $\times$ 1	Dual input capture/ compare-match $\times$ 8, overflow $\times$ 1* (* Same vector)	Dual input capture/ compare-match $\times$ 12, overflow $\times$ 3	
Inter-channel and inter-module connection signals	A/D converter activation by interval interrupt request, DMAC activation by input capture interrupt, channel 10 compare-match signal capture trigger input	Compare-match signal trigger output to channel 8 one-shot pulse output down-counter Channel 10 compare-match signal counter clear input	Compare-match signal trigger output to channel 8 one-shot pulse output down-counter Channel 10 compare-match signal counter clear input	Channel 9 compare-match signal input to capture trigger (Channel 3 only)	

**Table 10.1 ATU-II Functions (cont)**

Item	Channels 6, 7	Channel 8	Channel 9	Channel 10	Channel 11	
Counter configuration	Clock sources	$(\phi \text{ to } \phi/32) \times (1/2n)$ (n = 0 to 5)	$(\phi \text{ to } \phi/32) \times (1/2n)$ (n = 0 to 5)	—	$(\phi \text{ to } \phi/32)$	$(\phi \text{ to } \phi/32) \times (1/2n)$ (n = 0 to 5) TCLKA, TCLKB
	Counters	TCNT6A to D, TCNT7A to D	DCNT8A to P	ECNT9A to F	TCNT10AH, TCNT10AL, TCNT10B to H	TCNT11
	General registers	—	—	—	—	GR11A, GR11B
	Dedicated input capture	—	—	—	ICR10AH, ICR10AL	—
	Dedicated output compare	—	—	GR9A to F	GR10G	—
	PWM output	CYLR6A to D, CYLR7A to D, DTR6A to D, DTR7A to D, BFR6A to D, BFR7A to D	—	—	—	—
Input pins	—	—	TI9A to F	TI10	—	
I/O pins	—	—	—	—	—	
Output pins	TO6A to D, TO7A to D	TO8A to P	—	—	—	
Counter clearing function	O	—	O	O	—	
Interrupt sources	8 sources	16 sources	6 sources	3 sources	3 sources	
	Compare-match $\times 8$	Underflow $\times 16$	Compare-match $\times 6$	Compare-match $\times 2$ , dual input capture/compare-match $\times 1$	Compare-match $\times 2$ , overflow $\times 1$	
Inter-channel and inter-module connection signals	DMAC activation compare-match signal output	Channel 1 and 2 compare-match signal trigger input to one-shot pulse output down-counter	Compare-match channel 3 capture trigger output	Compare-match signal channel 0 capture trigger output  Channel 1 and 2 counter clear output	Compare-match signal output to APC	

O: Available

—: Not available

## 10.1.2 Pin Configuration

Table 10.2 shows the pin configuration of the ATU-II. When these external pin functions are used, the pin function controller (PFC) should also be set in accordance with the ATU-II settings. If there are a number of pins with the same function, make settings so that only one of the pins is used. For details, see section 18, Pin Function Controller.

**Table 10.2 ATU-II Pins**

Channel	Name	Abbreviation	I/O	Function
Common	Clock input A	TCLKA	Input	External clock A input pin
	Clock input B	TCLKB	Input	External clock B input pin
0	Input capture 0A	TIO0A	Input	ICR0AH, ICR0AL input capture input pin
	Input capture 0B	TIO0B	Input	ICR0BH, ICR0BL input capture input pin
	Input capture 0C	TIO0C	Input	ICR0CH, ICR0CL input capture input pin
	Input capture 0D	TIO0D	Input	ICR0DH, ICR0DL input capture input pin
1	Input capture/output compare 1A	TIO1A	Input/output	GR1A output compare output/input capture input
	Input capture/output compare 1B	TIO1B	Input/output	GR1B output compare output/input capture input
	Input capture/output compare 1C	TIO1C	Input/output	GR1C output compare output/input capture input
	Input capture/output compare 1D	TIO1D	Input/output	GR1D output compare output/input capture input
	Input capture/output compare 1E	TIO1E	Input/output	GR1E output compare output/input capture input
	Input capture/output compare 1F	TIO1F	Input/output	GR1F output compare output/input capture input
	Input capture/output compare 1G	TIO1G	Input/output	GR1G output compare output/input capture input
	Input capture/output compare 1H	TIO1H	Input/output	GR1H output compare output/input capture input

**Table 10.2 ATU-II Pins (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbreviation</b>	<b>I/O</b>	<b>Function</b>
2	Input capture/output compare 2A	TIO2A	Input/output	GR2A output compare output/input capture input
	Input capture/output compare 2B	TIO2B	Input/output	GR2B output compare output/input capture input
	Input capture/output compare 2C	TIO2C	Input/output	GR2C output compare output/input capture input
	Input capture/output compare 2D	TIO2D	Input/output	GR2D output compare output/input capture input
	Input capture/output compare 2E	TIO2E	Input/output	GR2E output compare output/input capture input
	Input capture/output compare 2F	TIO2F	Input/output	GR2F output compare output/input capture input
	Input capture/output compare 2G	TIO2G	Input/output	GR2G output compare output/input capture input
	Input capture/output compare 2H	TIO2H	Input/output	GR2H output compare output/input capture input
3	Input capture/output compare 3A	TIO3A	Input/output	GR3A output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 3B	TIO3B	Input/output	GR3B output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 3C	TIO3C	Input/output	GR3C output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 3D	TIO3D	Input/output	GR3D output compare output/input capture input
4	Input capture/output compare 4A	TIO4A	Input/output	GR4A output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 4B	TIO4B	Input/output	GR4B output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 4C	TIO4C	Input/output	GR4C output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 4D	TIO4D	Input/output	GR4D output compare output/input capture input

**Table 10.2 ATU-II Pins (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbreviation</b>	<b>I/O</b>	<b>Function</b>
5	Input capture/output compare 5A	TIO5A	Input/output	GR5A output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 5B	TIO5B	Input/output	GR5B output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 5C	TIO5C	Input/output	GR5C output compare output/input capture input/PWM output pin (PWM mode)
	Input capture/output compare 5D	TIO5D	Input/output	GR5D output compare output/input capture input
6	Output compare 6A	TO6A	Output	PWM output pin
	Output compare 6B	TO6B	Output	PWM output pin
	Output compare 6C	TO6C	Output	PWM output pin
	Output compare 6D	TO6D	Output	PWM output pin
7	Output compare 7A	TO7A	Output	PWM output pin
	Output compare 7B	TO7B	Output	PWM output pin
	Output compare 7C	TO7C	Output	PWM output pin
	Output compare 7D	TO7D	Output	PWM output pin
8	One-shot pulse 8A	TO8A	Output	One-shot pulse output pin
	One-shot pulse 8B	TO8B	Output	One-shot pulse output pin
	One-shot pulse 8C	TO8C	Output	One-shot pulse output pin
	One-shot pulse 8D	TO8D	Output	One-shot pulse output pin
	One-shot pulse 8E	TO8E	Output	One-shot pulse output pin
	One-shot pulse 8F	TO8F	Output	One-shot pulse output pin
	One-shot pulse 8G	TO8G	Output	One-shot pulse output pin
	One-shot pulse 8H	TO8H	Output	One-shot pulse output pin
	One-shot pulse 8I	TO8I	Output	One-shot pulse output pin
	One-shot pulse 8J	TO8J	Output	One-shot pulse output pin
	One-shot pulse 8K	TO8K	Output	One-shot pulse output pin
	One-shot pulse 8L	TO8L	Output	One-shot pulse output pin
	One-shot pulse 8M	TO8M	Output	One-shot pulse output pin
	One-shot pulse 8N	TO8N	Output	One-shot pulse output pin

**Table 10.2 ATU-II Pins (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbreviation</b>	<b>I/O</b>	<b>Function</b>
8	One-shot pulse 8O	TO8O	Output	One-shot pulse output pin
	One-shot pulse 8P	TO8P	Output	One-shot pulse output pin
9	Event input 9A	TI9A	Input	GR9A event input
	Event input 9B	TI9B	Input	GR9B event input
	Event input 9C	TI9C	Input	GR9C event input
	Event input 9D	TI9D	Input	GR9D event input
	Event input 9E	TI9E	Input	GR9E event input
	Event input 9F	TI9F	Input	GR9F event input
10	Input capture	TI10	Input	ICR10AH, ICR10AL input capture input

### 10.1.3 Register Configuration

Table 10.3 summarizes the ATU-II registers.

**Table 10.3 ATU-II Registers**

Channel	Name	Abbrevia- tion	R/W	Initial Value	Address	Access Size (Bits)
Common	Timer start register 1	TSTR1	R/W	H'00	H'FFFFFF401	8, 16, 32
	Timer start register 2	TSTR2	R/W	H'00	H'FFFFFF400	
	Timer start register 3	TSTR3	R/W	H'00	H'FFFFFF402	
	Prescaler register 1	PSCR1	W	H'00	H'FFFFFF404	8
	Prescaler register 2	PSCR2	W	H'00	H'FFFFFF406	
	Prescaler register 3	PSCR3	W	H'00	H'FFFFFF408	
	Prescaler register 4	PSCR4	W	H'00	H'FFFFFF40A	
0	Free-running counter 0H	TCNT0H	R/W	H'0000	H'FFFFFF430	32
	Free-running counter 0L	TCNT0L	R/W	H'0000		
	Input capture register 0AH	ICR0AH	R	H'0000	H'FFFFFF434	
	Input capture register 0AL	ICR0AL	R	H'0000		
	Input capture register 0BH	ICR0BH	R	H'0000	H'FFFFFF438	
	Input capture register 0BL	ICR0BL	R	H'0000		
	Input capture register 0CH	ICR0CH	R	H'0000	H'FFFFFF43C	
	Input capture register 0CL	ICR0CL	R	H'0000		
	Input capture register 0DH	ICR0DH	R	H'0000	H'FFFFFF420	
	Input capture register 0DL	ICR0DL	R	H'0000		
	Timer interval interrupt request register 1	ITVRR1	R/W	H'00	H'FFFFFF424	8
	Timer interval interrupt request register 2A	ITVRR2A	R/W	H'00		



**Table 10.3 ATU-II Registers (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbrevia- tion</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size (Bits)</b>
0	Timer interval interrupt request register 2B	ITVRR2B	R/W	H'00	H'FFFFFF428	8
	Timer I/O control register	TIOR0	R/W	H'00	H'FFFFFF42A	
	Timer status register 0	TSR0	R/(W)*	H'0000	H'FFFFFF42C	16
	Timer interrupt enable register 0	TIER0	R/W	H'0000	H'FFFFFF42E	
1	Free-running counter 1A	TCNT1A	R/W	H'0000	H'FFFFFF440	16
	Free-running counter 1B	TCNT1B	R/W	H'0000	H'FFFFFF442	
	General register 1A	GR1A	R/W	H'FFFF	H'FFFFFF444	
	General register 1B	GR1B	R/W	H'FFFF	H'FFFFFF446	
	General register 1C	GR1C	R/W	H'FFFF	H'FFFFFF448	
	General register 1D	GR1D	R/W	H'FFFF	H'FFFFFF44A	
	General register 1E	GR1E	R/W	H'FFFF	H'FFFFFF44C	
	General register 1F	GR1F	R/W	H'FFFF	H'FFFFFF44E	
	General register 1G	GR1G	R/W	H'FFFF	H'FFFFFF450	
	General register 1H	GR1H	R/W	H'FFFF	H'FFFFFF452	
	Output compare register 1	OCR1	R/W	H'FFFF	H'FFFFFF454	
	Offset base register 1	OSBR1	R	H'0000	H'FFFFFF456	
	Timer I/O control register 1A	TIOR1A	R/W	H'00	H'FFFFFF459	8, 16
	Timer I/O control register 1B	TIOR1B	R/W	H'00	H'FFFFFF458	
	Timer I/O control register 1C	TIOR1C	R/W	H'00	H'FFFFFF45B	
	Timer I/O control register 1D	TIOR1D	R/W	H'00	H'FFFFFF45A	
	Timer control register 1A	TCR1A	R/W	H'00	H'FFFFFF45D	
Timer control register 1B	TCR1B	R/W	H'00	H'FFFFFF45C		

**Table 10.3 ATU-II Registers (cont)**

Channel	Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
1	Timer status register 1A	TSR1A	R/(W)*	H'0000	H'FFFFFF45E	16
	Timer status register 1B	TSR1B	R/(W)*	H'0000	H'FFFFFF460	
	Timer interrupt enable register 1A	TIER1A	R/W	H'0000	H'FFFFFF462	
	Timer interrupt enable register 1B	TIER1B	R/W	H'0000	H'FFFFFF464	
	Trigger mode register	TRGMDR	R/W	H'00	H'FFFFFF466	8
2	Free-running counter 2A	TCNT2A	R/W	H'0000	H'FFFFFF600	16
	Free-running counter 2B	TCNT2B	R/W	H'0000	H'FFFFFF602	
	General register 2A	GR2A	R/W	H'FFFF	H'FFFFFF604	
	General register 2B	GR2B	R/W	H'FFFF	H'FFFFFF606	
	General register 2C	GR2C	R/W	H'FFFF	H'FFFFFF608	
	General register 2D	GR2D	R/W	H'FFFF	H'FFFFFF60A	
	General register 2E	GR2E	R/W	H'FFFF	H'FFFFFF60C	
	General register 2F	GR2F	R/W	H'FFFF	H'FFFFFF60E	
	General register 2G	GR2G	R/W	H'FFFF	H'FFFFFF610	
	General register 2H	GR2H	R/W	H'FFFF	H'FFFFFF612	
	Output compare register 2A	OCR2A	R/W	H'FFFF	H'FFFFFF614	
	Output compare register 2B	OCR2B	R/W	H'FFFF	H'FFFFFF616	
	Output compare register 2C	OCR2C	R/W	H'FFFF	H'FFFFFF618	
	Output compare register 2D	OCR2D	R/W	H'FFFF	H'FFFFFF61A	
	Output compare register 2E	OCR2E	R/W	H'FFFF	H'FFFFFF61C	
Output compare register 2F	OCR2F	R/W	H'FFFF	H'FFFFFF61E		

**Table 10.3 ATU-II Registers (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbrevia- tion</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size (Bits)</b>
2	Output compare register 2G	OCR2G	R/W	H'FFFF	H'FFFFFF620	16
	Output compare register 2H	OCR2H	R/W	H'FFFF	H'FFFFFF622	
	Offset base register 2	OSBR2	R	H'0000	H'FFFFFF624	
	Timer I/O control register 2A	TIOR2A	R/W	H'00	H'FFFFFF627	8, 16
	Timer I/O control register 2B	TIOR2B	R/W	H'00	H'FFFFFF626	
	Timer I/O control register 2C	TIOR2C	R/W	H'00	H'FFFFFF629	
	Timer I/O control register 2D	TIOR2D	R/W	H'00	H'FFFFFF628	
	Timer control register 2A	TCR2A	R/W	H'00	H'FFFFFF62B	
	Timer control register 2B	TCR2B	R/W	H'00	H'FFFFFF62A	
	Timer status register 2A	TSR2A	R/(W)*	H'0000	H'FFFFFF62C	16
	Timer status register 2B	TSR2B	R/(W)*	H'0000	H'FFFFFF62E	
	Timer interrupt enable register 2A	TIER2A	R/W	H'0000	H'FFFFFF630	
Timer interrupt enable register 2B	TIER2B	R/W	H'0000	H'FFFFFF632		
3 to 5	Timer status register 3	TSR3	R/(W)*	H'0000	H'FFFFFF480	16
	Timer interrupt enable register 3	TIER3	R/W	H'0000	H'FFFFFF482	
	Timer mode register	TMDR	R/W	H'00	H'FFFFFF484	8
3	Free-running counter 3	TCNT3	R/W	H'0000	H'FFFFFF4A0	16
	General register 3A	GR3A	R/W	H'FFFF	H'FFFFFF4A2	
	General register 3B	GR3B	R/W	H'FFFF	H'FFFFFF4A4	
	General register 3C	GR3C	R/W	H'FFFF	H'FFFFFF4A6	
	General register 3D	GR3D	R/W	H'FFFF	H'FFFFFF4A8	

**Table 10.3 ATU-II Registers (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbrevia- tion</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size (Bits)</b>
3	Timer I/O control register 3A	TIOR3A	R/W	H'00	H'FFFFFF4AB	8, 16
	Timer I/O control register 3B	TIOR3B	R/W	H'00	H'FFFFFF4AA	
	Timer control register 3	TCR3	R/W	H'00	H'FFFFFF4AC	8
4	Free-running counter 4	TCNT4	R/W	H'0000	H'FFFFFF4C0	16
	General register 4A	GR4A	R/W	H'FFFF	H'FFFFFF4C2	
	General register 4B	GR4B	R/W	H'FFFF	H'FFFFFF4C4	
	General register 4C	GR4C	R/W	H'FFFF	H'FFFFFF4C6	
	General register 4D	GR4D	R/W	H'FFFF	H'FFFFFF4C8	
	Timer I/O control register 4A	TIOR4A	R/W	H'00	H'FFFFFF4CB	8, 16
	Timer I/O control register 4B	TIOR4B	R/W	H'00	H'FFFFFF4CA	
	Timer control register 4	TCR4	R/W	H'00	H'FFFFFF4CC	8
5	Free-running counter 5	TCNT5	R/W	H'0000	H'FFFFFF4E0	16
	General register 5A	GR5A	R/W	H'FFFF	H'FFFFFF4E2	
	General register 5B	GR5B	R/W	H'FFFF	H'FFFFFF4E4	
	General register 5C	GR5C	R/W	H'FFFF	H'FFFFFF4E6	
	General register 5D	GR5D	R/W	H'FFFF	H'FFFFFF4E8	
	Timer I/O control register 5A	TIOR5A	R/W	H'00	H'FFFFFF4EB	8, 16
	Timer I/O control register 5B	TIOR5B	R/W	H'00	H'FFFFFF4EA	
	Timer control register 5	TCR5	R/W	H'00	H'FFFFFF4EC	8
6	Free-running counter 6A	TCNT6A	R/W	H'0001	H'FFFFFF500	16
	Free-running counter 6B	TCNT6B	R/W	H'0001	H'FFFFFF502	
	Free-running counter 6C	TCNT6C	R/W	H'0001	H'FFFFFF504	
	Free-running counter 6D	TCNT6D	R/W	H'0001	H'FFFFFF506	

**Table 10.3 ATU-II Registers (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbreviation</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size (Bits)</b>
6	Cycle register 6A	CYLR6A	R/W	H'FFFF	H'FFFFFF508	16
	Cycle register 6B	CYLR6B	R/W	H'FFFF	H'FFFFFF50A	
	Cycle register 6C	CYLR6C	R/W	H'FFFF	H'FFFFFF50C	
	Cycle register 6D	CYLR6D	R/W	H'FFFF	H'FFFFFF50E	
	Buffer register 6A	BFR6A	R/W	H'FFFF	H'FFFFFF510	
	Buffer register 6B	BFR6B	R/W	H'FFFF	H'FFFFFF512	
	Buffer register 6C	BFR6C	R/W	H'FFFF	H'FFFFFF514	
	Buffer register 6D	BFR6D	R/W	H'FFFF	H'FFFFFF516	
	Duty register 6A	DTR6A	R/W	H'FFFF	H'FFFFFF518	
	Duty register 6B	DTR6B	R/W	H'FFFF	H'FFFFFF51A	
	Duty register 6C	DTR6C	R/W	H'FFFF	H'FFFFFF51C	
	Duty register 6D	DTR6D	R/W	H'FFFF	H'FFFFFF51E	
	Timer control register 6A	TCR6A	R/W	H'00	H'FFFFFF521	8, 16
	Timer control register 6B	TCR6B	R/W	H'00	H'FFFFFF520	
Timer status register 6	TSR6	R/(W)*	H'0000	H'FFFFFF522	16	
Timer interrupt enable register 6	TIER6	R/W	H'0000	H'FFFFFF524		
PWM mode register	PMDR	R/W	H'00	H'FFFFFF526	8	
7	Free-running counter 7A	TCNT7A	R/W	H'0001	H'FFFFFF580	16
	Free-running counter 7B	TCNT7B	R/W	H'0001	H'FFFFFF582	
	Free-running counter 7C	TCNT7C	R/W	H'0001	H'FFFFFF584	
	Free-running counter 7D	TCNT7D	R/W	H'0001	H'FFFFFF586	
	Cycle register 7A	CYLR7A	R/W	H'FFFF	H'FFFFFF588	
	Cycle register 7B	CYLR7B	R/W	H'FFFF	H'FFFFFF58A	
	Cycle register 7C	CYLR7C	R/W	H'FFFF	H'FFFFFF58C	
	Cycle register 7D	CYLR7D	R/W	H'FFFF	H'FFFFFF58E	

**Table 10.3 ATU-II Registers (cont)**

Channel	Name	Abbrevia- tion	R/W	Initial Value	Address	Access Size (Bits)
7	Buffer register 7A	BFR7A	R/W	H'FFFF	H'FFFFFF590	16
	Buffer register 7B	BFR7B	R/W	H'FFFF	H'FFFFFF592	
	Buffer register 7C	BFR7C	R/W	H'FFFF	H'FFFFFF594	
	Buffer register 7D	BFR7D	R/W	H'FFFF	H'FFFFFF596	
	Duty register 7A	DTR7A	R/W	H'FFFF	H'FFFFFF598	
	Duty register 7B	DTR7B	R/W	H'FFFF	H'FFFFFF59A	
	Duty register 7C	DTR7C	R/W	H'FFFF	H'FFFFFF59C	
	Duty register 7D	DTR7D	R/W	H'FFFF	H'FFFFFF59E	
	Timer control register 7A	TCR7A	R/W	H'00	H'FFFFFF5A1	8, 16
	Timer control register 7B	TCR7B	R/W	H'00	H'FFFFFF5A0	
	Timer status register 7	TSR7	R/(W)*	H'0000	H'FFFFFF5A2	16
	Timer interrupt enable register 7	TIER7	R/W	H'0000	H'FFFFFF5A4	
8	Down-counter 8A	DCNT8A	R/W	H'0000	H'FFFFFF640	16
	Down-counter 8B	DCNT8B	R/W	H'0000	H'FFFFFF642	
	Down-counter 8C	DCNT8C	R/W	H'0000	H'FFFFFF644	
	Down-counter 8D	DCNT8D	R/W	H'0000	H'FFFFFF646	
	Down-counter 8E	DCNT8E	R/W	H'0000	H'FFFFFF648	
	Down-counter 8F	DCNT8F	R/W	H'0000	H'FFFFFF64A	
	Down-counter 8G	DCNT8G	R/W	H'0000	H'FFFFFF64C	
	Down-counter 8H	DCNT8H	R/W	H'0000	H'FFFFFF64E	
	Down-counter 8I	DCNT8I	R/W	H'0000	H'FFFFFF650	
	Down-counter 8J	DCNT8J	R/W	H'0000	H'FFFFFF652	
	Down-counter 8K	DCNT8K	R/W	H'0000	H'FFFFFF654	
	Down-counter 8L	DCNT8L	R/W	H'0000	H'FFFFFF656	
	Down-counter 8M	DCNT8M	R/W	H'0000	H'FFFFFF658	
	Down-counter 8N	DCNT8N	R/W	H'0000	H'FFFFFF65A	
	Down-counter 8O	DCNT8O	R/W	H'0000	H'FFFFFF65C	
	Down-counter 8P	DCNT8P	R/W	H'0000	H'FFFFFF65E	

**Table 10.3 ATU-II Registers (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbrevia- tion</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size (Bits)</b>
8	Reload register 8	RLDR8	R/W	H'0000	H'FFFFFF660	16
	Timer connection register	TCNR	R/W	H'0000	H'FFFFFF662	
	One-shot pulse terminate register	OTR	R/W	H'0000	H'FFFFFF664	
	Down-count start register	DSTR	R/W	H'0000	H'FFFFFF666	
	Timer control register 8	TCR8	R/W	H'00	H'FFFFFF668	8
	Timer status register 8	TSR8	R/(W)*	H'0000	H'FFFFFF66A	16
	Timer interrupt enable register 8	TIER8	R/W	H'0000	H'FFFFFF66C	
	Reload enable register	RLDENR	R/W	H'00	H'FFFFFF66E	8
9	Event counter 9A	ECNT9A	R/W	H'00	H'FFFFFF680	8
	Event counter 9B	ECNT9B	R/W	H'00	H'FFFFFF682	
	Event counter 9C	ECNT9C	R/W	H'00	H'FFFFFF684	
	Event counter 9D	ECNT9D	R/W	H'00	H'FFFFFF686	
	Event counter 9E	ECNT9E	R/W	H'00	H'FFFFFF688	
	Event counter 9F	ECNT9F	R/W	H'00	H'FFFFFF68A	
	General register 9A	GR9A	R/W	H'FF	H'FFFFFF68C	
	General register 9B	GR9B	R/W	H'FF	H'FFFFFF68E	
	General register 9C	GR9C	R/W	H'FF	H'FFFFFF690	
	General register 9D	GR9D	R/W	H'FF	H'FFFFFF692	
	General register 9E	GR9E	R/W	H'FF	H'FFFFFF694	
	General register 9F	GR9F	R/W	H'FF	H'FFFFFF696	
	Timer control register 9A	TCR9A	R/W	H'00	H'FFFFFF698	
	Timer control register 9B	TCR9B	R/W	H'00	H'FFFFFF69A	
	Timer control register 9C	TCR9C	R/W	H'00	H'FFFFFF69C	
	Timer status register 9	TSR9	R/(W)*	H'0000	H'FFFFFF69E	16
	Timer interrupt enable register 9	TIER9	R/W	H'0000	H'FFFFFF6A0	

**Table 10.3 ATU-II Registers (cont)**

Channel	Name	Abbrevia- tion	R/W	Initial Value	Address	Access Size (Bits)
10	Free-running counter 10AH	TCNT10AH	R/W	H'0000	H'FFFFFF6C0	32
	Free-running counter 10AL	TCNT10AL	R/W	H'0001		
	Event counter 10B	TCNT10B	R/W	H'00	H'FFFFFF6C4	8
	Reload counter 10C	TCNT10C	R/W	H'0001	H'FFFFFF6C6	16
	Correction counter 10D	TCNT10D	R/W	H'00	H'FFFFFF6C8	8
	Correction angle counter 10E	TCNT10E	R/W	H'0000	H'FFFFFF6CA	16
	Correction angle counter 10F	TCNT10F	R/W	H'0001	H'FFFFFF6CC	
	Free-running counter 10G	TCNT10G	R/W	H'0000	H'FFFFFF6CE	
	Input capture register 10AH	ICR10AH	R	H'0000	H'FFFFFF6D0	32
	Input capture register 10AL	ICR10AL	R	H'0000		
	Output compare register 10AH	OCR10AH	R/W	H'FFFF	H'FFFFFF6D4	
	Output compare register 10AL	OCR10AL	R/W	H'FFFF		
	Output compare register 10B	OCR10B	R/W	H'FF	H'FFFFFF6D8	8
	Reload register 10C	RLD10C	R/W	H'0000	H'FFFFFF6DA	16
	General register 10G	GR10G	R/W	H'FFFF	H'FFFFFF6DC	
	Noise canceler counter 10H	TCNT10H	R/W	H'00	H'FFFFFF6DE	8
	Noise canceler register 10	NCR10	R/W	H'FF	H'FFFFFF6E0	
	Timer I/O control register 10	TIOR10	R/W	H'00	H'FFFFFF6E2	
	Timer control register 10	TCR10	R/W	H'00	H'FFFFFF6E4	



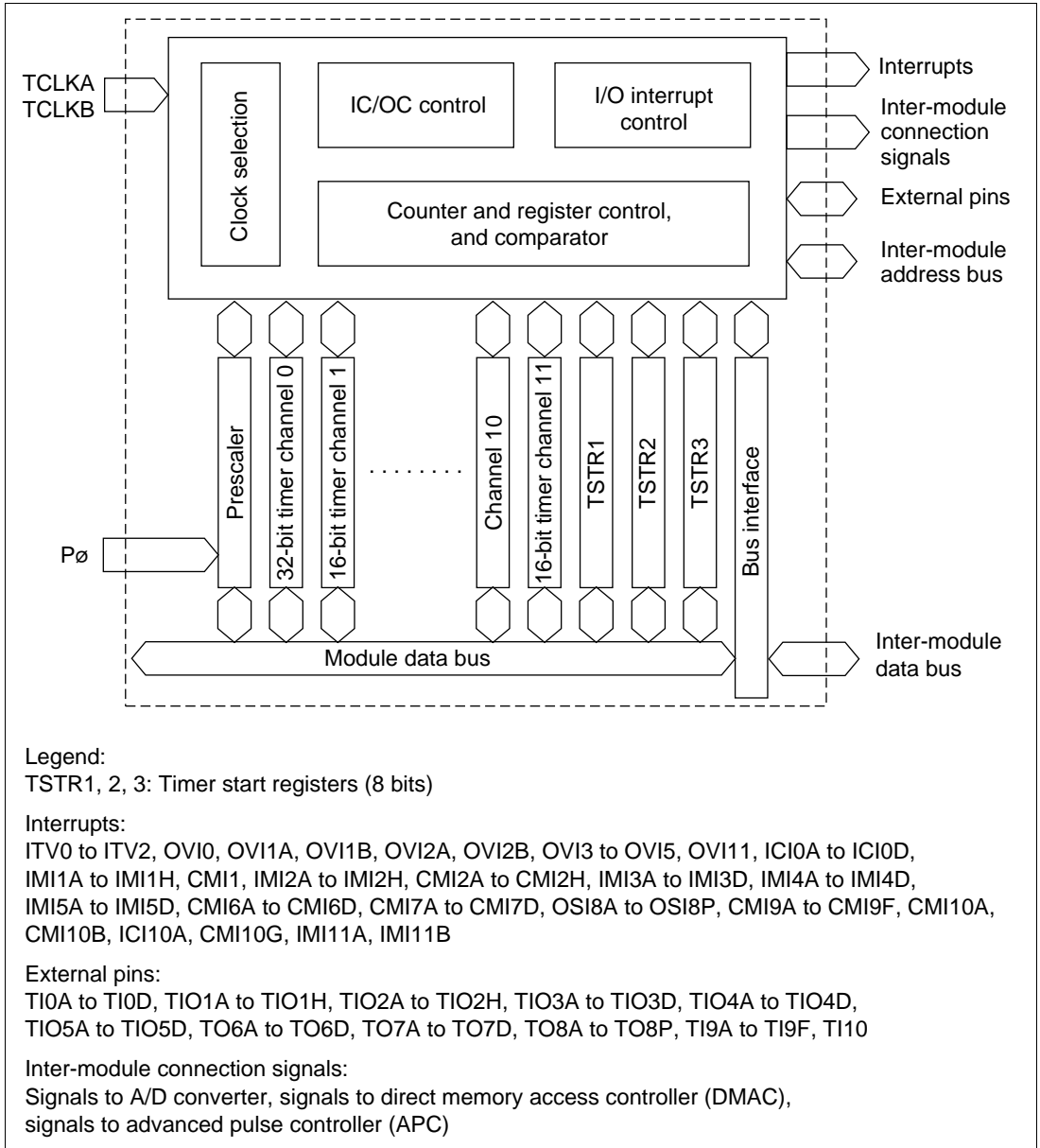
**Table 10.3 ATU-II Registers (cont)**

<b>Channel</b>	<b>Name</b>	<b>Abbrevia- tion</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size (Bits)</b>
10	Correction counter clear register 10	TCCLR10	R/W	H'0000	H'FFFFFF6E6	16
	Timer status register 10	TSR10	R/(W)*	H'FFFF	H'FFFFFF6E8	
	Timer interrupt enable register 10	TIER10	R/W	H'FFFF	H'FFFFFF6EA	
11	Free-running counter 11	TCNT11	R/W	H'0000	H'FFFFFF5C0	16
	General register 11A	GR11A	R/W	H'FFFF	H'FFFFFF5C2	
	General register 11B	GR11B	R/W	H'FFFF	H'FFFFFF5C4	
	Timer I/O control register 11	TIOR11	R/W	H'00	H'FFFFFF5C6	8
	Timer control register 11	TCR11	R/W	H'00	H'FFFFFF5C8	
	Timer status register 11	TSR11	R/(W)*	H'0000	H'FFFFFF5CA	16
	Timer interrupt enable register 11	TIER11	R/W	H'0000	H'FFFFFF5CC	

Note: \* 0 write after a read

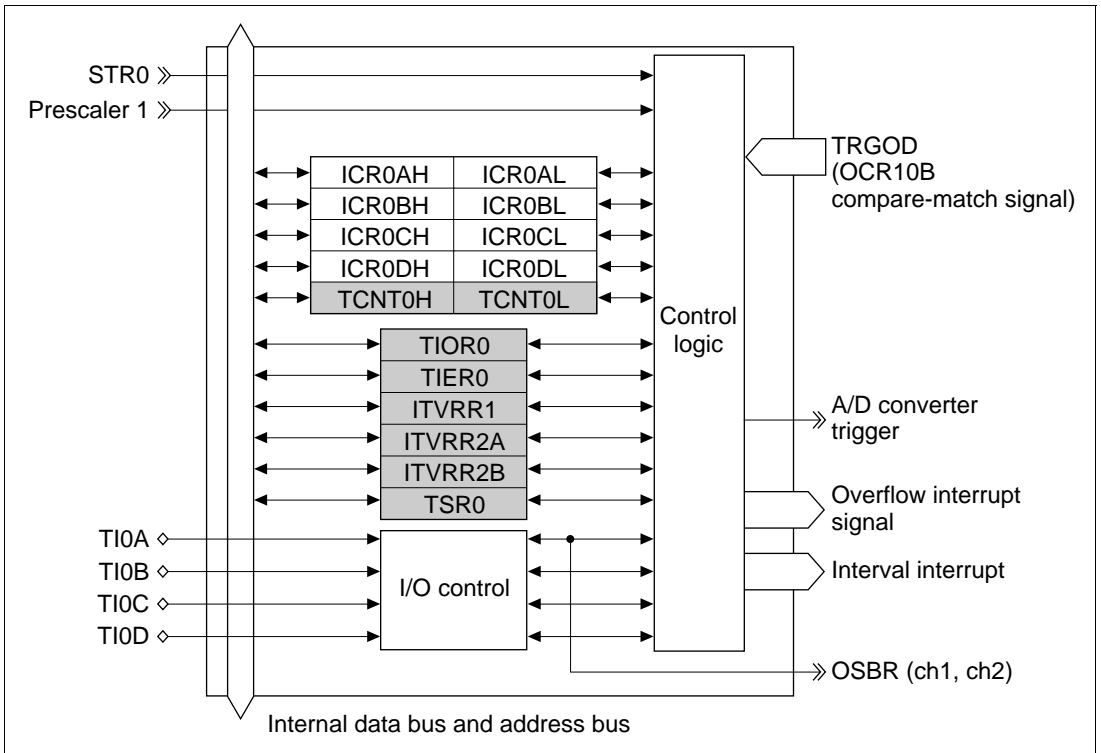
## 10.1.4 Block Diagrams

**Overall Block Diagram of ATU-II:** Figure 10.1 shows an overall block diagram of the ATU-II.



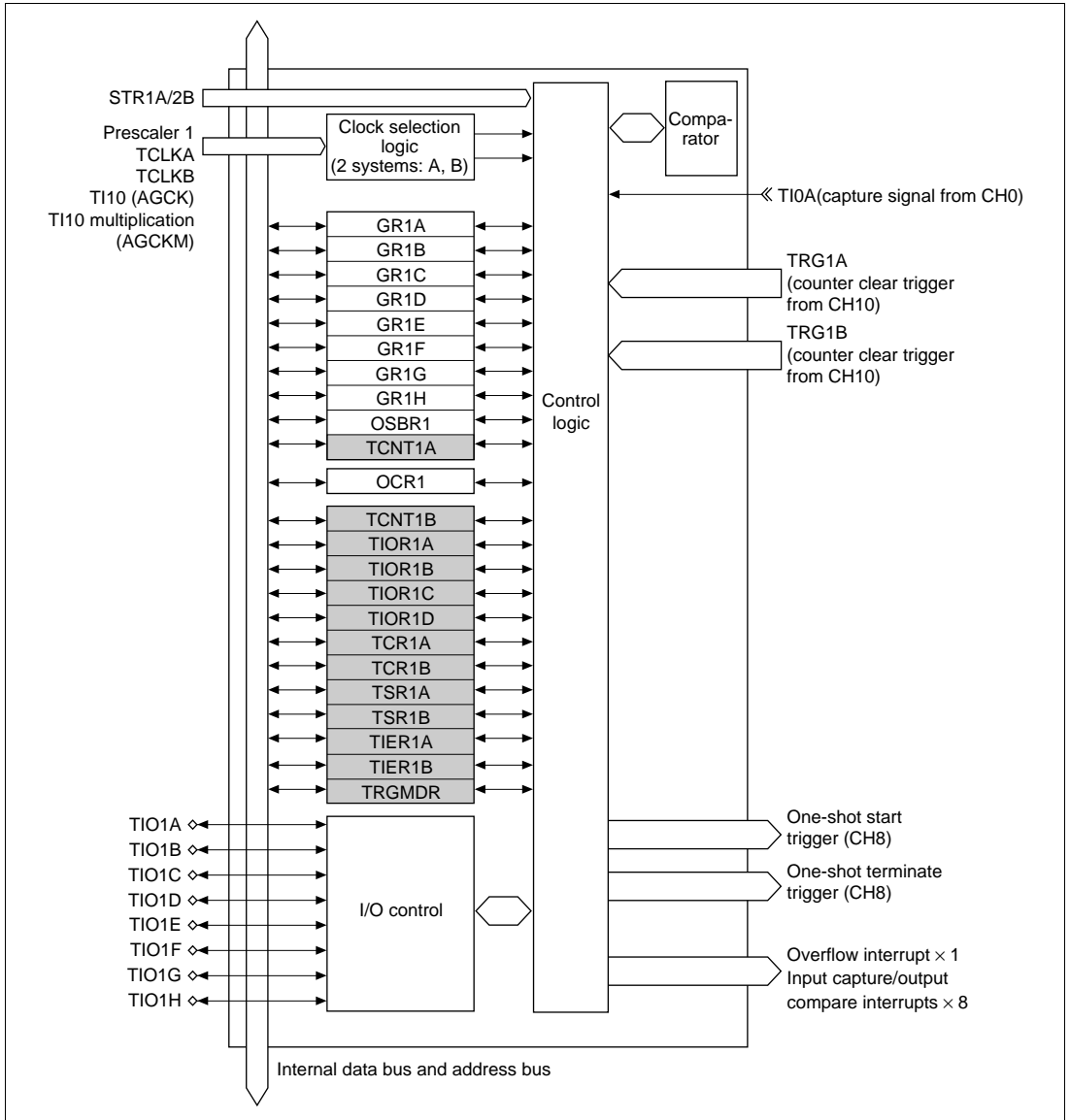
**Figure 10.1 Overall Block Diagram of ATU-II**

**Block Diagram of Channel 0:** Figure 10.2 shows a block diagram of ATU-II channel 0.



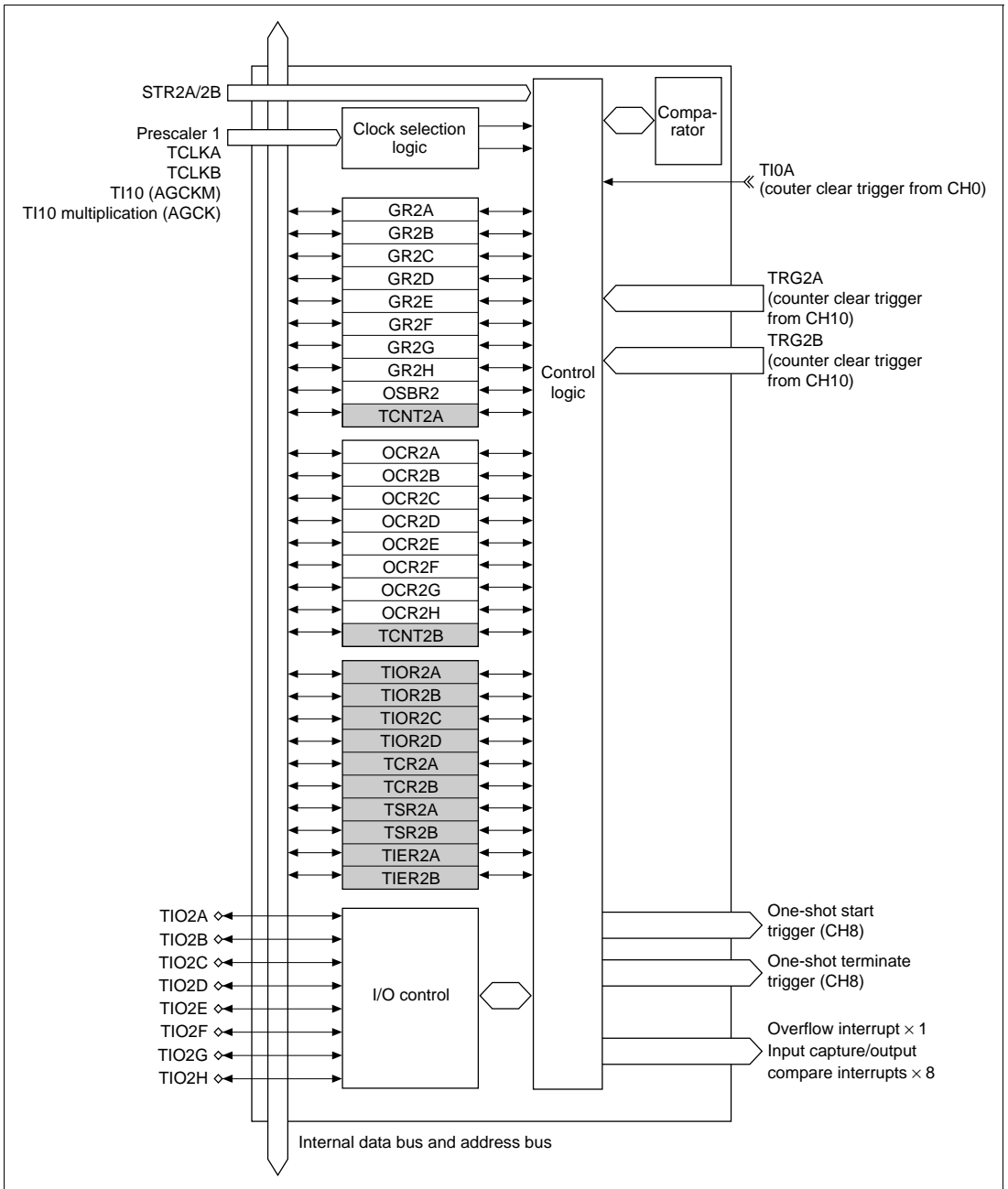
**Figure 10.2 Block Diagram of Channel 0**

**Block Diagram of Channel 1:** Figure 10.3 shows a block diagram of ATU-II channel 1.



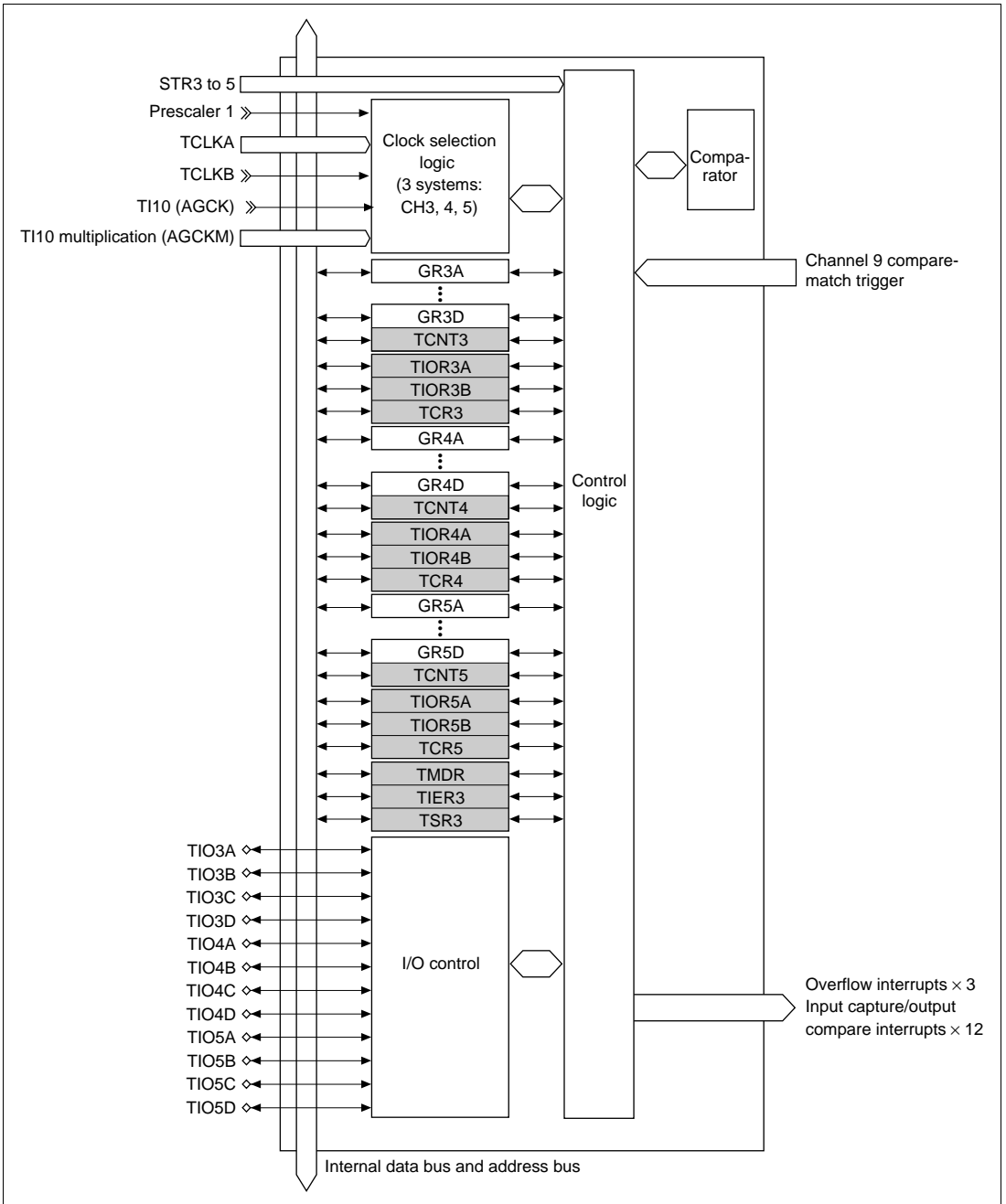
**Figure 10.3 Block Diagram of Channel 1**

**Block Diagram of Channel 2:** Figure 10.4 shows a block diagram of ATU-II channel 2.



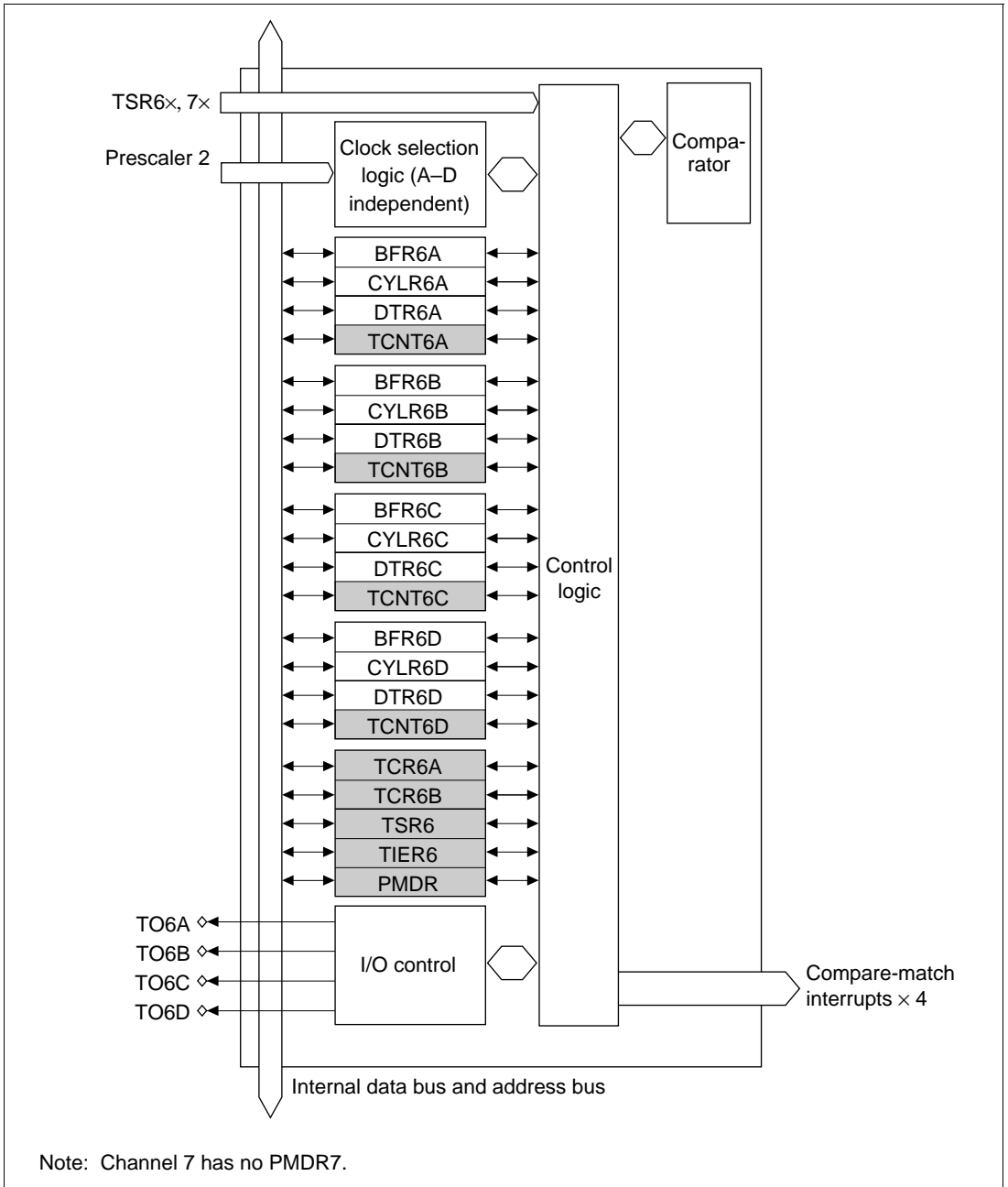
**Figure 10.4 Block Diagram of Channel 2**

**Block Diagram of Channels 3 to 5:** Figure 10.5 shows a block diagram of ATU-II channels 3, 4, and 5.



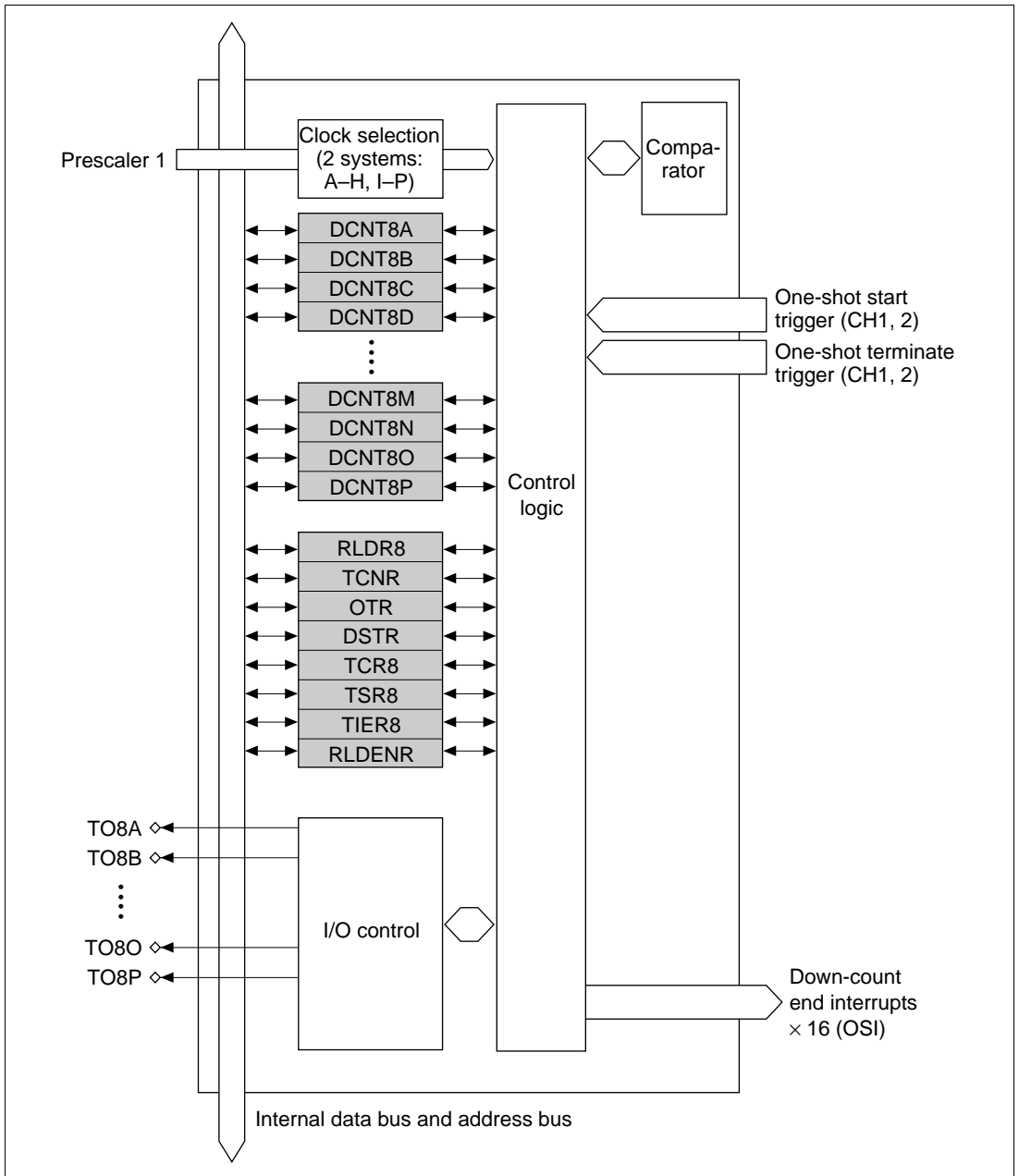
**Figure 10.5 Block Diagram of Channels 3 to 5**

**Block Diagram of Channels 6 and 7:** Figure 10.6 shows a block diagram of ATU-II channels 6 and 7.



**Figure 10.6 Block Diagram of Channel 6 (Same Configuration for Channel 7)**

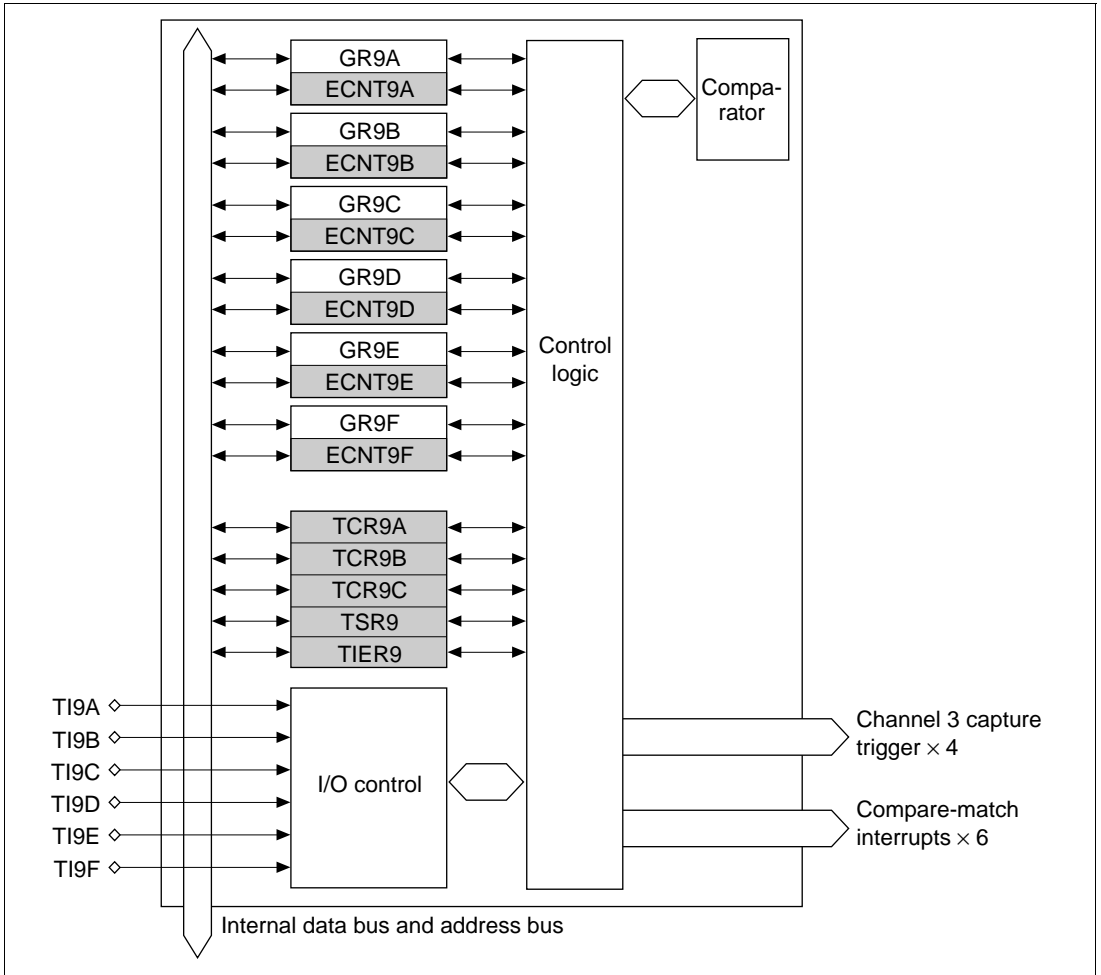
**Block Diagram of Channel 8:** Figure 10.7 shows a block diagram of ATU-II channel 8.



**Figure 10.7 Block Diagram of Channel 8**

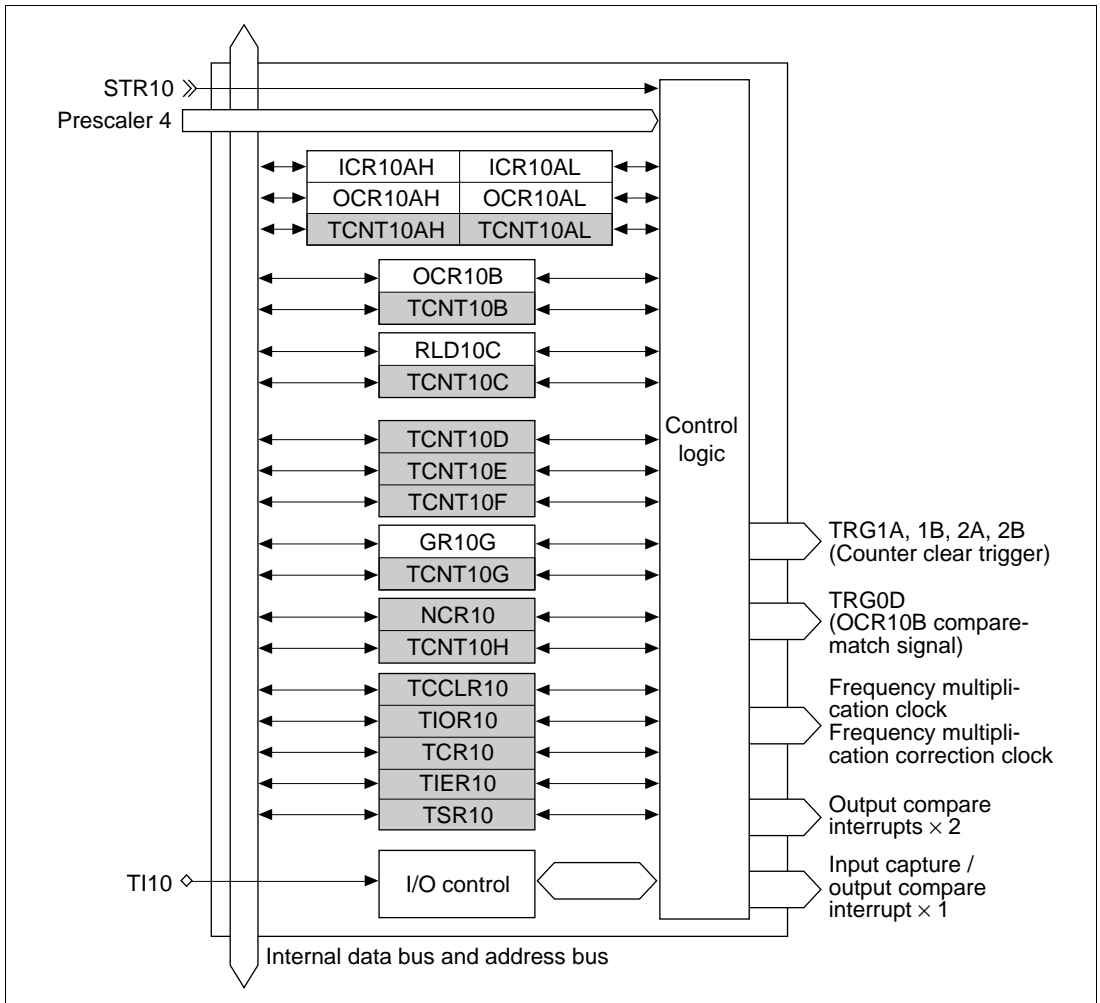


**Block Diagram of Channel 9:** Figure 10.8 shows a block diagram of ATU-II channel 9.



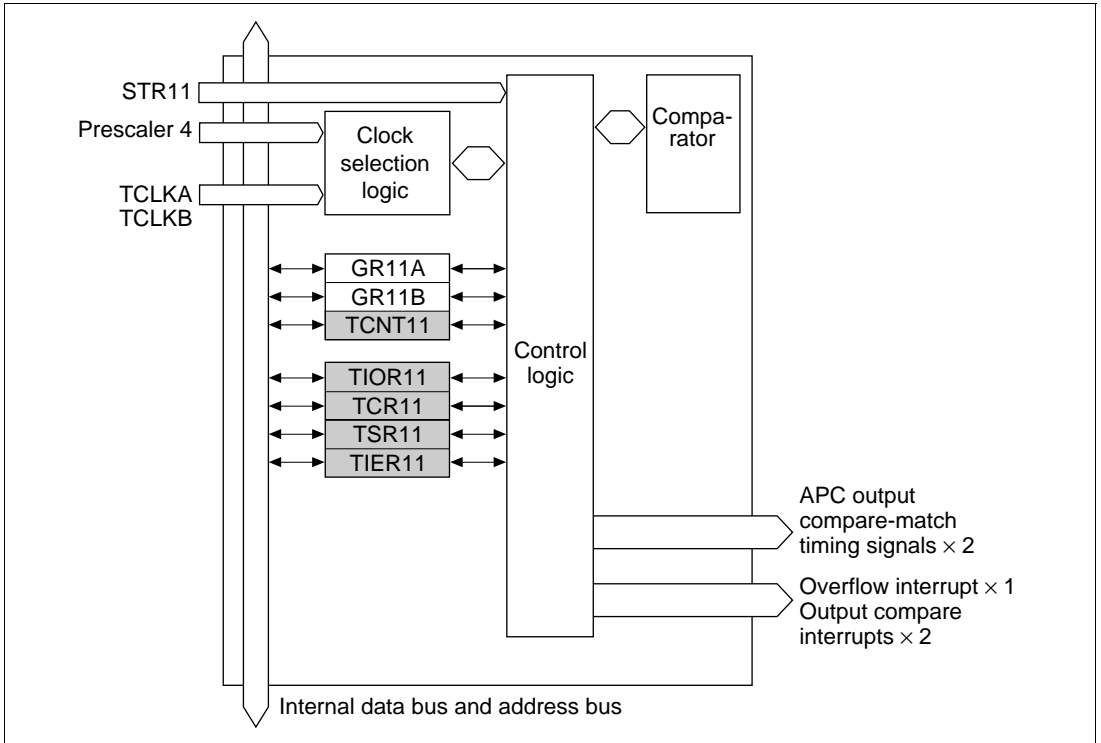
**Figure 10.8 Block Diagram of Channel 9**

**Block Diagram of Channel 10:** Figure 10.9 shows a block diagram of ATU-II channel 10.



**Figure 10.9 Block Diagram of Channel 10**

**Block Diagram of Channel 11:** Figure 10.10 shows a block diagram of ATU-II channel 11.



**Figure 10.10 Block Diagram of Channel 11**

## 10.1.5 Inter-Channel and Inter-Module Signal Communication Diagram

Figure 10.11 shows the connections between channels and between modules in the ATU-II.

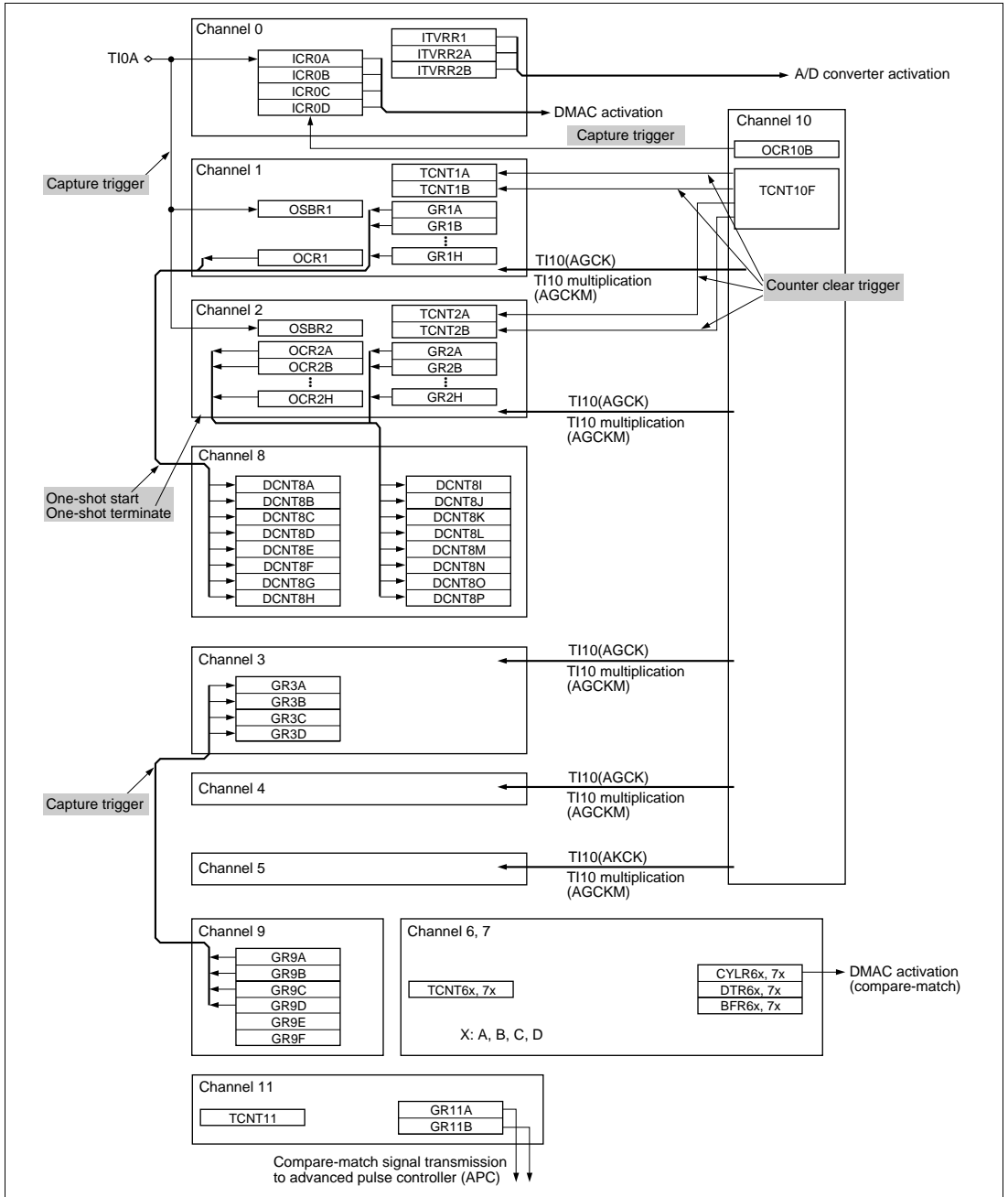
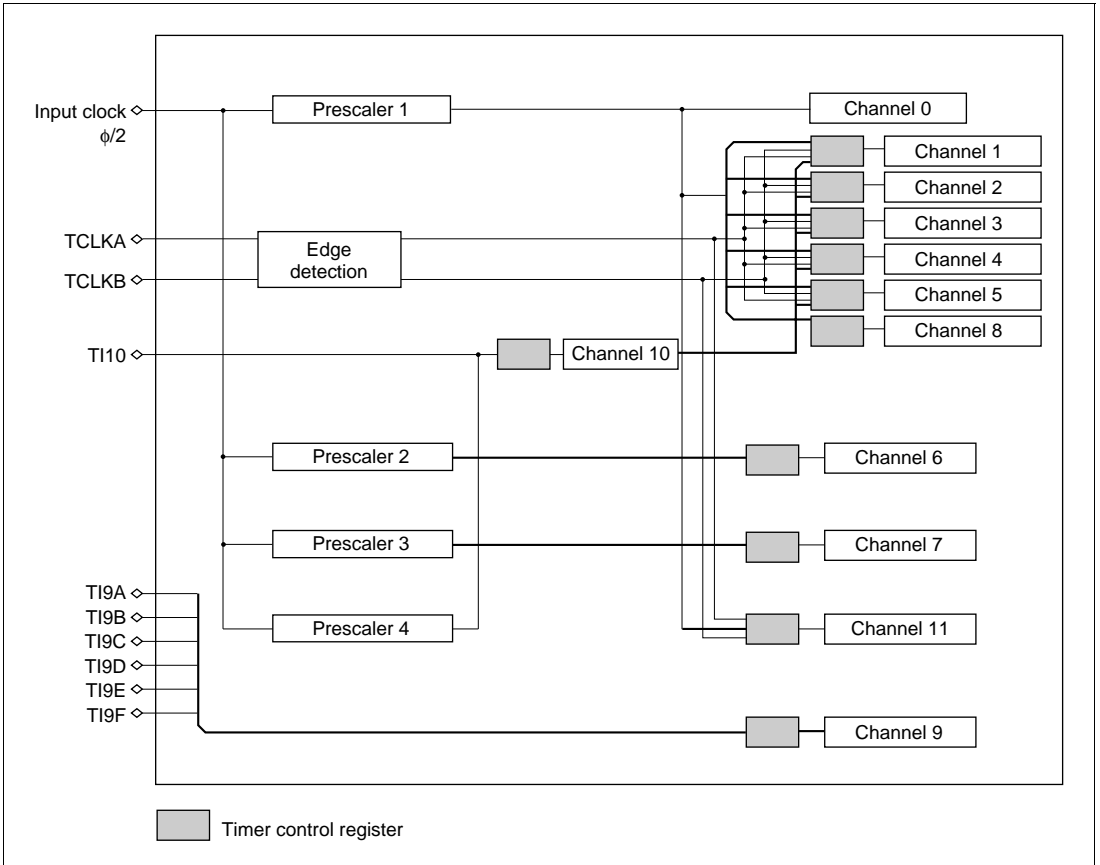


Figure 10.11 Inter-Module Communication Signals

## 10.1.6 Prescaler Diagram

Figure 10.12 shows a diagram of the ATU-II prescalers.



**Figure 10.12 Prescaler Diagram**

## 10.2 Register Descriptions

### 10.2.1 Timer Start Registers (TSTR)

The timer start registers (TSTR) are 8-bit registers. The ATU-II has three TSTR registers.

Channel	Abbreviation	Function
0, 1, 2, 3, 4, 5, 10	TSTR1	Free-running counter operation/stop setting
6, 7	TSTR2	
11	TSTR3	

#### Timer Start Register 1 (TSTR1)

Bit:	7	6	5	4	3	2	1	0
	STR10	STR5	STR4	STR3	STR1B, 2B	STR2A	STR1A	STR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TSTR1 is an 8-bit readable/writable register that starts and stops the free-running counter (TCNT) in channels 0 to 5 and 10.

TSTR1 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Counter Start 10 (STR10): Starts and stops channel 10 counters (TCNT10A, 10C, 10D, 10E, 10F, and 10G). TCNT10B and 10H are not stopped.

Bit 7: STR10	Description
0	TCNT10 is halted (Initial value)
1	TCNT10 counts

- Bit 6—Counter Start 5 (STR5): Starts and stops free-running counter 5 (TCNT5).

Bit 6: STR5	Description
0	TCNT5 is halted (Initial value)
1	TCNT5 counts

- Bit 5—Counter Start 4 (STR4): Starts and stops free-running counter 4 (TCNT4).

Bit 5: STR4	Description
0	TCNT4 is halted (Initial value)
1	TCNT4 counts

- Bit 4—Counter Start 3 (STR3): Starts and stops free-running counter 3 (TCNT3).

Bit 4: STR3	Description
0	TCNT3 is halted (Initial value)
1	TCNT3 counts

- Bit 3—Counter Start 1B, 2B (STR1B, STR2B): Starts and stops free-running counters 1B and 2B (TCNT1B, TCNT2B).

Bit 3: STR1B, STR2B	Description
0	TCNT1B and TCNT2B are halted (Initial value)
1	TCNT1B and TCNT2B count

- Bit 2—Counter Start 2A (STR2A): Starts and stops free-running counter 2A (TCNT2A).

Bit 2: STR2A	Description
0	TCNT2A is halted (Initial value)
1	TCNT2A counts

- Bit 1—Counter Start 1A (STR1A): Starts and stops free-running counter 1A (TCNT1A).

Bit 1: STR1A	Description
0	TCNT1A is halted (Initial value)
1	TCNT1A counts

- Bit 0—Counter Start 0 (STR0): Starts and stops free-running counter 0 (TCNT0).

Bit 0: STR0	Description
0	TCNT0 is halted (Initial value)
1	TCNT0 counts

## Timer Start Register 2 (TSTR2)

Bit:	7	6	5	4	3	2	1	0
	STR7D	STR7C	STR7B	STR7A	STR6D	STR6C	STR6B	STR6A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TSTR2 is an 8-bit readable/writable register that starts and stops the free-running counter (TCNT) in channels 6 and 7.

TSTR2 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Counter Start 7D (STR7D): Starts and stops free-running counter 7D (TCNT7D).

Bit 7: STR7D	Description
0	TCNT7D is halted (Initial value)
1	TCNT7D counts

- Bit 6—Counter Start 7C (STR7C): Starts and stops free-running counter 7C (TCNT7C).

Bit 6: STR7C	Description
0	TCNT7C is halted (Initial value)
1	TCNT7C counts

- Bit 5—Counter Start 7B (STR7B): Starts and stops free-running counter 7B (TCNT7B).

Bit 5: STR7B	Description
0	TCNT7B is halted (Initial value)
1	TCNT7B counts

- Bit 4—Counter Start 7A (STR7A): Starts and stops free-running counter 7A (TCNT7A).

Bit 4: STR7A	Description
0	TCNT7A is halted (Initial value)
1	TCNT7A counts



- Bit 3—Counter Start 6D (STR6D): Starts and stops free-running counter 6D (TCNT6D).

Bit 3: STR6D	Description
0	TCNT6D is halted (Initial value)
1	TCNT6D counts

- Bit 2—Counter Start 6C (STR6C): Starts and stops free-running counter 6C (TCNT6C).

Bit 2: STR6C	Description
0	TCNT6C is halted (Initial value)
1	TCNT6C counts

- Bit 1—Counter Start 6B (STR6B): Starts and stops free-running counter 6B (TCNT6B).

Bit 1: STR6B	Description
0	TCNT6B is halted (Initial value)
1	TCNT6B counts

- Bit 0—Counter Start 6A (STR6A): Starts and stops free-running counter 6A (TCNT6A).

Bit 0: STR6A	Description
0	TCNT6A is halted (Initial value)
1	TCNT6A counts

### Timer Start Register 3 (TSTR3)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	STR11
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

TSTR3 is an 8-bit readable/writable register that starts and stops the free-running counter (TCNT11) in channel 11.

TSTR3 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bits 7 to 1—Reserved: These bits always read 0. The write value should always be 0.

- Bit 0—Counter Start 11 (STR11): Starts and stops free-running counter 11 (TCNT11).

Bit 0: STR11	Description
0	TCNT11 is halted (Initial value)
1	TCNT11 counts

### 10.2.2 Prescaler Registers (PSCR)

The prescaler registers (PSCR) are 8-bit registers. The ATU-II has four PSCR registers.

Channel	Abbreviation	Function
0, 1, 2, 3, 4, 5, 8, 11	PSCR1	Prescaler setting for respective channels
6	PSCR2	
7	PSCR3	
10	PSCR4	

PSCR<sub>x</sub> is an 8-bit writable register that enables the first-stage counter clock  $\phi'$  input to each channel to be set to any value from  $P\phi/1$  to  $P\phi/32$ .

Bit:	7	6	5	4	3	2	1	0
	—	—	—	PSCxE	PSCxD	PSCxC	PSCxB	PSCxA
Initial value:	—	—	—	0	0	0	0	0
R/W:	—	—	—	W	W	W	W	W

x = 1 to 4

Input counter clock  $\phi'$  is determined by setting PSCxA to PSCxE:  $\phi'$  is  $P\phi/1$  when the set value is H'00, and  $P\phi/32$  when H'1F.

PSCR<sub>x</sub> is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

The internal clock  $\phi'$  set with this register can undergo further second-stage scaling to create clock  $\phi''$  for channels 1 to 8 and 11, the setting being made in the timer control register (TCR).

- Bits 7 to 5—Reserved. These bits cannot be modified.
- Bits 4 to 0—Prescaler (PSCxE, PSCxD, PSCxC, PSCxB, PSCxA): These bits specify frequency division of first-stage counter clock  $\phi'$  input to the corresponding channel.

### 10.2.3 Timer Control Registers (TCR)

The timer control registers (TCR) are 8-bit registers. The ATU-II has 16 TCR registers: two each for channels 1 and 2, one each for channels 3, 4, 5, 8, and 11, two each for channels 6 and 7, and three for channel 9. For details of channel 10, see section 10.2.26, Channel 10 Registers.

Channel	Abbreviation	Function
1	TCR1A, TCR1B	Internal clock/external clock/TI10 input clock selection
2	TCR2A, TCR2B	
3	TCR3	
4	TCR4	
5	TCR5	
6	TCR6A, TCR6B	Internal clock selection
7	TCR7A, TCR7B	
8	TCR8	
9	TCR9A, TCR9B, TCR9C	External clock selection/setting of channel 3 trigger in event of compare-match
11	TCR11	Internal clock/external clock selection

Each TCR is an 8-bit readable/writable register that selects whether an internal clock or external clock is used for channels 1 to 5 and 11. For channels 6 to 8, TCR selects an internal clock, and for channel 9, an external clock.

When an internal clock is selected, TCR selects the value of  $\phi''$  further scaled from clock  $\phi'$  scaled with prescaler register 1 (PSCR1). Scaled clock  $\phi''$  can be selected, for channels 1 to 8 and 11 only, from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$  (only  $\phi'$  is available for channel 0). Edge detection is performed on the rising edge.

When an external clock is selected, TCR selects whether TCLKA, TCLKB (channels 1 to 5 and 11 only), TI10 pin input (channels 1 to 5 only), or a TI10 pin input multiplied clock (channels 1 to 5 only) is used, and also performs edge selection.

Each TCR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

## Timer Control Registers 1A, 1B, 2A, 2B (TCR1A, TCR1B, TCR2A, TCR2B)

### TCR1A, TCR2A

Bit:	7	6	5	4	3	2	1	0
	—	—	CKEGA1	CKEGA0	CKSELA3	CKSELA2	CKSELA1	CKSELA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

### TCR1B, TCR2B

Bit:	7	6	5	4	3	2	1	0
	—	—	CKEGB1	CKEGB0	CKSELB3	CKSELB2	CKSELB1	CKSELB0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7 and 6—Reserved: These bits always read 0. The write value should always be 0.
- Bits 5 and 4—Clock Edge 1 and 0 (CKEGx1, CKEGx0): These bits select the count edge(s) for external clock TCLKA and TCLKB input.

Bit 5: CKEGx1	Bit 4: CKEGx0	Description
0	0	Rising edges counted (Initial value)
	1	Falling edges counted
1	0	Both rising and falling edges counted
	1	Count disabled

x = A or B

- Bits 3 to 0—Clock Select A3 to A0, B3 to B0 (CKSELA3 to CKSELA0, CKSELB3 to CKSELB0): These bits select whether an internal clock or external clock is used.  
When an internal clock is selected, scaled clock  $\phi''$  is selected from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .  
When an external clock is selected, TCLKA, TCLKB, TI10 pin input, or a TI10 pin input multiplied clock is selected.  
When TI10 pin input and TI10 pin input clock multiplication are selected, set CKEG1 and CKEG0 in TCR10 so that TI10 input is possible.

Bit 3: CKSELx3	Bit 2: CKSELx2	Bit 1: CKSELx1	Bit 0: CKSELx0	Description
0	0	0	0	Internal clock $\phi''$ : counting on $\phi'$ (Initial value)
			1	Internal clock $\phi''$ : counting on $\phi'/2$
		1	0	Internal clock $\phi''$ : counting on $\phi'/4$
			1	Internal clock $\phi''$ : counting on $\phi'/8$
	1	0	0	Internal clock $\phi''$ : counting on $\phi'/16$
			1	Internal clock $\phi''$ : counting on $\phi'/32$
		1	0	External clock: counting on TCLKA pin input
			1	External clock: counting on TCLKB pin input
1	0	0	0	Counting on TI10 pin input (AGCK)
			1	Counting on multiplied (corrected)(AGCKM) TI10 pin input clock
		1	*	Setting prohibited
	1	*	*	Setting prohibited

x = A or B

\*: Don't care

### Timer Control Registers 3 to 5 (TCR3, TCR4, TCR5)

Bit:	7	6	5	4	3	2	1	0
	—	—	CKEG1	CKEG0	CKSEL3	CKSEL2	CKSEL1	CKSEL0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 7 and 6—Reserved: These bits always read 0. The write value should always be 0.
- Bits 5 and 4—Clock Edge 1 and 0 (CKEG1, CKEG0): These bits select the count edge(s) for external clock TCLKA and TCLKB input.

Bit 5: CKEG1	Bit 4: CKEG0	Description
0	0	Rising edges counted (Initial value)
	1	Falling edges counted
1	0	Both rising and falling edges counted
	1	Count disabled

- Bits 3 to 0—Clock Select 3 to 0 (CKSEL3 to CKSEL0): These bits select whether an internal clock or external clock is used.

When an internal clock is selected, scaled clock  $\phi''$  is selected from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .

When an external clock is selected, TCLKA, TCLKB, TI10 pin input, or a TI10 pin input multiplied clock is selected.

When TI10 pin input and TI10 pin input clock multiplication are selected, set CKEG1 and CKEG0 in TCR10 so that TI10 input is possible.

Bit 3: CKSEL3	Bit 2: CKSEL2	Bit 1: CKSEL1	Bit 0: CKSEL0	Description
0	0	0	0	Internal clock $\phi''$ : counting on $\phi'$ (Initial value)
			1	Internal clock $\phi''$ : counting on $\phi'/2$
		1	0	Internal clock $\phi''$ : counting on $\phi'/4$
			1	Internal clock $\phi''$ : counting on $\phi'/8$
	1	0	0	Internal clock $\phi''$ : counting on $\phi'/16$
			1	Internal clock $\phi''$ : counting on $\phi'/32$
		1	0	External clock: counting on TCLKA pin input
			1	External clock: counting on TCLKB pin input
1	0	0	0	Counting on TI10 pin input (AGCK)
			1	Counting on multiplied (corrected)(AGCKM) TI10 pin input clock
	1	1	*	Setting prohibited
		1	*	Setting prohibited

\*: Don't care

## Timer Control Registers 6A, 6B, 7A, 7B (TCR6A, TCR6B, TCR7A, TCR7B)

### TCR6A, TCR7A

Bit:	7	6	5	4	3	2	1	0
	—	CKSELB2	CKSELB1	CKSELB0	—	CKSELA2	CKSELA1	CKSELA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TCR6B, TCR7B

Bit:	7	6	5	4	3	2	1	0
	—	CKSELD2	CKSELD1	CKSELD0	—	CKSELC2	CKSELC1	CKSELC0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bits 6 to 4—Clock Select B2 to B0, D2 to D0 (CKSELB2 to CKSELB0, CKSELD2 to CKSELD0): These bits select clock  $\phi''$ , scaled from the internal clock source, from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .

Bit 6: CKSELx2	Bit 5: CKSELx1	Bit 4: CKSELx0	Description
0	0	0	Internal clock $\phi''$ : counting on $\phi'$ (Initial value)
		1	Internal clock $\phi''$ : counting on $\phi'/2$
	1	0	Internal clock $\phi''$ : counting on $\phi'/4$
		1	Internal clock $\phi''$ : counting on $\phi'/8$
1	0	0	Internal clock $\phi''$ : counting on $\phi'/16$
		1	Internal clock $\phi''$ : counting on $\phi'/32$
	1	0	Setting prohibited
		1	Setting prohibited

x = B or D

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.

- Bits 2 to 0—Clock Select A2 to A0, C2 to C0 (CKSELA2 to CKSELA0, CKSELC2 to CKSELC0): These bits select clock  $\phi''$ , scaled from the internal clock source, from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .

Bit 2: CKSELx2	Bit 1 CKSELx1	Bit 0 CKSELx0	Description
0	0	0	Internal clock $\phi''$ : counting on $\phi'$ (Initial value)
		1	Internal clock $\phi''$ : counting on $\phi'/2$
	1	0	Internal clock $\phi''$ : counting on $\phi'/4$
		1	Internal clock $\phi''$ : counting on $\phi'/8$
1	0	0	Internal clock $\phi''$ : counting on $\phi'/16$
		1	Internal clock $\phi''$ : counting on $\phi'/32$
	1	0	Setting prohibited
		1	Setting prohibited

x = A or C

### Timer Control Register 8 (TCR8)

Bit:	7	6	5	4	3	2	1	0
	—	CKSELB2	CKSELB1	CKSELB0	—	CKSELA2	CKSELA1	CKSELA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

The CKSELAx bits relate to DCNT8A to DCNT8H, and the CKSELBx bits relate to DCNT8I to DCNT8P.

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.



- Bits 6 to 4—Clock Select B2 to B0 (CKSELB2 to CKSELB0): These bits, relating to counters DCNT8I to DCNT8P, select clock  $\phi^n$ , scaled from the internal clock source, from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .

Bit 6: CKSELB2	Bit 5: CKSELB1	Bit 4: CKSELB0	Description
0	0	0	Internal clock $\phi^n$ : counting on $\phi'$ (Initial value)
		1	Internal clock $\phi^n$ : counting on $\phi'/2$
	1	0	Internal clock $\phi^n$ : counting on $\phi'/4$
		1	Internal clock $\phi^n$ : counting on $\phi'/8$
1	0	0	Internal clock $\phi^n$ : counting on $\phi'/16$
		1	Internal clock $\phi^n$ : counting on $\phi'/32$
	1	0	Setting prohibited
		1	Setting prohibited

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bits 2 to 0—Clock Select A2 to A0 (CKSELA2 to CKSELA0): These bits, relating to counters DCNT8A to DCNT8H, select clock  $\phi^n$ , scaled from the internal clock source, from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .

Bit 2: CKSELA2	Bit 1: CKSELA1	Bit 0: CKSELA0	Description
0	0	0	Internal clock $\phi^n$ : counting on $\phi'$ (Initial value)
		1	Internal clock $\phi^n$ : counting on $\phi'/2$
	1	0	Internal clock $\phi^n$ : counting on $\phi'/4$
		1	Internal clock $\phi^n$ : counting on $\phi'/8$
1	0	0	Internal clock $\phi^n$ : counting on $\phi'/16$
		1	Internal clock $\phi^n$ : counting on $\phi'/32$
	1	0	Setting prohibited
		1	Setting prohibited

## Timer Control Registers 9A, 9B, 9C (TCR9A, TCR9B, TCR9C)

### TCR9A

Bit:	7	6	5	4	3	2	1	0
	—	TRG3BEN	EGSELB1	EGSELB0	—	TRG3AEN	EGSELA1	EGSELA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TCR9B

Bit:	7	6	5	4	3	2	1	0
	—	TRG3DEN	EGSELD1	EGSELD0	—	TRG3CEN	EGSELC1	EGSELC0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TCR9C

Bit:	7	6	5	4	3	2	1	0
	—	—	EGSELF1	EGSELF0	—	—	EGSELE1	EGSELE0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—Trigger Channel 3BEN, 3DEN (TRG3BEN, TRG3DEN): These bits select the channel 9 event counter compare-match signal channel 3 input capture trigger.

#### Bit 6: TRG3xEN Description

0	Channel 3 input capture trigger in event of channel 9 compare-match (ECNT9x = GR9x) is disabled (Initial value)
1	Channel 3 input capture trigger in event of channel 9 compare-match (ECNT9x = GR9x) is enabled

x = B or D

- Bits 5 and 4—Edge Select B1, B0, D1, D0, F1, F0 (EGSELB1, EGSELB0, EGSELD1, EGSELD0, EGSELF1, EGSELF0): These bits select the event counter counted edge(s).

Bit 5: EGSELx1	Bit 4: EGSELx0	Description
0	0	Count disabled (Initial value)
	1	Rising edges counted
1	0	Falling edges counted
	1	Both rising and falling edges counted

x = B, D, or F

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—Trigger Channel 3AEN, 3CEN (TRG3AEN, TRG3CEN): These bits select the channel 9 event counter compare-match signal channel 3 input capture trigger.

Bit 2: TRG3xEN	Description
0	Channel 3 input capture trigger in event of channel 9 compare-match (ECNT9x = GR9x) is disabled (Initial value)
1	Channel 3 input capture trigger in event of channel 9 compare-match (ECNT9x = GR9x) is enabled

x = A or C

- Bits 1 and 0—Edge Select A1, A0, C1, C0, E1, E0 (EGSELA1, EGSELA0, EGSELC1, EGSELC0, EGSELE1, EGSELE0): These bits select the event counter counted edge(s).

Bit 1: EGSELx1	Bit 0: EGSELx0	Description
0	0	Count disabled (Initial value)
	1	Rising edges counted
1	0	Falling edges counted
	1	Both rising and falling edges counted

x = A, C, or E

## Timer Control Register 11 (TCR11)

Bit:	7	6	5	4	3	2	1	0
	—	—	CKEG1	CKEG0	—	CKSELA2	CKSELA1	CKSELA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W

- Bits 7, 6, and 3—Reserved: These bits always read 0. The write value should always be 0.
- Bits 5 and 4—Edge Select: These bits select the event counter counted edge(s).

Bit 5: CKEG1	Bit 4: CKEG0	Description
0	0	Rising edges counted (Initial value)
	1	Falling edges counted
1	0	Both rising and falling edges counted
	1	Count disabled

- Bits 2 to 0—Clock Select A2 to A0 (CKSELA2 to CKSELA0): These bits select clock  $\phi''$ , scaled from the internal clock source, from  $\phi'$ ,  $\phi'/2$ ,  $\phi'/4$ ,  $\phi'/8$ ,  $\phi'/16$ , and  $\phi'/32$ .

Bit 2: CKSELA2	Bit 1: CKSELA1	Bit 0: CKSELA0	Description
0	0	0	Internal clock $\phi''$ : counting on $\phi'$ (Initial value)
		1	Internal clock $\phi''$ : counting on $\phi'/2$
	1	0	Internal clock $\phi''$ : counting on $\phi'/4$
		1	Internal clock $\phi''$ : counting on $\phi'/8$
1	0	0	Internal clock $\phi''$ : counting on $\phi'/16$
		1	Internal clock $\phi''$ : counting on $\phi'/32$
	1	0	External clock: counting on TCLKA pin input
		1	External clock: counting on TCLKB pin input

## 10.2.4 Timer I/O Control Registers (TIOR)

The timer I/O control registers (TIOR) are 8-bit registers. The ATU-II has 16 TIOR registers: one for channel 0, four each for channels 1 and 2, two each for channels 3 to 5, and one for channel 11. For details of channel 10, see section 10.2.26, Channel 10 Registers.

Channel	Abbreviation	Function
0	TIOR0	ICR0 edge detection setting
1	TIOR1A to 1D	GR input capture/compare-match switching, edge detection/ output value setting
2	TIOR2A to 2D	
3	TIOR3A, TIOR3B	GR input capture/compare-match switching, edge detection/ output value setting, TCNT3 to TCNT5 clear enable/disable setting
4	TIOR4A, TIOR4B	
5	TIOR5A, TIOR5B	
11	TIOR11	GR input capture/compare-match switching, edge detection/output value setting

Each TIOR is an 8-bit readable/writable register used to select the functions of dedicated input capture registers and general registers.

For dedicated input capture registers (ICR), TIOR performs edge detection setting.

For general registers (GR), TIOR selects use as an input capture register or output compare register, and performs edge detection setting. For channels 3 to 5, TIOR also selects enabling or disabling of free-running counter (TCNT) clearing in the event of a compare-match.

### Timer I/O Control Register 0 (TIOR0)

Bit:	7	6	5	4	3	2	1	0
	IO0D1	IO0D0	IO0C1	IO0C0	IO0B1	IO0B0	IO0A1	IO0A0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TIOR0 specifies edge detection for input capture registers ICR0A to ICR0D.

TIOR0 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bits 7 and 6—I/O Control 0D1 and 0D0 (IO0D1, IO0D0): These bits select TIOD pin input capture signal edge detection.

Bit 7: IO0D1	Bit 6: IO0D0	Description
0	0	Input capture disabled (input capture possible in TCNT10B compare-match) (Initial value)
	1	Input capture in ICR0D on rising edge
1	0	Input capture in ICR0D on falling edge
	1	Input capture in ICR0D on both rising and falling edges

- Bits 5 and 4—I/O Control 0C1 and 0C0 (IO0C1, IO0C0): These bits select TIOC pin input capture signal edge detection.

Bit 5: IO0C1	Bit 4: IO0C0	Description
0	0	Input capture disabled (Initial value)
	1	Input capture in ICR0C on rising edge
1	0	Input capture in ICR0C on falling edge
	1	Input capture in ICR0C on both rising and falling edges

- Bits 3 and 2—I/O Control 0B1 and 0B0 (IO0B1, IO0B0): These bits select TIOB pin input capture signal edge detection.

Bit 3: IO0B1	Bit 2: IO0B0	Description
0	0	Input capture disabled (Initial value)
	1	Input capture in ICR0B on rising edge
1	0	Input capture in ICR0B on falling edge
	1	Input capture in ICR0B on both rising and falling edges

- Bits 1 and 0—I/O Control 0A1 and 0A0 (IO0A1, IO0A0): These bits select TIOA pin input capture signal edge detection.

Bit 1: IO0A1	Bit 0: IO0A0	Description
0	0	Input capture disabled (Initial value)
	1	Input capture in ICR0A on rising edge
1	0	Input capture in ICR0A on falling edge
	1	Input capture in ICR0A on both rising and falling edges

## Timer I/O Control Registers 1A to 1D (TIOR1A to TIOR1D)

### TIOR1A

Bit:	7	6	5	4	3	2	1	0
	—	IO1B2	IO1B1	IO1B0	—	IO1A2	IO1A1	IO1A0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TIOR1B

Bit:	7	6	5	4	3	2	1	0
	—	IO1D2	IO1D1	IO1D0	—	IO1C2	IO1C1	IO1C0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TIOR1C

Bit:	7	6	5	4	3	2	1	0
	—	IO1F2	IO1F1	IO1F0	—	IO1E2	IO1E1	IO1E0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TIOR1D

Bit:	7	6	5	4	3	2	1	0
	—	IO1H2	IO1H1	IO1H0	—	IO1G2	IO1G1	IO1G0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Registers TIOR1A to TIOR1D specify whether general registers GR1A to GR1H are used as input capture or compare-match registers, and also perform edge detection and output value setting.

Each TIOR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.

- Bits 6 to 4—I/O Control 1B2 to 1B0, 1D2 to 1D0, 1F2 to 1F0, 1H2 to 1H0 (IO1B2 to IO1B0, IO1D2 to IO1D0, IO1F2 to IO1F0, IO1H2 to IO1H0): These bits select the general register (GR) function.

Bit 6: IO1x2	Bit 5: IO1x1	Bit 4: IO1x0	Description
0	0	0	GR is an output compare register Compare-match disabled; pin output undefined (Initial value)
		1	0 output on GR compare-match
	1	0	1 output on GR compare-match
		1	Toggle output on GR compare-match
1	0	0	GR is an input capture register Input capture disabled (GR cannot be written to)
		1	Input capture in GR on rising edge at TIO1x pin (GR cannot be written to)
	1	0	Input capture in GR on falling edge at TIO1x pin (GR cannot be written to)
		1	Input capture in GR on both rising and falling edges at TIO1x pin (GR cannot be written to)

x = B, D, F, or H

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.



- Bits 2 to 0—I/O Control 1A2 to 1A0, 1C2 to 1C0, 1E2 to 1E0, 1G2 to 1G0 (IO1A2 to IO1A0, IO1C2 to IO1C0, IO1E2 to IO1E0, IO1G2 to IO1G0): These bits select the general register (GR) function.

Bit 2: IO1x2	Bit 1: IO1x1	Bit 0: IO1x0	Description
0	0	0	GR is an output compare register Compare-match disabled; pin output undefined (Initial value)
		1	0 output on GR compare-match
	1	0	1 output on GR compare-match
		1	Toggle output on GR compare-match
1	0	0	GR is an input capture register Input capture disabled (GR cannot be written to)
		1	Input capture in GR on rising edge at TIO1x pin (GR cannot be written to)
	1	0	Input capture in GR on falling edge at TIO1x pin (GR cannot be written to)
		1	Input capture in GR on both rising and falling edges at TIO1x pin (GR cannot be written to)

## Timer I/O Control Registers 2A to 2D (TIOR2A to TIOR2D)

### TIOR2A

Bit:	7	6	5	4	3	2	1	0
	—	IO2B2	IO2B1	IO2B0	—	IO2A2	IO2A1	IO2A0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TIOR2B

Bit:	7	6	5	4	3	2	1	0
	—	IO2D2	IO2D1	IO2D0	—	IO2C2	IO2C1	IO2C0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TIOR2C

Bit:	7	6	5	4	3	2	1	0
	—	IO2F2	IO2F1	IO2F0	—	IO2E2	IO2E1	IO2E0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

### TIOR2D

Bit:	7	6	5	4	3	2	1	0
	—	IO2H2	IO2H1	IO2H0	—	IO2G2	IO2G1	IO2G0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Registers TIOR2A to TIOR2D specify whether general registers GR2A to GR2H are used as input capture or compare-match registers, and also perform edge detection and output value setting.

Each TIOR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bits 6 to 4—I/O Control 2B2 to 2B0, 2D2 to 2D0, 2F2 to 2F0, 2H2 to 2H0 (IO2B2 to IO2B0, IO2D2 to IO2D0, IO2F2 to IO2F0, IO2H2 to IO2H0): These bits select the general register (GR) function.

Bit 6: IO2x2	Bit 5: IO2x1	Bit 4: IO2x0	Description
0	0	0	GR is an output compare register
		1	GR is an output compare register
	1	0	GR is an output compare register
		1	GR is an output compare register
1	0	0	GR is an input capture register
		1	GR is an input capture register
	1	0	GR is an input capture register
		1	GR is an input capture register

x = B, D, F, or H

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.

- Bits 2 to 0—I/O Control 2A2 to 2A0, 2C2 to 2C0, 2E2 to 2E0, 2G2 to 2G0 (IO2A2 to IO2A0, IO2C2 to IO2C0, IO2E2 to IO2E0, IO2G2 to IO2G0): These bits select the general register (GR) function.

Bit 2: IO2x2	Bit 1: IO2x1	Bit 0: IO2x0	Description
0	0	0	GR is an output compare register Compare-match disabled; pin output undefined (Initial value)
		1	0 output on GR compare-match
	1	0	1 output on GR compare-match
		1	Toggle output on GR compare-match
1	0	0	GR is an input capture register Input capture disabled
		1	Input capture in GR on rising edge at TIO2x pin (GR cannot be written to)
	1	0	Input capture in GR on falling edge at TIO2x pin (GR cannot be written to)
		1	Input capture in GR on both rising and falling edges at TIO2x pin (GR cannot be written to)

x = A, C, E, or G

### Timer I/O Control Registers 3A, 3B, 4A, 4B, 5A, 5B (TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, TIOR5B)

#### TIOR3A, TIOR4A, TIOR5A

Bit:	7	6	5	4	3	2	1	0
	CClxB	IOxB2	IOxB1	IOxB0	CClxA	IOxA2	IOxA1	IOxA0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

x = 3 to 5

## TIOR3B, TIOR4B, TIOR5B

Bit:	7	6	5	4	3	2	1	0
	CCIxD	IOxD2	IOxD1	IOxD0	CCIxC	IOxC2	IOxC1	IOxC0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

x = 3 to 5

TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, and TIOR5B specify whether general registers GR3A to GR3D, GR4A to GR4D, and GR5A to GR5D are used as input capture or compare-match registers, and also perform edge detection and output value setting. They also select enabling or disabling of free-running counter (TCNT3 to TCNT5) clearing.

Each TIOR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Clear Counter Enable Flag 3B, 4B, 5B, 3D, 4D, 5D (CCI3B, CCI4B, CCI5B, CCI3D, CCI4D, CCI5D): These bits select enabling or disabling of free-running counter (TCNT) clearing.

Bit 7: CCIxx	Description
0	TCNT clearing disabled (Initial value)
1	TCNT cleared on GR compare-match

xx = 3B, 4B, 5B, 3D, 4D, or 5D

TCNT is cleared on compare-match only when GR is functioning as an output compare register.

- Bits 6 to 4—I/O Control 3B2 to 3B0, 4B2 to 4B0, 5B2 to 5B0, 3D2 to 3D0, 4D2 to 4D0, 5D2 to 5D0 (IO3B2 to IO3B0, IO4B2 to IO4B0, IO5B2 to IO5B0, IO3D2 to IO3D0, IO4D2 to IO4D0, IO5D2 to IO5D0): These bits select the general register (GR) function.

Bit 6: IOxx2	Bit 5: IOxx1	Bit 4: IOxx0	Description
0	0	0	GR is an output compare register Compare-match disabled; pin output undefined (Initial value)
		1	0 output on GR compare-match
	1	0	1 output on GR compare-match
		1	Toggle output on GR compare-match
1	0	0	GR is an input capture register Input capture disabled (input capture by channel 3 and 9 compare-match enabled) (In channel 3 only, GR cannot be written to)
		1	Input capture in GR on rising edge at TIOxx pin (GR cannot be written to)
	1	0	Input capture in GR on falling edge at TIOxx pin (GR cannot be written to)
		1	Input capture in GR on both rising and falling edges at TIOxx pin (GR cannot be written to)

xx = 3B, 4B, 5B, 3D, 4D, or 5D

- Bit 3—Clear Counter Enable Flag 3A, 4A, 5A, 3C, 4C, 5C (CCI3A, CCI4A, CCI5A, CCI3C, CCI4C, CCI5C): These bits select enabling or disabling of free-running counter (TCNT) clearing.

Bit 3: CCIxx	Description
0	TCNT clearing disabled (Initial value)
1	TCNT cleared on GR compare-match

xx = 3A, 4A, 5A, 3C, 4C, or 5C

TCNT is cleared on compare-match only when GR is functioning as an output compare register.

- Bits 2 to 0—I/O Control 3A2 to 3A0, 4A2 to 4A0, 5A2 to 5A0, 3C2 to 3C0, 4C2 to 4C0, 5C2 to 5C0 (IO3A2 to IO3A0, IO4A2 to IO4A0, IO5A2 to IO5A0, IO3C2 to IO3C0, IO4C2 to IO4C0, IO5C2 to IO5C0): These bits select the general register (GR) function.

Bit 2: IOxx2	Bit 1: IOxx1	Bit 0: IOxx0	Description
0	0	0	GR is an output compare register Compare-match disabled; pin output undefined (Initial value)
		1	0 output on GR compare-match
	1	0	1 output on GR compare-match
		1	Toggle output on GR compare-match
1	0	0	GR is an input capture register Input capture disabled (input capture by channel 3 and 9 compare-match enabled) (In channel 3 only, GR cannot be written to)
		1	Input capture in GR on rising edge at TIOxx pin (GR cannot be written to)
	1	0	Input capture in GR on falling edge at TIOxx pin (GR cannot be written to)
		1	Input capture in GR on both rising and falling edges at TIOxx pin (GR cannot be written to)

xx = 3A, 4A, 5A, 3C, 4C, or 5C

## Timer I/O Control Register 11 (TIOR11)

### TIOR11

Bit:	7	6	5	4	3	2	1	0
	—	—	—	IO11B0	—	—	—	IO11A0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R/W	R/W	R/W

TIOR11 specifies whether general registers GR11A and GR11B are used as input capture or compare-match registers, and also performs edge detection and output value setting.

TIOR11 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bits 7 to 5—Reserved: These bits always reads 0. The write value should always be 0.
- Bit 4—I/O Control 11B0 (IO11B0): These bits select the general register (GR) function.

Bit 4: IO11B0	Description
0	Compare-match is disabled (Initial value)
1	Ccompare-match is enabled

- Bits 3 to 1—Reserved: These bits always reads 0. The write value should always be 0.
- Bit 0—I/O Control 11A0 (IO11A0): This bit select the general register (GR) function.

Bit 0: IO11A0	Description
0	Compare-match is disabled (Initial value)
1	Ccompare-match is enabled



## 10.2.5 Timer Status Registers (TSR)

The timer status registers (TSR) are 16-bit registers. The ATU-II has 11 TSR registers: one each for channels 0, 6 to 9, and 11, two each for channels 1 and 2, and one for channels 3 to 5. For details of channel 10, see section 10.2.26, Channel 10 Registers.

Channel	Abbreviation	Function
0	TSR0	Indicates input capture, interval interrupt, and overflow status
1	TSR1A, TSR1B	Indicate input capture, compare-match, and overflow status
2	TSR2A, TSR2B	
3	TSR3	Indicates input capture, compare-match, and overflow status
4		
5		
6	TSR6	Indicate cycle register compare-match status
7	TSR7	
8	TSR8	Indicates down-counter output end (low) status
9	TSR9	Indicates event counter compare-match status
11	TSR11	Indicates compare-match and overflow status

The TSR registers are 16-bit readable/writable registers containing flags that indicate free-running counter (TCNT) overflow, channel 0 input capture or interval interrupt generation, channel 3, 4, 5, and 11 general register input capture or compare-match, channel 6 and 7 compare-matches, channel 8 down-counter output end, and channel 9 event counter compare-matches.

Each flag is an interrupt source, and issues an interrupt request to the CPU if the interrupt is enabled by the corresponding bit in the timer interrupt enable register (TIER).

Each TSR is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

## Timer Status Register 0 (TSR0)

TSR0 indicates the status of channel 0 interval interrupts, input capture, and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	IIF2B	IIF2A	IIF1	OVF0	ICF0D	ICF0C	ICF0B	ICF0A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 8—Reserved: These bits always read 0. The write value should always be 0.
- Bit 7—Interval Interrupt Flag 2B (IIF2B): Status flag that indicates the generation of an interval interrupt.

Bit 7: IIF2B	Description
0	[Clearing condition] (Initial value) When IIF2B is read while set to 1, then 0 is written to IIF2B
1	[Setting condition] When interval interrupt selected by ITVRR2B is generated

- Bit 6—Interval Interrupt Flag 2A (IIF2A): Status flag that indicates the generation of an interval interrupt.

Bit 6: IIF2A	Description
0	[Clearing condition] (Initial value) When IIF2A is read while set to 1, then 0 is written to IIF2A
1	[Setting condition] When interval interrupt selected by ITVRR2A is generated

- Bit 5—Interval Interrupt Flag 1 (IIF1): Status flag that indicates the generation of an interval interrupt.

Bit 5: IIF1	Description
0	[Clearing condition] (Initial value) When IIF1 is read while set to 1, then 0 is written to IIF1
1	[Setting condition] When interval interrupt selected by ITVRR1 is generated

- Bit 4—Overflow Flag 0 (OVF0): Status flag that indicates TCNT0 overflow.

Bit 4: OVF0	Description
0	[Clearing condition] (Initial value) When OVF0 is read while set to 1, then 0 is written to OVF0
1	[Setting condition] When the TCNT0 value overflows (from H'FFFFFFFF to H'00000000)

- Bit 3—Input Capture Flag 0D (ICF0D): Status flag that indicates ICR0D input capture.

Bit 3: ICF0D	Description
0	[Clearing condition] (Initial value) When ICF0D is read while set to 1, then 0 is written to ICF0D
1	[Setting condition] When the TCNT0 value is transferred to the input capture register by an input capture signal. Also set by input capture with a channel 10 compare match as the trigger

- Bit 2—Input Capture Flag 0C (ICF0C): Status flag that indicates ICR0C input capture.

Bit 2: ICF0C	Description
0	[Clearing condition] (Initial value) When ICF0C is read while set to 1, then 0 is written to ICF0C
1	[Setting condition] When the TCNT0 value is transferred to the input capture register by an input capture signal

- Bit 1—Input Capture Flag 0B (ICF0B): Status flag that indicates ICR0B input capture.

Bit 1: ICF0B	Description
0	[Clearing condition] (Initial value) When ICF0B is read while set to 1, then 0 is written to ICF0B
1	[Setting condition] When the TCNT0 value is transferred to the input capture register by an input capture signal

- Bit 0—Input Capture Flag 0A (ICF0A): Status flag that indicates ICR0A input capture.

Bit 0: ICF0A	Description
0	[Clearing condition] (Initial value) When ICF0A is read while set to 1, then 0 is written to ICF0A
1	[Setting condition] When the TCNT0 value is transferred to the input capture register by an input capture signal

### Timer Status Registers 1A and 1B (TSR1A, TSR1B)

**TSR1A:** TSR1A indicates the status of channel 1 input capture, compare-match, and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVF1A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*
Bit:	7	6	5	4	3	2	1	0
	IMF1H	IMF1G	IMF1F	IMF1E	IMF1D	IMF1C	IMF1B	IMF1A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.

- Bit 8—Overflow Flag 1A (OVF1A): Status flag that indicates TCNT1A overflow.

Bit 8: OVF1A	Description
0	[Clearing condition] (Initial value) When OVF1A is read while set to 1, then 0 is written to OVF1A
1	[Setting condition] When the TCNT1A value overflows (from H'FFFF to H'0000)

- Bit 7—Input Capture/Compare-Match Flag 1H (IMF1H): Status flag that indicates GR1H input capture or compare-match.

Bit 7: IMF1H	Description
0	[Clearing condition] (Initial value) When IMF1H is read while set to 1, then 0 is written to IMF1H
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1H by an input capture signal while GR1H is functioning as an input capture register</li> <li>• When TCNT1A = GR1H while GR1H is functioning as an output compare register</li> </ul>

- Bit 6—Input Capture/Compare-Match Flag 1G (IMF1G): Status flag that indicates GR1G input capture or compare-match.

Bit 6: IMF1G	Description
0	[Clearing condition] (Initial value) When IMF1G is read while set to 1, then 0 is written to IMF1G
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1G by an input capture signal while GR1G is functioning as an input capture register</li> <li>• When TCNT1A = GR1G while GR1G is functioning as an output compare register</li> </ul>

- Bit 5—Input Capture/Compare-Match Flag 1F (IMF1F): Status flag that indicates GR1F input capture or compare-match.

Bit 5: IMF1F	Description
0	[Clearing condition] (Initial value) When IMF1F is read while set to 1, then 0 is written to IMF1F
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1F by an input capture signal while GR1F is functioning as an input capture register</li> <li>• When TCNT1A = GR1F while GR1F is functioning as an output compare register</li> </ul>

- Bit 4—Input Capture/Compare-Match Flag 1E (IMF1E): Status flag that indicates GR1E input capture or compare-match.

Bit 4: IMF1E	Description
0	[Clearing condition] (Initial value) When IMF1E is read while set to 1, then 0 is written to IMF1E
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1E by an input capture signal while GR1E is functioning as an input capture register</li> <li>• When TCNT1A = GR1E while GR1E is functioning as an output compare register</li> </ul>

- Bit 3—Input Capture/Compare-Match Flag 1D (IMF1D): Status flag that indicates GR1D input capture or compare-match.

Bit 3: IMF1D	Description
0	[Clearing condition] (Initial value) When IMF1D is read while set to 1, then 0 is written to IMF1D
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1D by an input capture signal while GR1D is functioning as an input capture register</li> <li>• When TCNT1A = GR1D while GR1D is functioning as an output compare register</li> </ul>

- Bit 2—Input Capture/Compare-Match Flag 1C (IMF1C): Status flag that indicates GR1C input capture or compare-match.

Bit 2: IMF1C	Description
0	[Clearing condition] (Initial value) When IMF1C is read while set to 1, then 0 is written to IMF1C
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1C by an input capture signal while GR1C is functioning as an input capture register</li> <li>• When TCNT1A = GR1C while GR1C is functioning as an output compare register</li> </ul>

- Bit 1—Input Capture/Compare-Match Flag 1B (IMF1B): Status flag that indicates GR1B input capture or compare-match.

Bit 1: IMF1B	Description
0	[Clearing condition] (Initial value) When IMF1B is read while set to 1, then 0 is written to IMF1B
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1B by an input capture signal while GR1B is functioning as an input capture register</li> <li>• When TCNT1A = GR1B while GR1B is functioning as an output compare register</li> </ul>

- Bit 0—Input Capture/Compare-Match Flag 1A (IMF1A): Status flag that indicates GR1A input capture or compare-match.

Bit 0: IMF1A	Description
0	[Clearing condition] (Initial value) When IMF1A is read while set to 1, then 0 is written to IMF1A
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT1A value is transferred to GR1A by an input capture signal while GR1A is functioning as an input capture register</li> <li>• When TCNT1A = GR1A while GR1A is functioning as an output compare register</li> </ul>

**TSR1B:** TSR1B indicates the status of channel 1 compare-match and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVF1B
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CMF1
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Flag 1B (OVF1B): Status flag that indicates TCNT1B overflow.

Bit 8: OVF1B	Description
0	[Clearing condition] (Initial value) When OVF1B is read while set to 1, then 0 is written to OVF1B
1	[Setting condition] When the TCNT1B value overflows (from H'FFFF to H'0000)

- Bits 7 to 1—Reserved: These bits always read 0. The write value should always be 0.
- Bit 0—Compare-Match Flag 1 (CMF1): Status flag that indicates OCR1 compare-match.

Bit 0: CMF1	Description
0	[Clearing condition] (Initial value) When CMF1 is read while set to 1, then 0 is written to CMF1
1	[Setting condition] When TCNT1B = OCR1



## Timer Status Registers 2A and 2B (TSR2A, TSR2B)

**TSR2A:** TSR2A indicates the status of channel 2 input capture, compare-match, and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVF2A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*

Bit:	7	6	5	4	3	2	1	0
	IMF2H	IMF2G	IMF2F	IMF2E	IMF2D	IMF2C	IMF2B	IMF2A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Flag 2A (OVF2A): Status flag that indicates TCNT2A overflow.

Bit 8: OVF2A	Description
0	[Clearing condition] (Initial value) When OVF2A is read while set to 1, then 0 is written to OVF2A
1	[Setting condition] When the TCNT2A value overflows (from H'FFFF to H'0000)

- Bit 7—Input Capture/Compare-Match Flag 2H (IMF2H): Status flag that indicates GR2H input capture or compare-match.

Bit 7: IMF2H	Description
0	[Clearing condition] (Initial value) When IMF2H is read while set to 1, then 0 is written to IMF2H
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2H by an input capture signal while GR2H is functioning as an input capture register</li> <li>• When TCNT2A = GR2H while GR2H is functioning as an output compare register</li> </ul>

- Bit 6—Input Capture/Compare-Match Flag 2G (IMF2G): Status flag that indicates GR2G input capture or compare-match.

Bit 6: IMF2G	Description
0	[Clearing condition] (Initial value) When IMF2G is read while set to 1, then 0 is written to IMF2G
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2G by an input capture signal while GR2G is functioning as an input capture register</li> <li>• When TCNT2A = GR2G while GR2G is functioning as an output compare register</li> </ul>

- Bit 5—Input Capture/Compare-Match Flag 2F (IMF2F): Status flag that indicates GR2F input capture or compare-match.

Bit 5: IMF2F	Description
0	[Clearing condition] (Initial value) When IMF2F is read while set to 1, then 0 is written to IMF2F
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2F by an input capture signal while GR2F is functioning as an input capture register</li> <li>• When TCNT2A = GR2F while GR2F is functioning as an output compare register</li> </ul>

- Bit 4—Input Capture/Compare-Match Flag 2E (IMF2E): Status flag that indicates GR2E input capture or compare-match.

Bit 4: IMF2E	Description
0	[Clearing condition] (Initial value) When IMF2E is read while set to 1, then 0 is written to IMF2E
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2E by an input capture signal while GR2E is functioning as an input capture register</li> <li>• When TCNT2A = GR2E while GR2E is functioning as an output compare register</li> </ul>

- Bit 3—Input Capture/Compare-Match Flag 2D (IMF2D): Status flag that indicates GR2D input capture or compare-match.

Bit 3: IMF2D	Description
0	[Clearing condition] (Initial value) When IMF2D is read while set to 1, then 0 is written to IMF2D
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2D by an input capture signal while GR2D is functioning as an input capture register</li> <li>• When TCNT2A = GR2D while GR2D is functioning as an output compare register</li> </ul>

- Bit 2—Input Capture/Compare-Match Flag 2C (IMF2C): Status flag that indicates GR2C input capture or compare-match.

Bit 2: IMF2C	Description
0	[Clearing condition] (Initial value) When IMF2C is read while set to 1, then 0 is written to IMF2C
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2C by an input capture signal while GR2C is functioning as an input capture register</li> <li>• When TCNT2A = GR2C while GR2C is functioning as an output compare register</li> </ul>

- Bit 1—Input Capture/Compare-Match Flag 2B (IMF2B): Status flag that indicates GR2B input capture or compare-match.

Bit 1: IMF2B	Description
0	[Clearing condition] (Initial value) When IMF2B is read while set to 1, then 0 is written to IMF2B
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2B by an input capture signal while GR2B is functioning as an input capture register</li> <li>• When TCNT2A = GR2B while GR2B is functioning as an output compare register</li> </ul>

- Bit 0—Input Capture/Compare-Match Flag 2A (IMF2A): Status flag that indicates GR2A input capture or compare-match.

Bit 0: IMF2A	Description
0	[Clearing condition] (Initial value) When IMF2A is read while set to 1, then 0 is written to IMF2A
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT2A value is transferred to GR2A by an input capture signal while GR2A is functioning as an input capture register</li> <li>• When TCNT2A = GR2A while GR2A is functioning as an output compare register</li> </ul>

**TSR2B:** TSR2B indicates the status of channel 2 compare-match and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVF2B
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*
Bit:	7	6	5	4	3	2	1	0
	CMF2H	CMF2G	CMF2F	CMF2E	CMF2D	CMF2C	CMF2B	CMF2A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Flag 2B (OVF2B): Status flag that indicates TCNT2B overflow.

Bit 8: OVF2B	Description
0	[Clearing condition] (Initial value) When OVF2B is read while set to 1, then 0 is written to OVF2B
1	[Setting condition] When the TCNT2B value overflows (from H'FFFF to H'0000)

- Bit 7—Compare-Match Flag 2H (CMF2H): Status flag that indicates OCR2H compare-match.

Bit 7: CMF2H	Description
0	[Clearing condition] (Initial value) When CMF2H is read while set to 1, then 0 is written to CMF2H
1	[Setting condition] When TCNT2B = OCR2H

- Bit 6—Compare-Match Flag 2G (CMF2G): Status flag that indicates OCR2G compare-match.

Bit 6: CMF2G	Description
0	[Clearing condition] (Initial value) When CMF2G is read while set to 1, then 0 is written to CMF2G
1	[Setting condition] When TCNT2B = OCR2G

- Bit 5—Compare-Match Flag 2F (CMF2F): Status flag that indicates OCR2F compare-match.

Bit 5: CMF2F	Description
0	[Clearing condition] (Initial value) When CMF2F is read while set to 1, then 0 is written to CMF2F
1	[Setting condition] When TCNT2B = OCR2F

- Bit 4—Compare-Match Flag 2E (CMF2E): Status flag that indicates OCR2E compare-match.

Bit 4: CMF2E	Description
0	[Clearing condition] (Initial value) When CMF2E is read while set to 1, then 0 is written to CMF2E
1	[Setting condition] When TCNT2B = OCR2E

- Bit 3—Compare-Match Flag 2D (CMF2D): Status flag that indicates OCR2D compare-match.

Bit 3: CMF2D	Description
0	[Clearing condition] (Initial value) When CMF2D is read while set to 1, then 0 is written to CMF2D
1	[Setting condition] When TCNT2B = OCR2D

- Bit 2—Compare-Match Flag 2C (CMF2C): Status flag that indicates OCR2C compare-match.

Bit 2: CMF2C	Description
0	[Clearing condition] (Initial value) When CMF2C is read while set to 1, then 0 is written to CMF2C
1	[Setting condition] When TCNT2B = OCR2C

- Bit 1—Compare-Match Flag 2B (CMF2B): Status flag that indicates OCR2B compare-match.

Bit 1: CMF2B	Description
0	[Clearing condition] (Initial value) When CMF2B is read while set to 1, then 0 is written to CMF2B
1	[Setting condition] When TCNT2B = OCR2B

- Bit 0—Compare-Match Flag 2A (CMF2A): Status flag that indicates OCR2A compare-match.

Bit 0: CMF2A	Description
0	[Clearing condition] (Initial value) When CMF2A is read while set to 1, then 0 is written to CMF2A
1	[Setting condition] When TCNT2B = OCR2A

### Timer Status Register 3 (TSR3)

TSR3 indicates the status of channel 3 to 5 input capture, compare-match, and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	OVF5	IMF5D	IMF5C	IMF5B	IMF5A	OVF4	IMF4D
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*
Bit:	7	6	5	4	3	2	1	0
	IMF4C	IMF4B	IMF4A	OVF3	IMF3D	IMF3C	IMF3B	IMF3A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—Overflow Flag 5 (OVF5): Status flag that indicates TCNT5 overflow.

Bit 14: OVF5	Description
0	[Clearing condition] (Initial value) When OVF5 is read while set to 1, then 0 is written to OVF5
1	[Setting condition] When the TCNT5 value overflows (from H'FFFF to H'0000)

- Bit 13—Input Capture/Compare-Match Flag 5D (IMF5D): Status flag that indicates GR5D input capture or compare-match.

Bit 13: IMF5D	Description
0	[Clearing condition] (Initial value) When IMF5D is read while set to 1, then 0 is written to IMF5D
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT5 value is transferred to GR5D by an input capture signal while GR5D is functioning as an input capture register</li> <li>• When TCNT5 = GR5D while GR5D is functioning as an output compare register</li> <li>• When TCNT5 = GR5D while GR5D is functioning as a synchronous register in PWM mode</li> </ul>

- Bit 12—Input Capture/Compare-Match Flag 5C (IMF5C): Status flag that indicates GR5C input capture or compare-match. The flag is not set in PWM mode.

Bit 12: IMF5C	Description
0	[Clearing condition] (Initial value) When IMF5C is read while set to 1, then 0 is written to IMF5C
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT5 value is transferred to GR5C by an input capture signal while GR5C is functioning as an input capture register</li> <li>• When TCNT5 = GR5C while GR5C is functioning as an output compare register</li> </ul>

- Bit 11—Input Capture/Compare-Match Flag 5B (IMF5B): Status flag that indicates GR5B input capture or compare-match. The flag is not set in PWM mode.

Bit 11: IMF5B	Description
0	[Clearing condition] (Initial value) When IMF5B is read while set to 1, then 0 is written to IMF5B
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT5 value is transferred to GR5B by an input capture signal while GR5B is functioning as an input capture register</li> <li>• When TCNT5 = GR5B while GR5B is functioning as an output compare register</li> </ul>

- Bit 10—Input Capture/Compare-Match Flag 5A (IMF5A): Status flag that indicates GR5A input capture or compare-match. The flag is not set in PWM mode.

Bit 10: IMF5A	Description
0	[Clearing condition] (Initial value) When IMF5A is read while set to 1, then 0 is written to IMF5A
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT5 value is transferred to GR5A by an input capture signal while GR5A is functioning as an input capture register</li> <li>• When TCNT5 = GR5A while GR5A is functioning as an output compare register</li> </ul>

- Bit 9—Overflow Flag 4 (OVF4): Status flag that indicates TCNT4 overflow.

Bit 9: OVF4	Description
0	[Clearing condition] (Initial value) When OVF4 is read while set to 1, then 0 is written to OVF4
1	[Setting condition] When the TCNT4 value overflows (from H'FFFF to H'0000)



- Bit 8—Input Capture/Compare-Match Flag 4D (IMF4D): Status flag that indicates GR4D input capture or compare-match.

Bit 8: IMF4D	Description
0	[Clearing condition] (Initial value) When IMF4D is read while set to 1, then 0 is written to IMF4D
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT4 value is transferred to GR4D by an input capture signal while GR4D is functioning as an input capture register</li> <li>• When TCNT4 = GR4D while GR4D is functioning as an output compare register</li> <li>• When TCNT4 = GR4D while GR4D is functioning as a PWM mode synchronous register</li> </ul>

- Bit 7—Input Capture/Compare-Match Flag 4C (IMF4C): Status flag that indicates GR4C input capture or compare-match. The flag is not set in PWM mode.

Bit 7: IMF4C	Description
0	[Clearing condition] (Initial value) When IMF4C is read while set to 1, then 0 is written to IMF4C
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT4 value is transferred to GR4C by an input capture signal while GR4C is functioning as an input capture register</li> <li>• When TCNT4 = GR4C while GR4C is functioning as an output compare register</li> </ul>

- Bit 6—Input Capture/Compare-Match Flag 4B (IMF4B): Status flag that indicates GR4B input capture or compare-match. The flag is not set in PWM mode.

Bit 6: IMF4B	Description
0	[Clearing condition] (Initial value) When IMF4B is read while set to 1, then 0 is written to IMF4B
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT4 value is transferred to GR4B by an input capture signal while GR4B is functioning as an input capture register</li> <li>• When TCNT4 = GR4B while GR4B is functioning as an output compare register</li> </ul>

- Bit 5—Input Capture/Compare-Match Flag 4A (IMF4A): Status flag that indicates GR4A input capture or compare-match. The flag is not set in PWM mode.

Bit 5: IMF4A	Description
0	[Clearing condition] (Initial value) When IMF4A is read while set to 1, then 0 is written to IMF4A
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT4 value is transferred to GR4A by an input capture signal while GR4A is functioning as an input capture register</li> <li>• When TCNT4 = GR4A while GR4A is functioning as an output compare register</li> </ul>

- Bit 4—Overflow Flag 3 (OVF3): Status flag that indicates TCNT3 input capture or compare-match.

Bit 4: OVF3	Description
0	[Clearing condition] (Initial value) When OVF3 is read while set to 1, then 0 is written to OVF3
1	[Setting condition] When the TCNT3 value overflows (from H'FFFF to H'0000)

- Bit 3—Input Capture/Compare-Match Flag 3D (IMF3D): Status flag that indicates GR5D input capture or compare-match.

Bit 3: IMF3D	Description
0	[Clearing condition] (Initial value) When IMF3D is read while set to 1, then 0 is written to IMF3D
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT3 value is transferred to GR3D by an input capture signal while GR3D is functioning as an input capture register. However, IMF3D is not set by input capture with a channel 9 compare match as the trigger</li> <li>• When TCNT3 = GR3D while GR3D is functioning as an output compare register</li> <li>• When TCNT3 = GR3D while GR3D is functioning as a synchronous register in PWM mode</li> </ul>

- Bit 2—Input Capture/Compare-Match Flag 3C (IMF3C): Status flag that indicates GR3C input capture or compare-match. The flag is not set in PWM mode.

Bit 2: IMF3C	Description
0	[Clearing condition] (Initial value) When IMF3C is read while set to 1, then 0 is written to IMF3C
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT3 value is transferred to GR3C by an input capture signal while GR3C is functioning as an input capture register. However, IMF3C is not set by input capture with a channel 9 compare match as the trigger</li> <li>• When TCNT3 = GR3C while GR3C is functioning as an output compare register</li> </ul>

- Bit 1—Input Capture/Compare-Match Flag 3B (IMF3B): Status flag that indicates GR3B input capture or compare-match. The flag is not set in PWM mode.

Bit 1: IMF3B	Description
0	[Clearing condition] (Initial value) When IMF3B is read while set to 1, then 0 is written to IMF3B
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT3 value is transferred to GR3B by an input capture signal while GR3B is functioning as an input capture register. However, IMF3B is not set by input capture with a channel 9 compare match as the trigger</li> <li>• When TCNT3 = GR3B while GR3B is functioning as an output compare register</li> </ul>

- Bit 0—Input Capture/Compare-Match Flag 3A (IMF3A): Status flag that indicates GR3A input capture or compare-match. The flag is not set in PWM mode.

Bit 0: IMF3A	Description
0	[Clearing condition] (Initial value) When IMF3A is read while set to 1, then 0 is written to IMF3A
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When the TCNT3 value is transferred to GR3A by an input capture signal while GR3A is functioning as an input capture register. However, IMF3A is not set by input capture with a channel 9 compare match as the trigger</li> <li>• When TCNT3 = GR3A while GR3A is functioning as an output compare register</li> </ul>

## Timer Status Registers 6 and 7 (TSR6, TSR7)

TSR6 and TRS7 indicate the channel 6 and 7 free-running counter up-count and down-count status, and cycle register compare status.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	UDxD	UDxC	UDxB	UDxA	CMFxD	CMFxC	CMFxB	CMFxA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.  
x = 6 or 7

UDxA to UDxD relate to TSR6 only. Bits relating to TSR7 always read 0.

- Bits 15 to 8—Reserved: These bits always read 0. The write value should always be 0.
- Bit 7—Count-Up/Count-Down Flag 6D (UD6D): Status flag that indicates the TCNT6D count operation.

Bit 7: UD6D	Description
0	Free-running counter TCNT6D operates as an up-counter
1	Free-running counter TCNT6D operates as a down-counter

- Bit 6—Count-Up/Count-Down Flag 6C (UD6C): Status flag that indicates the TCNT6C count operation.

Bit 6: UD6C	Description
0	Free-running counter TCNT6C operates as an up-counter
1	Free-running counter TCNT6C operates as a down-counter

- Bit 5—Count-Up/Count-Down Flag 6B (UD6B): Status flag that indicates the TCNT6B count operation.

Bit 5: UD6B	Description
0	Free-running counter TCNT6B operates as an up-counter
1	Free-running counter TCNT6B operates as a down-counter

- Bit 4—Count-Up/Count-Down Flag 6A (UD6A): Status flag that indicates the TCNT6A count operation.

Bit 4: UD6A	Description
0	Free-running counter TCNT6A operates as an up-counter
1	Free-running counter TCNT6A operates as a down-counter

- Bit 3—Cycle Register Compare-Match Flag 6D/7D (CMF6D/CMF7D): Status flag that indicates CYLRxD compare-match.

Bit 3: CMFxD	Description
0	[Clearing condition] (Initial value) When CMFxD is read while set to 1, then 0 is written to CMFxD
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When TCNTxD = CYLRxD (in non-complementary PWM mode)</li> <li>• When TCNT6D = H'0000 in a down-count (in complementary PWM mode)</li> </ul>

x = 6 or 7

- Bit 2—Cycle Register Compare-Match Flag 6C/7C (CMF6C/CMF7C): Status flag that indicates CYLRxC compare-match.

Bit 2: CMFxC	Description
0	[Clearing condition] (Initial value) When CMFxC is read while set to 1, then 0 is written to CMFxC
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When TCNTxC = CYLRxC (in non-complementary PWM mode)</li> <li>• When TCNT6C = H'0000 in a down-count (in complementary PWM mode)</li> </ul>

x = 6 or 7

- Bit 1—Cycle Register Compare-Match Flag 6B/7B (CMF6B/CMF7B): Status flag that indicates CYLRxB compare-match.

Bit 1: CMFxB	Description
0	[Clearing condition] (Initial value) When CMFxB is read while set to 1, then 0 is written to CMFxB
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When TCNTxB = CYLRxB (in non-complementary PWM mode)</li> <li>• When TCNT6B = H'0000 in a down-count (in complementary PWM mode)</li> </ul>

x = 6 or 7

- Bit 0—Cycle Register Compare-Match Flag 6A/7A (CMF6A/CMF7A): Status flag that indicates CYLRxA compare-match.

Bit 0: CMFxA	Description
0	[Clearing condition] (Initial value) When CMFxA is read while set to 1, then 0 is written to CMFxA
1	[Setting conditions] <ul style="list-style-type: none"> <li>• When TCNTxA = CYLRxA (in non-complementary PWM mode)</li> <li>• When TCNT6A = H'0000 in a down-count (in complementary PWM mode)</li> </ul>

x = 6 or 7

## Timer Status Register 8 (TSR8)

TSR8 indicates the channel 8 one-shot pulse status.

Bit:	15	14	13	12	11	10	9	8
	OSF8P	OSF8O	OSF8N	OSF8M	OSF8L	OSF8K	OSF8J	OSF8I
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit:	7	6	5	4	3	2	1	0
	OSF8H	OSF8G	OSF8F	OSF8E	OSF8D	OSF8C	OSF8B	OSF8A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bit 15—One-Shot Pulse Flag 8P (OSF8P): Status flag that indicates a DCNT8P one-shot pulse.

Bit 15: OSF8P	Description
0	[Clearing condition] (Initial value) When OSF8P is read while set to 1, then 0 is written to OSF8P
1	[Setting condition] When DCNT8P underflows

- Bit 14—One-Shot Pulse Flag 8O (OSF8O): Status flag that indicates a DCNT8O one-shot pulse.

Bit 14: OSF8O	Description
0	[Clearing condition] (Initial value) When OSF8O is read while set to 1, then 0 is written to OSF8O
1	[Setting condition] When DCNT8O underflows

- Bit 13—One-Shot Pulse Flag 8N (OSF8N): Status flag that indicates a DCNT8N one-shot pulse.

Bit 13: OSF8N	Description
0	[Clearing condition] (Initial value) When OSF8N is read while set to 1, then 0 is written to OSF8N
1	[Setting condition] When DCNT8N underflows

- Bit 12—One-Shot Pulse Flag 8M (OSF8M): Status flag that indicates a DCNT8M one-shot pulse.

Bit 12: OSF8M	Description
0	[Clearing condition] (Initial value) When OSF8M is read while set to 1, then 0 is written to OSF8M
1	[Setting condition] When DCNT8M underflows

- Bit 11—One-Shot Pulse Flag 8L (OSF8L): Status flag that indicates a DCNT8L one-shot pulse.

Bit 11: OSF8L	Description
0	[Clearing condition] (Initial value) When OSF8L is read while set to 1, then 0 is written to OSF8L
1	[Setting condition] When DCNT8L underflows

- Bit 10—One-Shot Pulse Flag 8K (OSF8K): Status flag that indicates a DCNT8K one-shot pulse.

Bit 10: OSF8K	Description
0	[Clearing condition] (Initial value) When OSF8K is read while set to 1, then 0 is written to OSF8K
1	[Setting condition] When DCNT8K underflows

- Bit 9—One-Shot Pulse Flag 8J (OSF8J): Status flag that indicates a DCNT8J one-shot pulse.

Bit 9: OSF8J	Description
0	[Clearing condition] (Initial value) When OSF8J is read while set to 1, then 0 is written to OSF8J
1	[Setting condition] When DCNT8J underflows

- Bit 8—One-Shot Pulse Flag 8I (OSF8I): Status flag that indicates a DCNT8I one-shot pulse.

Bit 8: OSF8I	Description
0	[Clearing condition] (Initial value) When OSF8I is read while set to 1, then 0 is written to OSF8I
1	[Setting condition] When DCNT8I underflows



- Bit 7—One-Shot Pulse Flag 8H (OSF8H): Status flag that indicates a DCNT8H one-shot pulse.

Bit 7: OSF8H	Description
0	[Clearing condition] (Initial value) When OSF8H is read while set to 1, then 0 is written to OSF8H
1	[Setting condition] When DCNT8H underflows

- Bit 6—One-Shot Pulse Flag 8G (OSF8G): Status flag that indicates a DCNT8G one-shot pulse.

Bit 6: OSF8G	Description
0	[Clearing condition] (Initial value) When OSF8G is read while set to 1, then 0 is written to OSF8G
1	[Setting condition] When DCNT8G underflows

- Bit 5—One-Shot Pulse Flag 8F (OSF8F): Status flag that indicates a DCNT8F one-shot pulse.

Bit 5: OSF8F	Description
0	[Clearing condition] (Initial value) When OSF8F is read while set to 1, then 0 is written to OSF8F
1	[Setting condition] When DCNT8F underflows

- Bit 4—One-Shot Pulse Flag 8E (OSF8E): Status flag that indicates a DCNT8E one-shot pulse.

Bit 4: OSF8E	Description
0	[Clearing condition] (Initial value) When OSF8E is read while set to 1, then 0 is written to OSF8E
1	[Setting condition] When DCNT8E underflows

- Bit 3—One-Shot Pulse Flag 8D (OSF8D): Status flag that indicates a DCNT8D one-shot pulse.

Bit 3: OSF8D	Description
0	[Clearing condition] (Initial value) When OSF8D is read while set to 1, then 0 is written to OSF8D
1	[Setting condition] When DCNT8D underflows

- Bit 2—One-Shot Pulse Flag 8C (OSF8C): Status flag that indicates a DCNT8C one-shot pulse.

Bit 2: OSF8C	Description
0	[Clearing condition] (Initial value) When OSF8C is read while set to 1, then 0 is written to OSF8C
1	[Setting condition] When DCNT8C underflows

- Bit 1—One-Shot Pulse Flag 8B (OSF8B): Status flag that indicates a DCNT8B one-shot pulse.

Bit 1: OSF8B	Description
0	[Clearing condition] (Initial value) When OSF8B is read while set to 1, then 0 is written to OSF8B
1	[Setting condition] When DCNT8B underflows

- Bit 0—One-Shot Pulse Flag 8A (OSF8A): Status flag that indicates a DCNT8A one-shot pulse.

Bit 0: OSF8A	Description
0	[Clearing condition] (Initial value) When OSF8A is read while set to 1, then 0 is written to OSF8A
1	[Setting condition] When DCNT8A underflows

## Timer Status Register 9 (TSR9)

TSR9 indicates the channel 9 event counter compare-match status.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	—	CMF9F	CMF9E	CMF9D	CMF9C	CMF9B	CMF9A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 6—Reserved: These bits always read 0. The write value should always be 0.
- Bit 5—Compare-Match Flag 9F (CMF9F): Status flag that indicates GR9F compare-match.

Bit 5: CMF9F	Description
0	[Clearing condition] (Initial value) When CMF9F is read while set to 1, then 0 is written to CMF9F
1	[Setting condition] When the next edge is input while ECNT9F = GR9F

- Bit 4—Compare-Match Flag 9E (CMF9E): Status flag that indicates GR9E compare-match.

Bit 4: CMF9E	Description
0	[Clearing condition] (Initial value) When CMF9E is read while set to 1, then 0 is written to CMF9E
1	[Setting condition] When the next edge is input while ECNT9E = GR9E

- Bit 3—Compare-Match Flag 9D (CMF9D): Status flag that indicates GR9D compare-match.

Bit 3: CMF9D	Description
0	[Clearing condition] (Initial value) When CMF9D is read while set to 1, then 0 is written to CMF9D
1	[Setting condition] When the next edge is input while ECNT9D = GR9D

- Bit 2—Compare-Match Flag 9C (CMF9C): Status flag that indicates GR9C compare-match.

Bit 2: CMF9C	Description
0	[Clearing condition] (Initial value) When CMF9C is read while set to 1, then 0 is written to CMF9C
1	[Setting condition] When the next edge is input while ECNT9C = GR9C

- Bit 1—Compare-Match Flag 9B (CMF9B): Status flag that indicates GR9B compare-match.

Bit 1: CMF9B	Description
0	[Clearing condition] (Initial value) When CMF9B is read while set to 1, then 0 is written to CMF9B
1	[Setting condition] When the next edge is input while ECNT9B = GR9B

- Bit 0—Compare-Match Flag 9A (CMF9A): Status flag that indicates GR9A compare-match.

Bit 0: CMF9A	Description
0	[Clearing condition] (Initial value) When CMF9A is read while set to 1, then 0 is written to CMF9A
1	[Setting condition] When the next edge is input while ECNT9A = GR9A

## Timer Status Register 11 (TSR11)

TSR11 indicates the status of channel 11 compare-match and overflow.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVF11
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/(W)*
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IMF11B	IMF11A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Flag 11 (OVF11): Status flag that indicates TCNT11 overflow.

Bit 8: OVF11	Description
0	[Clearing condition] (Initial value) When OVF11 is read while set to 1, then 0 is written to OVF11
1	[Setting condition] When the TCNT11 value overflows (from H'FFFF to H'0000)

- Bits 7 to 2—Reserved: These bits always read 0. The write value should always be 0.
- Bit 1—Compare-Match Flag 11B (IMF11B): Status flag that indicates GR11B compare-match.

Bit 1: IMF11B	Description
0	[Clearing condition] (Initial value) When IMF11B is read while set to 1, then 0 is written to IMF11B
1	[Setting condition] When TCNT11 = GR11B while GR11B is functioning as an output compare register

- Bit 0—Compare-Match Flag 11A (IMF11A): Status flag that indicates GR11A compare-match.

Bit 0: IMF11A	Description
0	[Clearing condition] (Initial value) When IMF11A is read while set to 1, then 0 is written to IMF11A
1	[Setting condition] When TCNT11 = GR11A while GR11A is functioning as an output compare register

## 10.2.6 Timer Interrupt Enable Registers (TIER)

The timer interrupt enable registers (TIER) are 16-bit registers. The ATU-II has 11 TIER registers: one each for channels 0, 6 to 9, and 11, two each for channels 1 and 2, and one for channels 3 to 5. For details of channel 10, see section 10.2.26, Channel 10 Registers.

Channel	Abbreviation	Function
0	TIER0	Controls input capture, and overflow interrupt request enabling/disabling.
1	TIER1A, TIER1B	Control input capture, compare-match, and overflow interrupt request enabling/disabling.
2	TIER2A, TIER2B	
3	TIER3	Controls input capture, compare-match, and overflow interrupt request enabling/disabling.
4		
5		
6	TIER6	Control cycle register compare-match interrupt request enabling/disabling.
7	TIER7	
8	TIER8	Controls down-counter output end (low) interrupt request enabling/disabling.
9	TIER9	Controls event counter compare-match interrupt request enabling/disabling.
11	TIER11	Controls input capture, compare-match, and overflow interrupt request enabling/disabling.

The TIER registers are 16-bit readable/writable registers that control enabling and disabling of timer interrupt requests. These cover free-running counter (TCNT) overflow interrupts, channel 0 input capture interrupts, channel 1 to 5 general register input capture/compare-match interrupts, channel 6 and 7 compare-match interrupts, channel 8 down-counter output pin interrupts, channel 9 event counter compare-match interrupts, and channel 11 general register compare-match interrupts.

Each TIER is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

### Timer Interrupt Enable Register 0 (TIER0)

TIER0 controls enabling/disabling of channel 0 input capture and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit:	7	6	5	4	3	2	1	0
	—	—	—	OVE0	ICE0D	ICE0C	ICE0B	ICE0A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 5—Reserved: These bits always read 0. The write value should always be 0.
- Bit 4—Overflow Interrupt Enable 0 (OVE0): Enables or disables interrupt requests by the overflow flag (OVF0) in TSR0 when OVF0 is set to 1.

Bit 4: OVE0	Description
0	OVI0 interrupt requested by OVF0 is disabled (Initial value)
1	OVI0 interrupt requested by OVF0 is enabled

- Bit 3—Input Capture Interrupt Enable 0D (ICE0D): Enables or disables interrupt requests by the input capture flag (ICF0D) in TSR0 when ICF0D is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 3: ICE0D	Description
0	ICI0D interrupt requested by ICF0D is disabled (Initial value)
1	ICI0D interrupt requested by ICF0D is enabled

- Bit 2—Input Capture Interrupt Enable 0C (ICE0C): Enables or disables interrupt requests by the input capture flag (ICF0C) in TSR0 when ICF0C is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 2: ICE0C	Description
0	IC10C interrupt requested by ICF0C is disabled (Initial value)
1	IC10C interrupt requested by ICF0C is enabled

- Bit 1—Input Capture Interrupt Enable 0B (ICE0B): Enables or disables interrupt requests by the input capture flag (ICF0B) in TSR0 when ICF0B is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 1: ICE0B	Description
0	IC10B interrupt requested by ICF0B is disabled (Initial value)
1	IC10B interrupt requested by ICF0B is enabled

- Bit 0—Input Capture Interrupt Enable 0A (ICE0A): Enables or disables interrupt requests by the input capture flag (ICF0A) in TSR0 when ICF0A is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 0: ICE0A	Description
0	IC10A interrupt requested by ICF0A is disabled (Initial value)
1	IC10A interrupt requested by ICF0A is enabled

### Timer Interrupt Enable Registers 1A and 1B (TIER1A, TIER1B)

**TIER1A:** TIER1A controls enabling/disabling of channel 1 input capture, compare-match, and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVE1A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W
Bit:	7	6	5	4	3	2	1	0
	IME1H	IME1G	IME1F	IME1E	IME1D	IME1C	IME1B	IME1A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Interrupt Enable 1A (OVE1A): Enables or disables interrupt requests by OVF1A in TSR1A when OVF1A is set to 1.

Bit 8: OVE1A	Description
0	OVI1A interrupt requested by OVF1A is disabled (Initial value)
1	OVI1A interrupt requested by OVF1A is enabled

- Bit 7—Input Capture/Compare-Match Interrupt Enable 1H (IME1H): Enables or disables interrupt requests by IMF1H in TSR1A when IMF1H is set to 1.

Bit 7: IME1H	Description
0	IMI1H interrupt requested by IMF1H is disabled (Initial value)
1	IMI1H interrupt requested by IMF1H is enabled

- Bit 6—Input Capture/Compare-Match Interrupt Enable 1G (IME1G): Enables or disables interrupt requests by IMF1G in TSR1A when IMF1G is set to 1.

Bit 6: IME1G	Description
0	IMI1G interrupt requested by IMF1G is disabled (Initial value)
1	IMI1G interrupt requested by IMF1G is enabled

- Bit 5—Input Capture/Compare-Match Interrupt Enable 1F (IME1F): Enables or disables interrupt requests by IMF1F in TSR1A when IMF1F is set to 1.

Bit 5: IME1F	Description
0	IMI1F interrupt requested by IMF1F is disabled (Initial value)
1	IMI1F interrupt requested by IMF1F is enabled

- Bit 4—Input Capture/Compare-Match Interrupt Enable 1E (IME1E): Enables or disables interrupt requests by IMF1E in TSR1A when IMF1E is set to 1.

Bit 4: IME1E	Description
0	IMI1E interrupt requested by IMF1E is disabled (Initial value)
1	IMI1E interrupt requested by IMF1E is enabled

- Bit 3—Input Capture/Compare-Match Interrupt Enable 1D (IME1D): Enables or disables interrupt requests by IMF1D in TSR1A when IMF1D is set to 1.

Bit 3: IME1D	Description
0	IMI1D interrupt requested by IMF1D is disabled (Initial value)
1	IMI1D interrupt requested by IMF1D is enabled

- Bit 2—Input Capture/Compare-Match Interrupt Enable 1C (IME1C): Enables or disables interrupt requests by IMF1C in TSR1A when IMF1C is set to 1.

Bit 2: IME1C	Description
0	IMI1C interrupt requested by IMF1C is disabled (Initial value)
1	IMI1C interrupt requested by IMF1C is enabled

- Bit 1—Input Capture/Compare-Match Interrupt Enable 1B (IME1B): Enables or disables interrupt requests by IMF1B in TSR1A when IMF1B is set to 1.

Bit 1: IME1B	Description
0	IMI1B interrupt requested by IMF1B is disabled (Initial value)
1	IMI1B interrupt requested by IMF1B is enabled

- Bit 0—Input Capture/Compare-Match Interrupt Enable 1A (IME1A): Enables or disables interrupt requests by IMF1A in TSR1A when IMF1A is set to 1.

Bit 0: IME1A	Description
0	IMI1A interrupt requested by IMF1A is disabled (Initial value)
1	IMI1A interrupt requested by IMF1A is enabled

**TIER1B:** TIER1B controls enabling/disabling of channel 1 compare-match and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVE1B
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CME1
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Interrupt Enable 1B (OVE1B): Enables or disables interrupt requests by OVF1B in TSR1B when OVF1B is set to 1.

Bit 8: OVE1B	Description
0	OVI1B interrupt requested by OVF1B is disabled (Initial value)
1	OVI1B interrupt requested by OVF1B is enabled

- Bits 7 to 1—Reserved: These bits always read 0. The write value should always be 0.
- Bit 0—Compare-Match Interrupt Enable 1 (CME1): Enables or disables interrupt requests by CMF1 in TSR1B when CMF1 is set to 1.

Bit 0: CME1	Description
0	CMI1 interrupt requested by CMF1 is disabled (Initial value)
1	CMI1 interrupt requested by CMF1 is enabled

## Timer Interrupt Enable Registers 2A and 2B (TIER2A, TIER2B)

**TIER2A:** TIER2A controls enabling/disabling of channel 2 input capture, compare-match, and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVE2A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W
Bit:	7	6	5	4	3	2	1	0
	IME2H	IME2G	IME2F	IME2E	IME2D	IME2C	IME2B	IME2A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Interrupt Enable 2A (OVE2A): Enables or disables interrupt requests by OVF2A in TSR2A when OVF2A is set to 1.

Bit 8: OVE2A	Description
0	OVI2A interrupt requested by OVF2A is disabled (Initial value)
1	OVI2A interrupt requested by OVF2A is enabled

- Bit 7—Input Capture/Compare-Match Interrupt Enable 2H (IME2H): Enables or disables interrupt requests by IMF2H in TSR2A when IMF2H is set to 1.

Bit 7: IME2H	Description
0	IMI2H interrupt requested by IMF2H is disabled (Initial value)
1	IMI2H interrupt requested by IMF2H is enabled

- Bit 6—Input Capture/Compare-Match Interrupt Enable 2G (IME2G): Enables or disables interrupt requests by IMF2G in TSR2A when IMF2G is set to 1.

Bit 6: IME2G	Description
0	IMI2G interrupt requested by IMF2G is disabled (Initial value)
1	IMI2G interrupt requested by IMF2G is enabled

- Bit 5—Input Capture/Compare-Match Interrupt Enable 2F (IME2F): Enables or disables interrupt requests by IMF2F in TSR2A when IMF2F is set to 1.

Bit 5: IME2F	Description
0	IMI2F interrupt requested by IMF2F is disabled (Initial value)
1	IMI2F interrupt requested by IMF2F is enabled

- Bit 4—Input Capture/Compare-Match Interrupt Enable 2E (IME2E): Enables or disables interrupt requests by IMF2E in TSR2A when IMF2E is set to 1.

Bit 4: IME2E	Description
0	IMI2E interrupt requested by IMF2E is disabled (Initial value)
1	IMI2E interrupt requested by IMF2E is enabled

- Bit 3—Input Capture/Compare-Match Interrupt Enable 2D (IME2D): Enables or disables interrupt requests by IMF2D in TSR2A when IMF2D is set to 1.

Bit 3: IME2D	Description
0	IMI2D interrupt requested by IMF2D is disabled (Initial value)
1	IMI2D interrupt requested by IMF2D is enabled

- Bit 2—Input Capture/Compare-Match Interrupt Enable 2C (IME2C): Enables or disables interrupt requests by IMF2C in TSR2A when IMF2C is set to 1.

Bit 2: IME2C	Description
0	IMI2C interrupt requested by IMF2C is disabled (Initial value)
1	IMI2C interrupt requested by IMF2C is enabled

- Bit 1—Input Capture/Compare-Match Interrupt Enable 2B (IME2B): Enables or disables interrupt requests by IMF2B in TSR2A when IMF2B is set to 1.

Bit 1: IME2B	Description
0	IMI2B interrupt requested by IMF2B is disabled (Initial value)
1	IMI2B interrupt requested by IMF2B is enabled

- Bit 0—Input Capture/Compare-Match Interrupt Enable 2A (IME2A): Enables or disables interrupt requests by IMF2A in TSR2A when IMF2A is set to 1.

Bit 0: IME2A	Description
0	IMI2A interrupt requested by IMF2A is disabled (Initial value)
1	IMI2A interrupt requested by IMF2A is enabled

**TIER2B:** TIER2B controls enabling/disabling of channel 2 compare-match and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVE2B
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit:	7	6	5	4	3	2	1	0
	CME2H	CME2G	CME2F	CME2E	CME2D	CME2C	CME2B	CME2A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Interrupt Enable 2B (OVE2B): Enables or disables interrupt requests by OVF2B in TSR2B when OVF2B is set to 1.

Bit 8: OVE2B	Description
0	OVI2B interrupt requested by OVF2B is disabled (Initial value)
1	OVI2B interrupt requested by OVF2B is enabled

- Bit 7—Compare-Match Interrupt Enable 2H (CME2H): Enables or disables interrupt requests by CMF2F in TSR2B when CMF2H is set to 1.

Bit 7: CME2H	Description
0	CMI2H interrupt requested by CMF2H is disabled (Initial value)
1	CMI2H interrupt requested by CMF2H is enabled

- Bit 6—Compare-Match Interrupt Enable 2G (CME2G): Enables or disables interrupt requests by CMF2G in TSR2B when CMF2G is set to 1.

Bit 6: CME2G	Description
0	CMI2G interrupt requested by CMF2G is disabled (Initial value)
1	CMI2G interrupt requested by CMF2G is enabled

- Bit 5—Compare-Match Interrupt Enable 2F (CME2F): Enables or disables interrupt requests by CMF2F in TSR2B when CMF2F is set to 1.

Bit 5: CME2F	Description
0	CMI2F interrupt requested by CMF2F is disabled (Initial value)
1	CMI2F interrupt requested by CMF2F is enabled

- Bit 4—Compare-Match Interrupt Enable 2E (CME2E): Enables or disables interrupt requests by CMF2E in TSR2B when CMF2E is set to 1.

Bit 4: CME2E	Description
0	CMI2E interrupt requested by CMF2E is disabled (Initial value)
1	CMI2E interrupt requested by CMF2E is enabled

- Bit 3—Compare-Match Interrupt Enable 2D (CME2D): Enables or disables interrupt requests by CMF2D in TSR2B when CMF2D is set to 1.

Bit 3: CME2D	Description
0	CMI2D interrupt requested by CMF2D is disabled (Initial value)
1	CMI2D interrupt requested by CMF2D is enabled

- Bit 2—Compare-Match Interrupt Enable 2C (CME2C): Enables or disables interrupt requests by CMF2C in TSR2B when CMF2C is set to 1.

Bit 2: CME2C	Description
0	CMI2C interrupt requested by CMF2C is disabled (Initial value)
1	CMI2C interrupt requested by CMF2C is enabled

- Bit 1—Compare-Match Interrupt Enable 2B (CME2BB): Enables or disables interrupt requests by CMF2B in TSR2B when CMF2B is set to 1.

Bit 1: CME2B	Description
0	CMI2B interrupt requested by CMF2B is disabled (Initial value)
1	CMI2B interrupt requested by CMF2B is enabled

- Bit 0—Compare-Match Interrupt Enable 2A (CME2A): Enables or disables interrupt requests by CMF2A in TSR2B when CMF2A is set to 1.

Bit 0: CME2A	Description
0	CMI2A interrupt requested by CMF2A is disabled (Initial value)
1	CMI2A interrupt requested by CMF2A is enabled

### Timer Interrupt Enable Register 3 (TIER3)

TIER3 controls enabling/disabling of channel 3 to 5 input capture, compare-match, and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	OVE5	IME5D	IME5C	IME5B	IME5A	OVE4	IME4D
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	IME4C	IME4B	IME4A	OVE3	IME3D	IME3C	IME3B	IME3A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—Overflow Interrupt Enable 5 (OVE5): Enables or disables interrupt requests by OVF5 in TSR3 when OVF5 is set to 1.

Bit 14: OVE5	Description
0	OVI5 interrupt requested by OVF5 is disabled (Initial value)
1	OVI5 interrupt requested by OVF5 is enabled



- Bit 13—Input Capture/Compare-Match Interrupt Enable 5D (IME5D): Enables or disables interrupt requests by IMF5D in TSR3 when IMF5D is set to 1.

Bit 13: IME5D	Description
0	IMI5D interrupt requested by IMF5D is disabled (Initial value)
1	IMI5D interrupt requested by IMF5D is enabled

- Bit 12—Input Capture/Compare-Match Interrupt Enable 5C (IME5C): Enables or disables interrupt requests by IMF5C in TSR3 when IMF5C is set to 1.

Bit 12: IME5C	Description
0	IMI5C interrupt requested by IMF5C is disabled (Initial value)
1	IMI5C interrupt requested by IMF5C is enabled

- Bit 11—Input Capture/Compare-Match Interrupt Enable 5B (IME5B): Enables or disables interrupt requests by IMF5B in TSR3 when IMF5B is set to 1.

Bit 11: IME5B	Description
0	IMI5B interrupt requested by IMF5B is disabled (Initial value)
1	IMI5B interrupt requested by IMF5B is enabled

- Bit 10—Input Capture/Compare-Match Interrupt Enable 5A (IME5A): Enables or disables interrupt requests by IMF5A in TSR3 when IMF5A is set to 1.

Bit 10: IME5A	Description
0	IMI5A interrupt requested by IMF5A is disabled (Initial value)
1	IMI5A interrupt requested by IMF5A is enabled

- Bit 9—Overflow Interrupt Enable 4 (OVE4): Enables or disables interrupt requests by OVF4 in TSR3 when OVF4 is set to 1.

Bit 9: OVE4	Description
0	OVI4 interrupt requested by OVF4 is disabled (Initial value)
1	OVI4 interrupt requested by OVF4 is enabled

- Bit 8—Input Capture/Compare-Match Interrupt Enable 4D (IME4D): Enables or disables interrupt requests by IMF4D in TSR3 when IMF4D is set to 1.

Bit 8: IME4D	Description
0	IMI4D interrupt requested by IMF4D is disabled (Initial value)
1	IMI4D interrupt requested by IMF4D is enabled

- Bit 7—Input Capture/Compare-Match Interrupt Enable 4C (IME4C): Enables or disables interrupt requests by IMF4C in TSR3 when IMF4C is set to 1.

Bit 7: IME4C	Description
0	IMI4C interrupt requested by IMF4C is disabled (Initial value)
1	IMI4C interrupt requested by IMF4C is enabled

- Bit 6—Input Capture/Compare-Match Interrupt Enable 4B (IME4B): Enables or disables interrupt requests by IMF4B in TSR3 when IMF4B is set to 1.

Bit 6: IME4B	Description
0	IMI4B interrupt requested by IMF4B is disabled (Initial value)
1	IMI4B interrupt requested by IMF4B is enabled

- Bit 5—Input Capture/Compare-Match Interrupt Enable 4A (IME4A): Enables or disables interrupt requests by IMF4A in TSR3 when IMF4A is set to 1.

Bit 5: IME4A	Description
0	IMI4A interrupt requested by IMF4A is disabled (Initial value)
1	IMI4A interrupt requested by IMF4A is enabled

- Bit 4—Overflow Interrupt Enable 3 (OVE3): Enables or disables interrupt requests by OVF3 in TSR3 when OVF3 is set to 1.

Bit 4: OVE3	Description
0	OVI3 interrupt requested by OVF3 is disabled (Initial value)
1	OVI3 interrupt requested by OVF3 is enabled

- Bit 3—Input Capture/Compare-Match Interrupt Enable 3D (IME3D): Enables or disables interrupt requests by IMF3D in TSR3 when IMF3D is set to 1.

Bit 3: IME3D	Description
0	IMI3D interrupt requested by IMF3D is disabled (Initial value)
1	IMI3D interrupt requested by IMF3D is enabled

- Bit 2—Input Capture/Compare-Match Interrupt Enable 3C (IME3C): Enables or disables interrupt requests by IMF3C in TSR3 when IMF3C is set to 1.

Bit 2: IME3C	Description
0	IMI3C interrupt requested by IMF3C is disabled (Initial value)
1	IMI3C interrupt requested by IMF3C is enabled

- Bit 1—Input Capture/Compare-Match Interrupt Enable 3B (IME3B): Enables or disables interrupt requests by IMF3B in TSR3 when IMF3B is set to 1.

Bit 1: IME3B	Description
0	IMI3B interrupt requested by IMF3B is disabled (Initial value)
1	IMI3B interrupt requested by IMF3B is enabled

- Bit 0—Input Capture/Compare-Match Interrupt Enable 3A (IME3A): Enables or disables interrupt requests by IMF3A in TSR3 when IMF3A is set to 1.

Bit 0: IME3A	Description
0	IMI3A interrupt requested by IMF3A is disabled (Initial value)
1	IMI3A interrupt requested by IMF3A is enabled

## Timer Interrupt Enable Registers 6 and 7 (TIER6, TIER7)

TIER6 and TIER7 control enabling/disabling of channel 6 and 7 cycle register compare interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	CMExD	CMExC	CMExB	CMExA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

x = 6 or 7

- Bits 15 to 4—Reserved: These bits always read 0. The write value should always be 0.
- Bit 3—Cycle Register Compare-Match Interrupt Enable 6D/7D (CME6D/CME7D): Enables or disables interrupt requests by CMFxD in TSR6 or TSR7 when CMFxD is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 3: CMExD	Description
0	CMIxD interrupt requested by CMFxD is disabled (Initial value)
1	CMIxD interrupt requested by CMFxD is enabled

x = 6 or 7

- Bit 2—Cycle Register Compare-Match Interrupt Enable 6C/7C (CME6C/CME7C): Enables or disables interrupt requests by CMFxC in TSR6 or TSR7 when CMFxC is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 2: CMExC	Description
0	CMIxC interrupt requested by CMFxC is disabled (Initial value)
1	CMIxC interrupt requested by CMFxC is enabled

x = 6 or 7

- Bit 1—Cycle Register Compare-Match Interrupt Enable 6B/7B (CME6B/CME7B): Enables or disables interrupt requests by CMFxB in TSR6 or TSR7 when CMFxB is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 1: CMExB	Description
0	CMlxB interrupt requested by CMFxB is disabled (Initial value)
1	CMlxB interrupt requested by CMFxB is enabled

x = 6 or 7

- Bit 0—Cycle Register Compare-Match Interrupt Enable 6A/7A (CME6A/CME7A): Enables or disables interrupt requests by CMFxA in TSR6 or TSR7 when CMFxA is set to 1. Setting the DMAC while interrupt requests are enabled allows the DMAC to be activated by an interrupt request.

Bit 0: CMExA	Description
0	CMlxA interrupt requested by CMFxA is disabled (Initial value)
1	CMlxA interrupt requested by CMFxA is enabled

x = 6 or 7

### Timer Interrupt Enable Register 8 (TIER8)

TIER8 controls enabling/disabling of channel 8 one-shot pulse interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	OSE8P	OSE8O	OSE8N	OSE8M	OSE8L	OSE8K	OSE8J	OSE8I
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	OSE8H	OSE8G	OSE8F	OSE8E	OSE8D	OSE8C	OSE8B	OSE8A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 15—One-Shot Pulse Interrupt Enable 8P (OSE8P): Enables or disables interrupt requests by OSF8P in TSR8 when OSF8P is set to 1.

Bit 15: OSE8P	Description
0	OSI8P interrupt requested by OSF8P is disabled (Initial value)
1	OSI8P interrupt requested by OSF8P is enabled

- Bit 14—One-Shot Pulse Interrupt Enable 8O (OSE8O): Enables or disables interrupt requests by OSF8O in TSR8 when OSF8O is set to 1.

Bit 14: OSE8O	Description
0	OSI8O interrupt requested by OSF8O is disabled (Initial value)
1	OSI8O interrupt requested by OSF8O is enabled

- Bit 13—One-Shot Pulse Interrupt Enable 8N (OSE8N): Enables or disables interrupt requests by OSF8N in TSR8 when OSF8N is set to 1.

Bit 13: OSE8N	Description
0	OSI8N interrupt requested by OSF8N is disabled (Initial value)
1	OSI8N interrupt requested by OSF8N is enabled

- Bit 12—One-Shot Pulse Interrupt Enable 8M (OSE8M): Enables or disables interrupt requests by OSF8M in TSR8 when OSF8M is set to 1.

Bit 12: OSE8M	Description
0	OSI8M interrupt requested by OSF8M is disabled (Initial value)
1	OSI8M interrupt requested by OSF8M is enabled

- Bit 11—One-Shot Pulse Interrupt Enable 8L (OSE8L): Enables or disables interrupt requests by OSF8L in TSR8 when OSF8L is set to 1.

Bit 11: OSE8L	Description
0	OSI8L interrupt requested by OSF8L is disabled (Initial value)
1	OSI8L interrupt requested by OSF8L is enabled

- Bit 10—One-Shot Pulse Interrupt Enable 8K (OSE8K): Enables or disables interrupt requests by OSF8K in TSR8 when OSF8K is set to 1.

Bit 10: OSE8K	Description
0	OSI8K interrupt requested by OSF8K is disabled (Initial value)
1	OSI8K interrupt requested by OSF8K is enabled

- Bit 9—One-Shot Pulse Interrupt Enable 8J (OSE8J): Enables or disables interrupt requests by OSF8J in TSR8 when OSF8J is set to 1.

Bit 9: OSE8J	Description
0	OSI8J interrupt requested by OSF8J is disabled (Initial value)
1	OSI8J interrupt requested by OSF8J is enabled

- Bit 8—One-Shot Pulse Interrupt Enable 8I (OSE8I): Enables or disables interrupt requests by OSF8I in TSR8 when OSF8I is set to 1.

Bit 8: OSE8I	Description
0	OSI8I interrupt requested by OSF8I is disabled (Initial value)
1	OSI8I interrupt requested by OSF8I is enabled

- Bit 7—One-Shot Pulse Interrupt Enable 8H (OSE8H): Enables or disables interrupt requests by OSF8H in TSR8 when OSF8H is set to 1.

Bit 7: OSE8H	Description
0	OSI8H interrupt requested by OSF8H is disabled (Initial value)
1	OSI8H interrupt requested by OSF8H is enabled

- Bit 6—One-Shot Pulse Interrupt Enable 8G (OSE8G): Enables or disables interrupt requests by OSF8G in TSR8 when OSF8G is set to 1.

Bit 6: OSE8G	Description
0	OSI8G interrupt requested by OSF8G is disabled (Initial value)
1	OSI8G interrupt requested by OSF8G is enabled

- Bit 5—One-Shot Pulse Interrupt Enable 8F (OSE8F): Enables or disables interrupt requests by OSF8F in TSR8 when OSF8F is set to 1.

Bit 5: OSE8F	Description
0	OSI8F interrupt requested by OSF8F is disabled (Initial value)
1	OSI8F interrupt requested by OSF8F is enabled

- Bit 4—One-Shot Pulse Interrupt Enable 8E (OSE8E): Enables or disables interrupt requests by OSF8E in TSR8 when OSF8E is set to 1.

Bit 4: OSE8E	Description
0	OSI8E interrupt requested by OSF8E is disabled (Initial value)
1	OSI8E interrupt requested by OSF8E is enabled

- Bit 3—One-Shot Pulse Interrupt Enable 8D (OSE8D): Enables or disables interrupt requests by OSF8D in TSR8 when OSF8D is set to 1.

Bit 3: OSE8D	Description
0	OSI8D interrupt requested by OSF8D is disabled (Initial value)
1	OSI8D interrupt requested by OSF8D is enabled

- Bit 2—One-Shot Pulse Interrupt Enable 8C (OSE8C): Enables or disables interrupt requests by OSF8C in TSR8 when OSF8C is set to 1.

Bit 2: OSE8C	Description
0	OSI8C interrupt requested by OSF8C is disabled (Initial value)
1	OSI8C interrupt requested by OSF8C is enabled

- Bit 1—One-Shot Pulse Interrupt Enable 8B (OSE8B): Enables or disables interrupt requests by OSF8B in TSR8 when OSF8B is set to 1.

Bit 1: OSE8B	Description
0	OSI8B interrupt requested by OSF8B is disabled (Initial value)
1	OSI8B interrupt requested by OSF8B is enabled



- Bit 0—One-Shot Pulse Interrupt Enable 8A (OSE8A): Enables or disables interrupt requests by OSF8A in TSR8 when OSF8A is set to 1.

Bit 0: OSE8A	Description
0	OSI8A interrupt requested by OSF8A is disabled (Initial value)
1	OSI8A interrupt requested by OSF8A is enabled

### Timer Interrupt Enable Register 9 (TIER9)

TIER9 controls enabling/disabling of channel 9 event counter compare-match interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	CME9F	CME9E	CME9D	CME9C	CME9B	CME9A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 6—Reserved: These bits always read 0. The write value should always be 0.
- Bit 5—Compare-Match Interrupt Enable 9F (CME9F): Enables or disables interrupt requests by CMF9F in TSR9 when CMF9F is set to 1.

Bit 5: CME9F	Description
0	CMI9F interrupt requested by CMF9F is disabled (Initial value)
1	CMI9F interrupt requested by CMF9F is enabled

- Bit 4—Compare-Match Interrupt Enable 9E (CME9E): Enables or disables interrupt requests by CMF9E in TSR9 when CMF9E is set to 1.

Bit 4: CME9E	Description
0	CMI9E interrupt requested by CMF9E is disabled (Initial value)
1	CMI9E interrupt requested by CMF9E is enabled

- Bit 3—Compare-Match Interrupt Enable 9D (CME9D): Enables or disables interrupt requests by CMF9D in TSR9 when CMF9D is set to 1.

Bit 3: CME9D	Description
0	CMI9D interrupt requested by CMF9D is disabled (Initial value)
1	CMI9D interrupt requested by CMF9D is enabled

- Bit 2—Compare-Match Interrupt Enable 9C (CME9C): Enables or disables interrupt requests by CMF9C in TSR9 when CMF9C is set to 1.

Bit 2: CME9C	Description
0	CMI9C interrupt requested by CMF9C is disabled (Initial value)
1	CMI9C interrupt requested by CMF9C is enabled

- Bit 1—Compare-Match Interrupt Enable 9B (CME9B): Enables or disables interrupt requests by CMF9B in TSR9 when CMF9B is set to 1.

Bit 1: CME9B	Description
0	CMI9B interrupt requested by CMF9B is disabled (Initial value)
1	CMI9B interrupt requested by CMF9B is enabled

- Bit 0—Compare-Match Interrupt Enable 9A (CME9A): Enables or disables interrupt requests by CMF9A in TSR9 when CMF9A is set to 1.

Bit 0: CME9A	Description
0	CMI9A interrupt requested by CMF9A is disabled (Initial value)
1	CMI9A interrupt requested by CMF9A is enabled

## Timer Interrupt Enable Register 11 (TIER11)

TIER11 controls enabling/disabling of channel 11 compare-match and overflow interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	OVE11
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IME11B	IME11A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—Overflow Interrupt Enable 11 (OVE11): Enables or disables interrupt requests by OVF11 in TSR11 when OVF11 is set to 1.

Bit 8: OVE11	Description
0	OVI11 interrupt requested by OVF11 is disabled (Initial value)
1	OVI11 interrupt requested by OVF11 is enabled

- Bits 7 to 2—Reserved: These bits always read 0. The write value should always be 0.
- Bit 1—Compare-Match Interrupt Enable 11B (IME11B): Enables or disables interrupt requests by IMF11B in TSR11 when IMF11B is set to 1.

Bit 1: IME11B	Description
0	IMI11B interrupt requested by IMF11B is disabled (Initial value)
1	IMI11B interrupt requested by IMF11B is enabled

- Bit 0—Compare-Match Interrupt Enable 11A (IME11A): Enables or disables interrupt requests by IMF11A in TSR11 when IMF11A is set to 1.

Bit 0: IME11A	Description
0	IMI11A interrupt requested by IMF11A is disabled (Initial value)
1	IMI11A interrupt requested by IMF11A is enabled

## 10.2.7 Interval Interrupt Request Registers (ITVRR)

The interval interrupt request registers (ITVRR) are 8-bit registers. The ATU-II has three ITVRR registers in channel 0.

Channel	Abbreviation	Function
0	ITVRR1	TCNT0 bit 6 to 9 interval interrupt generation
	ITVRR2A	TCNT0 bit 10 to 13 interval interrupt generation and A/D0 converter activation
	ITVRR2B	TCNT0 bit 10 to 13 interval interrupt generation and A/D1 converter activation

### Interval Interrupt Request Register 1 (ITVRR1)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	ITVE9	ITVE8	ITVE7	ITVE6
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ITVRR1 is an 8-bit readable/writable register that detects the rise of bits corresponding to the channel 0 free-running counter (TCNT0) and requests cyclic interrupt.

ITVRR1 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7 to 4—Reserved: These bits always read 0. The write value should always be 0.
- Bit 3—Interval Interrupt Bit 9 (ITVE9): INTC interval interrupt setting bit corresponding to bit 9 in TCNT0. The rise of bit 9 in TCNT0 is ANDed with ITVE9, the result is stored in IIF1 in TSR0, and an interrupt request is sent to the CPU.

Bit 3: ITVE9	Description
0	Interrupt request (ITV1) by rise of TCNT0 bit 9 is disabled (Initial value)
1	Interrupt request (ITV1) by rise of TCNT0 bit 9 is enabled

- Bit 2—Interval Interrupt Bit 8 (ITVE8): INTC interval interrupt setting bit corresponding to bit 8 in TCNT0. The rise of bit 8 in TCNT0 is ANDed with ITVE8, the result is stored in IIF1 in TSR0, and an interrupt request is sent to the CPU.

Bit 2: ITVE8	Description
0	Interrupt request (ITV1) by rise of TCNT0 bit 8 is disabled (Initial value)
1	Interrupt request (ITV1) by rise of TCNT0 bit 8 is enabled

- Bit 1—Interval Interrupt Bit 7 (ITVE7): INTC interval interrupt setting bit corresponding to bit 7 in TCNT0. The rise of bit 7 in TCNT0 is ANDed with ITVE7, the result is stored in IIF1 in TSR0, and an interrupt request is sent to the CPU.

Bit 1: ITVE7	Description
0	Interrupt request (ITV1) by rise of TCNT0 bit 7 is disabled (Initial value)
1	Interrupt request (ITV1) by rise of TCNT0 bit 7 is enabled

- Bit 0—Interval Interrupt Bit 6 (ITVE6): INTC interval interrupt setting bit corresponding to bit 6 in TCNT0. The rise of bit 6 in TCNT0 is ANDed with ITVE6, the result is stored in IIF1 in TSR0, and an interrupt request is sent to the CPU.

Bit 0: ITVE6	Description
0	Interrupt request (ITV1) by rise of TCNT0 bit 6 is disabled (Initial value)
1	Interrupt request (ITV1) by rise of TCNT0 bit 6 is enabled

### Interval Interrupt Request Registers 2A and 2B (ITVRR2A, ITVRR2B)

Bit:	7	6	5	4	3	2	1	0
	ITVA13x	ITVA12x	ITVA11x	ITVA10x	ITVE13x	ITVE12x	ITVE11x	ITVE10x
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

x = A or B

- Bit 7—A/D0 / A/D1 Converter Interval Activation Bit 13A/13B (ITVA13A/ITVA13B): A/D0 or A/D1 (ITVRR2A: A/D0; ITVRR2B: A/D1) converter activation setting bit corresponding to bit 13 in TCNT0. The rise of bit 13 in TCNT0 is ANDed with ITVA13x, and the result is output to the A/D0 or A/D1 converter as an activation signal.

Bit 7: ITVA13x	Description
0	A/D0 or A/D1 converter activation by rise of TCNT0 bit 13 is disabled (Initial value)
1	A/D0 or A/D1 converter activation by rise of TCNT0 bit 13 is enabled

x = A or B

- Bit 6—A/D0 / A/D1 Converter Interval Activation Bit 12A/12B (ITVA12A/ITVA12B): A/D0 or A/D1 (ITVRR2A: A/D0; ITVRR2B: A/D1) converter activation setting bit corresponding to bit 12 in TCNT0. The rise of bit 12 in TCNT0 is ANDed with ITVA12x, and the result is output to the A/D0 or A/D1 converter as an activation signal.

Bit 6: ITVA12x	Description
0	A/D0 or A/D1 converter activation by rise of TCNT0 bit 12 is disabled (Initial value)
1	A/D0 or A/D1 converter activation by rise of TCNT0 bit 12 is enabled

x = A or B

- Bit 5—A/D0 / A/D1 Converter Interval Activation Bit 11A/11B (ITVA11A/ITVA11B): A/D0 or A/D1 (ITVRR2A: A/D0; ITVRR2B: A/D1) converter activation setting bit corresponding to bit 11 in TCNT0. The rise of bit 11 in TCNT0 is ANDed with ITVA11x, and the result is output to the A/D0 or A/D1 converter as an activation signal.

Bit 5: ITVA11x	Description
0	A/D0 or A/D1 converter activation by rise of TCNT0 bit 11 is disabled (Initial value)
1	A/D0 or A/D1 converter activation by rise of TCNT0 bit 11 is enabled

x = A or B

- Bit 4—A/D0 / A/D1 Converter Interval Activation Bit 10A/10B (ITVA10A/ITVA10B): A/D0 or A/D1 (ITVRR2A: A/D0; ITVRR2B: A/D1) converter activation setting bit corresponding to bit 10 in TCNT0. The rise of bit 10 in TCNT0 is ANDed with ITVA10x, and the result is output to the A/D0 or A/D1 converter as an activation signal.

Bit 4: ITVA10x	Description
0	A/D0 or A/D1 converter activation by rise of TCNT0 bit 10 is disabled (Initial value)
1	A/D0 or A/D1 converter activation by rise of TCNT0 bit 10 is enabled

x = A or B

- Bit 3—Interval Interrupt Bit 13A/13B (ITVE13A/ITVE13B): INTC interval interrupt setting bit corresponding to bit 13 in TCNT0. The rise of bit 13 in TCNT0 is ANDed with ITVE13x, the result is stored in IIF2x in TSR0, and an interrupt request is sent to the CPU.

Bit 3: ITVE13x	Description
0	Interrupt request (ITV2x) by rise of TCNT0 bit 13 is disabled (Initial value)
1	Interrupt request (ITV2x) by rise of TCNT0 bit 13 is enabled

x = A or B

- Bit 2—Interval Interrupt Bit 12A/12B (ITVE12A/ITVE12B): INTC interval interrupt setting bit corresponding to bit 12 in TCNT0. The rise of bit 12 in TCNT0 is ANDed with ITVE12x, the result is stored in IIF2x in TSR0, and an interrupt request is sent to the CPU.

Bit 2: ITVE12x	Description
0	Interrupt request (ITV2x) by rise of TCNT0 bit 12 is disabled (Initial value)
1	Interrupt request (ITV2x) by rise of TCNT0 bit 12 is enabled

x = A or B

- Bit 1—Interval Interrupt Bit 11A/11B (ITVE11A/ITVE11B): INTC interval interrupt setting bit corresponding to bit 11 in TCNT0. The rise of bit 11 in TCNT0 is ANDed with ITVE11x, the result is stored in IIF2x in TSR0, and an interrupt request is sent to the CPU.

Bit 1: ITVE11x	Description
0	Interrupt request (ITV2x) by rise of TCNT0 bit 11 is disabled (Initial value)
1	Interrupt request (ITV2x) by rise of TCNT0 bit 11 is enabled

x = A or B

- Bit 0—Interval Interrupt Bit 10 (ITVE10): INTC interval interrupt setting bit corresponding to bit 10 in TCNT0. The rise of bit 10 in TCNT0 is ANDed with ITVE10x, the result is stored in IIF2x in TSR0, and an interrupt request is sent to the CPU.

Bit 0: ITVE10x	Description
0	Interrupt request (ITV2x) by rise of TCNT0 bit 10 is disabled (Initial value)
1	Interrupt request (ITV2x) by rise of TCNT0 bit 10 is enabled

x = A or B

For details, see section 10.3.7, Interval Timer Functions.

## 10.2.8 Trigger Mode Register (TRGMDR)

The trigger mode register (TRGMDR) is an 8-bit register. The ATU-II has one TRGMDR register.

Bit:	7	6	5	4	3	2	1	0
	TRGMD	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R

TRGMDR is an 8-bit readable/writable register that selects whether a channel 1 compare-match is used as a channel 8 one-shot pulse start trigger or as a one-shot pulse terminate trigger when channel 1 and channel 8 are used in combination.

TRGMDR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Trigger Mode Selection Register (TRGMD): Selects the channel 8 one-shot pulse start trigger/one-shot pulse terminate trigger setting.

Bit 7: TRGMD	Description
0	One-shot pulse start trigger (TCNT1B = OCR1) (Initial value) One-shot pulse terminate trigger (TCNT1A = GR1A to GR1H)
1	One-shot pulse start trigger (TCNT1A = GR1A to GR1H) One-shot pulse terminate trigger (TCNT1B = OCR1)

- Bits 6 to 0—Reserved: These bits always read 0. The write value should always be 0.

## 10.2.9 Timer Mode Register (TMDR)

The timer mode register (TMDR) is an 8-bit register. The ATU-II has one TDR register.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	T5PWM	T4PWM	T3PWM
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

TMDR is an 8-bit readable/writable register that specifies whether channels 3 to 5 are used in input capture/output compare mode or PWM mode.

TMDR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.



- Bits 7 to 3—Reserved: These bits always read 0. The write value should always be 0.
- Bit 2—PWM Mode 5 (T5PWM): Selects whether channel 5 operates in input capture/output compare mode or PWM mode.

Bit 2: T5PWM	Description
0	Channel 5 operates in input capture/output compare mode (Initial value)
1	Channel 5 operates in PWM mode

When bit T5PWM is set to 1 to select PWM mode, pins TIO5A to TIO5C become PWM output pins, general register 5D (GR5D) functions as a cycle register, and general registers 5A to 5C (GR5A to GR5C) function as duty registers. Settings in the timer I/O control registers (TIOR5A, TIOR5B) are invalid, and general registers 5A to 5D (GR5A to GR5D) can be written to. Do not use the TIO5D pin as a timer output.

- Bit 1—PWM Mode 4 (T4PWM): Selects whether channel 4 operates in input capture/output compare mode or PWM mode.

Bit 1: T4PWM	Description
0	Channel 4 operates in input capture/output compare mode (Initial value)
1	Channel 4 operates in PWM mode

When bit T4PWM is set to 1 to select PWM mode, pins TIO4A to TIO4C become PWM output pins, general register 4D (GR4D) functions as a cycle register, and general registers 4A to 4C (GR4A to GR4C) function as duty registers. Settings in the timer I/O control registers (TIOR4A, TIOR4B) are invalid, and general registers 4A to 4D (GR4A to GR4D) can be written to. Do not use the TIO4D pin as a timer output.

- Bit 0—PWM Mode 3 (T3PWM): Selects whether channel 3 operates in input capture/output compare mode or PWM mode.

Bit 0: T3PWM	Description
0	Channel 3 operates in input capture/output compare mode (Initial value)
1	Channel 3 operates in PWM mode

When bit T3PWM is set to 1 to select PWM mode, pins TIO3A to TIO3C become PWM output pins, general register 3D (GR3D) functions as a cycle register, and general registers 3A to 3C (GR3A to GR3C) function as duty registers. Settings in the timer I/O control registers (TIOR3A, TIOR3B) are invalid, and general registers 3A to 3D (GR3A to GR3D) can be written to. Do not use the TIO3D pin as a timer output.

## 10.2.10 PWM Mode Register (PMDR)

The PWM mode register (PMDR) is an 8-bit register. The ATU-II has one PMDR register.

Bit:	7	6	5	4	3	2	1	0
	DTSEL D	DTSEL C	DTSEL B	DTSEL A	CNTSEL D	CNTSEL C	CNTSEL B	CNTSEL A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMDR is an 8-bit readable/writable register that selects whether channel 6 PWM output is set to on-duty/off-duty, or to non-complementary PWM mode/complementary PWM mode.

PMDR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 7—Duty Selection Register D (DTSEL D): Selects whether channel 6D TO6D output PWM is set to on-duty or to off-duty.

Bit 7: DTSEL D	Description
0	TO6D PWM output is on-duty (Initial value)
1	TO6D PWM output is off-duty

- Bit 6—Duty Selection Register C (DTSEL C): Selects whether channel 6C TO6C output PWM is set to on-duty or to off-duty.

Bit 6: DTSEL C	Description
0	TO6C PWM output is on-duty (Initial value)
1	TO6C PWM output is off-duty

- Bit 5—Duty Selection Register B (DTSEL B): Selects whether channel 6B TO6B output PWM is set to on-duty or to off-duty.

Bit 5: DTSEL B	Description
0	TO6B PWM output is on-duty (Initial value)
1	TO6B PWM output is off-duty

- Bit 4—Duty Selection Register A (DTSELA): Selects whether channel 6A TO6A output PWM is set to on-duty or to off-duty.

Bit 4: DTSELA	Description
0	TO6A PWM output is on-duty (Initial value)
1	TO6A PWM output is off-duty

- Bit 3—Counter Selection Register D (CNTSELD): Selects whether channel 6D PWM is set to non-complementary PWM mode or to complementary PWM mode.

Bit 3: CNTSELD	Description
0	TCNT6D is set to non-complementary PWM mode (Initial value)
1	TCNT6D is set to complementary PWM mode

- Bit 2—Counter Selection Register C (CNTSELC): Selects whether channel 6C PWM is set to non-complementary PWM mode or to complementary PWM mode.

Bit 2: CNTSELC	Description
0	TCNT6C is set to non-complementary PWM mode (Initial value)
1	TCNT6C is set to complementary PWM mode

- Bit 1—Counter Selection Register B (CNTSELB): Selects whether channel 6B PWM is set to non-complementary PWM mode or to complementary PWM mode.

Bit 1: CNTSELB	Description
0	TCNT6B is set to non-complementary PWM mode (Initial value)
1	TCNT6B is set to complementary PWM mode

- Bit 0—Counter Selection Register A (CNTSELA): Selects whether channel 6A PWM is set to non-complementary PWM mode or to complementary PWM mode.

Bit 0: CNTSELA	Description
0	TCNT6A is set to non-complementary PWM mode (Initial value)
1	TCNT6A is set to complementary PWM mode

### 10.2.11 Down-Count Start Register (DSTR)

The down-count start register (DSTR) is a 16-bit register. The ATU-II has one DSTR register in channel 8.

Bit:	15	14	13	12	11	10	9	8
	DST8P	DST8O	DST8N	DST8M	DST8L	DST8K	DST8J	DST8I
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Bit:	7	6	5	4	3	2	1	0
	DST8H	DST8G	DST8F	DST8E	DST8D	DST8C	DST8B	DST8A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Note: \* Only 1 can be written.

DSTR is a 16-bit readable/writable register that starts the channel 8 down-counter (DCNT).

When the one-shot pulse function is used, a value of 1 can be set in a DST8x bit at any time by the user program, except when the corresponding DCNT8x value is H'0000. The DST8x bits are cleared to 0 automatically when the DCNT value overflows.

When the offset one-shot pulse function is used, DST8x is automatically set to 1 (except when the DCNT8x value is H'0000) when a compare-match occurs between the channel 1 or 2 free-running counter (TCNT) and a general register (GR) or the output compare register (OCR1) while the corresponding timer connection register (TCNR) bit is set to 1. As regards DST8I to DST8P, if the RL DEN bit in the reload enable register (RLDENR) is set to 1 and the reload register (RLDR8) value is not H'0000, a reload is performed into the corresponding DCNT8x, and the DST8x bit is set to 1. DST8x is automatically cleared to 0 when the DCNT8x value underflows, or by input of a channel 1 or 2 one-shot terminate trigger signal set in the trigger mode register (TRGMDR) while the corresponding one-shot pulse terminate register (OTR) bit is set to 1, whichever occurs first.

DCNT8x is cleared to H'0000 when underflow occurs.

DSTR is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

For details, see sections 10.3.5, One-Shot Pulse Function, and 10.3.6, Offset One-Shot Pulse Function and Output Cutoff Function.

- Bit 15—Down-Count Start 8P (DST8P): Starts down-counter 8P (DCNT8P).

Bit 15: DST8P	Description
0	DCNT8P is halted (Initial value) [Clearing conditions] When the DCNT8P value underflows, or on channel 2 (GR2H) compare-match
1	DCNT8P counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8P ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2H compare-match (DCNT8P ≠ H'0000 or reload possible) or by user program (DCNT8P ≠ H'0000)</li> </ul>

- Bit 14—Down-Count Start 8O (DST8O): Starts down-counter 8O (DCNT8O).

Bit 14: DST8O	Description
0	DCNT8O is halted (Initial value) [Clearing conditions] When the DCNT8O value underflows, or on channel 2 (GR2G) compare-match
1	DCNT8O counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8O ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2G compare-match (DCNT8O ≠ H'0000 or reload possible) or by user program (DCNT8O ≠ H'0000)</li> </ul>

- Bit 13—Down-Count Start 8N (DST8N): Starts down-counter 8N (DCNT8N).

Bit 13: DST8N	Description
0	DCNT8N is halted (Initial value) [Clearing conditions] When the DCNT8N value underflows, or on channel 2 (GR2F) compare-match
1	DCNT8N counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8N ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2F compare-match (DCNT8N ≠ H'0000 or reload possible) or by user program (DCNT8N ≠ H'0000)</li> </ul>

- Bit 12—Down-Count Start 8M (DST8M): Starts down-counter 8M (DCNT8M).

Bit 12: DST8M	Description
0	DCNT8M is halted (Initial value) [Clearing conditions] When the DCNT8M value underflows, or on channel 2 (GR2E) compare-match
1	DCNT8M counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8M ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2E compare-match (DCNT8M ≠ H'0000 or reload possible) or by user program (DCNT8M ≠ H'0000)</li> </ul>

- Bit 11—Down-Count Start 8L (DST8L): Starts down-counter 8L (DCNT8L).

Bit 11: DST8L	Description
0	DCNT8L is halted (Initial value) [Clearing conditions] When the DCNT8L value underflows, or on channel 2 (GR2D) compare-match
1	DCNT8L counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8L ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2D compare-match (DCNT8L ≠ H'0000 or reload possible) or by user program (DCNT8L ≠ H'0000)</li> </ul>

- Bit 10—Down-Count Start 8K (DST8K): Starts down-counter 8K (DCNT8K).

Bit 10: DST8K	Description
0	DCNT8K is halted (Initial value) [Clearing conditions] When the DCNT8K value underflows, or on channel 2 (GR2C) compare-match
1	DCNT8K counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8K ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2C compare-match (DCNT8K ≠ H'0000 or reload possible) or by user program (DCNT8K ≠ H'0000)</li> </ul>

- Bit 9—Down-Count Start 8J (DST8J): Starts down-counter 8J (DCNT8J).

Bit 9: DST8J	Description
0	DCNT8J is halted (Initial value) [Clearing conditions] When the DCNT8J value underflows, or on channel 2 (GR2B) compare-match
1	DCNT8J counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8J ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2B compare-match (DCNT8J ≠ H'0000 or reload possible) or by user program (DCNT8J ≠ H'0000)</li> </ul>

- Bit 8—Down-Count Start 8I (DST8I): Starts down-counter 8I (DCNT8I).

Bit 8: DST8I	Description
0	DCNT8I is halted (Initial value) [Clearing conditions] When the DCNT8I value underflows, or on channel 2 (GR2A) compare-match
1	DCNT8I counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8I ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR2A compare-match (DCNT8I ≠ H'0000 or reload possible) or by user program (DCNT8I ≠ H'0000)</li> </ul>

- Bit 7—Down-Count Start 8H (DST8H): Starts down-counter 8H (DCNT8H).

Bit 7: DST8H	Description
0	DCNT8H is halted (Initial value) [Clearing conditions] When the DCNT8H value underflows, or on channel 1 (GR1H or OCR1) compare-match
1	DCNT8H counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8H ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1H compare-match, or by user program (DCNT8H ≠ H'0000)</li> </ul>

- Bit 6—Down-Count Start 8G (DST8G): Starts down-counter 8G (DCNT8G).

Bit 6: DST8G	Description
0	DCNT8G is halted (Initial value) [Clearing conditions] When the DCNT8G value underflows, or on channel 1 (GR1G or OCR1) compare-match
1	DCNT8G counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8G ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1G compare-match, or by user program (DCNT8G ≠ H'0000)</li> </ul>

- Bit 5—Down-Count Start 8F (DST8F): Starts down-counter 8F (DCNT8F).

Bit 5: DST8F	Description
0	DCNT8F is halted (Initial value) [Clearing conditions] When the DCNT8F value underflows, or on channel 1 (GR1F or OCR1) compare-match
1	DCNT8F counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8F ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1F compare-match, or by user program (DCNT8F ≠ H'0000)</li> </ul>

- Bit 4—Down-Count Start 8E (DST8E): Starts down-counter 8E (DCNT8E).

Bit 4: DST8E	Description
0	DCNT8E is halted (Initial value) [Clearing conditions] When the DCNT8E value underflows, or on channel 1 (GR1E or OCR1) compare-match
1	DCNT8E counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8E ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1E compare-match, or by user program (DCNT8E ≠ H'0000)</li> </ul>



- Bit 3—Down-Count Start 8D (DST8D): Starts down-counter 8D (DCNT8D).

Bit 3: DST8D	Description
0	DCNT8D is halted (Initial value) [Clearing conditions] When the DCNT8D value underflows, or on channel 1 (GR1D or OCR1) compare-match
1	DCNT8D counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8D ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1D compare-match, or by user program (DCNT8D ≠ H'0000)</li> </ul>

- Bit 2—Down-Count Start 8C (DST8C): Starts down-counter 8C (DCNT8C).

Bit 2: DST8C	Description
0	DCNT8C is halted (Initial value) [Clearing conditions] When the DCNT8C value underflows, or on channel 1 (GR1C or OCR1) compare-match
1	DCNT8C counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8C ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1C compare-match, or by user program (DCNT8C ≠ H'0000)</li> </ul>

- Bit 1—Down-Count Start 8B (DST8B): Starts down-counter 8B (DCNT8B).

Bit 1: DST8B	Description
0	DCNT8B is halted (Initial value) [Clearing conditions] When the DCNT8B value underflows, or on channel 1 (GR1B or OCR1) compare-match
1	DCNT8B counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8B ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1B compare-match, or by user program (DCNT8B ≠ H'0000)</li> </ul>

- Bit 0—Down-Count Start 8A (DST8A): Starts down-counter 8A (DCNT8A).

Bit 0: DST8A	Description
0	DCNT8A is halted (Initial value) [Clearing conditions] When the DCNT8A value underflows, or on channel 1 (GR1A or OCR1) compare-match
1	DCNT8A counts [Setting conditions] <ul style="list-style-type: none"> <li>• One-shot pulse function: Set by user program (DCNT8A ≠ H'0000)</li> <li>• Offset one-shot pulse function: Set on OCR1 compare-match or GR1A compare-match, or by user program (DCNT8A ≠ H'0000)</li> </ul>

### 10.2.12 Timer Connection Register (TCNR)

The timer connection register (TCNR) is a 16-bit register. The ATU-II has one TCNR register in channel 8.

Bit:	15	14	13	12	11	10	9	8
	CN8P	CN8O	CN8N	CN8M	CN8L	CN8K	CN8J	CN8I
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	CN8H	CN8G	CN8F	CN8E	CN8D	CN8C	CN8B	CN8A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNR is a 16-bit readable/writable register that enables or disables connection between the channel 8 down-count start register (DSTR) and channel 1 and 2 compare-match signals (down-count start triggers). Channel 1 down-count start triggers A to H are channel 1 OCR1 compare-match signals or GR1x compare-match signals (set in TRGMDR). Channel 2 down-count start triggers A to H are channel 2 OCR2x compare-match signals. When GR1x compare-matches are used, set TIOR1A to TIOR1D to allow compare-matches.

TCNR is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

For details, see sections 10.3.5, One-Shot Pulse Function, and 10.3.6, Offset One-Shot Pulse Function and Output Cutoff Operation.

- Bit 15—Connection Flag 8P (CN8P): Enables or disables connection between DST8P and the channel 2 down-count start trigger.

Bit 15: CN8P	Description
0	Connection between DST8P and channel 2 down-count start trigger H is disabled (Initial value)
1	Connection between DST8P and channel 2 down-count start trigger H is enabled

- Bit 14—Connection Flag 8O (CN8O): Enables or disables connection between DST8O and the channel 2 down-count start trigger.

Bit 14: CN8O	Description
0	Connection between DST8O and channel 2 down-count start trigger G is disabled (Initial value)
1	Connection between DST8O and channel 2 down-count start trigger G is enabled

- Bit 13—Connection Flag 8N (CN8N): Enables or disables connection between DST8N and the channel 2 down-count start trigger.

Bit 13: CN8N	Description
0	Connection between DST8N and channel 2 down-count start trigger F is disabled (Initial value)
1	Connection between DST8N and channel 2 down-count start trigger F is enabled

- Bit 12—Connection Flag 8M (CN8M): Enables or disables connection between DST8M and the channel 2 down-count start trigger.

Bit 12: CN8M	Description
0	Connection between DST8M and channel 2 down-count start trigger E is disabled (Initial value)
1	Connection between DST8M and channel 2 down-count start trigger E is enabled

- Bit 11—Connection Flag 8L (CN8L): Enables or disables connection between DST8L and the channel 2 down-count start trigger.

Bit 11: CN8L	Description
0	Connection between DST8L and channel 2 down-count start trigger D is disabled (Initial value)
1	Connection between DST8L and channel 2 down-count start trigger D is enabled

- Bit 10—Connection Flag 8K (CN8K): Enables or disables connection between DST8K and the channel 2 down-count start trigger.

Bit 10: CN8K	Description
0	Connection between DST8K and channel 2 down-count start trigger C is disabled (Initial value)
1	Connection between DST8K and channel 2 down-count start trigger C is enabled

- Bit 9—Connection Flag 8J (CN8J): Enables or disables connection between DST8J and the channel 2 down-count start trigger.

Bit 9: CN8J	Description
0	Connection between DST8J and channel 2 down-count start trigger B is disabled (Initial value)
1	Connection between DST8J and channel 2 down-count start trigger B is enabled

- Bit 8—Connection Flag 8I (CN8I): Enables or disables connection between DST8I and the channel 2 down-count start trigger.

Bit 8: CN8I	Description
0	Connection between DST8I and channel 2 down-count start trigger A is disabled (Initial value)
1	Connection between DST8I and channel 2 down-count start trigger A is enabled

- Bit 7—Connection Flag 8H (CN8H): Enables or disables connection between DST8H and the channel 1 down-count start trigger.

Bit 7: CN8H	Description
0	Connection between DST8H and channel 1 down-count start trigger H is disabled (Initial value)
1	Connection between DST8H and channel 1 down-count start trigger H is enabled

- Bit 6—Connection Flag 8G (CN8G): Enables or disables connection between DST8G and the channel 1 down-count start trigger.

Bit 6: CN8G	Description
0	Connection between DST8G and channel 1 down-count start trigger G is disabled (Initial value)
1	Connection between DST8G and channel 1 down-count start trigger G is enabled

- Bit 5—Connection Flag 8F (CN8F): Enables or disables connection between DST8F and the channel 1 down-count start trigger.

Bit 5: CN8F	Description
0	Connection between DST8F and channel 1 down-count start trigger F is disabled (Initial value)
1	Connection between DST8F and channel 1 down-count start trigger F is enabled

- Bit 4—Connection Flag 8E (CN8E): Enables or disables connection between DST8E and the channel 1 down-count start trigger.

Bit 4: CN8E	Description
0	Connection between DST8E and channel 1 down-count start trigger E is disabled (Initial value)
1	Connection between DST8E and channel 1 down-count start trigger E is enabled

- Bit 3—Connection Flag 8D (CN8D): Enables or disables connection between DST8D and the channel 1 down-count start trigger.

Bit 3: CN8D	Description
0	Connection between DST8D and channel 1 down-count start trigger D is disabled (Initial value)
1	Connection between DST8D and channel 1 down-count start trigger D is enabled

- Bit 2—Connection Flag 8C (CN8C): Enables or disables connection between DST8C and the channel 1 down-count start trigger.

Bit 2: CN8C	Description
0	Connection between DST8C and channel 1 down-count start trigger C is disabled (Initial value)
1	Connection between DST8C and channel 1 down-count start trigger C is enabled

- Bit 1—Connection Flag 8B (CN8B): Enables or disables connection between DST8B and the channel 1 down-count start trigger.

Bit 1: CN8B	Description
0	Connection between DST8B and channel 1 down-count start trigger B is disabled (Initial value)
1	Connection between DST8B and channel 1 down-count start trigger B is enabled

- Bit 0—Connection Flag 8A (CN8A): Enables or disables connection between DST8A and the channel 1 down-count start trigger.

Bit 0: CN8A	Description
0	Connection between DST8A and channel 1 down-count start trigger A is disabled (Initial value)
1	Connection between DST8A and channel 1 down-count start trigger A is enabled

### 10.2.13 One-Shot Pulse Terminate Register (OTR)

The one-shot pulse terminate register (OTR) is a 16-bit register. The ATU-II has one OTR register in channel 8.

Bit:	15	14	13	12	11	10	9	8
	OTEP	OTEO	OTEN	OTEM	OTEL	OTEK	OTEJ	OTEI
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	OTEH	OTEG	OTEF	OTEE	OTED	OTEC	OTEB	OTEA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OTR is a 16-bit readable/writable register that enables or disables forced termination of channel 8 one-shot pulse output by channel 1 and 2 compare-match signals. When one-shot pulse output is forcibly terminated, the corresponding DSTR bit and down-counter are cleared, and the corresponding TSR8 bit is set. The channel 1 one-shot pulse terminate signal is generated by GR1A to GR1H compare-matches and OCR1 compare-match (see TRGMDR). The channel 2 one-shot pulse terminate signal is generated by GR2A to GR2H compare-matches. To generate the terminate signal with GR1A to GR1H and GR2A to GR2H, select the respective compare-matches in TIOR1A to TIOR1D.

OTR is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

- Bit 15—One-Shot Pulse Terminate Enable P (OTEP): Enables or disables forced termination of output by channel 2 down-counter terminate trigger H.

Bit 15: OTEP	Description
0	Forced termination of TO8P by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8P by down-counter terminate trigger is enabled

- Bit 14—One-Shot Pulse Terminate Enable O (OTE0): Enables or disables forced termination of output by channel 2 down-counter terminate trigger G.

Bit 14: OTE0	Description
0	Forced termination of TO8O by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8O by down-counter terminate trigger is enabled

- Bit 13—One-Shot Pulse Terminate Enable N (OTEN): Enables or disables forced termination of output by channel 2 down-counter terminate trigger F.

Bit 13: OTEN	Description
0	Forced termination of TO8N by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8N by down-counter terminate trigger is enabled

- Bit 12—One-Shot Pulse Terminate Enable M (OTEM): Enables or disables forced termination of output by channel 2 down-counter terminate trigger E.

Bit 12: OTEM	Description
0	Forced termination of TO8M by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8M by down-counter terminate trigger is enabled

- Bit 11—One-Shot Pulse Terminate Enable L (OTEL): Enables or disables forced termination of output by channel 2 down-counter terminate trigger D.

Bit 11: OTEL	Description
0	Forced termination of TO8L by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8L by down-counter terminate trigger is enabled

- Bit 10—One-Shot Pulse Terminate Enable K (OTEK): Enables or disables forced termination of output by channel 2 down-counter terminate trigger C.

Bit 10: OTEK	Description
0	Forced termination of TO8K by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8K by down-counter terminate trigger is enabled



- Bit 9—One-Shot Pulse Terminate Enable J (OTEJ): Enables or disables forced termination of output by channel 2 down-counter terminate trigger B.

Bit 9: OTEJ	Description
0	Forced termination of TO8J by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8J by down-counter terminate trigger is enabled

- Bit 8—One-Shot Pulse Terminate Enable I (OTEI): Enables or disables forced termination of output by channel 2 down-counter terminate trigger A.

Bit 8: OTEI	Description
0	Forced termination of TO8I by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8I by down-counter terminate trigger is enabled

- Bit 7—One-Shot Pulse Terminate Enable H (OTEH): Enables or disables forced termination of output by channel 1 down-counter terminate trigger H.

Bit 7: OTEH	Description
0	Forced termination of TO8H by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8H by down-counter terminate trigger is enabled

- Bit 6—One-Shot Pulse Terminate Enable G (OTEG): Enables or disables forced termination of output by channel 1 down-counter terminate trigger G.

Bit 6: OTEG	Description
0	Forced termination of TO8G by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8G by down-counter terminate trigger is enabled

- Bit 5—One-Shot Pulse Terminate Enable F (OTEF): Enables or disables forced termination of output by channel 1 down-counter terminate trigger F.

Bit 5: OTEF	Description
0	Forced termination of TO8F by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8F by down-counter terminate trigger is enabled

- Bit 4—One-Shot Pulse Terminate Enable E (OTEE): Enables or disables forced termination of output by channel 1 down-counter terminate trigger E.

Bit 4: OTEE	Description
0	Forced termination of TO8E by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8E by down-counter terminate trigger is enabled

- Bit 3—One-Shot Pulse Terminate Enable D (OTED): Enables or disables forced termination of output by channel 1 down-counter terminate trigger D.

Bit 3: OTED	Description
0	Forced termination of TO8D by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8D by down-counter terminate trigger is enabled

- Bit 2—One-Shot Pulse Terminate Enable C (OTEC): Enables or disables forced termination of output by channel 1 down-counter terminate trigger C.

Bit 2: OTEC	Description
0	Forced termination of TO8C by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8C by down-counter terminate trigger is enabled

- Bit 1—One-Shot Pulse Terminate Enable B (OTEB): Enables or disables forced termination of output by channel 1 down-counter terminate trigger B.

Bit 1: OTEB	Description
0	Forced termination of TO8B by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8B by down-counter terminate trigger is enabled

- Bit 0—One-Shot Pulse Terminate Enable A (OTEA): Enables or disables forced termination of output by channel 1 down-counter terminate trigger A.

Bit 0: OTEA	Description
0	Forced termination of TO8A by down-counter terminate trigger is disabled (Initial value)
1	Forced termination of TO8A by down-counter terminate trigger is enabled

## 10.2.14 Reload Enable Register (RLDENR)

The reload enable register (RLDENR) is an 8-bit register. The ATU-II has one RLDENR register in channel 8.

Bit:	7	6	5	4	3	2	1	0
	RLDEN	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R

RLDENR is an 8-bit readable/writable register that enables or disables loading of the reload register8 (RLDR8) value into the down-counters (DCNT8I to DCNT8P). Loading is performed on generation of a channel 2 compare-match signal one-shot pulse start trigger. Reloading is not performed if there is no linkage with channel 2 (one-shot pulse function), or while the down-counter (DCNT8I to DCNT8P) is running.

RLDENR is initialized to H'00 by a power-on reset and in hardware standby mode and software standby mode.

- Bit 7—Reload Enable (RLDEN): Enables or disables loading of the RLDR value into DCNT8I to DCNT8P.

Bit 7: RLDEN	Description
0	Loading of reload register value into down-counters is disabled (Initial value)
1	Loading of reload register value into down-counters is enabled

- Bits 6 to 0—Reserved: These bits always read 0. The write value should always be 0.

## 10.2.15 Free-Running Counters (TCNT)

The free-running counters (TCNT) are 32- or 16-bit up- or up/down-counters. The ATU-II has 17 TCNT counters: one 32-bit TCNT in channel 0, and sixteen 16-bit TCNTs in each of channels 1 to 7 and 11.

Channel	Abbreviation	Function
0	TCNT0H, TCNT0L	32-bit up-counter (initial value H'00000000)
1	TCNT1A, TCNT1B	16-bit up-counters (initial value H'0000)
2	TCNT2A, TCNT2B	
3	TCNT3	16-bit up-counters (initial value H'0001)
4	TCNT4	
5	TCNT5	16-bit up/down-counters (initial value H'0001)
6	TCNT6A to TCNT6D	
7	TCNT7A to TCNT7D	16-bit up-counters (initial value H'0000)
11	TCNT11	

**Free-Running Counter 0 (TCNT0H, TCNT0L):** Free-running counter 0 (comprising TCNT0H and TCNT0L) is a 32-bit readable/writable register that counts on an input clock. When the bits corresponding to the timer start register 1 (TSTR1) are set to 1, this counter starts to count. The input clock is selected with prescaler register 1 (PSCR1).

Bit: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W

Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W

When TCNT0 overflows (from H'FFFFFFFF to H'00000000), the OVF0 overflow flag in the timer status register (TSR0) is set to 1.

TCNT0 can only be accessed by a longword read or write. Word reads or writes cannot be used.

TCNT0 is initialized to H'00000000 by a power-on reset, and in hardware standby mode and software standby mode.

**Free-Running Counters 1A, 1B, 2A, 2B, 3, 4, 5, 11 (TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, TCNT5, TCNT11):** Free-running counters 1A, 1B, 2A, 2B, 3, 4, 5, and 11 (TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, TCNT5, TCNT11) are 16-bit readable/writable registers that count on an input clock. When the bits corresponding to the timer start register 1, 3 (TSTR1, TSTR3) are set to 1, these counters start to count. The input clock is selected with prescaler register 1 (PSCR1) and the timer control register (TCR).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name:																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The TCNT1A, TCNT1B, TCNT2A, and TCNT2B counters are cleared if incremented during counter clear trigger input from channel 10.

TCNT3 to TCNT5 counter clearing is performed by a compare-match with the corresponding general register, according to the setting in TIOR.

When one of counters TCNT1A/1B/2A/2B/3/4/5/11 overflows (from H'FFFF to H'0000), the overflow flag (OVF) for the corresponding channel in the timer status register (TSR) is set to 1.

TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, TCNT5, and TCNT11 can only be accessed by a word read or write.

TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, TCNT5, and TCNT11 are initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, and TCNT5 can count on external clock (TCLKA or TCLKB) input.

TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, and TCNT5 can count on an external interrupt clock (TI10) (AGCK) generated in channel 10 and on a channel 10 multiplied clock (AGCKM).

**Free-Running Counters 6A to 6D and 7A to 7D (TCNT6A to TCNT6D, TCNT7A to TCNT7D):** Free-running counters 6A to 6D and 7A to 7D (TCNT6A to TCNT6D, TCNT7A to TCNT7D) are 16-bit readable/writable registers. Channel 6 and 7 counts are started by the timer start register (TSTR2).

The clock input to channels 6 and 7 is selected with prescaler registers 2 and 3 (PSCR2, PSCR3) and timer control registers 6 and 7 (TCR6, TCR7).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT6A to TCNT6D (in non-complementary PWM mode) and TCNT7A to TCNT7D are cleared by a compare-match with the cycle register (CYLR).

TCNT6A to TCNT6D (in complementary PWM mode) count up and down between zero and the cycle register value.

TCNT6A to TCNT6D and TCNT7A to TCNT7D are connected to the CPU by an internal 16-bit bus, and can only be accessed by a word read or write.

TCNT6A to TCNT6D and TCNT7A to TCNT7D are initialized to H'0001 by a power-on reset, and in hardware standby mode and software standby mode.

### 10.2.16 Down-Counters (DCNT)

The DCNT registers are 16-bit down-counters. The ATU-II has 16 DCNT counters in channel 8.

Channel	Abbreviation	Function
8	DCNT8A, DCNT8B, DCNT8C, DCNT8D, DCNT8E, DCNT8F, DCNT8G, DCNT8H, DCNT8I, DCNT8J, DCNT8K, DCNT8L, DCNT8M, DCNT8N, DCNT8O, DCNT8P	16-bit down-counters

**Down-Counters 8A to 8P (DCNT8A to DCNT8P):** Down-counters 8A to 8P (DCNT8A to DCNT8P) are 16-bit readable/writable registers that count on an input clock. The input clock is selected with prescaler register 1 (PSCR1) and the timer control register (TCR).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name:																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

When the one-shot pulse function is used, DCNT8x starts counting down when the corresponding DSTR bit is set to 1 by the user program after the DCNT8x value has been set. When the DCNT8x value underflows, DSTR and DCNT8x are automatically cleared to 0, and the count is stopped. At the same time, the corresponding channel 8 timer status register 8 (TSR8) status flag is set to 1.

When the offset one-shot pulse function is used, on compare-match with a channel 1 or 2 general register (GR) or output compare register (OCR) (the compare-match setting being made in the trigger mode register (TRGMDR) (for channel 1 only) ) when the corresponding timer connection register (TCNR) bit is 1, the corresponding down-count start register (DSTR) bit is automatically set to 1 and the down-count is started. When the DCNT8x value underflows, the corresponding DSTR bit and DCNT8x are automatically cleared to 0, the count is stopped, and the output is inverted, or, if a one-shot terminate register (OTR) setting has been made to forcibly terminate output by means of a trigger, DSTR is cleared to 0 by a channel 1 or 2 compare-match between GR and OCR, the count is forcibly terminated, and the output is inverted. The output is inverted for whichever is first. At the same time, the corresponding channel 8 TSR8 status flag is set to 1.

The DCNT8x counters can only be accessed by a word read or write.

The DCNT8x counters are initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

For details, see sections 10.3.5, One-Shot Pulse Function, and 10.3.6, Offset One-Shot Pulse Function and Output Cutoff Function.

### 10.2.17 Event Counters (ECNT)

The event counters (ECNT) are 8-bit up-counters. The ATU-II has six ECNT counters in channel 9.

Channel	Abbreviation	Function
9	ECNT9A, ECNT9B, ECNT9C, ECNT9D, ECNT9E, ECNT9F	8-bit event counters

The ECNT counters are 8-bit readable/writable registers that count on detection of an input signal from input pins TI9A to TI9F. Rising edge, falling edge, or both rising and falling edges can be selected for edge detection.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

When a compare-match with GR9 corresponding to an ECNT9x counter occurs, the compare-match flag (CMF9) in the timer status register (TSR9) is set to 1. When a compare-match with GR occurs, the ECNT9x counter is cleared automatically.

The ECNT9x counters can only be accessed by a byte read or write.

The ECNT9x counters are initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

### 10.2.18 Output Compare Registers (OCR)

The output compare registers (OCR) are 16-bit registers. The ATU-II has nine OCR registers: one in channel 1 and eight in channel 2.

Channel	Abbreviation	Function
1	OCR1	Output compare registers
2	OCR2A, OCR2B, OCR2C, OCR2D, OCR2E, OCR2F, OCR2G, OCR2H	

### Output Compare Registers 1 and 2A to 2H (OCR1, OCR2A to OCR2H)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The OCR registers are 16-bit readable/writable registers that have an output compare register function.

The OCR and free-running counter (TCNT1B, TCNT2B) values are constantly compared, and if the two values match, the CMF bit in the timer status register (TSR) is set to 1. If channels 1 and 2



and channel 8 are linked by the timer connection register (TCNR), the corresponding channel 8 down-counter (DCNT) is started at the same time.

The OCR registers can only be accessed by a word read.

The OCR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

### 10.2.19 Input Capture Registers (ICR)

The input capture registers (ICR) are 32-bit registers. The ATU-II has four 32-bit ICR registers in channel 0.

Channel	Abbreviation	Function
0	ICR0AH, ICR0AL, ICR0BH, ICR0BL, ICR0CH, ICR0CL, ICR0DH, ICR0DL	Dedicated input capture registers

#### Input Capture Registers 0AH, 0AL to 0DH, 0DL (ICR0AH, ICR0AL to ICR0DH, ICR0DL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

The ICR registers are 32-bit read-only registers used exclusively for input capture.

These dedicated input capture registers store the TCNT0 value on detection of an input capture signal from an external source. The corresponding TSR0 bit is set to 1 at this time. The input capture signal edge to be detected is specified by timer I/O control register TIOR0. By setting the TRG0DEN bit in TCR10, ICR0DH and ICR0DL can also be used for input capture in a compare match between TCNT10B and OCR10B.

The ICR registers can only be accessed by a longword read. Word reads cannot be used.

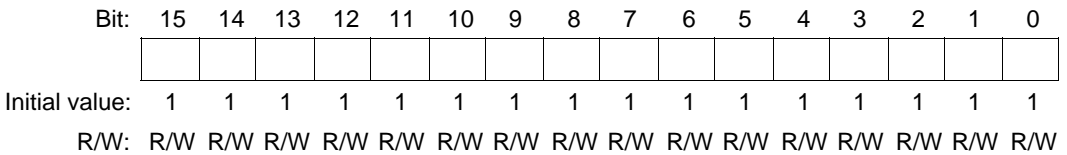
The ICR registers are initialized to H'00000000 by a power-on reset, and in hardware standby mode and software standby mode.

### 10.2.20 General Registers (GR)

The general registers (GR) are 16-bit registers. The ATU-II has 36 general registers: eight each in channels 1 and 2, four each in channels 3 to 5, six in channel 9, and two in channel 11.

Channel	Abbreviation	Function
1	GR1A to GR1H	Dual-purpose input capture and output compare registers
2	GR2A to GR2H	
3	GR3A to GR3D	
4	GR4A to GR4D	
5	GR5A to GR5D	
9	GR9A to GR9F	Dedicated output compare registers
11	GR11A, GR11B	Compare match registers

#### General Registers 1A to 1H and 2A to 2H (GR1A to GR1H, GR2A to GR2H)



These GR registers are 16-bit readable/writable registers with both input capture and output compare functions. Function switching is performed by means of the timer I/O control registers (TIOR).

When a general register is used for input capture, it stores the TCNT1A or TCNT2A value on detection of an input capture signal from an external source. The corresponding IMF bit in TSR is set to 1 at this time. The input capture signal edge to be detected is specified by the corresponding TIOR.

When a general register is used for output compare, the GR value and free-running counter (TCNT1A, TCNT2A) value are constantly compared, and when both values match, the IMF bit in the timer status register (TSR) is set to 1. If connection of channels 1 and 2 and channel 8 is specified in the timer connection register (TCNR), the corresponding channel 8 down-counter (DCNT) is started. Compare-match output is specified by the corresponding TIOR.

The GR registers can only be accessed by a word read or write.

The GR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

### General Registers 3A to 3D, 4A to 4D, and 5A to 5D (GR3A to GR3D, GR4A to GR4D, and GR5A to GR5D)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These GR registers are 16-bit readable/writable registers with both input capture and output compare functions. Function switching is performed by means of the timer I/O control registers (TIOR).

When a general register is used for input capture, it stores the corresponding TCNT value on detection of an input capture signal from an external source. The corresponding IMF bit in TSR is set to 1 at this time. The input capture signal edge to be detected is specified by the corresponding TIOR. GR3A to GR3D can also be used for input capture with a channel 9 compare-match as the trigger. In this case, the corresponding IMF bit in TSR is not set.

When a general register is used for output compare, the GR value and free-running counter (TCNT) value are constantly compared, and when both values match, the IMF bit in the timer status register (TSR) is set to 1. Compare-match output is specified by the corresponding TIOR.

The GR registers can only be accessed by a word read or write.

The GR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

### General Registers 9A to 9F (GR9A to GR9F)

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These GR registers are 8-bit readable/writable registers with a compare-match function.

The GR value and event counter (ECNT) value are constantly compared, and when both values match a compare-match signal is generated and the next edge is input, the corresponding CMF bit in TSR is set to 1.

In addition, channel 3 (GR3A to GR3D) input capture can be generated by GR9A to GR9D compare-matches. This function is set by TRG3xEN in the timer control register (TCR).

The GR registers can be accessed by a byte read or write.

The GR registers are initialized to H'FF by a power-on reset, and in hardware standby mode and software standby mode.

### General Registers 11A, B (GR11A, B)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These GR registers are 16-bit readable/writable registers with compare-match function.

When a general register is used as a compare-match register, the GR value and free-running counter (TCNT) value are constantly compared, and when both values match, the IMF bit in the timer status register (TSR) is set to 1. Compare-match output is specified by the corresponding TIOR.

GR11A and GR11B compare-mach signals are transmitted to the advanced pulse controller (APC). For details, see section 11, Advanced Pulse Controller (APC).

The GR registers can only be accessed by a word read or write.

The GR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

#### 10.2.21 Offset Base Registers (OSBR)

The offset base registers (OSBR) are 16-bit registers. The ATU-II has two OSBR registers, one each in channels 1 and 2.

Channel	Abbreviation	Function
1	OSBR1	Dedicated input capture registers with signal from channel 0
2	OSBR2	ICR0A as input trigger

## Offset Base Registers 1 and 2 (OSBR1, OSBR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

OSBR1 and OSBR2 are 16-bit read-only registers used exclusively for input capture. OSBR1 and OSBR2 use the channel 0 ICR0A input capture register input as their trigger signal, and store the TCNT1A or TCNT2A value on detection of an edge.

The OSBR registers can only be accessed by a word read.

The OSBR registers are initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

For details, see sections 10.3.8, Twin-Capture Function.

### 10.2.22 Cycle Registers (CYLR)

The cycle registers (CYLR) are 16-bit registers. The ATU-II has eight cycle registers, four each in channels 6 and 7.

Channel	Abbreviation	Function
6	CYLR6A to CYLR6D	16-bit PWM cycle registers
7	CYLR7A to CYLR7D	

### Cycle Registers (CYLR6A to CYLR6D, CYLR7A to CYLR7D)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CYLR registers are 16-bit readable/writable registers used for PWM cycle storage.

The CYLR value is constantly compared with the corresponding free-running counter (TCNT6A to TCNT6D, TCNT7A to TCNT7D) value, and when the two values match, the corresponding timer start register (TSR) bit (CMF6A to CMF6D, CMF7A to CMF7D) is set to 1, and the free-running counter (TCNT6A to TCNT6D, TCNT7A to TCNT7D) is cleared. At the same time, the buffer register (BFR) value is transferred to the duty register (DTR).

The CYLR registers can only be accessed by a word read or write.

The CYLR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

For details of the CYLR, BFR, and DTR registers, see section 10.3.9, PWM Timer Function.

### 10.2.23 Buffer Registers (BFR)

The buffer registers (BFR) are 16-bit registers. The ATU-II has eight buffer registers, four each in channels 6 and 7.

Channel	Abbreviation	Function
6	BFR6A to BFR6D	16-bit PWM buffer registers
7	BFR7A to BFR7D	Buffer register (BFR) value is transferred to duty register (DTR) on compare-match of corresponding cycle register (CYLR)

#### Buffer Registers (BFR6A to BFR6D, BFR7A to BFR7D)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The BFR registers are 16-bit readable/writable registers that store the value to be transferred to the duty register (DTR) in the event of a cycle register (CYLR) compare-match.

The BFR registers can only be accessed by a word read or write.

The BFR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

## 10.2.24 Duty Registers (DTR)

The duty registers (DTR) are 16-bit registers. The ATU-II has eight duty registers, four each in channels 6 and 7.

Channel	Abbreviation	Function
6	DTR6A to DTR6D	16-bit PWM duty registers
7	DTR7A to DTR7D	

### Duty Registers (DTR6A to DTR6D, DTR7A to DTR7D)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DTR registers are 16-bit readable/writable registers used for PWM duty storage.

The DTR value is constantly compared with the corresponding free-running counter (TCNT6A to TCNT6D, TCNT7A to TCNT7D) value, and when the two values match, the corresponding channel output pin (TO6A to TO6D, TO7A to TO7D) goes to 0 output. Also, when CYLR and the corresponding the free-running counter match, the corresponding BFR value is loaded. Set a value in the range 0 to CYLR for DTR; do not set a value greater than CYLR.

The DTR registers can only be accessed by a word read or write.

The DTR registers are initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

### 10.2.25 Reload Register (RLDR)

The reload register is a 16-bit register. The ATU-II has one RLDR register in channel 8.

#### Reload Register 8 (RLDR8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RLDR8 is a 16-bit readable/writable register. When reload is enabled (by a setting in RL DENR) and DSTR8I to DSTR8P are set to 1 by the channel 2 compare-match signal one-shot pulse start trigger, the reload register value is transferred to DCNT8I to DCNT8P before the down-count is started. The reload register value is not transferred when the one-shot pulse function is used independently, without linkage to channel 2, or when down-counters DCNT8I to DCNT8P are running.

RLDR8 can only be accessed by a word read or write.

RLDR is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

### 10.2.26 Channel 10 Registers

#### Counters (TCNT)

Channel 10 has seven TCNT counters: one 32-bit TCNT, four 16-bit TCNTs, and two 8-bit TCNTs.

The input clock is selected with prescaler register 4 (PSCR4). Count operations are performed by setting STR10 to 1 in timer start register 1 (TSTR1).

Channel	Abbreviation	Function
10	TCNT10AH, AL	32-bit free-running counter (initial value H'00000001)
	TCNT10B	8-bit event counter (initial value H'00)
	TCNT10C	16-bit reload counter (initial value H'0001)
	TCNT10D	8-bit correction counter (initial value H'00)
	TCNT10E	16-bit correction counter (initial value H'0000)
	TCNT10F	16-bit correction counter (initial value H'0001)
	TCNT10G	16-bit free-running counter (initial value H'0000)



**Free-Running Counter 10AH, AL (TCNT10AH, TCNT10AL):** Free-running counter 10AH, AL (comprising TCNT10AH and TCNT10AL) is a 32-bit readable/writable register that counts on an input clock and is cleared by input capture input (TI10) (AGCK).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT10A can only be accessed by a longword read or write. Word reads or writes cannot be used.

TCNT10A is initialized to H'00000001 by a power-on reset, and in hardware standby mode and software standby mode.

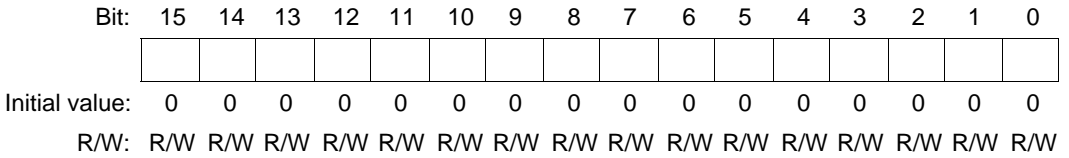
**Event Counter 10B (TCNT10B):** Event counter 10B (TCNT10B) is an 8-bit readable/writable register that counts on external clock input (TI10) (AGCK). For this operation, TI10 input must be set with bits CKEG1 and CKEG0 in TCR10. TI10 input will be counted even if halting of the count operation is specified by bit STR10 in TSTR1.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT10B can only be accessed by a byte read or write.

TCNT10B is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

**Reload Counter 10C (TCNT10C):** Reload counter 10C (TCNT10C) is a 16-bit readable/writable register.

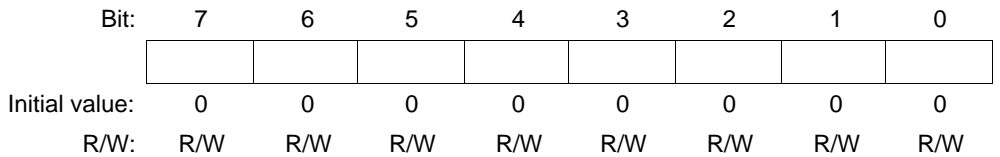


When TCNT10C = H'0001 in the down-count operation, the value in the reload register (RLD10C) is transferred to TCNT10C, and a multiplied clock (AGCK1) is generated.

TCNT10C is connected to the CPU via an internal 16-bit bus, and can only be accessed by a word read or write.

TCNT10C is initialized to H'0001 by a power-on reset, and in hardware standby mode and software standby mode.

**Correction Counter 10D (TCNT10D):** Correction counter 10D (TCNT10D) is an 8-bit readable/writable register that counts on external clock input (TI10) after transfer of the counter value to correction counter E (TCNT10E). Set TI10 input with bits CKEG1 and CKEG0 in TCR10. Counting will not be performed on TI10 input unless the count operation is enabled by bit STR10 in TSTR1.

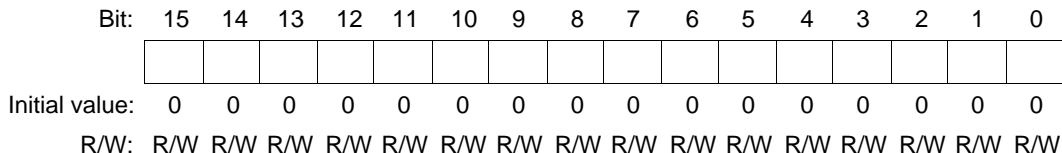


At the external clock input (TI10) (AGCK) timing, the value in this counter is shifted according to the multiplication factor set by bits PIM1 and PIM0 in timer I/O control register 10 (TIOR10) and transferred to correction counter E (TCNT10E).

TCNT10D can only be accessed by a byte read or write.

TCNT10D is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

**Correction Counter 10E (TCNT10E):** Correction counter 10E (TCNT10E) is a 16-bit readable/writable register that loads the TCNT10D shift value at the external input (TI10) timing, and counts on the multiplied clock (AGCK1) output by reload counter 10C (TCNT10C). However, if CCS in timer I/O control register 10 (TIOR10) is set to 1, when the TCNT10D shifted value is reached the count is halted.

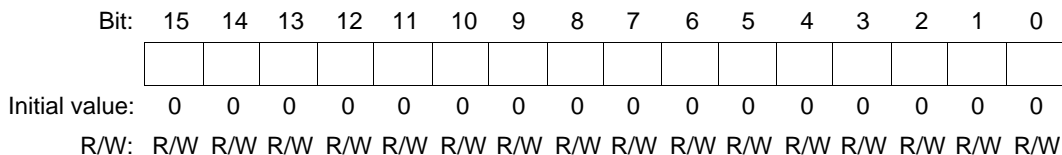


TCNT10E can only be accessed by a word read or write.

TCNT10E is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

**Correction Counter 10F (TCNT10F):** Correction counter 10F (TCNT10F) is a 16-bit readable/writable register that counts up if the counter value is smaller than the correction counter 10E (TCNT10E) value when the STR10 bit in TSTR1 has been set for counter operation. The count is halted by a match with the correction counter clear register (TCCLR10). If TI10 is input when TCNT10D = H'0000, TCNT10F is initialized and correction is carried out. When TCNT10F = TCCLR10, TCNT10F is cleared to H'0001. While TCNT10F ≠ TCCLR10, TCNT10F is incremented automatically until it reaches the TCCLR10 value, and is then cleared to H'0001.

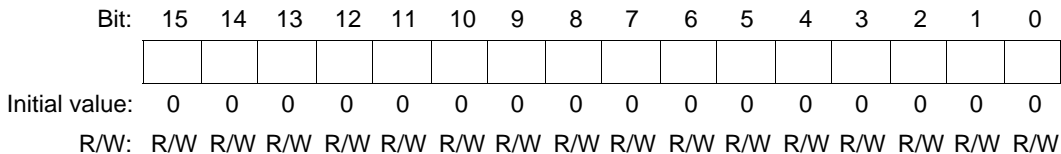
A corrected clock (AGCKM) is output following correction each time this counter is incremented.



TCNT10F is can only be accessed by a word read or write.

TCNT10F is initialized to H'0001 by a power-on reset, and in hardware standby mode and software standby mode.

**Free-Running Counter 10G (TCNT10G):** Free-running counter 10G (TCNT10G) is a 16-bit readable/writable register that counts up on the multiplied clock (AGCK1). TCNT10G is initialized to H'0000 by input from external input (TI10) (AGCK).



TCNT10G can only be accessed by a word read or write.

TCNT10G is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

### Registers

There are six registers in channel 10: a 32-bit ICR, 32-bit OCR, 16-bit GR, 16-bit RLD, 16-bit TCCLR, and 8-bit OCR.

Channel	Abbreviation	Function
10	ICR10AH, AL	32-bit input capture register (initial value H'00000000)
	OCR10AH, AL	32-bit output compare register (initial value H'FFFFFFFF)
	OCR10B	8-bit output compare register (initial value H'FF)
	RLD10C	16-bit reload register (initial value H'0000)
	GR10G	16-bit general register (initial value H'FFFF)
	TCCLR10	16-bit correction counter clear register (initial value H'0000)

**Input Capture Register 10AH, AL (ICR10AH, ICR10AL):** Input capture register 10AH, AL (comprising ICR10AH and ICR10AL) is a 32-bit read-only register to which the TCNT10AH, AL value is transferred on external input (TI10) (AGCK). At the same time, ICF10A in timer status register 10 (TCR10) is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ICR10A is initialized to H'00000000 by a power-on reset, and in hardware standby mode and software standby mode.

**Output Compare Register 10AH, AL (OCR10AH, OCR10AL):** Output compare register 10AH, AL (comprising OCR10AH and OCR10AL) is a 32-bit readable/writable register that is constantly compared with free-running counter 10AH, AL (TCNT10AH, TCNT10AL). When both values match, CMF10A in timer status register 10 (TSR10) is set to 1.

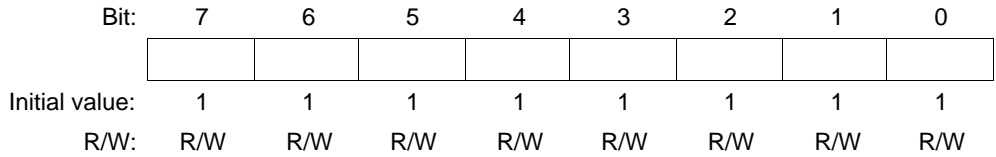
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

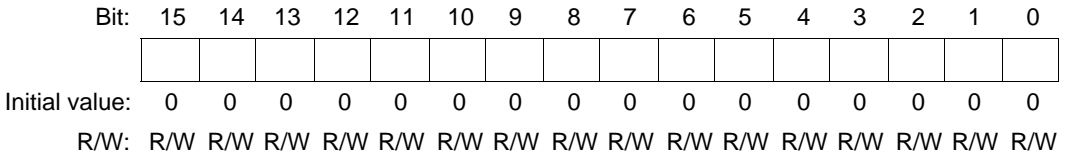
OCR10A is initialized to H'FFFFFFFF by a power-on reset, and in hardware standby mode and software standby mode.

**Output Compare Register 10B (OCR10B):** Output compare register 10B (OCR10B) is an 8-bit readable/writable register that is constantly compared with free-running counter 10B (TCNT10B). When AGCK is input with both values matching, CMF10B in timer status register 10 (TSR10) is set to 1.



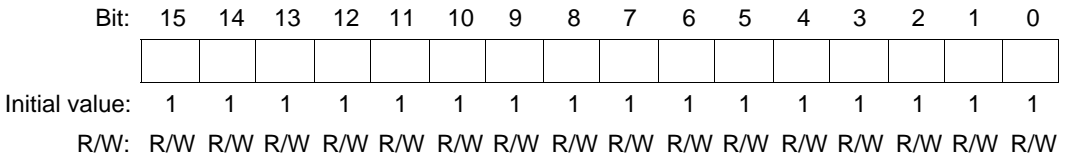
OCR10B is initialized to H'FF by a power-on reset, and in hardware standby mode and software standby mode.

**Reload Register 10C (RLD10C):** Reload register 10C (RLD10C) is a 16-bit readable/writable register. When STR10 in timer start register 1 (TSTR1) is 1 and RLDEN in the timer I/O control register (TIOR10) is 0, and the value of TCNT10A is captured into input capture register 10A (ICR10A), the ICR10A capture value is shifted according to the multiplication factor set by bits PIM1 and PIM0 in TIOR10 before being transferred to RLD10C. The contents of reload register 10C (RLD10C) are loaded when reload counter 10C (TCNT10C) reaches H'0001.



RLD10C is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

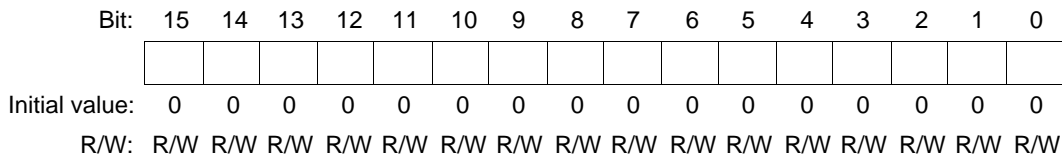
**General Register 10G (GR10G):** General register 10G (GR10G) is a 16-bit readable/writable register with an output compare function. Function switching is performed by means of timer I/O control register 10 (TIOR10). The GR10G value and free-running counter 10G (TCNT10G) value are constantly compared, and when AGCK is input with both values matching, CMF10G in timer status register 10 (TSR10) is set to 1.



GR10G is initialized to H'FFFF by a power-on reset, and in hardware standby mode and software standby mode.

**Correction Counter Clear Register 10 (TCCLR10):** Correction counter clear register 10 (TCCLR10) is a 16-bit readable/writable register.

TCCLR10 is constantly compared with TCNT10F, and when the two values match, TCNT10F halts. TCNT<sub>xx</sub> can be cleared at this time by setting TRG<sub>xx</sub>EN (xx = 1A, 1B, 2A, 2B) in TCR10. Then, when TCNT10D is H'0000 and TI10 is input, TCNT10F is cleared to H'0001.



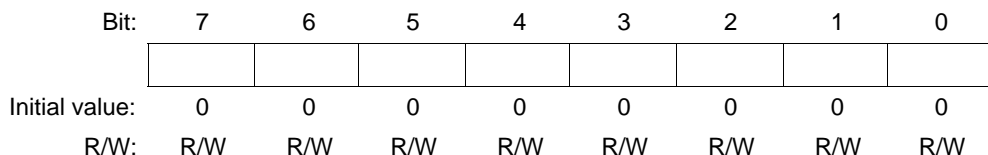
TCCLR10 is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

### Noise Canceler Registers

There are two 8-bit noise canceler registers in channel 10: TCNT10H and NCR10.

Channel	Abbreviation	Function	
10	TCNT10H	Noise canceler counter	(Initial value H'00)
	NCR10	Noise canceler compare-match register	(Initial value H'FF)

**Noise Canceler Counter 10H (TCNT10H):** Noise canceler counter 10H (TCNT10H) is an 8-bit readable/writable register. When the noise canceler function is enabled, TCNT10H starts counting up on Pφ × 10, with the signal from external input (TI10) (AGCK) as a trigger. The counter operates even if STR10 is cleared to 0 in the timer start register (TSTR1). TI10 input is masked while the counter is running. When the count matches the noise canceler register (NCR10) value, the counter is cleared and TI10 input masking is released.



TCNT10H is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

**Noise Canceler Register 10 (NCR10):** Noise canceler register 10 (NCR10) is an 8-bit readable/writable register used to set the upper count limit of noise canceler counter 10H (TCNT10H). TCNT10H is constantly compared with NCR10 during the count, and when a compare-match occurs the TCNT10H counter is halted and input signal masking is released.

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NCR10 is initialized to H'FF by a power-on reset, and in hardware standby mode and software standby mode.

### Channel 10 Control Registers

There are four control registers in channel 10.

Channel	Abbreviation	Function
10	TIOR10	Reload setting, counter correction setting, external input (TI10) edge interval multiplier setting GR compare-match setting (Initial value H'00)
	TCR10	TCCLR10 counter clear source Noise canceler function enabling/disabling selection External input (TI10) edge selection (Initial value H'00)
	TSR10	Input capture/compare-match status (Initial value H'0000)
	TIER10	Input capture/compare-match interrupt request enabling/disabling selection (Initial value H'0000)



**Timer I/O Control Register 10 (TIOR10):** TIOR10 is an 8-bit readable/writable register that selects the value for multiplication of the external input (TI10) edge interval. It also makes a setting for using the general register (GR10G) for output compare, and makes the edge detection setting.

TIOR10 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
	RLDEN	CCS	PIM1	PIM0	—	IO10G2	IO10G1	IO10G0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W

- Bit 7—Reload Enable (RLDEN): Enables or disables transfer of the input capture register 10A (ICR10A) value to reload register 10C (RLD10C).

Bit 7: RLDEN	Description
0	Transfer of ICR10A value to RLD10C on input capture is enabled (Initial value)
1	Transfer of ICR10A value to RLD10C on input capture is disabled

- Bit 6—Counter Clock Select (CCS): Selects the operation of correction counter 10E (TCNT10E). Set the multiplication factor with bits PIM1 and PIM0.

Bit 6: CCS	Description
0	TCNT10E count is not halted when TCNT10D x multiplication factor = TCNT10E* (Initial value)
1	TCNT10E count is halted when TCNT10D x multiplication factor = TCNT10E*

Note: \*When [TCNT10D × multiplication factor] matches the value of TCNT10E with bits 8 to 0 masked.

- Bits 5 and 4—Pulse Interval Multiplier (PIM1, PIM0): These bits select the external input (TI10) cycle multiplier.

Bit 5: PIM1	Bit 4: PIM0	Description
0	0	Counting on external input cycle × 32 (Initial value)
	1	Counting on external input cycle × 64
1	0	Counting on external input cycle × 128
	1	Counting on external input cycle × 256

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bits 2 to 0—I/O Control 10G2 to 10G0 (IO10G2 to IO10G0): These bits select the function of general register 10G (GR10G).

Bit 2: IO10G2	Bit 1: IO10G1	Bit 0: IO10G0	Description
0	0	0	GR is an output compare register
		1	GR10G = TCNT10G compare-match
	1	*	Cannot be used
1	*	*	Cannot be used

**Timer Control Register 10 (TCR10):** TCR10 is an 8-bit readable/writable register that selects the correction counter clear register (TCCLR10) compare-match counter clear source, enables or disables the noise canceler function, and selects the external input (TI10) edge.

TCR10 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
	TRG2BEN	TRG1BEN	TRG2AEN	TRG1AEN	TRG0DEN	NCE	CKEG1	CKEG0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 7—Trigger 2B Enable (TRG2BEN): Enables or disables counter clearing for channel 2 TCNT2B. If TCNT2B counts while clearing is enabled, TCNT2B will be cleared.

Bit 7: TRG2BEN	Description
0	Channel 2 counter B (TCNT2B) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is disabled (Initial value)
1	Channel 2 counter B (TCNT2B) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is enabled

- Bit 6—Trigger 1B Enable (TRG1BEN): Enables or disables counter clearing for channel 1 TCNT1B. If TCNT1B counts while clearing is enabled, TCNT1B will be cleared.

Bit 6: TRG1BEN	Description
----------------	-------------

0	Channel 1 counter B (TCNT1B) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is disabled (Initial value)
1	Channel 1 counter B (TCNT1B) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is enabled

- Bit 5—Trigger 2A Enable (TRG2AEN): Enables or disables counter clearing for channel 2 TCNT2A. If TCNT2A counts while clearing is enabled, TCNT2A will be cleared.

Bit 5: TRG2AEN	Description
----------------	-------------

0	Channel 2 counter 2A (TCNT2A) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is disabled (Initial value)
1	Channel 2 counter 2A (TCNT2A) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is enabled

- Bit 4—Trigger 1A Enable (TRG1AEN): Enables or disables counter clearing for channel 1 TCNT1A. If TCNT1A counts while clearing is enabled, TCNT1A will be cleared.

Bit 4: TRG1AEN	Description
----------------	-------------

0	Channel 1 counter 1A (TCNT1A) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is disabled (Initial value)
1	Channel 1 counter 1A (TCNT1A) clearing when correction counter clear register (TCCLR10) = correction counter (TCNT10F) is enabled

- Bit 3—Trigger 0D Enable (TRG0DEN): Enables or disables channel 0 ICR0D input capture signal requests.

Bit 3: TRG0DEN	Description
----------------	-------------

0	Capture requests for channel 0 input capture register (ICR0D) on event counter (TCNT10B) compare-match are disabled (Initial value)
1	Capture requests for channel 0 input capture register (ICR0D) on event counter (TCNT10B) compare-match are enabled

- Bit 2—Noise Canceler Enable (NCE): Enables or disables the noise canceler function.

Bit 2: NCE	Description
0	Noise canceler function is disabled (Initial value)
1	Noise canceler function is enabled

- Bits 1 and 0—Clock Edge 1 and 0 (CKEG1, CKEG0): These bits select the channel 10 external input (TI10) edge(s). The clock (AGCK) is generated by the detected edge(s).

Bit 1: CKEG1	Bit 0: CKEG0	Description
0	0	TI10 input disabled (Initial value)
	1	TI10 input rising edges detected
1	0	TI10 input falling edges detected
	1	TI10 input rising and falling edges both detected

**Timer Status Register 10 (TSR10):** TSR10 is a 16-bit readable/writable register that indicates the occurrence of channel 10 input capture or compare-match.

Each flag is an interrupt source, and issues an interrupt request to the CPU if the interrupt is enabled by the corresponding bit in timer interrupt enable register 10 (TIER10).

TSR10 is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	CMF10G	CMF10B	ICF10A	CMF10A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: \* Only 0 can be written, to clear the flag.

- Bits 15 to 4—Reserved: These bits always read 0. The write value should always be 0.

- Bit 3—Compare-Match Flag 10G (CMF10G): Status flag that indicates GR10G compare-match.

Bit 3: CMF10G	Description
0	[Clearing condition] (Initial value) When CMF10G is read while set to 1, then 0 is written to IMF10G
1	[Setting condition] When TCNT10G = GR10G

- Bit 2—Compare-Match Flag 10B (CMF10B): Status flag that indicates OCR10B compare-match.

Bit 2: CMF10B	Description
0	[Clearing condition] (Initial value) When CMF10B is read while set to 1, then 0 is written to CMF10B
1	[Setting condition] When TCNT10B is incremented while TCNT10B = OCR10B

- Bit 1—Input Capture Flag 10A (ICF10A): Status flag that indicates ICR10A input capture.

Bit 1: ICF10A	Description
0	[Clearing condition] (Initial value) When ICR10A is read while set to 1, then 0 is written to ICR10A
1	[Setting condition] When the TCNT10A value is transferred to ICR10A by an input capture signal

- Bit 0—Compare-Match Flag 10A (CMF10A): Status flag that indicates OCR10A compare-match.

Bit 0: CMF10A	Description
0	[Clearing condition] (Initial value) When CMF10A is read while set to 1, then 0 is written to CMF10A
1	[Setting condition] When TCNT10A = OCR10A

**Timer Interrupt Enable Register 10 (TIER10):** TIER10 is a 16-bit readable/writable register that controls enabling/disabling of channel 10 input capture and compare-match interrupt requests.

TIER10 is initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	I REG	CME10G	CME10B	ICE10A	CME10A
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 5—Reserved: These bits always read 0. The write value should always be 0.
- Bit 4—Interrupt Enable Edge G (I REG): Specifies TSR10 CMF10G interrupt request timing.

Bit 4: I REG	Description
0	Interrupt is requested when CMF10G becomes 1 (Initial value)
1	Interrupt is requested by next external input (T110) (AGCK) after CMF10G becomes 1

- Bit 3—Compare-Match Interrupt Enable 10G (CME10G): Enables or disables interrupt requests by CMF10G in TSR10 when CMF10G is set to 1.

Bit 3: CME10G	Description
0	CMF10G interrupt requested by CMF10G is disabled (Initial value)
1	CMF10G interrupt requested by CMF10G is enabled

- Bit 2—Compare-Match Interrupt Enable 10B (CME10B): Enables or disables interrupt requests by CMF10B in TSR10 when CMF10B is set to 1.

Bit 2: CME10B	Description
0	CMF10B interrupt requested by CMF10B is disabled (Initial value)
1	CMF10B interrupt requested by CMF10B is enabled

- Bit 1—Input Capture Interrupt Enable 10A (ICE10A): Enables or disables interrupt requests by ICF10A in TSR10 when ICF10A is set to 1.

Bit 1: ICE10A	Description
0	ICI10A interrupt requested by ICF10A is disabled (Initial value)
1	ICI10A interrupt requested by ICF10A is enabled

- Bit 0—Compare-Match Interrupt Enable 10A (CME10A): Enables or disables interrupt requests by CMF10A in TSR10 when CMF10A is set to 1.

Bit 0: CME10A	Description
0	CMI10A interrupt requested by CMF10A is disabled (Initial value)
1	CMI10A interrupt requested by CMF10A is enabled

## 10.3 Operation

### 10.3.1 Overview

The ATU-II has twelve timers of eight kinds in channels 0 to 11. It also has a built-in prescaler that generates input clocks, and it is possible to generate or select internal clocks of the required frequency independently of circuitry outside the ATU-II.

The operation of each channel and the prescaler is outlined below.

**Channel 0:** Channel 0 has a 32-bit free-running counter (TCNT0) and four 32-bit input capture registers (ICR0A to ICR0D). TCNT0 is an up-counter that performs free-running operation. An interrupt request can be generated on counter overflow. The four input capture registers (ICR0A to ICR0D) capture the free-running counter (TCNT0) value by means of input from the corresponding external signal input pin (TI0A to TI0D). For capture by means of input from an external signal input pin, rising edge, falling edge, or both edges can be selected in the timer I/O control register (TIOR0). In the case of input capture register 0D (ICR0D) only, capture can be performed by means of a compare-match between free-running counter 10B (TCNT10B) and compare-match register 10B (OCR10B), by making a setting in timer control register 10 (TCR10). In this case, capture is performed even if an input capture disable setting has been made for TIOR0. In each case, the DMAC can be activated or an interrupt requested when capture occurs.

Channel 0 also has three interval interrupt request registers (ITVRR1, ITVRR2A, ITVRR2B). A/D converter (AD0 to AD2) activation can be selected by setting 1 in ITVA6 to ITVA13 in ITVRR, and an interrupt request to the CPU by setting 1 in ITVE6 to ITVE13. These operations are performed when the corresponding bit of bits 6 to 13 in TCNT0 changes to 1, enabling use as an interval timer function.

**Channel 1:** Channel 1 has two 16-bit free-running counters (TCNT1A, TCNT1B), eight 16-bit general registers (GR1A to GR1H), and a 16-bit output compare register (OCR1).

TCNT1A and TCNT1B are up-counters that perform free-running operation. When the clock generated in channel 10 (described below) is selected, these counters can be cleared at the count specified in channel 10. Each counter can generate an interrupt request when it overflows.

The eight general registers (GR1A to GR1H) can be used as input capture or output compare registers using the corresponding external signal I/O pin (TIO1A to TIO1H). When used for input capture, the free-running counter (TCNT1A) value is captured by means of input from the corresponding external signal I/O pin (TIO1A to TIO1H). Rising edge, falling edge, or both edges can be selected for the input capture signal in the timer I/O control registers (TIOR1A to TIOR1D). When used for output compare, compare-match with the free-running counter (TCNT1A) is performed. For the output from the external signal I/O pins by compare-match, 0 output, 1 output, or toggle output can be selected in the timer I/O control registers (TIOR1A to TIOR1D). When used as output compare registers, a compare-match can be used as a one-shot pulse start/terminate trigger by setting the channel 8 timer connection register (TCNR) and one-shot pulse terminate register (OTR), and using these in combination with the down-counters (DCNT8A to DCNT8H). Start/terminate trigger selection is performed by means of the trigger mode register (TRGMDR).

The output compare register (OCR1) can be used as a one-shot pulse offset function, in the same way as the general registers, in combination with channel 8 down-counters DCNT8A to DCNT8H. An interrupt can be requested on the occurrence of the respective input capture or compare-match.

In addition, channel 1 has a 16-bit dedicated input capture register (OSBR1). The channel 0 TIOA input pin can also be used as the OSBR1 trigger input, enabling use of a twin-capture function.

**Channel 2:** Channel 2 has two 16-bit free-running counters (TCNT2A, TCNT2B), eight 16-bit general registers (GR2A to GR2H), and eight 16-bit output compare registers (OCR2A to OCR2H).

TCNT2A and TCNT2B are up-counters that perform free-running operation. When the clock generated in channel 10 (described below) is selected, these counters can be cleared at the count specified in channel 10. Each counter can generate an interrupt request when it overflows.

The eight general registers (GR2A to GR2H) can be used as input capture or output compare registers using the corresponding external signal I/O pin (TIO2A to TIO2H). When used for input capture, the free-running counter (TCNT2A) value is captured by means of input from the corresponding external signal I/O pin (TIO2A to TIO2H). Rising edge, falling edge, or both edges can be selected for the input capture signal in the timer I/O control registers (TIOR2A to TIOR2D). When used for output compare, compare-match with the free-running counter (TCNT2A) is performed. For the output from the external signal I/O pins by compare-match, 0 output, 1 output, or toggle output can be selected in the timer I/O control registers (TIOR2A to



TIOR2D). When used as output compare registers, a compare-match can be used as a one-shot pulse terminate trigger by setting the channel 8 one-shot pulse terminate register (OTR), and using this in combination with the down-counters (DCNT8A to DCNT8H).

In the case of the output compare registers (OCR2A to OCR2H), a TCNT2B compare-match can be used as a one-shot pulse start trigger by setting the channel 8 timer connection register (TCNR), and using this in combination with the down-counters (DCNT8I to DCNT8P). An interrupt can be requested on the occurrence of the respective input capture or compare-match.

In addition, channel 2 has a 16-bit dedicated input capture register (OSBR2). The channel 0 TIOA input pin can also be used as the OSBR2 trigger input, enabling use of a twin-capture function.

**Channels 3 to 5:** Channels 3 to 5 each have a 16-bit free-running counter (TCNT3 to TCNT5) and four 16-bit general registers (GR3A to GR3D, GR4A to GR4D, GR5A to GR5D). TCNT3 to TCNT5 are up-counters that perform free-running operation. Channels 3 to 5 each have a 16-bit free-running counter (TCNT3 to TCNT5) and four 16-bit general registers (GR3A to GR3D, GR4A to GR4D, GR5A to GR5D). TCNT3 to TCNT5 are up-counters that perform free-running operation. In addition, counter clearing can be performed by compare-match by making a setting in the timer I/O control register (TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, TIOR5B). Each counter can generate an interrupt request when it overflows.

The four general registers (GR3A to GR3D, GR4A to GR4D, GR5A to GR5D) each have corresponding external signal I/O pins (TIO3A to TIO3D, TIO4A to TIO4D, TIO5A to TIO5D), and can be used as input capture or output compare registers. When used for input capture, the free-running counter (TCNT3 to TCNT5) value is captured by means of input from the corresponding external signal I/O pin (TIO3A to TIO3D, TIO4A to TIO4D, TIO5A to TIO5D). Rising edge, falling edge, or both edges can be selected for the input capture signal in the timer I/O control registers (TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, TIOR5B). Also, in use for input capture, input capture can be performed using a compare-match between a channel 9 event counter (ECNT9A to ECNT9D), described later, and a general register (GR9A to GR9D) as the trigger. In this case, capture is performed even if an input capture disable setting has been made for TIOR3A to TIOR3D. When used for output compare, compare-match with the free-running counter (TCNT3 to TCNT5) is performed. For the output from the external signal I/O pins by compare-match, 0 output, 1 output, or toggle output can be selected in the timer I/O control registers (TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, TIOR5B). An interrupt can be requested on the occurrence of the respective input capture or compare-match. However, in the case of input capture using channel 9 as a trigger, an interrupt request from channel 3 cannot be used.

By selecting PWM mode in the timer mode register (TMDR), PWM output can be obtained, with three outputs for each. In this case, GR3D, GR4D, and GR5D are automatically used as cycle registers, and GR3A to GR3C, GR4A to GR4C, GR5A to GR5C, as duty registers. TCNT3 to TCNT5 are cleared by the corresponding GR3D, GR4D, or GR5D compare-match.

**Channels 6 and 7:** Channels 6 and 7 each have 16-bit free-running counters (TCNT6A to TCNT6D, TCNT7A to TCNT7D), 16-bit cycle registers (CYLR6A to CYLR6D, CYLR7A to CYLR7D), 16-bit duty registers (DTR6A to DTR6D, DTR7A to DTR7D), and buffer registers (BFR6A to BFR6D, BFR7A to BFR7D). Channels 6 and 7 also each have external output pins (TO6A to TO6D, TO7A to TO7D), and can be used as buffered PWM timers. The TCNT registers are up-counters, and 0 is output to the corresponding external output pin when the TCNT value matches the DTR value (when  $DTR \neq CYLR$ ). When the TCNT value matches the CYLR value (when  $DTR \neq H'0000$ ), 1 is output to the external output pin, TCNT is initialized to H'0001, and the BFR value is transferred to DTR. Thus, the configuration of channels 6 and 7 enables them to perform waveform output with the CYLR value as the cycle and the DTR value as the duty, and to use BFR to absorb the time lag between setting of data in DTR and compare-match occurrence.

When  $DTR = CYLR$ , 1 is output continuously to the external output pin, giving a duty of 100%. When  $DTR = H'0000$ , 0 is output continuously to the external output pin, giving a duty of 0%. Do not set a value in DTR that will result in the condition  $DTR > CYLR$ .

In channel 6, TCNT can also be designated for complementary PWM output by means of the PWM mode register (PMDR). When the corresponding TSTR is set to 1, TCNT starts counting up, then switches to a down-count when the count matches the CYLR value. When TCNT reaches H'0000, it starts counting up again. When  $TCNT = DTR$ , the corresponding TO6A to TO6D output changes. Whether TCNT is counting up or down can be ascertained from the timer status register (TSR6).

DMAC activation and interrupt request generation, respectively, are possible when  $TCNT = CYLR$  in asynchronous PWM mode, and when  $TCNT = H'0000$  in complementary PWM mode.

**Channel 8:** Channel 8 has sixteen 16-bit down-counters (DCNT8A to DCNT8P). The down-counters have corresponding external signal output pins, and can generate one-shot pulses. Setting a value in DCNT and setting the corresponding bit to 1 in the down-count start register (DSTR) starts DCNT operation and simultaneously outputs 1 to the external output pin. When DCNT counts down to H'0000, it stops and outputs 0 to the external output pin. An interrupt can be requested when DCNT underflows.

Down-counter operation can be coupled with the channel 1 or channel 2 output compare function by means of settings in the timer connection register (TCNR) and one-shot pulse terminate register (OTR), respectively, so that DCNT8I to DCNT8H count operations are started and stopped from channel 1, and DCNT8I to DCNT8P count operations from channel 2.

DCNT8I to DCNT8P have a reload register (RLDR), and a setting in the reload enable register (RLDEN) enables count operations to be started after reading the value from this register.

**Channel 9:** Channel 9 has six 8-bit event counters (ECNT9A to ECNT9F) and six 8-bit general registers (GR9A to GR9F). The event counters are up-counters, each with a corresponding external input pin (ECNT9A to ECNT9F). The event counter value is incremented by input from

the corresponding external input pin. Incrementing on the rising edge, falling edge, or both edges can be selected by means of settings in the timer control registers (TCR9A to TCR9C). An event counter is cleared by edge input after a match with the corresponding general register. An interrupt can be requested when an event counter is cleared.

Timer control register (TCR9A, TCR9B) settings can be made to enable event counters ECNT9A to ECNT9D to send a compare-match signal to channel 3 when the count matches the corresponding general register (GR9A to GR9D), allowing input capture to be performed on channel 3. This enables the pulse input interval to be measured.

**Channel 10:** Channel 10 generates a multiplied clock based on external input, and supplies this to channels 1 to 5. Channel 10 is divided into three blocks: (1) an inter-edge measurement block, (2) a multiplied clock generation block, and (3) a multiplied clock correction block.

#### (1) Inter-edge measurement block

This block has a 32-bit free-running counter (TCNT10A), 32-bit input capture register (ICR10A), 32-bit output compare register (OCR10A), 8-bit event counter (TCNT10B), 8-bit output compare register (OCR10B), 8-bit noise canceler counter (TCNT10H), and 8-bit noise canceler compare-match register (NCR10).

The 32-bit free-running counter (TCNT10A) is an up-counter that performs free-running operations. When input capture is performed by means of TI10 input, this counter is cleared to H'00000001. When free-running counter (TCNT10A) reaches the value set in the output compare register (OCR10A), a compare-match interrupt can be requested.

The input capture register (ICR10A) has an external signal input pin (TI10), and the free-running counter (TCNT10A) value can be captured by means of input from TI10. Rising edge, falling edge, or both edges can be selected by making a setting in bits CKEG1 and CKEG0 in the timer control register (TCR10). The TI10 input has a noise canceler function, which can be enabled by setting the NCE bit in the timer control register (TCR10). When the counter value is captured, TCNT10A is cleared to 0 and an interrupt can be requested. The captured value can be transferred to the multiplied clock generation block reload register (RLD10C).

The 8-bit event counter (TCNT10B) is an up-counter that is incremented by TI10 input. When the event counter (TCNT10B) value reaches the value set in the output compare register (OCR10B), a compare-match interrupt can be requested. By setting the TRG0DEN bit in the timer control register (TCR10), a capture request can also be issued for the channel 0 input capture register 0D (ICR0D) when compare-match occurs.

The 8-bit noise canceler counter (TCNT10H) and 8-bit noise canceler compare-match register (NCR10) are used to set the period for which the noise canceler functions. By setting a value in the noise canceler compare-match register (TCNT10H) and setting the NCE bit in the timer control register (TCR10), TI10 input is masked when it occurs. At the same time as TI10 input is masked, the noise canceler counter (TCNT10H) starts counting up on the Pφx10 clock.

When the noise canceler counter (TCNT10H) value matches the noise canceler compare-match register (NCR10) value, the noise canceler counter (TCNT10H) is cleared to H'0000 and TI10 input masking is cleared.

## (2) Multiplied clock generation block

This block has 16-bit reload counters (TCNT10C, RLD10C), a 16-bit register free-running counter (TCNT10G), and a 16-bit general register (GR10G).

16-bit reload counter 10C (RLD10C) is captured by 32-bit input capture register 10A (ICR10A), and when RLDEN in the timer I/O control register (TIOR10) is 0, the value captured in input capture register 10A is transferred to the multiplied clock generation block reload register (RLD10C). The value transferred can be selected from 1/32, 1/64, 1/128, or 1/256 the original value, according to the setting of bits PIM1 and PIM0 in TIOR10.

16-bit reload counter 10C (TCNT10C) performs down-count operations. When TCNT10C reaches H'0001, the value is read automatically from the reload buffer (RLD10C), internal clock AGCK1 is generated, and the down-count operation is repeated. Internally generated AGCK1 is input as a clock to the multiplied clock correction block 16-bit correction counter (TCNT10E) and 16-bit free-running counter 10G (TCNT10G).

16-bit register free-running counter 10G (TCNT10G) counts on AGCK1 generated by TCNT10C. It is initialized to H'0000 by external input from TI10.

The 16-bit general register (GR10G) can be used in a compare-match with free-running counter 10G (TCNT10G) by setting bits IO10G2 to IO10G0 in the timer I/O control register (TIOR10). An interrupt can be requested when a compare-match occurs. Also, by setting timer interrupt enable register 10 (TIER10), an interrupt can be request in the event of TI10 input after a compare-match.

## (3) Multiplied clock correction block

This block has three 16-bit correction counters (TCNT10D, TCNT10E, TCNT10F) and a 16-bit correction counter clear register (TCCLR10). When 32-bit input capture register 10A (ICR10A) performs a capture operation due to input from external input pin TI10, the value in correction counter 10D (TCNT10D) is transferred to TCNT10E and TCNT10D is incremented. The value transferred to TCNT10E is 32, 64, 128, or 256 times the TCNT10D value, according to the setting of bits PIM1 and PIM0 in the timer I/O control register (TIOR10).

16-bit correction counter 10E (TCNT10E) counts up on AGCK1 generated by reload counter 10C (TCNT10C, RLD10C) in the multiplied clock generation block. However, by setting the CCS bit in the timer I/O control register (TIOR10), it is possible to stop free-running counter 10E (TCNT10E) when the free-running counter 10D (TCNT10D) multiplication value specified by PIM1 and PIM0 and the free-running counter 10E (TCNT10E) value match. The multiplied TCNT10D value is transferred when input capture register 10A (ICR10A) performs a capture operation due to TI10 input.

16-bit correction counter 10F (TCNT10F) has  $P\phi$  as its input and is constantly compared with 16-bit correction counter 10E (TCNT10E). When the 16-bit correction counter 10F (TCNT10F) value is smaller than that in 16-bit correction counter 10E (TCNT10E), it is incremented and generates count-up AGCKM. When the 16-bit correction counter 10F (TCNT10F) value exceeds that in 16-bit correction counter 10E (TCNT10E) (for example, when TCNT10F reloads TCNT10D), no count-up operation is performed. The TI10 multiplied signal (AGCKM) generated when TCNT10F is incremented is output to the channel 1 to 5 free-running counters (TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3, TCNT4, TCNT5), and an up-count can be performed on AGCKM by setting this as the counter clock on each channel. TCNT10F is constantly compared with the 16-bit correction counter clear register (TCCLR10), and when the free-running counter 10F (TCNT10F) and correction counter clear register (TCCLR10) values match, the TCNT10F up-count stops. Setting TRG1AEN, TRG1BEN, TRG2AEN, and TRG2BEN in the timer control register (TCR10) enables the channel 1 and 2 free-running counters (TCNT1A, TCNT1B, TCNT2A, TCNT2B) to be cleared at this time. If TI10 is input when TCNT10D = H'0000, initialization and correction operations are performed. When TCNT10F = TCCLR10, TCNT10F is cleared to H'0001. When TCNT10F  $\neq$  TCCLR10, TCNT10F automatically counts up to the TCCLR10 value, and is cleared to H'0001.

**Channel 11:** Channel 11 has a 16-bit free-running counter (TCNT11) and two 16-bit general registers (GR11A, GR11B). TCNT11 is an up-counter that performs free-running operation. The counter can generate an interrupt request when it overflows. When the two general registers (GR11A, GR11B) are designated for compare-match use, a compare-match signal can be output to the APC.

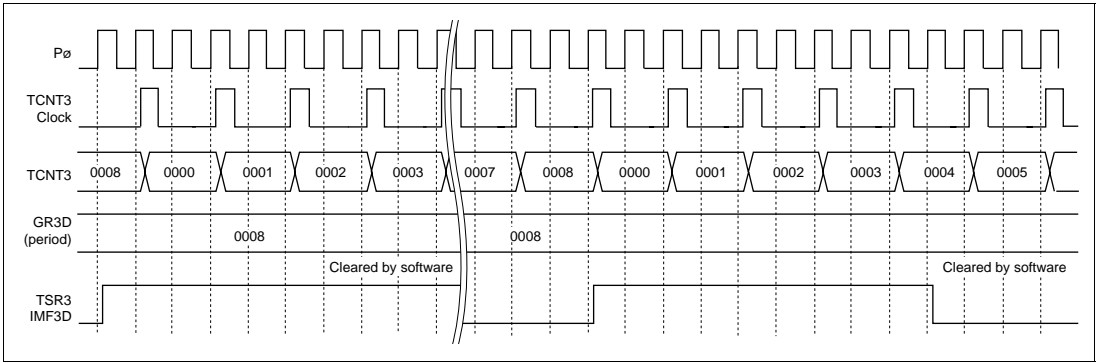
**Prescaler:** The ATU-II has a dedicated prescaler with a 2-stage configuration. The first stage comprises 5-bit prescalers (PSCR1 to PSCR4) that generate a  $1/m$  clock (where  $m = 1$  to 32) with respect to clock  $P\phi$ . The second prescaler stage allows selection of a clock obtained by further scaling the clock from the first stage by  $2^n$  (where  $n = 0$  to 5) according to the timer control registers for the respective channels (TCR1A, TCR1B, TCR2A, TCR2B, TCR3 to TCR5, TCR6A, TCR6B, TCR7A, TCR7B, TCR8, TCR11).

The prescalers of channels 1 to 8 and 11 have a 2-stage configuration, while the channel 0 and 10 prescalers only have a first stage. The first-stage prescaler is common to channels 0 to 5, 8, and 11, and it is not possible to set different first-stage division ratios for each. Channels 6, 7, and 10 each have a first-stage prescaler, and different first-stage division ratios can be set for each.

### 10.3.2 Free-Running Counter Operation and Cyclic Counter Operation

The free-running counters (TCNT) in ATU-II channels 0 to 5 and 11 start counting up as free-running counters when the corresponding timer start register (TSTR) bit is set to 1. When TCNT overflows (channel 0: from H'FFFFFFFF to H'00000000; channels 1 to 5 and 11: from H'FFFF to H'0000), the OVF bit in the timer status register (TSR) is set to 1. If the OVE bit in the





**Figure 10.14 Example of Cyclic Counter Operation**

### 10.3.3 Compare-Match Function

Designating general registers in channels 1 to 5 (GR1A to GR1H, GR2A to GR2H, GR3A to GR3D, GR4A to GR4D, GR5A to GR5D) for compare-match operation in the timer I/O control registers (TIOR1 to TIOR5) enables compare-match output to be performed at the corresponding external pins (TIO1A to TIO1H, TIO2A to TIO2H, TIO3A to TIO3D, TIO4A to TIO4D, TIO5A to TIO5D).

A free-running counter (TCNT) starts counting up when 1 is set in the timer status register (TSTR). When the desired number is set beforehand in GR, and the TCNT value matches the GR value, the timer status register (TSR) bit corresponding to GR is set and a waveform is output from the corresponding external pin.

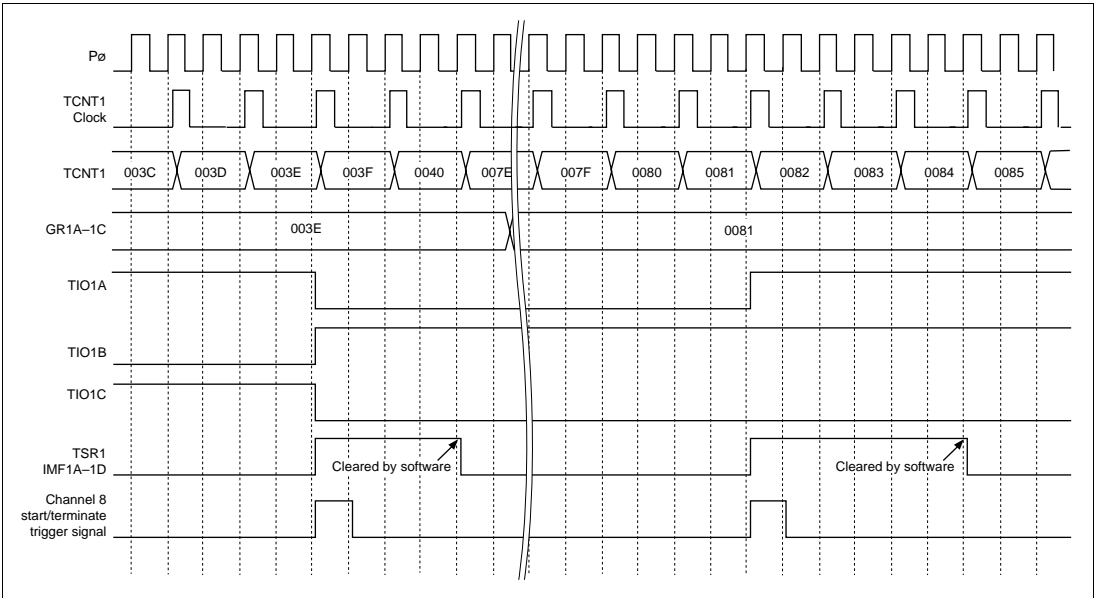
1 output, 0 output, or toggle output can be selected by means of a setting in TIOR. If the appropriate interrupt enable register (TIER) setting is made, an interrupt request will be sent to the CPU when a compare-match occurs.

Channel 1 and 2 compare-match registers (OCR1, OCR2A to OCR2H) perform compare-match operations unconditionally. However, there are no corresponding output pins. If the appropriate TIER setting is made, an interrupt request will be sent to the CPU when a compare-match occurs.

Channel 1 and 2 GR and OCR registers can send a trigger/terminate signal to channel 8 when a compare-match occurs. In this case, settings should be made in the trigger mode register (TRGMDR), timer connection register (TCNR), and one-shot pulse terminate register (OTR).

An example of compare-match operation is shown in figure 10.15.

In the example in figure 10.15, channel 1 is activated, and external output is performed with toggle output specified for GR1A, 1 output for GR1B, and 0 output for GR1C.



**Figure 10.15 Compare-Match Operation**

### 10.3.4 Input Capture Function

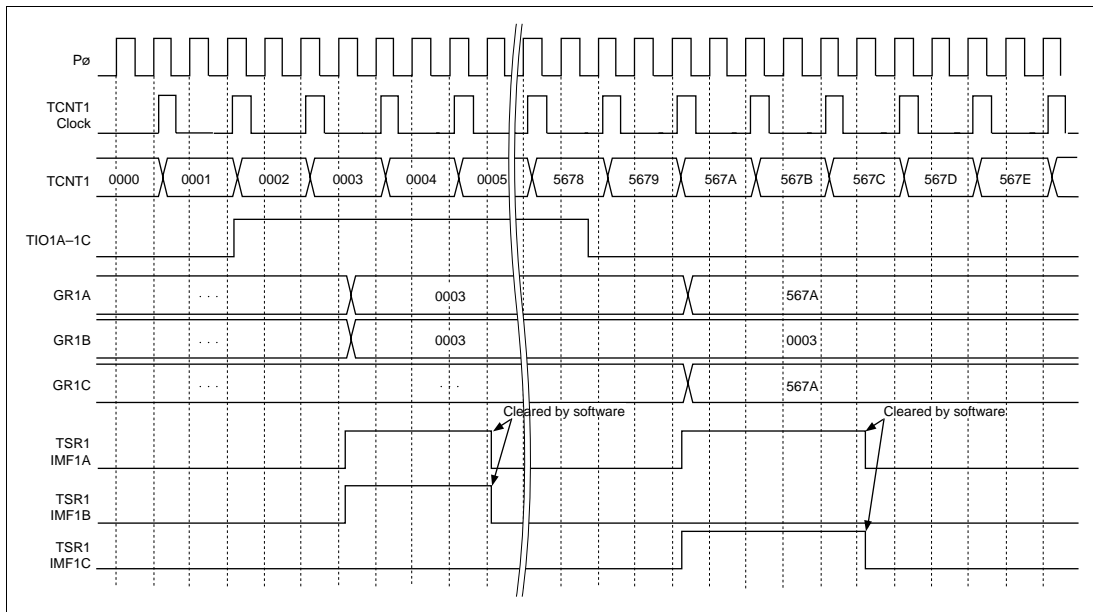
If input capture registers (ICR0A to ICR0D) and general registers (GR1A to GR1H, GR2A to GR2H, GR3A to GR3D, GR4A to GR4D, GR5A to GR5D) in channels 0 to 5 and 11 are designated for input capture operation in the timer I/O control registers (TIOR0 to TIOR5), input capture is performed when an edge is input at the corresponding external pins (TIOA to TIOD, TIO1A to TIO1H, TIO2A to TIO2H, TIO3A to TIO3D, TIO4A to TIO4D, TIO5A to TIO5D).

A free-running counter (TCNT) starts counting up when a setting is made in the timer start register (TSTR). When an edge is input at an external pin corresponding to ICR or GR, the corresponding timer status register (TSR) bit is set and the TCNT value is transferred to ICR or GR. Rising-edge, falling-edge, or both-edge detection can be selected. By making the appropriate setting in the interrupt enable register (TIER), an interrupt request can be sent to the CPU.



An example of input capture operation is shown in figure 10.16.

In the example in figure 10.16, channel 1 is activated, and input capture operation is performed with both-edge detection specified for TIO1A, rising-edge detection for TIO1B, and falling-edge detection for TIO1C.



**Figure 10.16 Input Capture Operation**

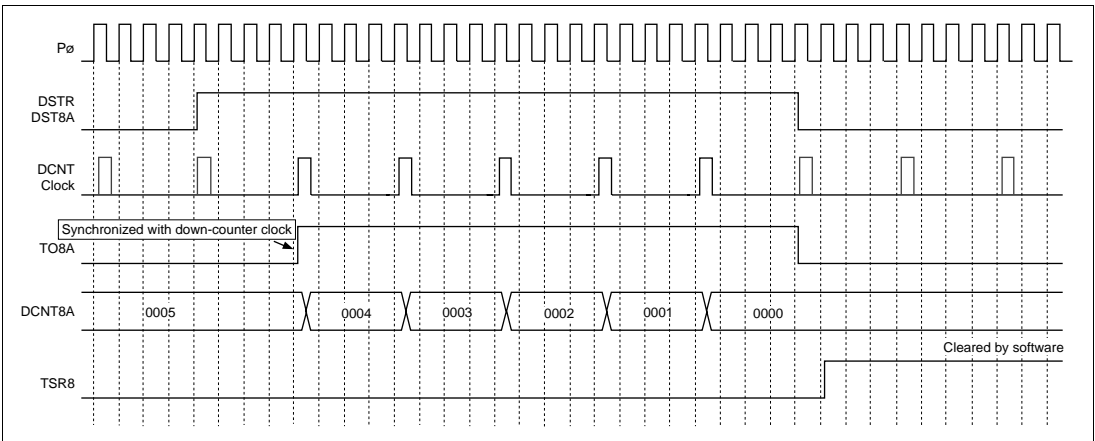
### 10.3.5 One-Shot Pulse Function

Channel 8 has sixteen down-counters (DCNT8A to DCNT8P) and corresponding external pins (TO8A to TO8P) which can be used as one-shot pulse output pins.

When a value is set beforehand in DCNT and the corresponding bit in the down-counter start register (DSTR) is set, DCNT starts counting down, and at the same time 1 is output from the corresponding external pin. When DCNT reaches H'0000 the down-count stops, the corresponding bit in the timer status register (TSR) is set, and 0 is output from the external pin. The corresponding bit in DSTR is cleared automatically. By making the appropriate setting in the interrupt enable register (TIER), an interrupt request can be sent to the CPU.

An example of one-shot pulse operation is shown in figure 10.17.

In the example in figure 10.17, H'0005 is set in DCNT and a down-count is started.



**Figure 10.17 One-Shot Pulse Output Operation**

### 10.3.6 Offset One-Shot Pulse Function and Output Cutoff Function

By making an appropriate setting in the timer connection register (TCNR), down-counting by channel 8 down-counters (DCNT8A to DCNT8P) can be started using compare-match signals from channel 1 general registers (GR1A to GR1H) or channel 1 and 2 compare-match registers (OCR1, OCR2A to OCR2H). DCNT8A to DCNT8H are connected to channel 1 OCR1 or GR1A to GR1H, and DCNT8I to DCNT8P are connected to channel 2 OCR2A to OCR2H or GR2A to GR2H. This enables one-shot pulse output from the external pin (TO8A to TO8P) corresponding to DCNT. The down-count can be forcibly stopped by making a setting in the one-shot pulse terminate register (OTR). On channel 1, down-count start or termination by a GR or OCR compare-match can be selected with the trigger mode register (TRGMDR).

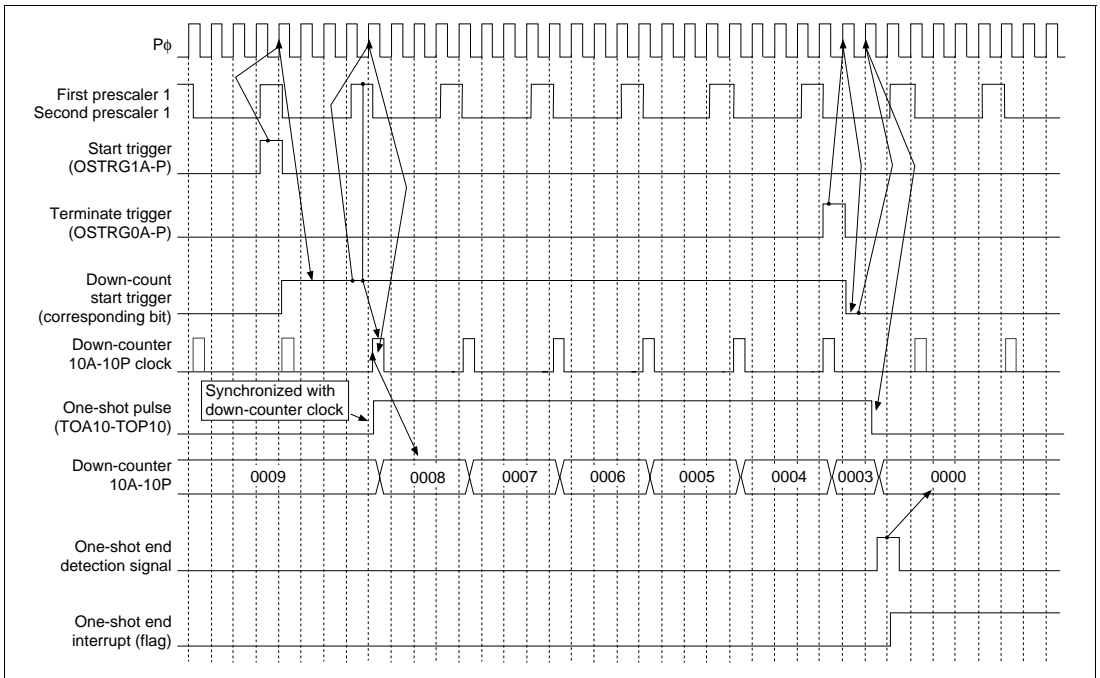
Making a setting in the timer start register (TSTR) starts an up-count by a free-running counter (TCNT) in channel 1 or 2. When TCNT matches GR or OCR while connection is enabled by TCNR, the corresponding DSTR is automatically set and DCNT starts counting down. At the same time, 1 is output from the corresponding external pin (TO8A to TO8P). By making the appropriate setting in the interrupt enable register (TIER), an interrupt request can be sent to the CPU.

When TCNT1 matches GR or OCR, or TCNT2 matches GR, while channel 8 one-shot pulse termination by a channel 1 or 2 compare-match signal is enabled by OTR, the corresponding DSTR is automatically cleared and DCNT stops counting down. DCNT is cleared to H'0000 at this time, and must be rewritten before the down-count is restarted.

DCNT8I to DCNT8P are connected to the reload register (RLDR8), and when the DSTR corresponding to DCNT8I to DCNT8P is set, the DCNT8I to DCNT8P counter loads RLDR8 before starting the down-count.

An example of the offset one-shot pulse output function and output cutoff function is shown in figure 10.18.

In the example shown in this figure, DCNT8I is started by OCR2A of channel 2, and DCNT8I output is cut off by GR2A.



**Figure 10.18 Offset One-Shot Pulse Output Function and Output Cutoff Operation**

### 10.3.7 Interval Timer Operation

The interval interrupt request registers (ITVRR1, ITVRR2A, ITVRR2B) are connected to bits 6 to 9 and 10 to 13 of the channel 0 free-running counter (TCNT0). The ITVRR registers are 8-bit registers; the upper 4 bits (ITVA) are used for A/D converter activation, and the lower 4 bits (ITVE) are used for interrupt requests. ITVRR1 is connected to A/D converter 2 (AD2), ITVRR2A to A/D converter 0 (AD0), and ITVRR2B to A/D converter 1 (AD1).

When the ITVA bit for the desired timing is set, the A/D converter is activated when the corresponding bit of TCNT0 changes to 1.

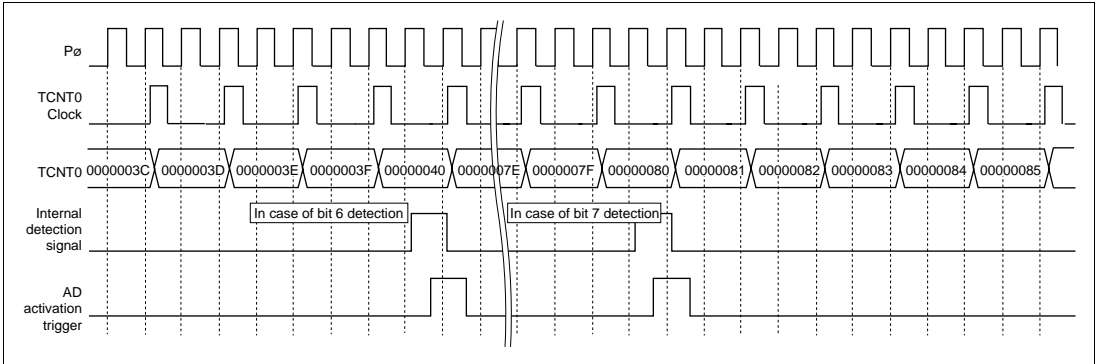
When the ITVE bit for the desired timing is set, an interrupt can be requested when the corresponding bit of TCNT0 changes to 1. At this time, the corresponding bit of the timer status

register (TSR0) is set. There are four interrupt sources for the respective ITVRR registers, but there is only one interrupt vector.

To suppress interrupts and A/D converter activation, ITVRR bits should be cleared to 0.

An example of interval timer function operation is shown in figure 10.19.

In the example in figure 10.19, TCNT0 is started by setting ITVE to 1 in ITVRR1.



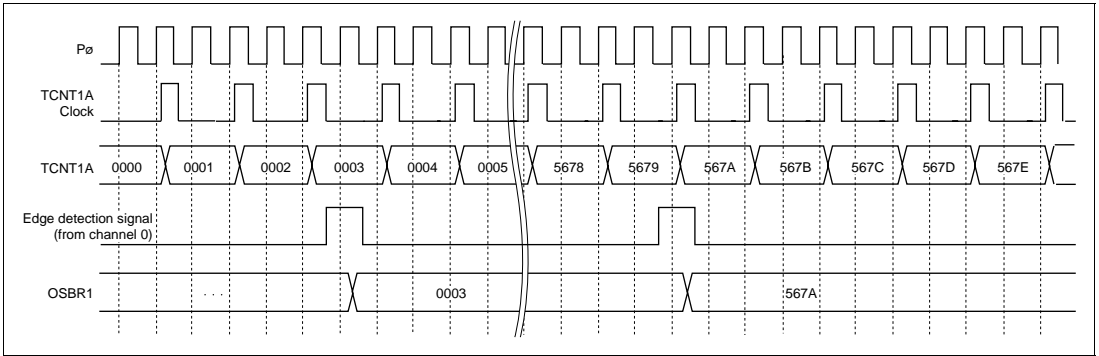
**Figure 10.19 Interval Timer Function**

### 10.3.8 Twin-Capture Function

Channel 0 input capture register (ICR0A), channel 1 offset base register 1 (OSBR1), and channel 2 offset base register 2 (OSBR2) can be made to perform input capture in response to the same trigger by means of a setting in timer I/O control register 0 (TIOR0).

When TCNT0, TCNT1A, and TCNT2A in channel 0, channel 1, and channel 2 are started by a setting in the timer status register (TSR), and an edge is input to ICR0A, the TCNT1A value is transferred to OSBR1, and the TCNT2A value to OSBR2. Edge detection is as described in section 10.3.4, Input Capture Function.

An example of twin-capture operation is shown in figure 10.20.



**Figure 10.20 Twin-Capture Operation**

### 10.3.9 PWM Timer Function

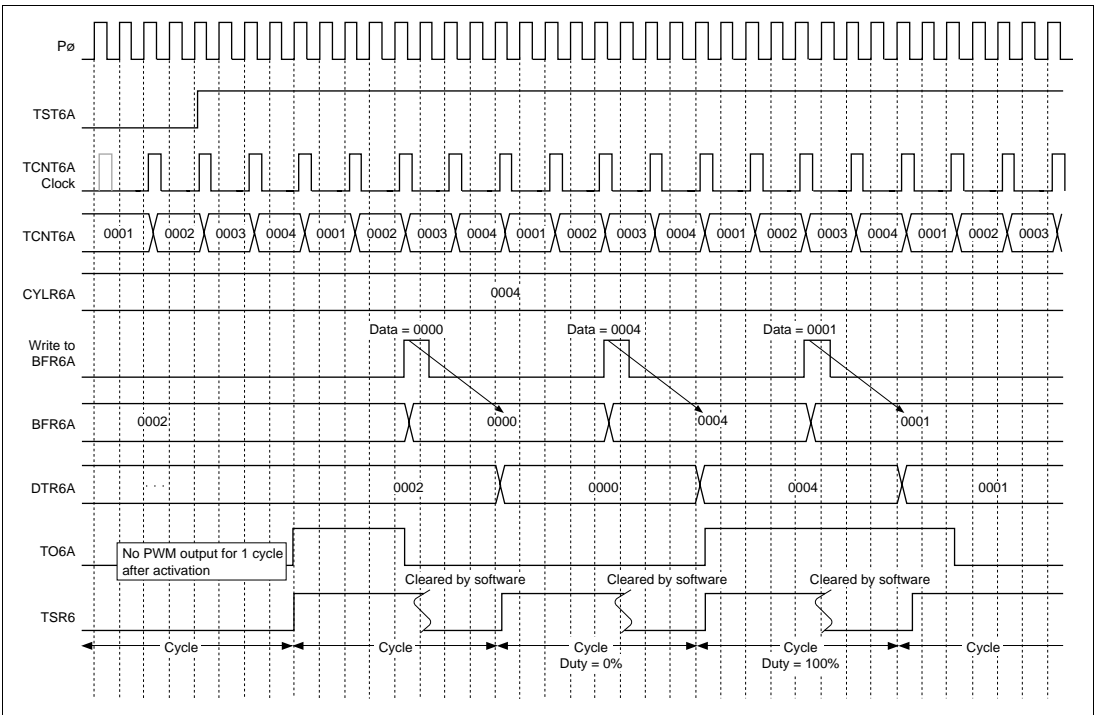
Channels 6 and 7 can be used unconditionally as PWM timers using external pins (TO6A to TO6D, TO7A to TO7D).

In channels 6 and 7, when the corresponding bit is set in the timer start register (TSTR) and the free-running counter (TCNT) is started, the counter counts up until its value matches the corresponding cycle register (CYLR). When TCNT matches CYLR, it is cleared to H'0001 and starts counting up again from that value. At this time, 1 is output from the corresponding external pin. An interrupt request can be sent to the CPU by setting the corresponding bit in the timer interrupt enable register (TIER). If a value has been set in the duty register (DTR), when TCNT matches DTR, 0 is output to the corresponding external pin. If the DTR value is H'0000, the output does not change (0% duty). A duty of 100% is specified by setting  $DTR = CYLR$ . Do not set a value in DTR that will result in the condition  $DTR > CYLR$ .

Channels 6 and 7 have buffers (BFR); the BFR value is transferred to DTR when TCNT matches CYLR. The duty value written into BFR is reflected in the output value in the cycle following that in which BFR is written to.

An example of PWM timer operation is shown in figure 10.21.

In the example in figure 10.21, H'0004 is set in channel 6 CYLR6A, and H'0002, H'0000 (0%), H'0004 (100%), and H'0001 in BFR6A.



**Figure 10.21 PWM Timer Operation**

Channel 6 can be used in complementary PWM mode by making a setting in the PWM mode control register (PMDR). On-duty or off-duty can also be selected with a setting in PMDR.

When TCNT6 is started by a setting in TSTR, it starts counting up. When TCNT6 reaches the CYLR6 value, it starts counting down, and on reaching H'000, starts counting up again. The counter status is shown by TSR6. When TCNT6 underflows, an interrupt request can be sent to the CPU by setting the corresponding bit in TIER. When TCNT6 matches the duty register (DTR6) value, the output is inverted. The output prior to the match depends on the PMDR setting. When a value including dead time is set in DTR6, a maximum of 4-phase PWM output is possible. Data transfer from BFR6 to DTR6 is performed when TCNT6 underflows.

An example of channel 6 complementary PWM mode operation is shown in figure 10.22.

In the example in figure 10.22, H'0004 is set in channel 6 CYLR6A, and H'0002, H'0003, H'0004 (100%), and H'0000 (0%) in BFR6A.

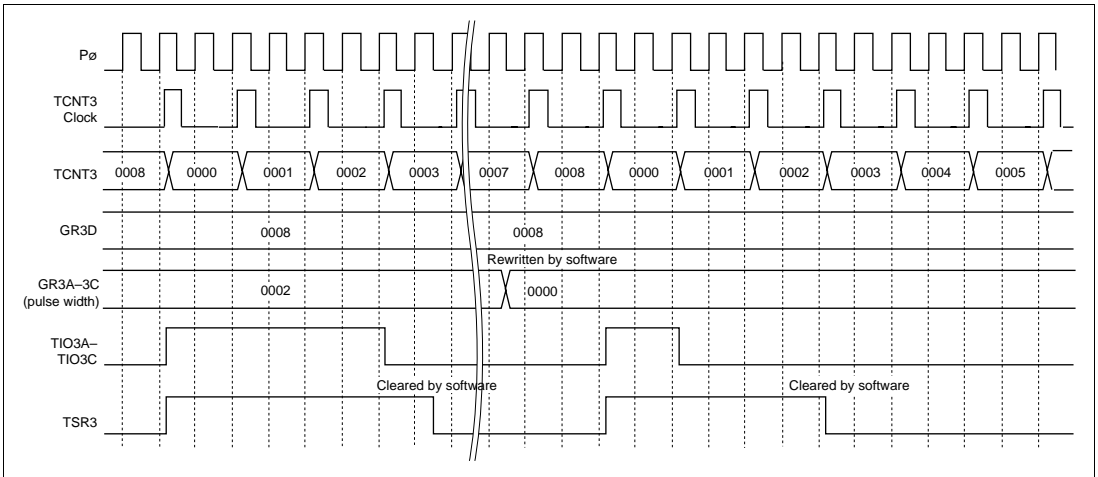


after setting H'FFFF in the cycle register, the cycle register's compare-match flag and overflow flag will be set simultaneously.

Note that 0% or 100% duty output is not possible in channel 3 to 5 PWM mode.

An example of channel 3 to 5 PWM mode operation is shown in figure 10.23.

In the example in figure 10.23, H'F0008 is set in GR3D, H'0002 is set in GR3A, GR3B, and GR3C, and channel 3 is activated; then, during operation, H'0000 is set in GR3A, GR3B, and GR3C, and output is performed to external pins TIOA3 to TIOC3. Note that 0% duty output is not possible even though H'0000 is set.



**Figure 10.23 Channel 3 to 5 PWM Mode Operation**

### 10.3.11 Event Count Function and Event Cycle Measurement

Channel 9 has six 8-bit event counters (ECNT9A to ECNT9F) and corresponding general registers (GR9A to GR9F). Each event counter has an external pin (TI9A to TI9F).

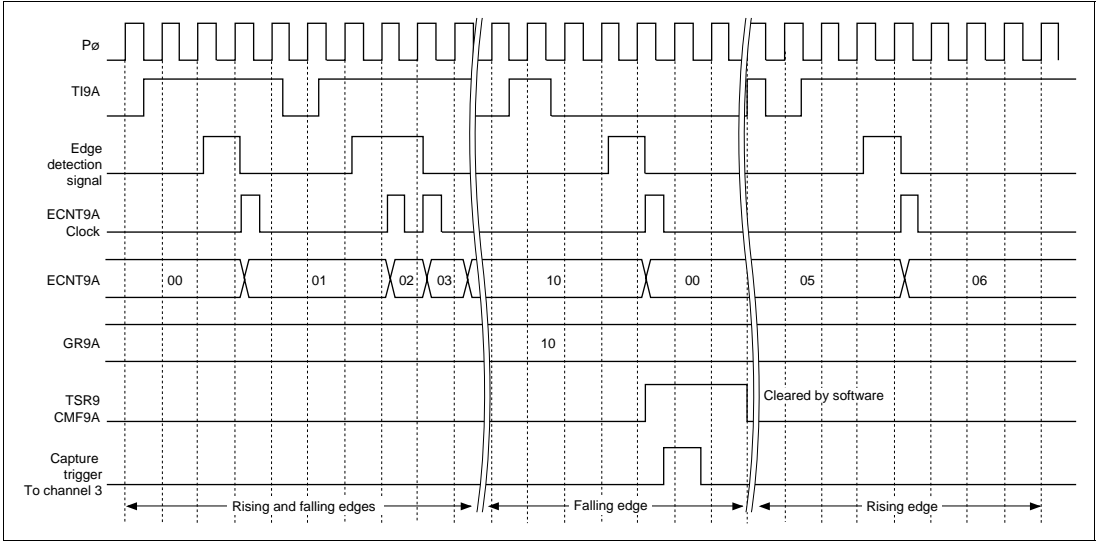
Each ECNT9 operates unconditionally as an event counter. When an edge is input from the external pin, ECNT9 is incremented. When ECNT9 matches the value set in GR9, it is cleared, and then counts up when an edge is again input at the external pin. By making the appropriate setting in the interrupt enable register (TIER) beforehand, an interrupt request can be sent to the CPU on compare-match.

For ECNT9A to ECNT9D, a trigger can be transmitted to channel 3 when a compare-match occurs. In channel 3, if the channel 9 trigger input is set in the timer I/O control register (TIOR) and the corresponding bit is set to 1 in the timer start register (TSTR), the TCNT3 value is captured in the corresponding general register (GR3A to GR3D) when an ECNT9A to ECNT9D compare-match occurs. This enables the event cycle to be measured.

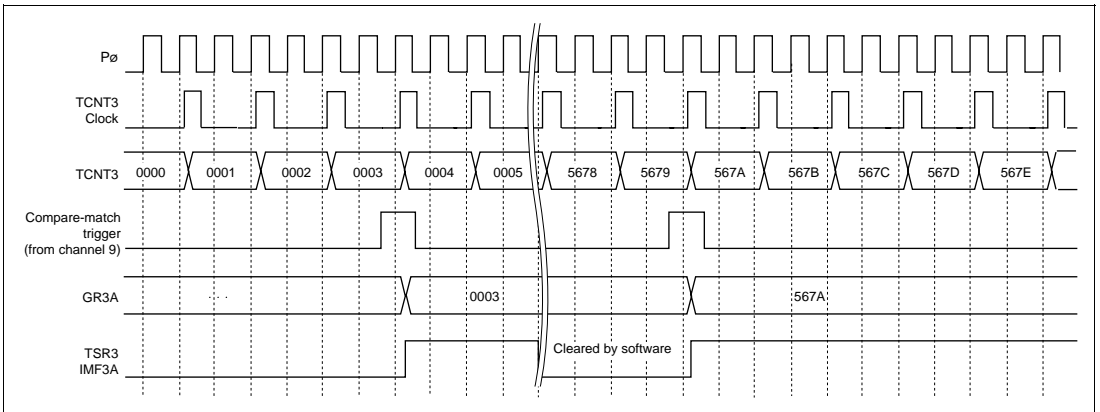


An example of event count operation is shown in figure 10.24. In this example, ECNT9A counts up on both-edge, falling-edge, and rising-edge detection, H'10 is set in GR9A, and a compare-match is generated.

An example of event cycle measurement operation is shown in figure 10.24. In this example, GR3A in channel 3 captures TCNT3 in response to a trigger from channel 9.



**Figure 10.24 Event Count Operation**



**Figure 10.25 Event Cycle Measurement Operation**

### 10.3.12 Channel 10 Functions

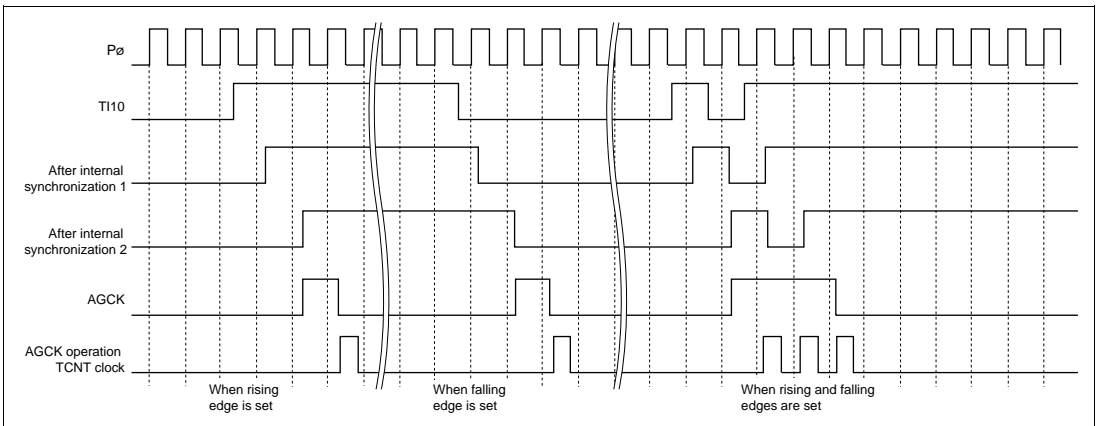
**Inter-Edge Measurement Function and Edge Input Cessation Detection Function:** 32-bit input capture register 10A (ICR10A) and 32-bit output compare register 10A (OCR10A) in channel 10 unconditionally perform input capture and compare-match operations, respectively. These registers are connected to 32-bit free-running counter TCNT10A.

When the corresponding bit is set in the timer start register (TSTR), the entire channel 10 starts operating. ICR10A has an external input pin (TI10), and when an edge is input at this input pin, ICR10A captures the TCNT10A value. At this time, TCNT10A is cleared to H'00000001. The captured value is transferred to the read register (RLD10C) in the multiplied clock generation block. By making the appropriate setting in the interrupt enable register (TIER), an interrupt request can be sent to the CPU. This allows inter-edge measurement to be carried out.

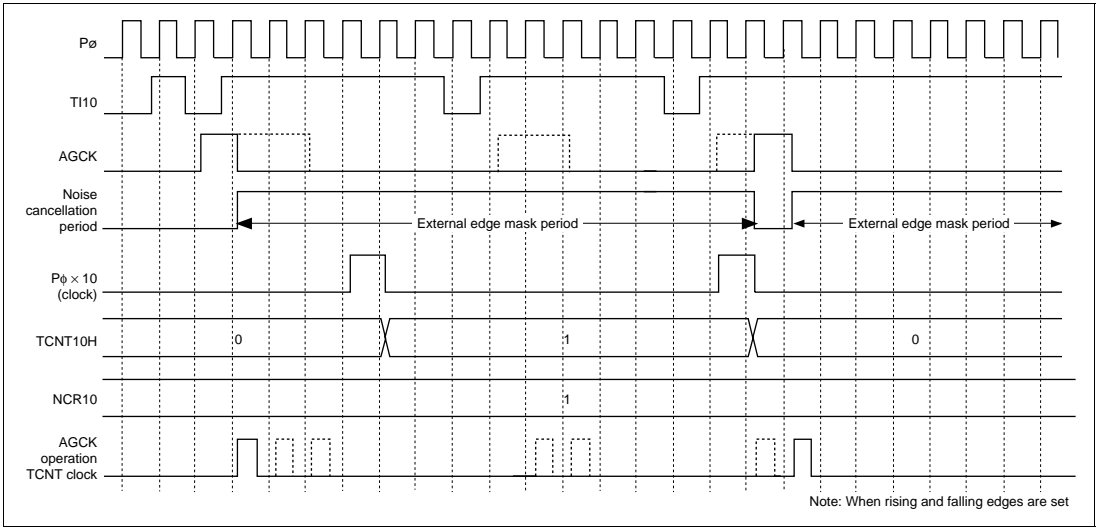
When TCNT10A reaches the value set in OCR10A, a compare-match interrupt can be requested. In this way it is possible to detect the cessation of edge input beyond the time set in OCR10A.

The input edge from TI10 is synchronized internally; the internal signal is AGCK. Noise cancellation is possible for edges input at TI10 using the timer 10H (TCNT10H) input cancellation function by setting the NCE bit in timer control register TCR10. When an edge is input at TI10, TCNT10H starts and input is disabled until it reaches compare-match register NCR10.

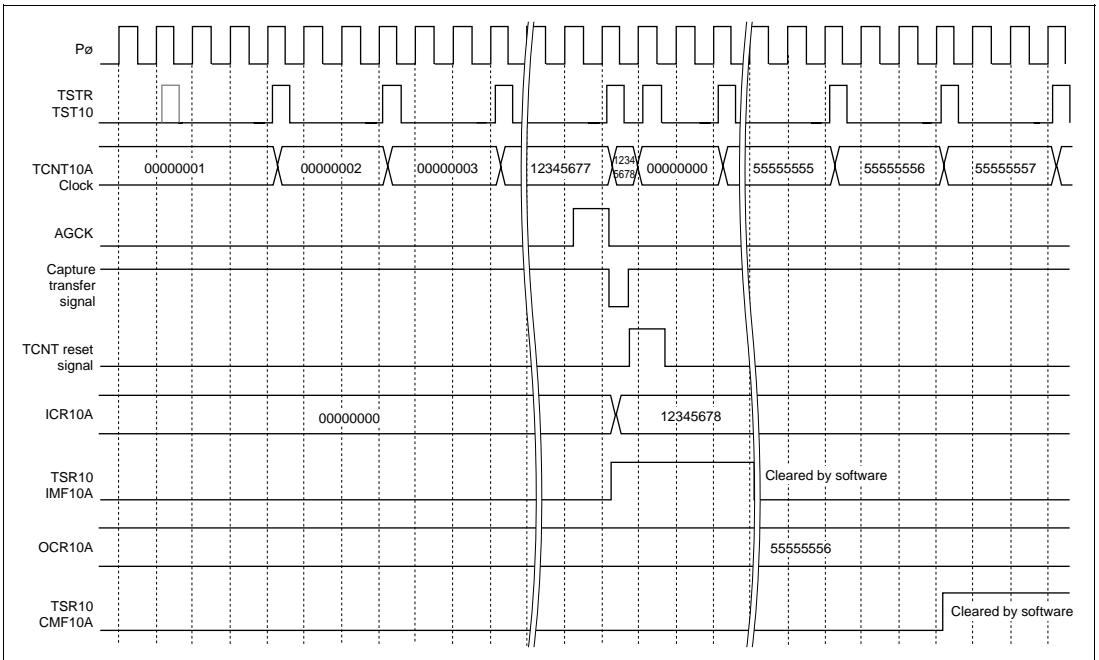
Edge input operation without noise cancellation is shown in figure 10.26, edge input operation with noise cancellation in figure 10.27, and TCNT10A capture operation and compare-match operation in figure 10.28.



**Figure 10.26 Edge Input Operation (Without Noise Cancellation)**



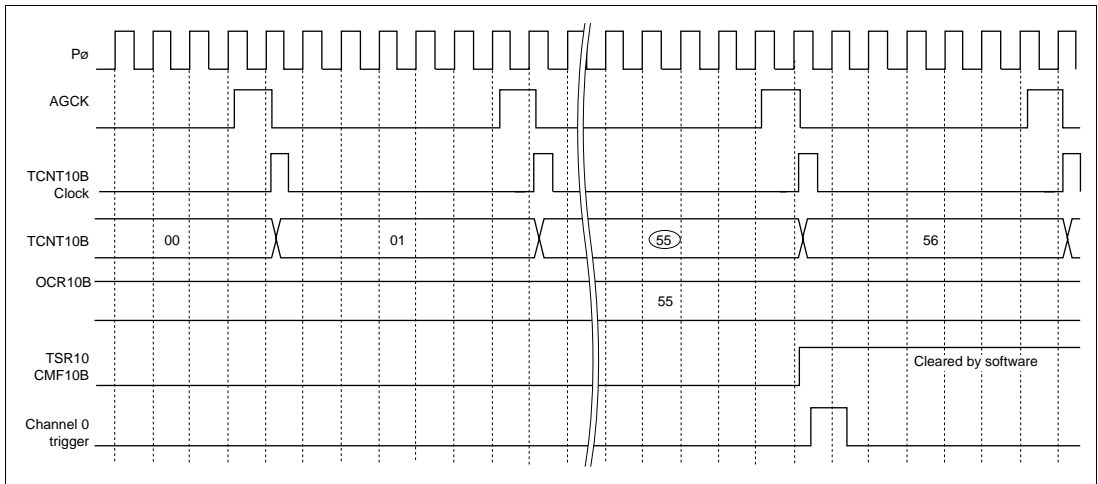
**Figure 10.27 Edge Input Operation (With Noise Cancellation)**



**Figure 10.28 TCNT10A Capture Operation and Compare-Match Operation**

Internally synchronized AGCK is counted by event count 10B (TCNT10B), and when TCNT10B reaches the value set beforehand in compare-match register 10B (OCR10B), a compare-match occurs, and the compare-match trigger signal is transmitted to channel 0. By setting the corresponding bit in TIER, an interrupt request can be sent to the CPU.

Figure 10.29 shows TCNT10B compare-match operation.



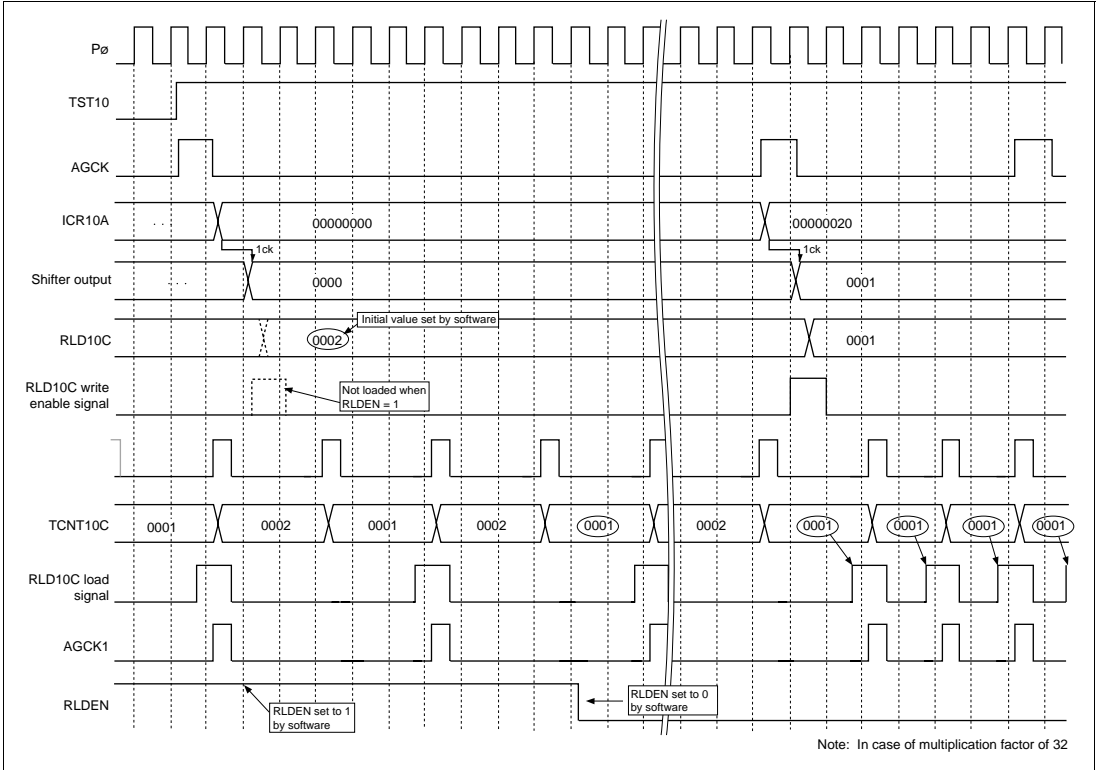
**Figure 10.29 TCNT10B Compare-Match Operation**

**Multiplied Clock Generation Function:** The channel 10 16-bit reload counter (TCNT10C, RLD10C) and 16-bit free-running counter 10G (TCNT10G) can be used to multiply the interval between edges input from external pin TI10 by 32, 64, 128, or 256.

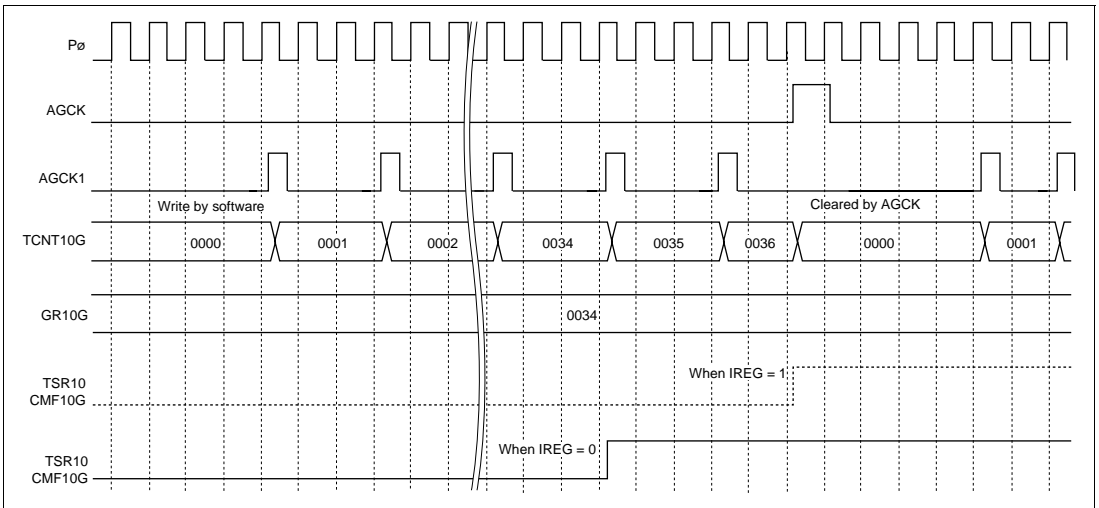
The value captured in ICR10A above is multiplied by 1/32, 1/64, 1/128, or 1/256 according to the value set in the timer I/O control register (TIOR10), and transferred to the reload buffer (RLD10C). At the same time, the same value is transferred to 16-bit reload counter 10C (TCNT10C) and a down-count operation is started. When this counter reaches H'0001, the value is read automatically from RLD10C and the down-count operation is repeated. When this reload occurs, a multiplied clock signal (AGCK1) is generated. AGCK1 is converted to a corrected clock (AGCKM) by the multiplied clock correction function described in the following section.

Channel 10 can also perform compare-match operation by means of the multiplied clock (AGCK1) using general register 10G (GR10G) and 16-bit free-running counter 10G (TCNT10G). TCNT10G is incremented unconditionally by AGCK1. By making the appropriate setting in the interrupt enable register (TIER), an interrupt request can be sent to the CPU when TCNT10G and GR10G match. The timing of this interrupt can be selected with the IREG bit in TIER as either on occurrence of the compare-match or on input of the first TI10 edge after the compare-match.

TCNT10C operation is shown in figure 10.30, and TCNT10G compare-match operation in figure 10.31.



**Figure 10.30 TCNT10C Operation**



**Figure 10.31 TCNT10G Compare-Match Operation**

**Multipled Clock Correction Function:** Channel 10's three 16-bit correction counters (TCNT10D, TCNT10E, TCNT10F) and correction counter clear register (TCCLR10) have a correction function that makes the interval between edges input from TI10 the frequency multiplication value set in TIOR10.

When AGCK is input, the value in TCNT10D multiplied by the multiplication factor set in TIOR10 is transferred to TCNT10E. At the same time, TCNT10D is incremented.

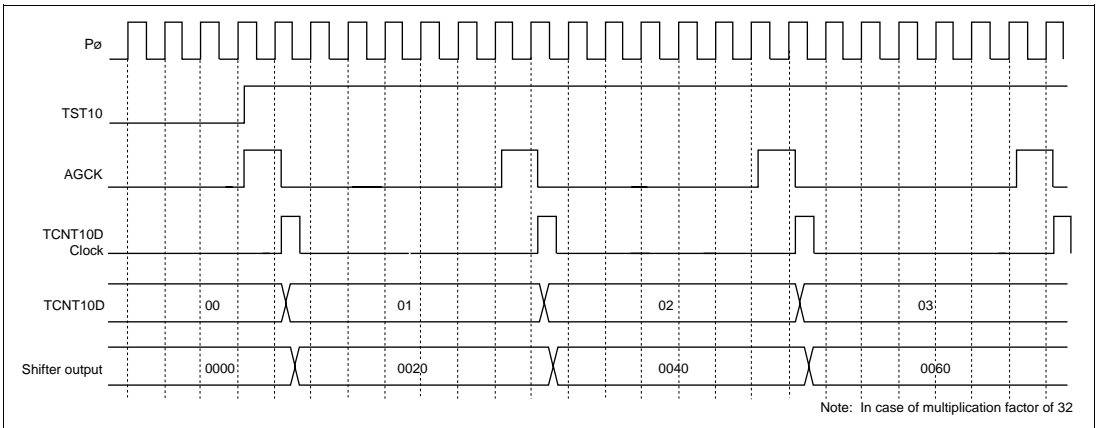
TCNT10E counts up on AGCK1. TCNT10E loads TCNT10D on AGCK, and counts up again on AGCK1. Using the counter correction select bit (CCS) in TIOR10, it is possible to select whether or not TCNT10E is halted when TCNT10D = TCNT10E.

TCNT10F has the peripheral clock (P $\phi$ ) as its input and is constantly compared with TCNT10E. When the TCNT10F value is smaller than that in TCNT10E, TCNT10F is incremented and outputs a corrected multiplied clock signal (AGCKM).

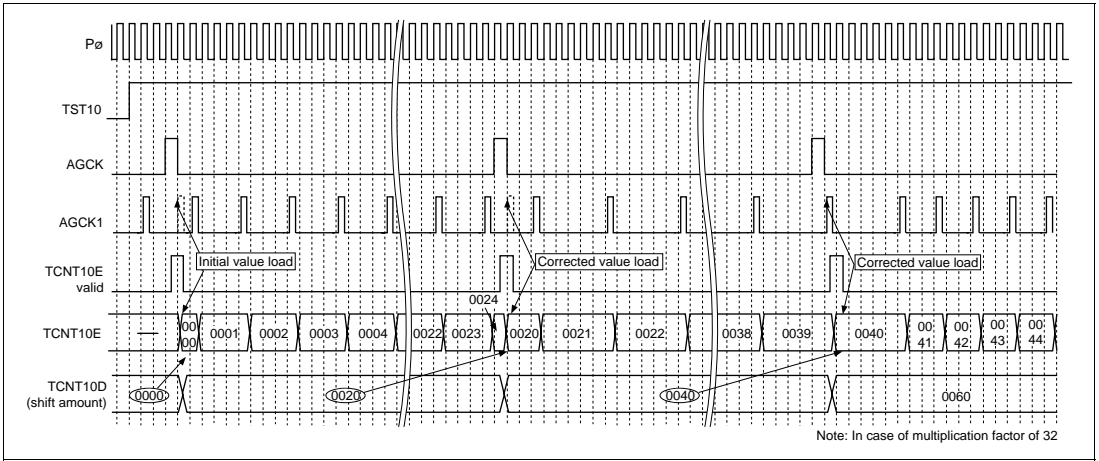
When the TCNT10E value exceeds the TCNT10F value (when TCNT10E loads TCNT10D), no count-up operation is performed. AGCKM is output to the channel 1 to 5 free-running counters (TCNT1 to TCNT5).

Channel 10 also has a correction counter clear register (TCCLR10). The correction counters (TCNT10D, TCNT10E, TCNT10F) and channel 1 and 2 free-running counters (TCNT1 and TCNT2) can be cleared when TCNT10F reaches the value set in TCCLR10.

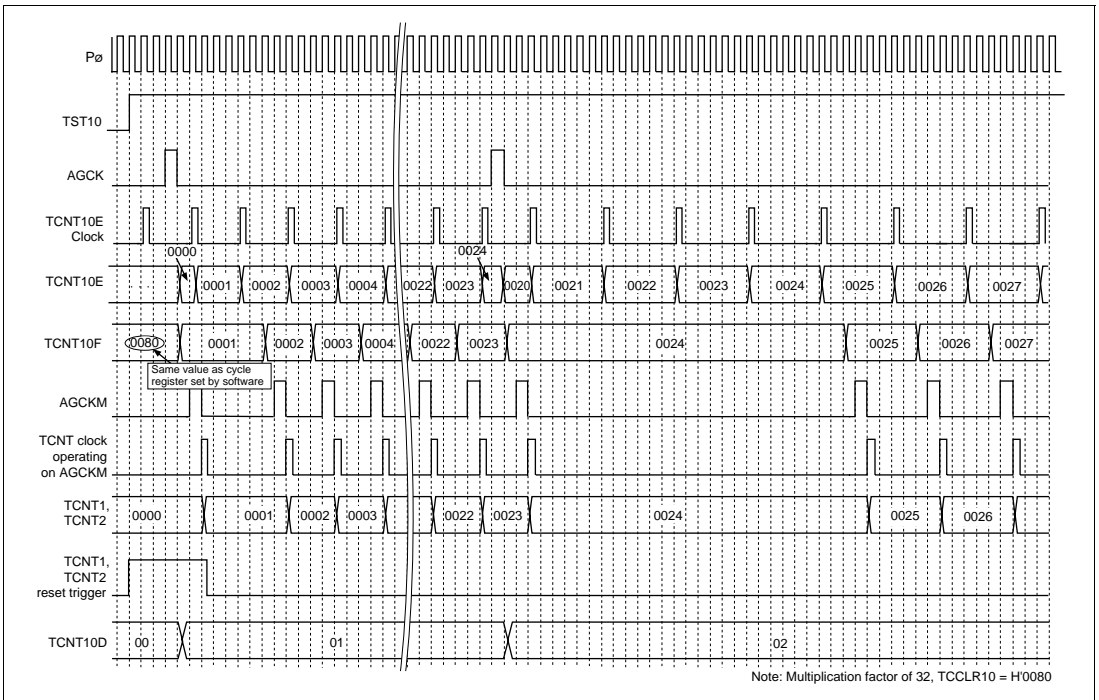
TCNT10D operation is shown in figure 10.32, TCNT10E operation in figure 10.33, TCNT10F operation (at startup) in figure 10.34, TCNT10F operation (end of cycle, with correction) in figure 10.35, and TCNT10F operation (end of cycle, without correction) in figure 10.36.



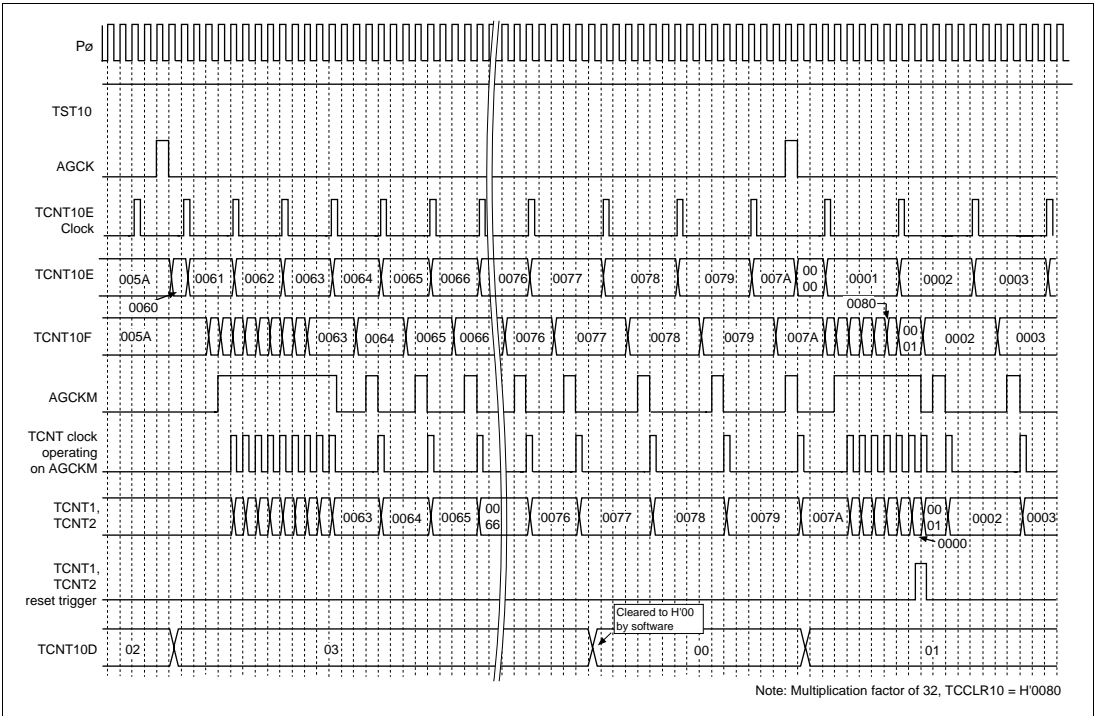
**Figure 10.32 TCNT10D Operation**



**Figure 10.33 TCNT10E Operation**

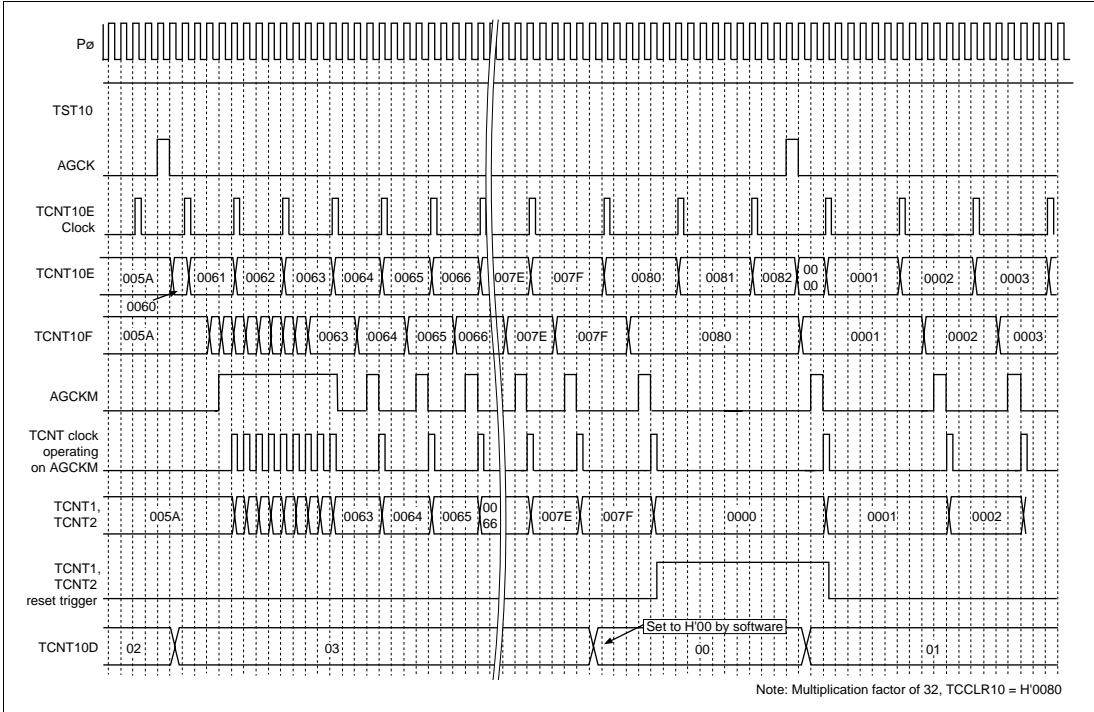


**Figure 10.34 TCNT10F Operation (At Startup)**



**Figure 10.35 TCNT10F Operation (End of Cycle, Acceleration, Deceleration)**





**Figure 10.36 TCNT10F Operation (End of Cycle, Steady-State)**

## 10.4 Interrupts

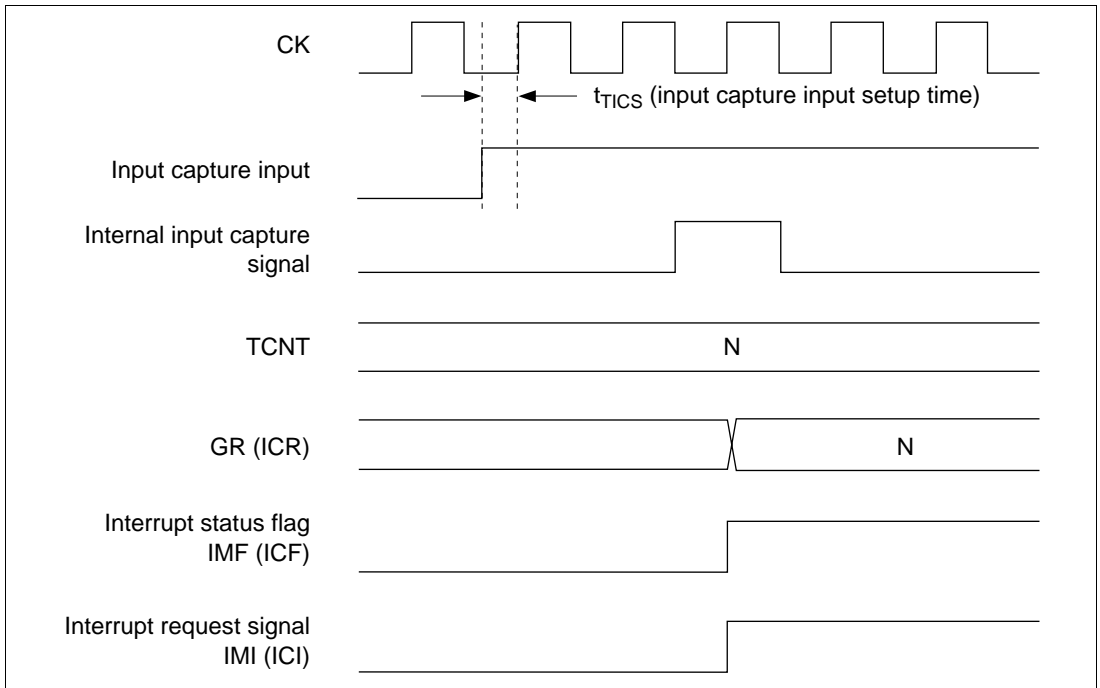
The ATU has 75 interrupt sources of five kinds: input capture interrupts, compare-match interrupts, overflow interrupts, underflow interrupts, and interval interrupts.

### 10.4.1 Status Flag Setting Timing

**IMF (ICF) Setting Timing in Input Capture:** When an input capture signal is generated, the IMF bit and ICF bit are set to 1 in the timer status register (TSR), and the TCNT value is simultaneously transferred to the corresponding GR, ICR and OSBR.

The timing in this case is shown in figure 10.37.

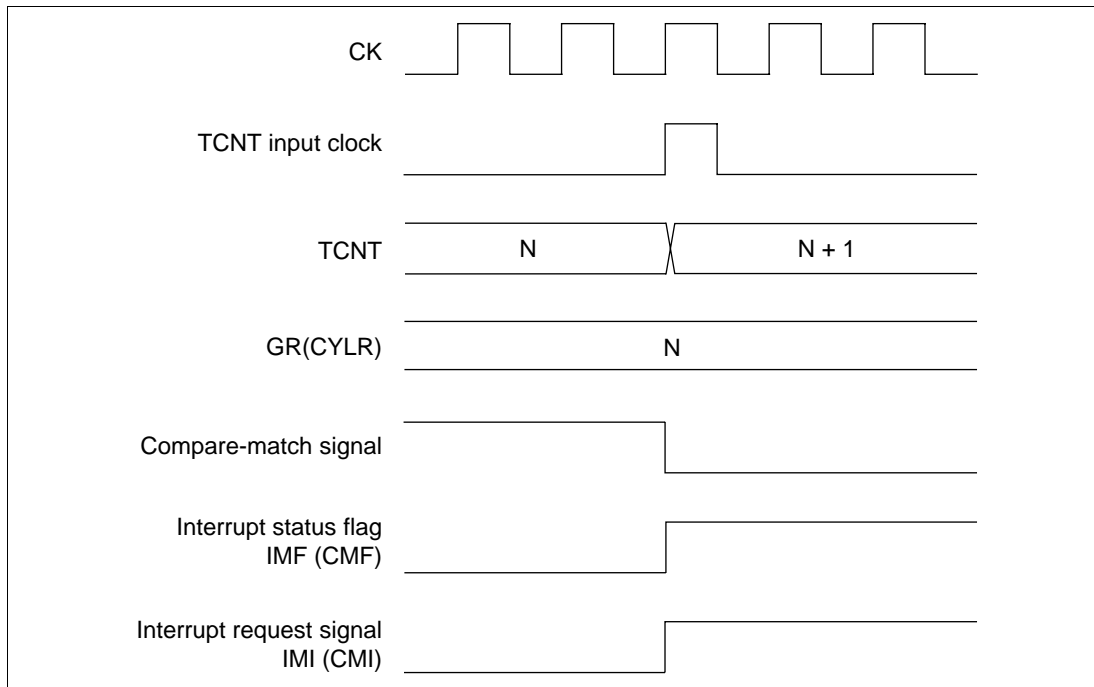
In the example in figure 10.37, a signal is input from an external pin, and input capture is performed on detection of a rising edge.



**Figure 10.37 IMF (ICF) Setting Timing in Input Capture**

**IMF (ICF) Setting Timing in Compare-Match:** The IMF bit and CMF bit are set to 1 in the timer status register (TSR) by the compare-match signal generated when the general register (GR) output compare register (OCR), or cycle register (CYLR) value matches the timer counter (TCNT) value. The compare-match signal is generated in the last state of the match (when the matched TCNT count value is updated).

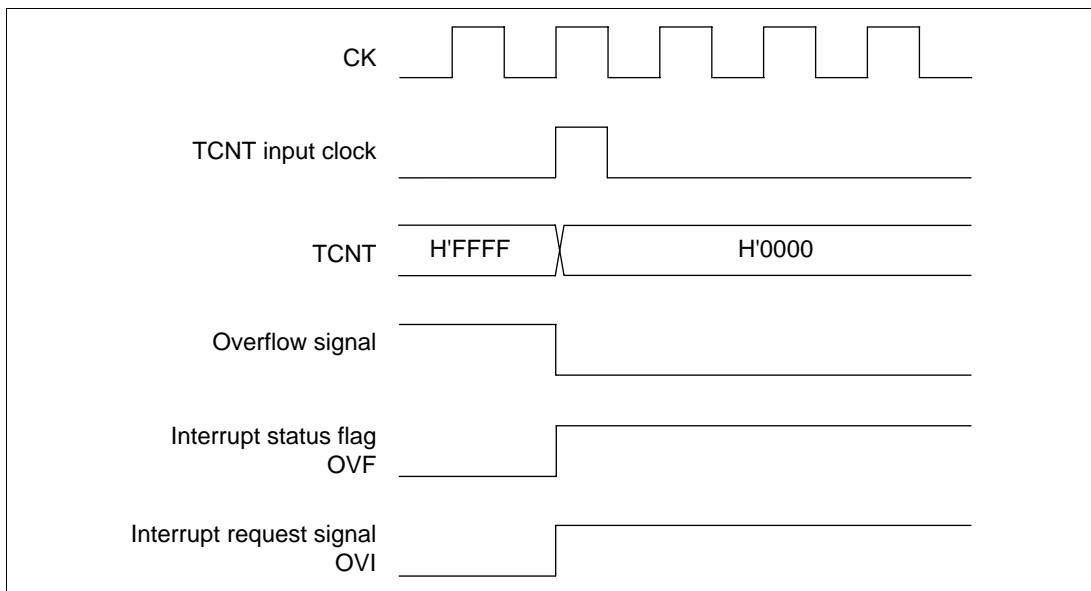
The timing in this case is shown in figure 10.38.



**Figure 10.38 IMF (CMF) Setting Timing in Compare-Match**

**OVF Setting Timing in Overflow:** When TCNT overflows (from H'FFFF to H'0000, or from H'FFFFFFF to H'00000000), the OVF bit is set to 1 in the timer status register (TSR).

The timing in this case is shown in figure 10.39.

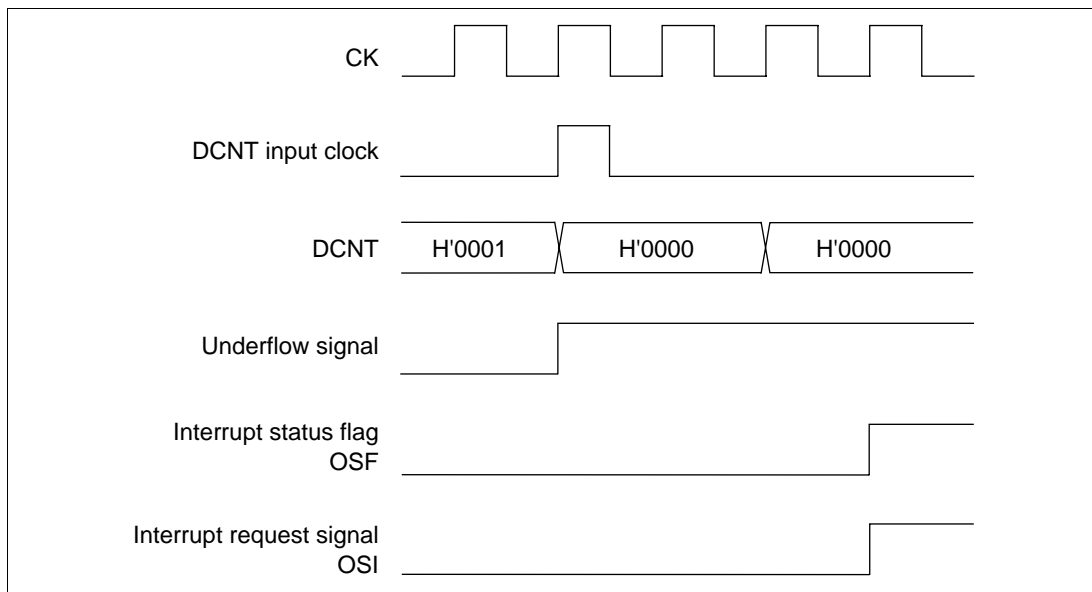


**Figure 10.39 OVF Setting Timing in Overflow**

**OSF Setting Timing in Underflow:** When a down-counter (DCNT) counts down from H'0001 to H'0000 on DCNT input clock input, the OSF bit is set to 1 in the timer status register (TSR) when the next DCNT input clock pulse is input (when underflow occurs). However, when DCNT is H'0000, it remains unchanged at H'0000 no matter how many DCNT input clock pulses are input.

When DCNT is cleared by means of the one-shot pulse function, the OSF bit is cleared when the next DCNT input clock is input.

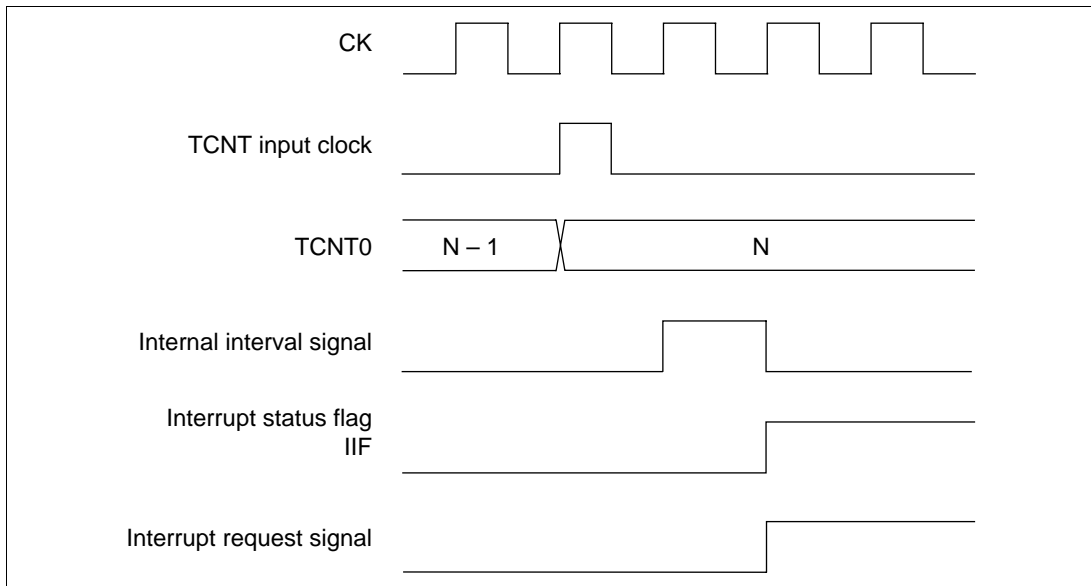
The timing in this case is shown in figure 10.40.



**Figure 10.40 OSF Setting Timing in Underflow**

**Timing of IIF Setting by Interval Timer:** When 1 is generated by ANDing the rise of bit 10 to 13 in free-running counter TCNT0L with bit ITVE0 to ITVE3 in the interval interrupt request register (ITVRR), the IIF bit is set to 1 in the timer status register (TSR).

The timing in this case is shown in figure 10.41. TCNT0 value N in the figure is the counter value when TCNT0L bit 6 to 13 changes to 1. (For example,  $N = H'00000400$  in the case of bit 10,  $H'00000800$  in the case of bit 11, etc.)

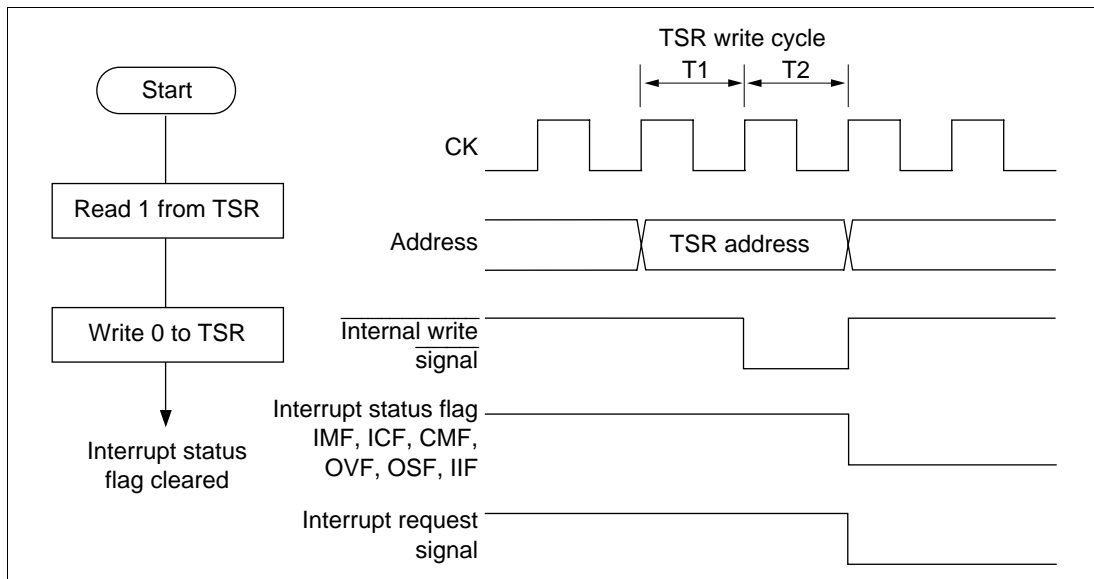


**Figure 10.41 Timing of IIF Setting Timing by Interval Timer**

## 10.4.2 Status Flag Clearing

**Clearing by CPU Program:** The interrupt status flag is cleared when the CPU writes 0 to the flag after reading it while set to 1.

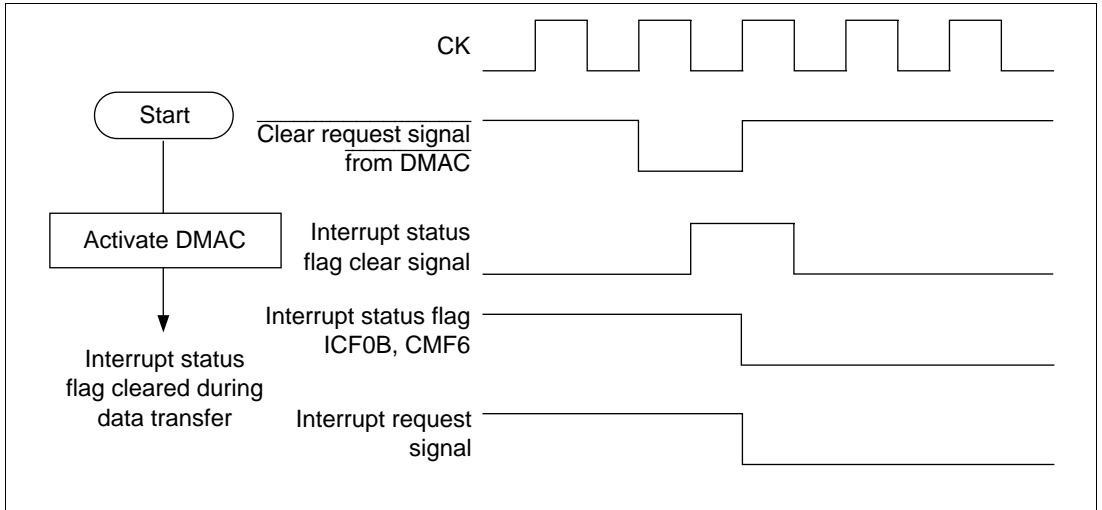
The procedure and timing in this case are shown in figure 10.42.



**Figure 10.42 Procedure and Timing for Clearing by CPU Program**

**Clearing by DMAC:** The interrupt status flag (ICF0A to ICF0D, CMF6A to CMF6D, CMF7A to CMF7D) is cleared automatically during data transfer when the DMAC is activated by input capture or compare-match.

The procedure and timing in this case are shown in figure 10.43.



**Figure 10.43 Procedure and Timing for Clearing by DMAC**



## 10.5 CPU Interface

### 10.5.1 Registers Requiring 32-Bit Access

Free-running counters 0 and 10A (TCNT0, TCNT10A), input capture registers 0A to 0D and 10A (ICR0A to ICR0D, ICR10A), and output compare register 10A (OCR10A) are 32-bit registers. As these registers are connected to the CPU via an internal 16-bit data bus, a read or write (read only, in the case of ICR0A to ICR0D and ICR10A) is automatically divided into two 16-bit accesses.

Figure 10.44 shows a read from TCNT0, and figure 10.45 a write to TCNT0.

When reading TCNT0, in the first read the TCNT0H (upper 16-bit) value is output to the internal data bus, and at the same time, the TCNT0L (lower 16-bit) value is output to an internal buffer register. Then, in the second read, the TCNT0L (lower 16-bit) value held in the internal buffer register is output to the internal data bus.

When writing to TCNT0, in the first write the upper 16 bits are output to an internal buffer register. Then, in the second write, the lower 16 bits are output to TCNT0L, and at the same time, the upper 16 bits held in the internal buffer register are output to TCNT0H to complete the write. The above method performs simultaneous reading and simultaneous writing of 32-bit data, preventing contention with an up-count.

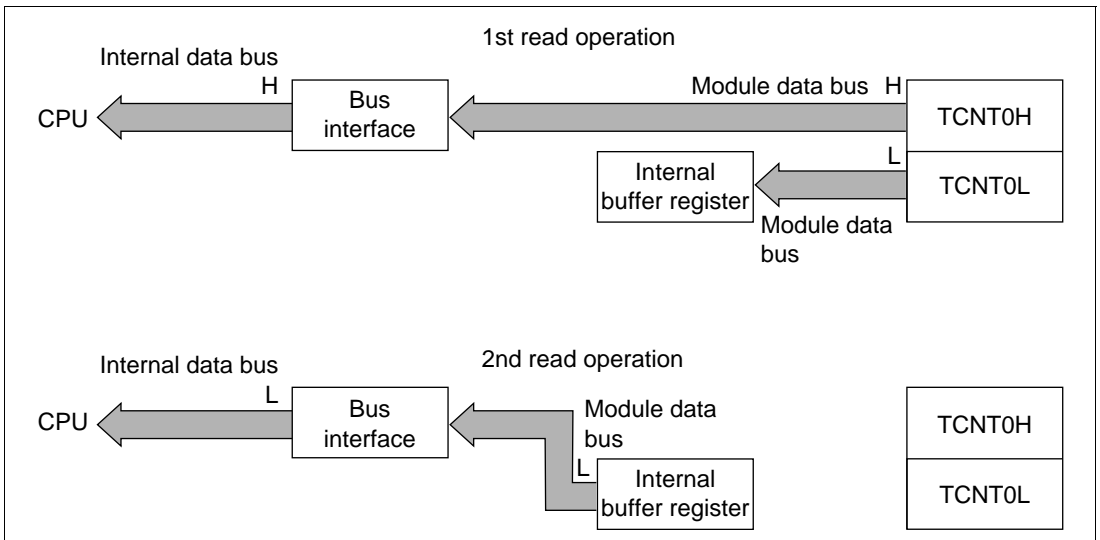
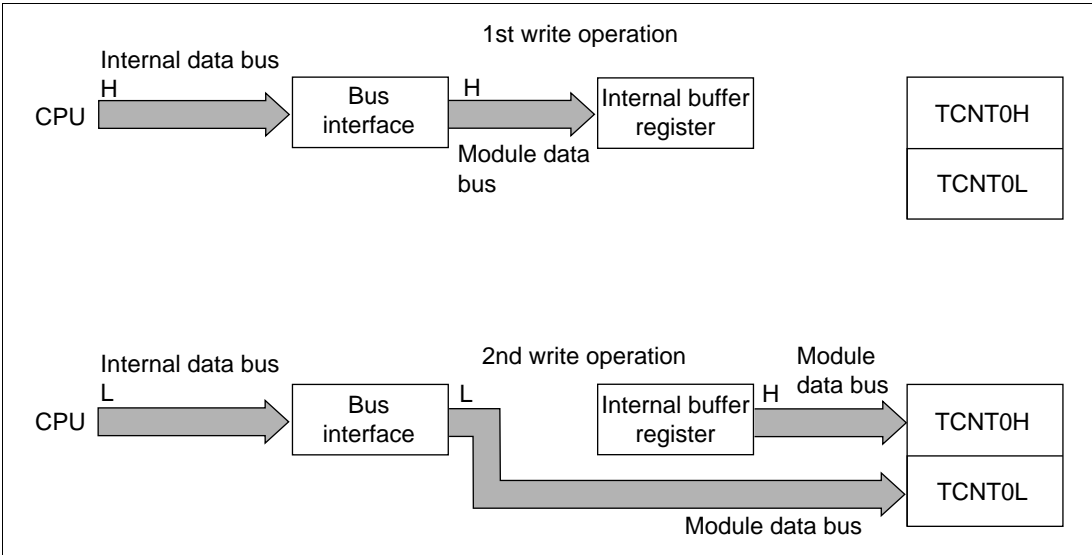


Figure 10.44 Read from TCNT0



**Figure 10.45 Write to TCNT0**

## 10.5.2 Registers Permitting 8-Bit, 16-Bit, or 32-Bit Access

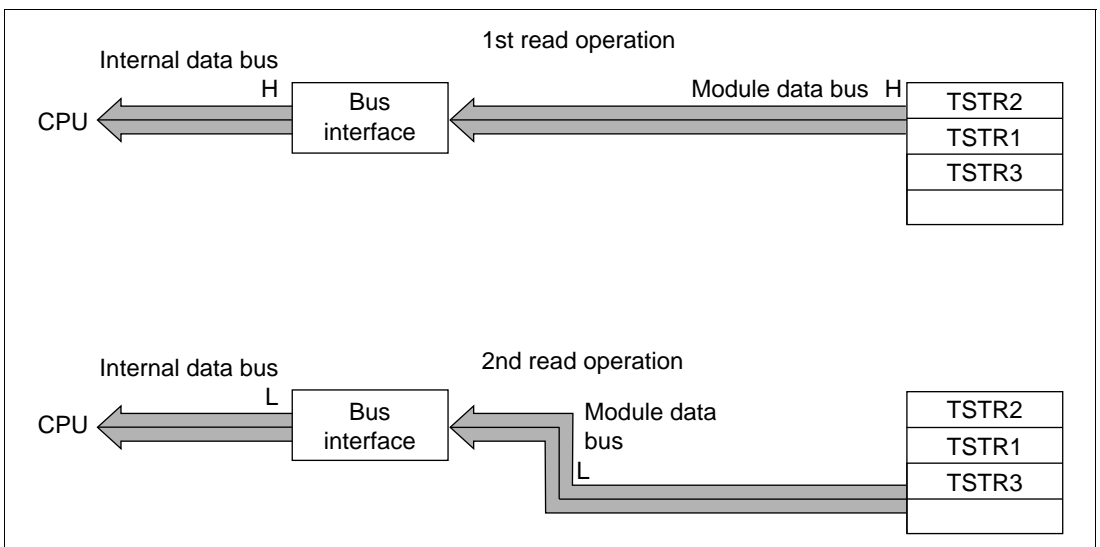
Timer registers 1, 2, and 3 (TSTR1, TSTR2, TSTR3) are 8-bit registers. As these registers are connected to the CPU via an internal 16-bit data bus, a simultaneous 32-bit read or write access to TSTR1, TSTR2, and TSTR3 is automatically divided into two 16-bit accesses.

Figure 10.46 shows a read from TSTR, and figure 10.47 a write to TSTR.

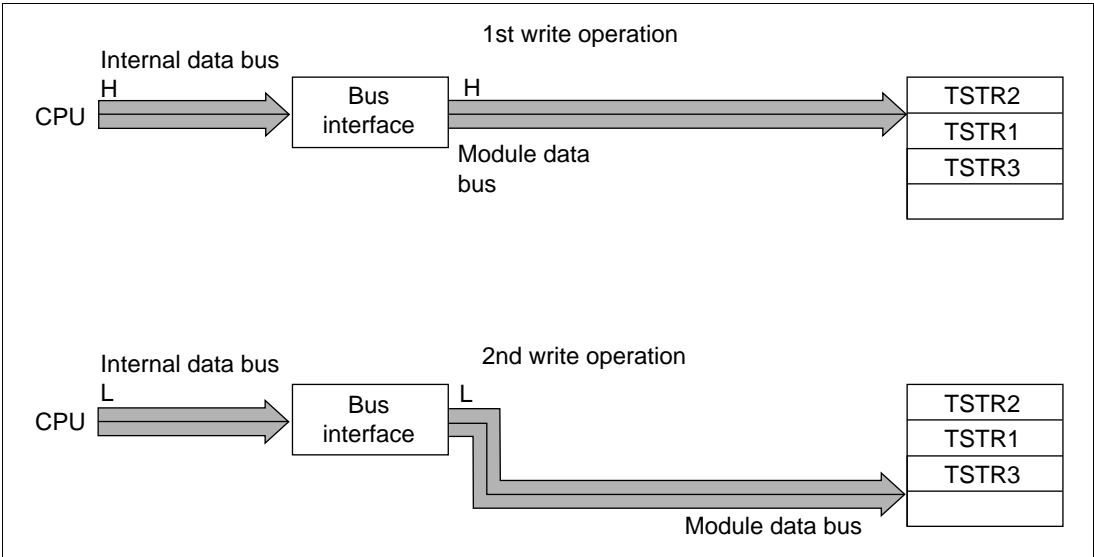
When reading TSTR, in the first read the TSTR1 and TSTR2 (upper 16-bit) value is output to the internal data bus. Then, in the second read, the TSTR3 (lower 16-bit) value is output to the internal data bus.

When writing to TSTR, in the first write the upper 16 bits are written to TSTR1 and TSTR2. Then, in the second write, the lower 16 bits are written to TSTR3. Note that, with the above method, in a 32-bit write the write timing is not the same for TSTR1/TSTR2 and TSTR3.

For information on 8-bit and 16-bit access, see section 10.5.4, 8-Bit or 16-Bit Accessible Registers.



**Figure 10.46 Read from TSTR1, TSTR2, and TSTR3**

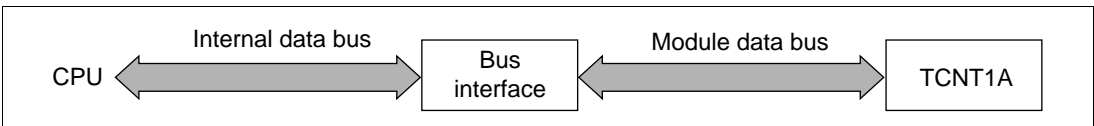


**Figure 10.47 Write to TSTR1, TSTR2 and TSTR3**

### 10.5.3 Registers Requiring 16-Bit Access

The free-running counters (TCNT; but excluding TCNT0, TCNT10A, TCNT10B, TCNT10D, and TCNT10H), the general registers (GR; but excluding GR9A to GR9D), down-counters (DCNT), offset base register (OSBR), cycle registers (CYLR), buffer registers (BFR), duty registers (DTR), timer connection register (TCNR), one-shot pulse terminate register (OTR), down-count start register (DSTR), output compare registers (OCR: but excluding OCR10B), reload registers (RLDR8, RLD10C), correction counter clear register (TCCLR10), timer interrupt enable register (TIER), and timer status register (TSR) are 16-bit registers. These registers are connected to the CPU via an internal 16-bit data bus, and can be read or written (read only, in the case of OSBR) a word at a time.

Figure 10.48 shows the operation when performing a word read or write access to TCNT1A.



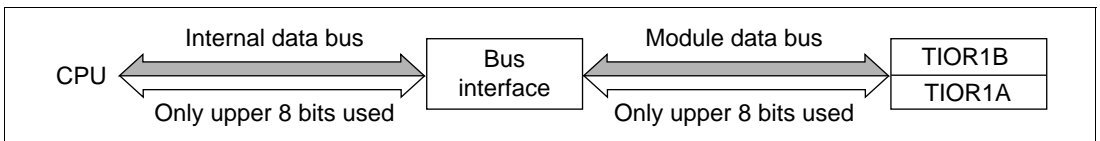
**Figure 10.48 TCNT1A Read/Write Operation**

## 10.5.4 8-Bit or 16-Bit Accessible Registers

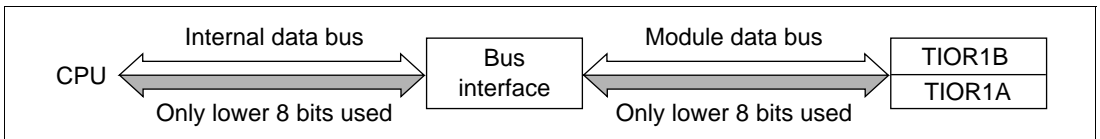
The timer control registers (TCR1A, TCR1B, TCR2A, TCR2B, TCR6A, TCR6B, TCR7A, TCR7B), timer I/O control registers (TIOR1A to TIOR1D, TIOR2A to TIOR2D, TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, TIOR5B), and the timer start register (TSTR1, TSTR2, TSTR3) are 8-bit registers. These registers are connected to the upper 8 bits or lower 8 bits of the internal 16-bit data bus, and can be read or written a byte at a time.

In addition, a pair of 8-bit registers for which only the least significant bit of the address is different, such as timer I/O control register 1A (TIOR1A) and timer I/O control register 1B (TIOR1B), can be read or written in combination a word at a time.

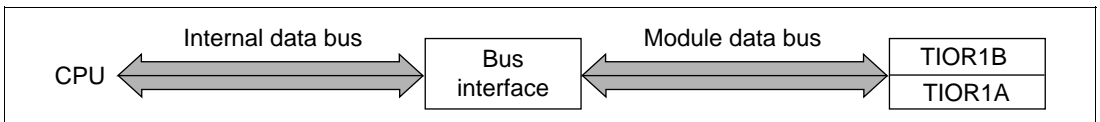
Figures 10.49 and 10.50 show the operation when performing individual byte read or write accesses to TIOR1A and TIOR1B. Figure 10.51 shows the operation when performing a word read or write access to TIOR1A and TIOR1B simultaneously.



**Figure 10.49 Byte Read/Write Access to TIOR1B**



**Figure 10.50 Byte Read/Write Access to TIOR1A**

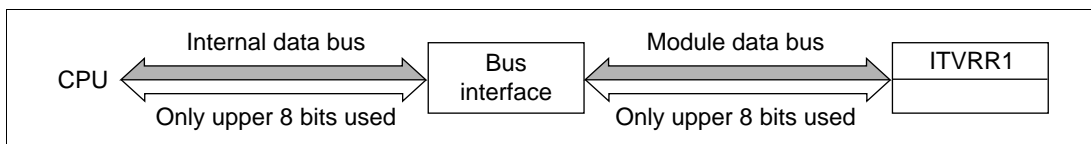


**Figure 10.51 Word Read/Write Access to TIOR1A and TIOR1B**

### 10.5.5 Registers Requiring 8-Bit Access

The timer mode register (TMDR), prescaler register (PSCR), timer I/O control registers (TIOR0, TIOR10, TIOR11), trigger mode register (TRGMDR), interval interrupt request register (ITVRR), timer control registers (TCR3, TCR4, TCR5, TCR8, TCR9A to TCR9C, TCR10, TCR11), PWM mode register (PMDR), reload enable register (RLDENR), free-running counters (TCNT10B, TCNT10D, TCNT10H), event counter (ECNT), general registers (GR9A to GR9F), output compare register (OCR10B), and noise canceler register (NCR) are 8-bit registers. These registers are connected to the upper 8 bits of the internal 16-bit data bus, and can be read or written a byte at a time.

Figure 10.52 shows the operation when performing individual byte read or write accesses to ITVRR1.



**Figure 10.52 Byte Read/Write Access to ITVRR1**

## 10.6 Sample Setup Procedures

Sample setup procedures for activating the various ATU-II functions are shown below.

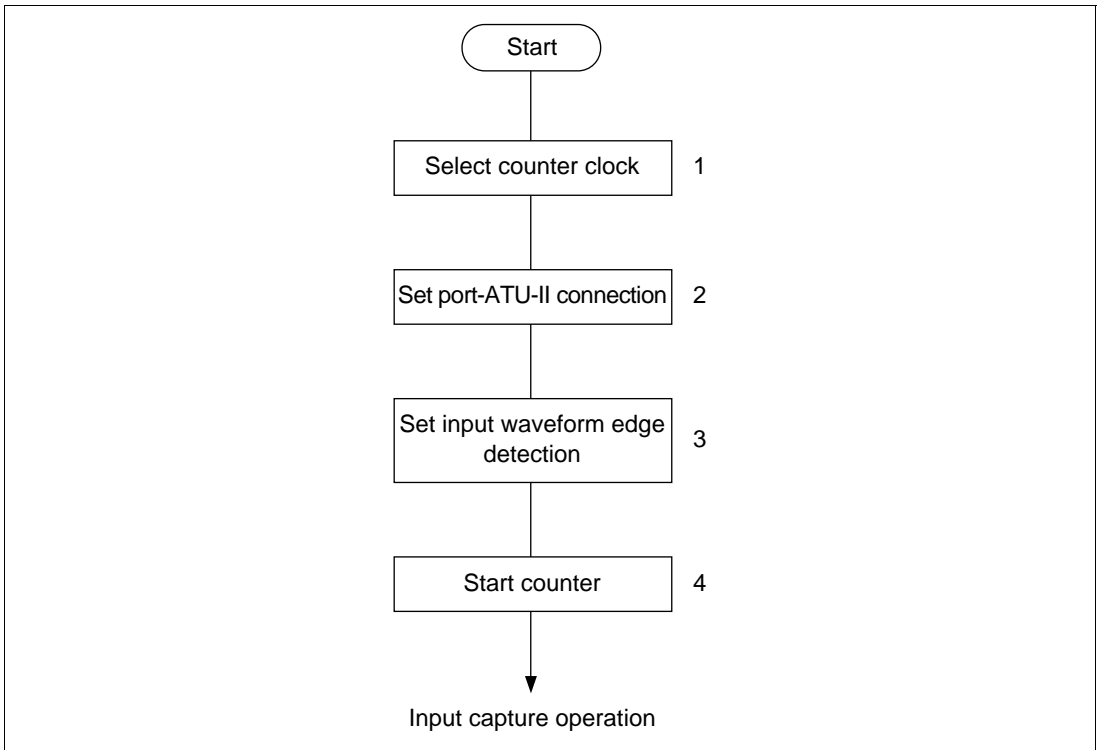
**Sample Setup Procedure for Input Capture:** An example of the setup procedure for input capture is shown in figure 10.53.

1. Select the first-stage counter clock  $\phi'$  in prescaler register (PSCR) and the second-stage counter clock  $\phi''$  with the CKSEL bit in the timer control register (TCR). When selecting an external clock, also select the external clock edge type with the CKEG bit in TCR.
2. Set the port control register, corresponding to the port for signal input as the input capture trigger, to ATU input capture input.
3. Select rising edge, falling edge, or both edges as the input capture signal input edge(s) with the timer I/O control register (TIOR).

If necessary, a timer interrupt request can be sent to the CPU on input capture by making the appropriate setting in the interrupt enable register (TIER). In channel 0, setting the DMAC allows DMAC activation to be performed.

4. Set the corresponding bit to 1 in the timer start register (TSTR) to start the free-running counter (TCNT) for the relevant channel.

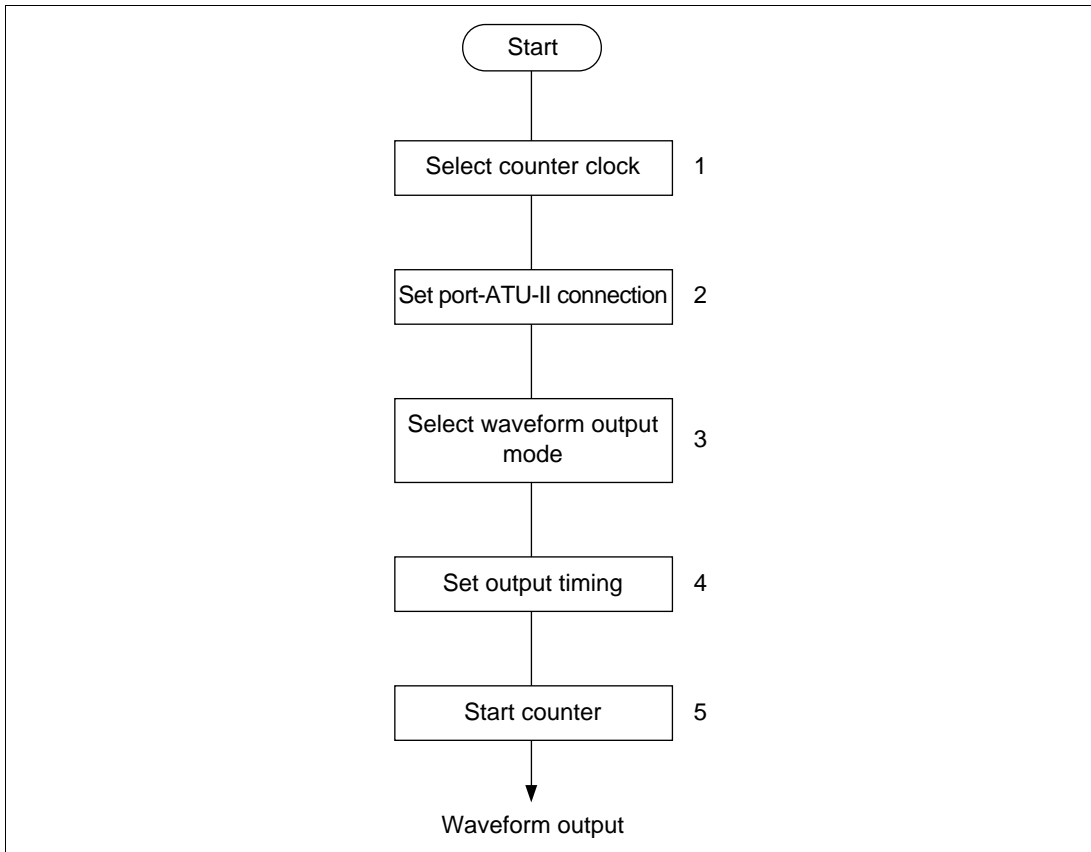
**Note:** When input capture occurs, the counter value is always captured, irrespective of free-running counter (TCNT) activation.



**Figure 10.53 Sample Setup Procedure for Input Capture**

**Sample Setup Procedure for Waveform Output by Output Compare-Match:** An example of the setup procedure for waveform output by output compare-match is shown in figure 10.54.

1. Select the first-stage counter clock  $\phi'$  in prescaler register (PSCR), and the second-stage counter clock  $\phi''$  with the CKSEL bit in the timer control register (TCR). When selecting an external clock, also select the external clock edge type with the CKEG bit in TCR.
2. Set the port control register corresponding to the waveform output port to ATU output compare-match output. Also set the corresponding bit to 1 in the port IO register to specify the output attribute for the port.
3. Select 0, 1, or toggle output for output compare-match output with the timer I/O control register (TIOR). If necessary, a timer interrupt request can be sent to the CPU on output compare-match by making the appropriate setting in the interrupt enable register (TIER).
4. Set the timing for compare-match generation in the ATU general register (GR) corresponding to the port set in 2.
5. Set the corresponding bit to 1 in the timer start register (TSTR) to start the free-running counter (TCNT). Waveform output is performed from the relevant port when the TCNT value and GR value match.



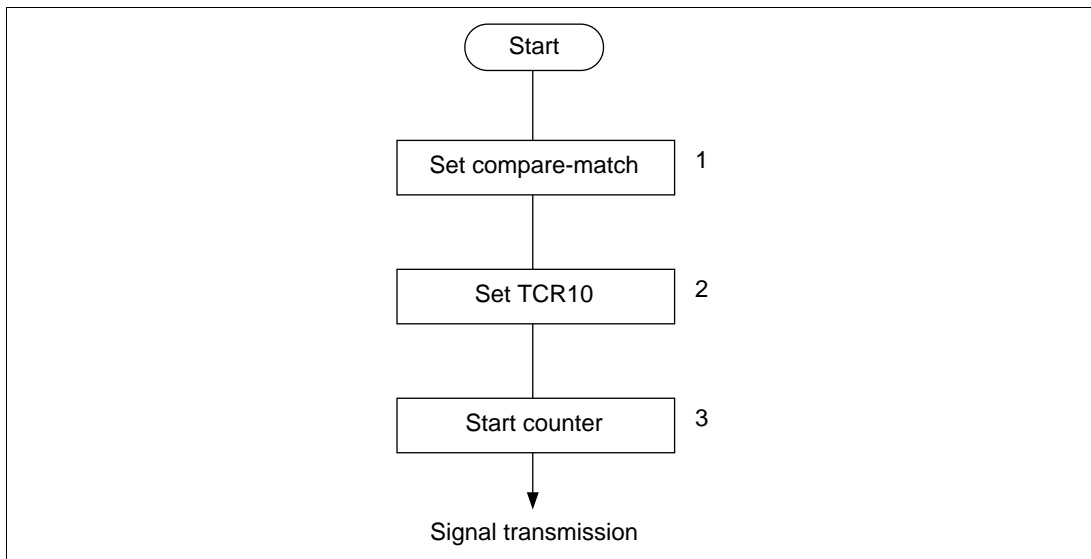
**Figure 10.54 Sample Setup Procedure for Waveform Output by Output Compare-Match**



### Sample Setup Procedure for Channel 0 Input Capture Triggered by Channel 10 Compare-Match

**Match:** An example of the setup procedure for compare-match transmission is shown in figure 10.55.

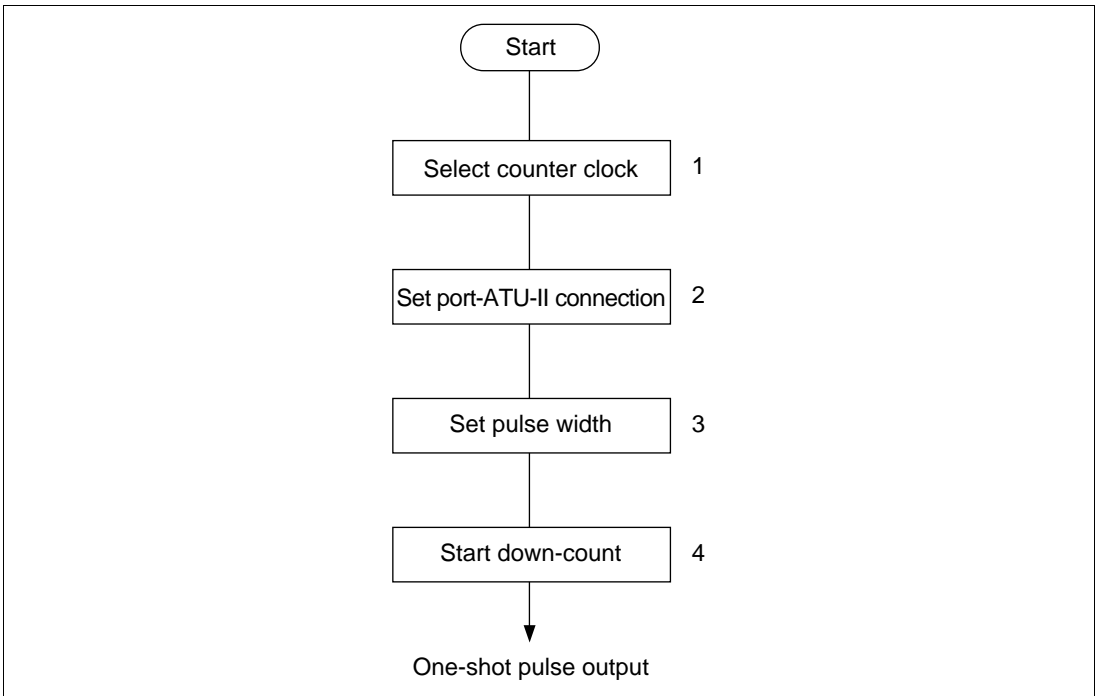
1. Set the timing for compare-match generation in the channel 10 output compare register (OCR10B).
2. Set the TRG0DEN bit to 1 in the channel 10 timer control register (TCR10).
3. Set the corresponding bit to 1 in the timer start register (TSTR) to start the channel 10 free-running counter (TCNT10B). On compare-match between TCNT10B and OCR10B, the compare-match signal is transmitted to channel 0 as the channel 0 ICR0D input capture signal.



**Figure 10.55 Sample Setup Procedure for Compare-Match Signal Transmission**

**Sample Setup Procedure for One-Shot pulse Output:** An example of the setup procedure for one-shot pulse output is shown in figure 10.56.

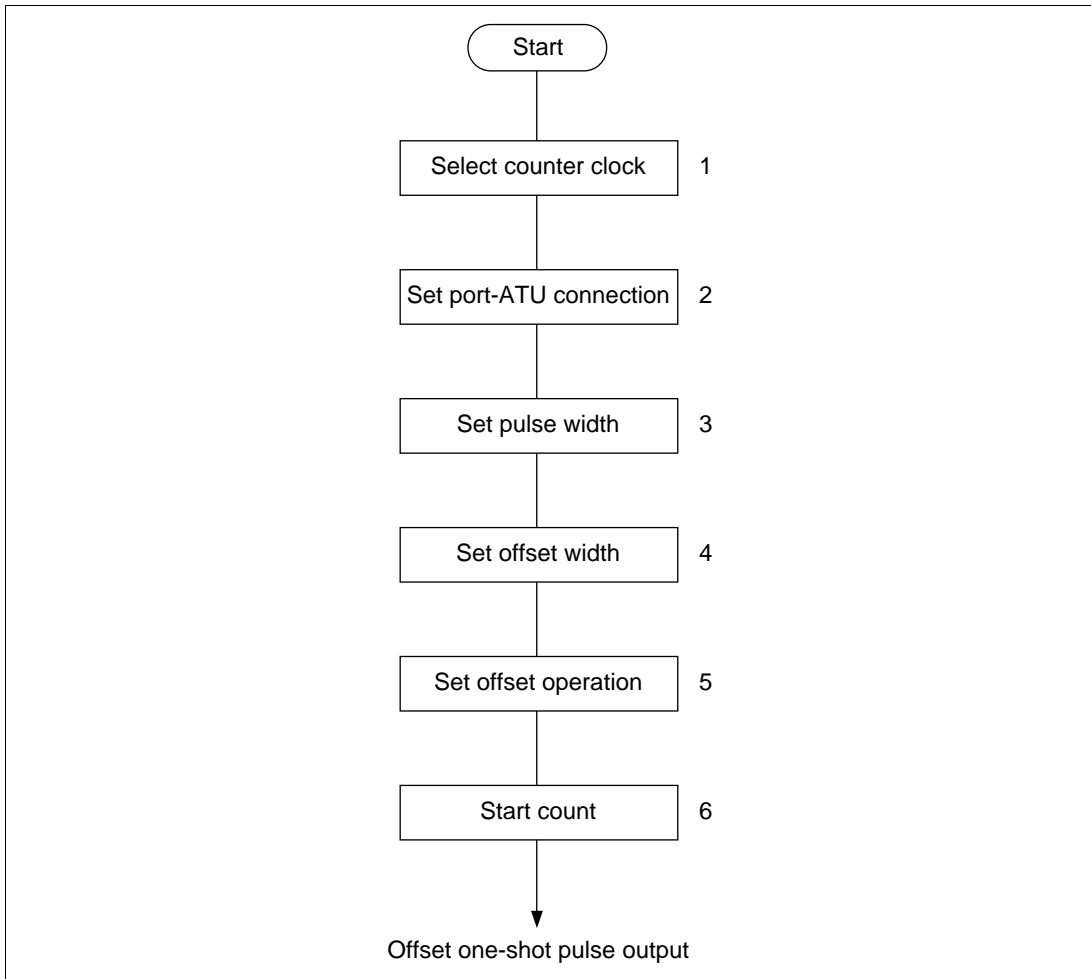
1. Set the first-stage counter clock  $\phi'$  in prescaler register 1 (PSCR1), and select the second-stage counter clock  $\phi''$  with the CKSEL bit in timer control register8 TCR8.
2. Set port K control registers H and L (PKCRH, PKCRL) corresponding to the waveform output port to ATU one-shot pulse output. Also set the corresponding bit to 1 in the port K IO register (PKIOR) to specify the output attribute.
3. Set the one-shot pulse width in the down-counter (DCNT) corresponding to the port set in (2). If necessary, a timer interrupt request can be sent to the CPU when the down-counter underflows by making the appropriate setting in the interrupt enable register (TIER8).
4. Set the corresponding bit (DST8A to DST8P) to 1 in the down-count start register (DSTR) to start the down-counter (DCNT).



**Figure 10.56 Sample Setup Procedure for One-Shot Pulse Output**

**Sample Setup Procedure for Offset One-Shot Pulse Output/Cutoff Operation:** An example of the setup procedure for offset one-shot pulse output is shown in figure 10.57.

1. Set the first-stage counter clock  $\phi'$  in prescaler register 1 (PSCR1), and select the second-stage counter clock  $\phi''$  with the CKSEL bit in the timer control register (TCR1, TCR2, TCR8).
2. Set port K control registers H and L (PKCRH, PKCRL) corresponding to the waveform output port to ATU one-shot pulse output. Also set the corresponding bit to 1 in the port K IO register (PKIOR) to specify the output attribute
3. Set the one-shot pulse width in the down-counter (DCNT) corresponding to the port set in (2). If necessary, a timer interrupt request can be sent to the CPU when the down-counter underflows by making the appropriate setting in the interrupt enable register (TIER8).
4. Set the offset width in the channel 1 or 2 general register (GR1A to GR1H, GR2A to GR2H) connected to the down-counter (DCNT) corresponding to the port set in 2, and in the output compare register (OCR1, OCR2A to OCR2H). Set the timer I/O control register (TIOR1A to TIOR1D, TIOR2A to TIOR2D) to the compare-match enabled state.
5. Set the start/terminate trigger by means of the trigger mode register (TRGMDR), timer connection register (TCNR), and one-shot pulse terminate register (OTR), so that it corresponds to the port set in step 2 above.
6. Set the corresponding bit to 1 in the timer start register (TSTR) to start the channel 1 or 2 free-running counter (TCNT1, TCNT2). When the TCNT value and GR value or OCR value match, the corresponding DCNT starts counting down or is forcibly cleared, and one-shot pulse output is performed.



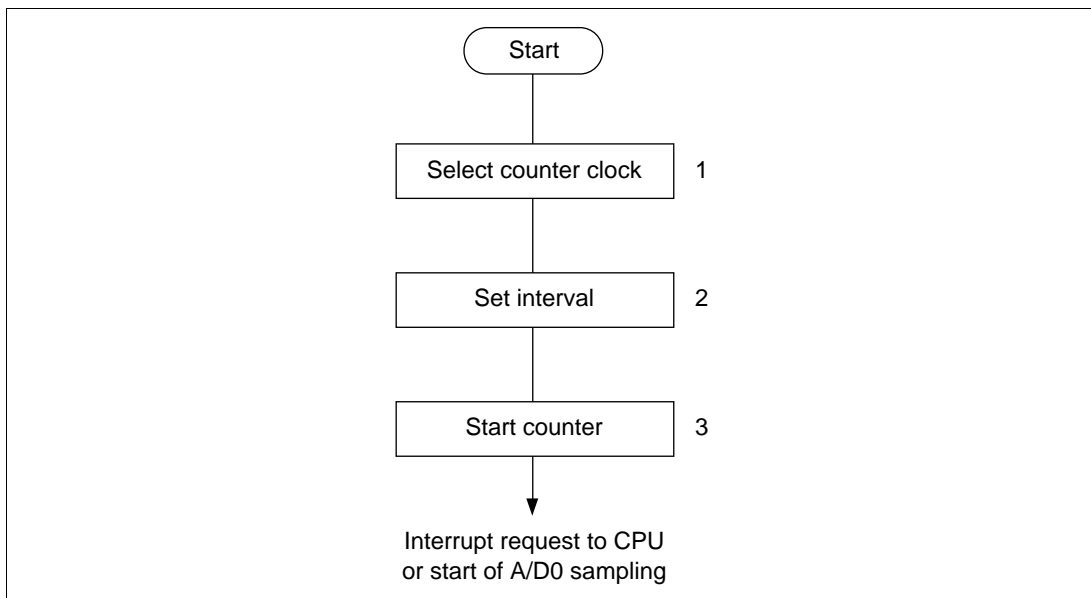
**Figure 10.57 Sample Setup Procedure for Offset One-Shot Pulse Output**

**Sample Setup Procedure for Interval Timer Operation:** An example of the setup procedure for interval timer operation is shown in figure 10.58.

1. Set the first-stage counter clock  $\phi'$  in prescaler register 1 (PSCR1).
2. Set the ITVE bit to be used in the interval interrupt request register (ITVRR) to 1. An interrupt request can be sent to the CPU when the corresponding bit changes to 1 in the channel 0 free-running counter (TCNT0).

To start A/D converter sampling, set the ITVA bit to be used in ITVRR to 1.

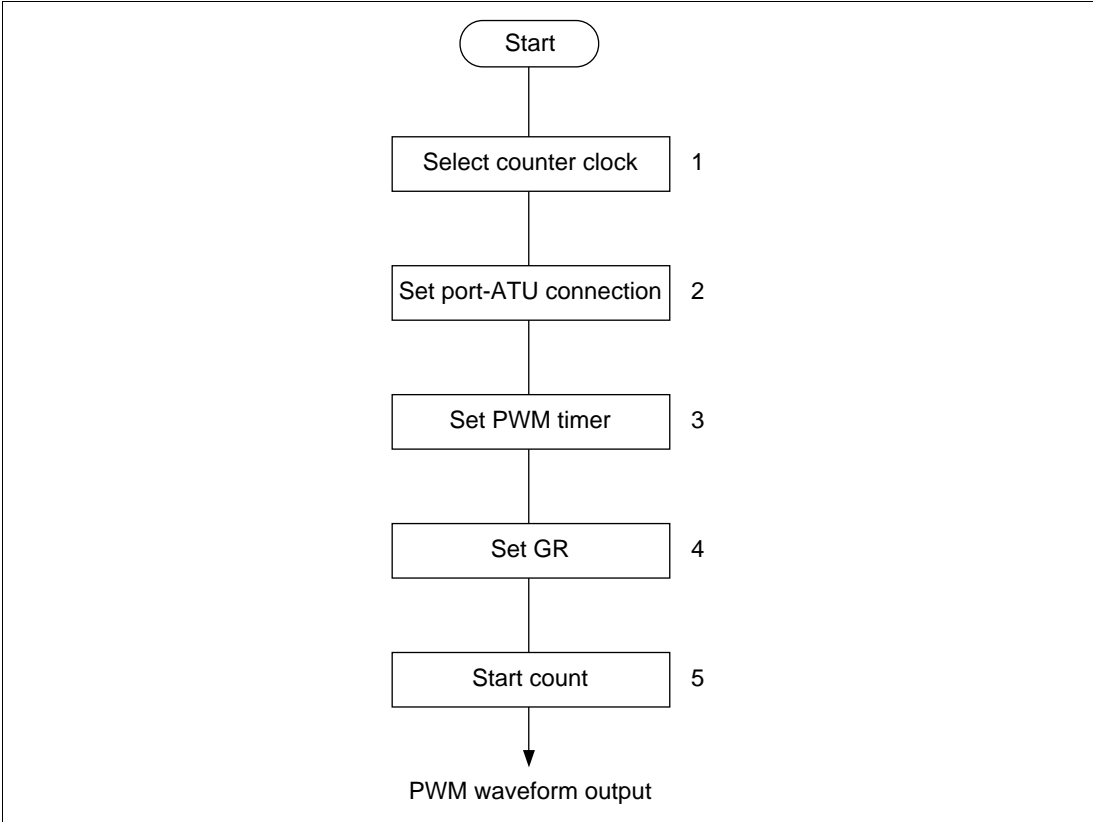
3. Set bit 0 to 1 in the timer start register (TSTR) to start TCNT0.



**Figure 10.58 Sample Setup Procedure for Interval Timer Operation**

**Sample Setup Procedure for PWM Timer Operation (Channels 3 to 5):** An example of the setup procedure for PWM timer operation (channels 3 to 5 ) is shown in figure 10.59.

1. Set the first-stage counter clock  $\phi'$  in prescaler register 1 (PSCR1), and select the second-stage counter clock  $\phi''$  with the CKSEL bit in the timer control register (TCR). When selecting an external clock, at the same time select the external clock edge type with the CKEG bit in TCR.
2. Set the port control registers (PxCRH, PxCRL) corresponding to the waveform output port to ATU output compare-match output. Also set the corresponding bit to 1 in the port IO register (PxIOR) to specify the output attribute.
3. Set bit T3PWM to T5PWM in the timer mode register (TMDR) to PWM mode. When PWM mode is set, the timer operates in PWM mode irrespective of the timer I/O control register (TIOR) contents, and general registers (GR3A to GR3D, GR4A to GR4D, GR5A to GR5D) can be written to.
4. The GR3A to GR3C, GR4A to GR4C, and GR5A to GR5C ATU general registers are used as duty registers (DTR), and the GR3D, GR4D, and GR5D ATU general registers as cycle registers (CYLR). Set the PWM waveform output 0 output timing in DTR, and the PWM waveform output 1 output timing in CYLR. Also, if necessary, interrupt requests can be sent to the CPU at the 0/1 output timing by making a setting in the timer interrupt enable register (TIER).
5. Set the corresponding bit to 1 in the timer start register (TSTR) to start the free-running counter (TCNT) for the relevant channel.



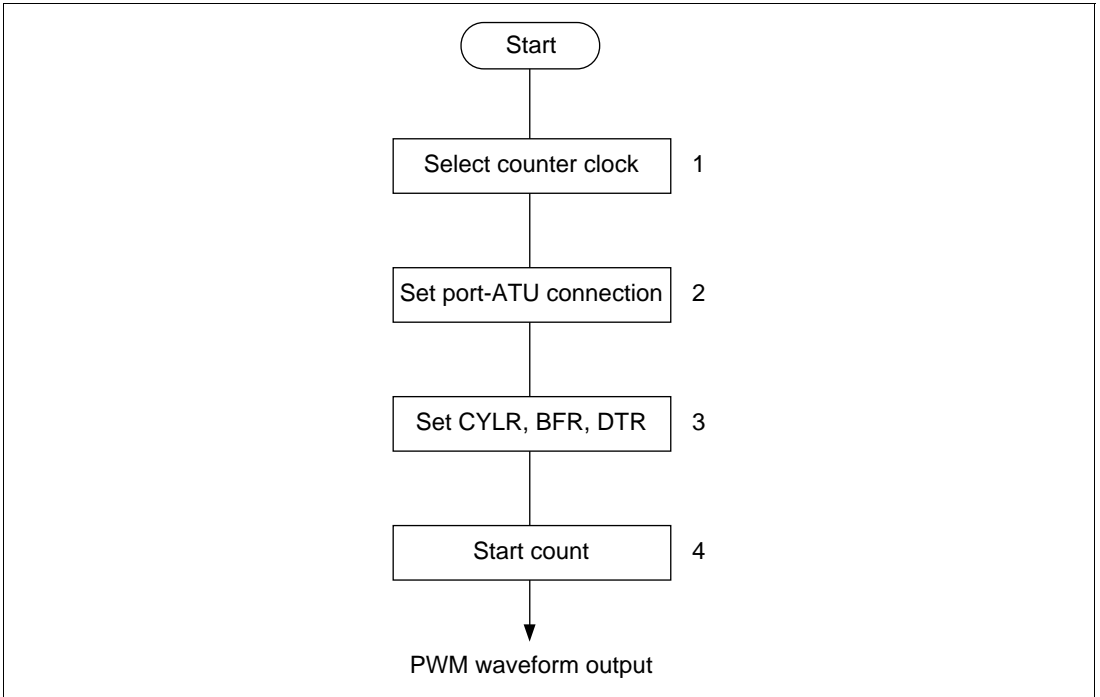
**Figure 10.59 Sample Setup Procedure for PWM Timer Operation (Channels 3 to 5)**

**Sample Setup Procedure for PWM Timer Operation (Channels 6 and 7):** An example of the setup procedure for PWM timer operation (channels 6 and 7) is shown in figure 10.60.

1. Set the first-stage counter clock  $\phi'$  in prescaler register 2 and 3 (PSCR2, PSCR3), and select the second-stage counter clock  $\phi''$  with the CKSEL bit in the timer control register (TCR6A, TCR6B, TCR7A, TCR7B).
2. Set the port B control register L (PBCRL) corresponding to the waveform output port to ATU PWM output. Also set the corresponding bit to 1 in the port B IO register (PBIOR) to specify the output attribute.
3. Set PWM waveform output 1 output timing in the cycle register (CYLR6A to CYLR6D, CYLR7A to CYLR7D), and set the PWM waveform output 0 output timing in the buffer register (BFR6A to BFR6D, BFR7A to BFR7D) and duty register (DTR6A to DTR6D, DTR7A to DTR7D). If necessary, an interrupt request can be sent to the CPU on a compare-match between the CYLR value and the free-running counter (TCNT) value by making the appropriate setting in the timer interrupt enable register (TIER). In addition, setting the DMAC allows DMAC activation to be performed.
4. Set the corresponding bit to 1 in the timer start register (TSTR) to start the TCNT counter for the relevant channel.

- Notes:
1. Do not make a setting in DTR after the counter is started. Use BFR to make a DTR setting.
  2. 0% duty is specified by setting H'0000 in the duty register (DTR), and 100% duty is specified by setting buffer register (BFR) = cycle register (CYLR). Do not set BFR > CYLR.

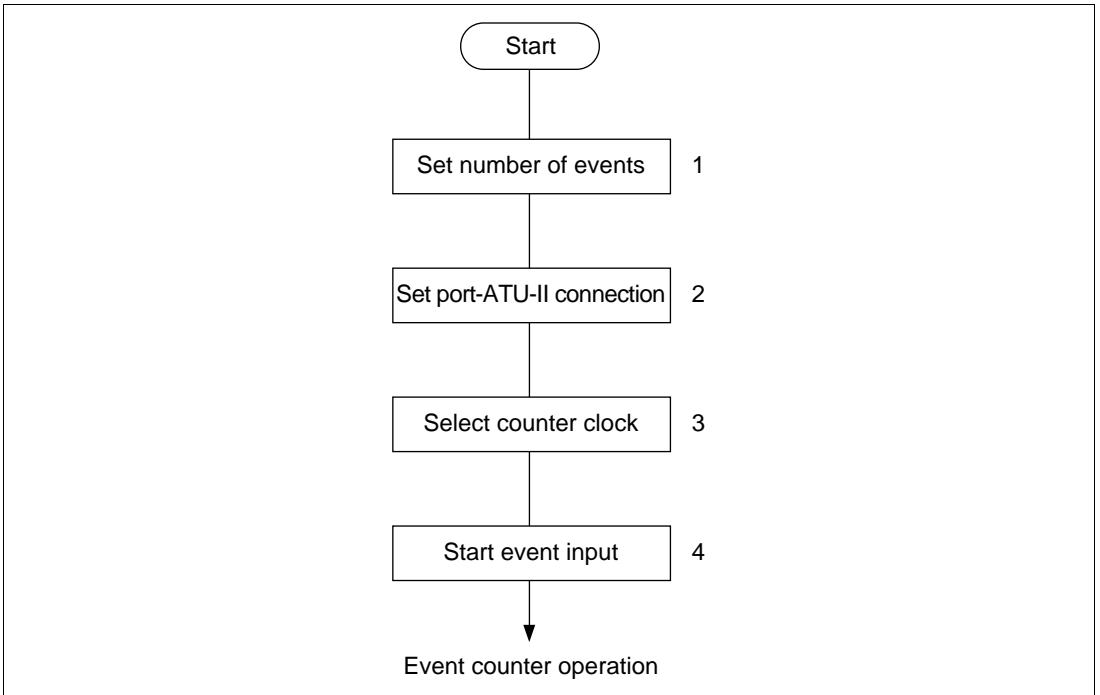




**Figure 10.60 Sample Setup Procedure for PWM Timer Operation (Channels 6 and 7)**

**Sample Setup Procedure for Event Counter Operation:** An example of the setup procedure for event counter operation is shown in figure 10.61.

1. Set the number of events to be counted in a general register (GR9A to GR9D). Also, if necessary, an interrupt request can be sent to the CPU upon compare-match by making a setting in the timer interrupt enable register (TIER).
2. Set the port control register, corresponding to the port for signal input to the event counter, to ATU event counter input.
3. Select the event counter count edge with the EGSEL bits in the channel 9 timer control register (TCR9A to TCR9C).
4. Input a signal to the event counter input pin.



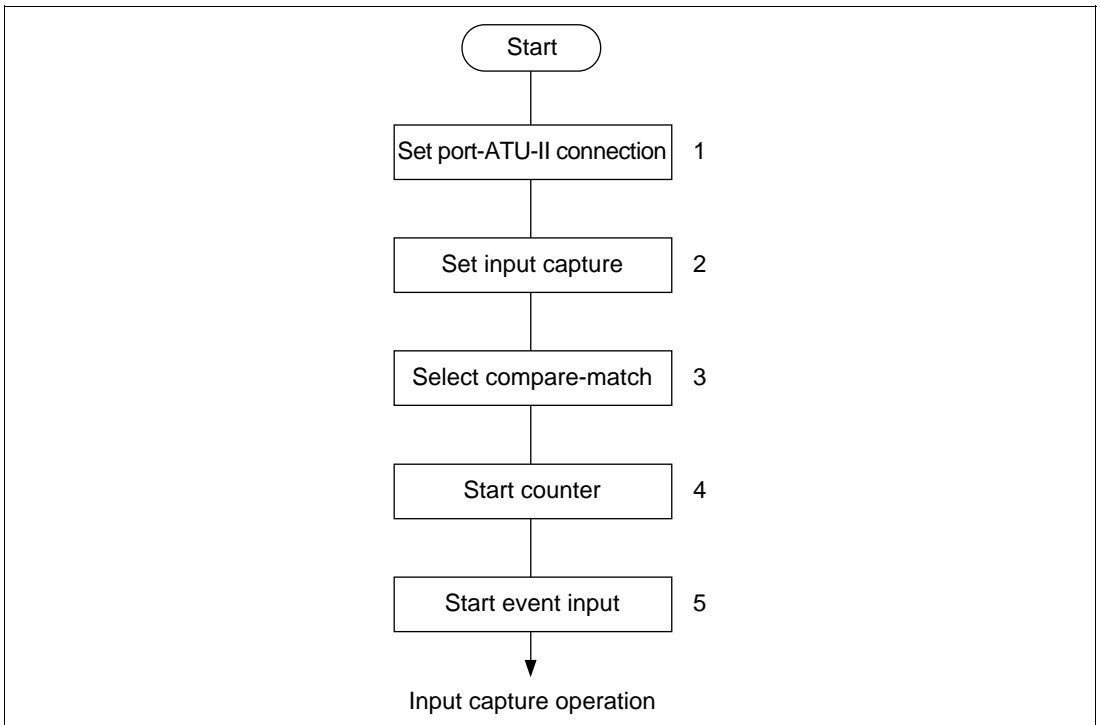
**Figure 10.61 Sample Setup Procedure for Event Counter Operation**

### Sample Setup Procedure for Channel 3 Input Capture Triggered by Channel 9 Compare-Match

**Match:** An example of the setup procedure for compare-match signal transmission is shown in figure 10.62.

1. Set the port control register, corresponding to the port for signal input to the event counter, to ATU event counter input.
2. Set the channel 3 timer I/O control register (TIOR3A, TIOR3B), and select the input capture disable setting for the general registers (GR3A to GR3D). Input from pins TIO3A to TIO3D is masked.
3. Select the event counter count edge with the EGSEL bits in the channel 9 timer control register (TCR9A, TCR9B), and set the TRG3xEN bit to 1. Set the timing for capture in the general register (GR9A to GR9D).
4. Set bit STR3 to 1 in the timer start register (TSTR) to start the channel 3 free-running counter (TCNT3).
5. Input a signal to the event counter input pin.

**Note:** An interrupt request can be sent to the CPU upon channel 9 compare-match by making a setting in the timer interrupt enable register (TIER), but an interrupt request cannot be sent to the CPU upon channel 3 input capture.

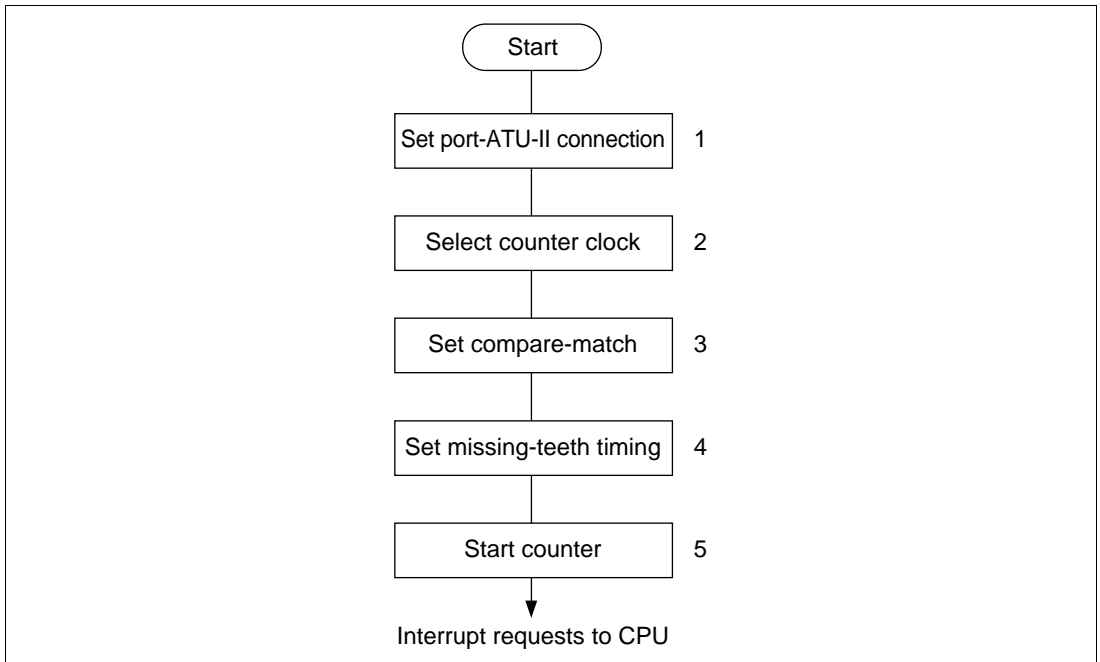


**Figure 10.62** Sample Setup Procedure for Compare-Match Signal Transmission

**Sample Setup Procedure for Channel 10 Missing-Teeth Detection:** An example of the setup procedure for missing-teeth detection is shown in figure 10.63.

1. Set port B control register H (PBCRH) or port L control register L (PLCRL), corresponding to the port for input of the external signal (missing-teeth signal), to ATU edge input (TI10).
2. Set 1st-stage counter clock  $\phi'$  in prescaler register 4 (PSCR4). Set the external input (TI10) cycle multiplication factor with the PIM bits in timer I/O control register 10 (TIOR10), and enable reload register 10C (RLD10C) updating with the RLDEN bit. Select the external input edge type with the CKEG bits in timer control register 10 (TCR10).
3. Set general register 10G (GR10G) to the compare-match function with bit IO10G in TIOR10. Also, an interrupt request can be sent to the CPU upon compare-match by making a setting in interrupt enable register 10 (TIER10).
4. Set the timing for compare-match generation in GR10G according to the multiplication factor and number of missing-teeths in the missing-teeth interval set in step 1.
5. Set the corresponding bit to 1 in timer start register 1 (TSTR1) to start the channel 10 count. A compare-match occurs when the values in free-running counter 10G (TCNT10G) and GR10G match.

Note: The TCNT10G counter clock is generated according to the external input edge interval and multiplication factor selected in step 1, and the counter is cleared to H'0000 by an external input edge.



**Figure 10.63 Sample Setup Procedure for Missing-Teeth Detection**

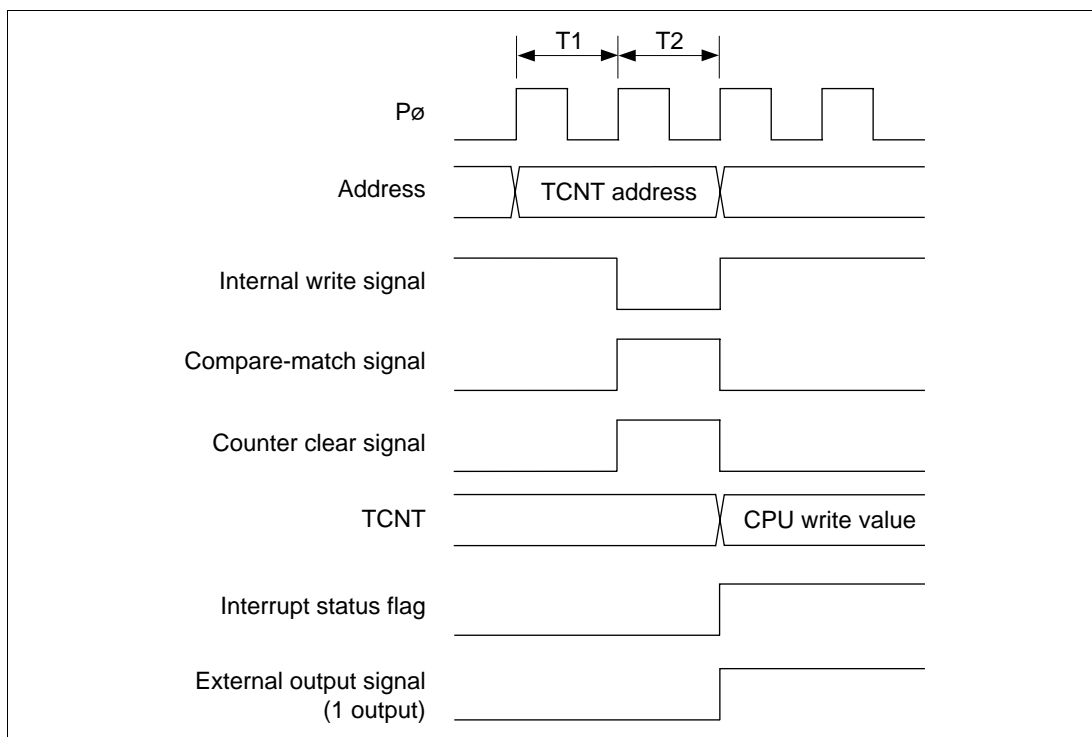
## 10.7 Usage Notes

Note that the kinds of operation and contention described below occur during ATU operation.

**Contention between TCNT Write and Clearing by Compare-Match:** With channel 3 to 7 free-running counters (TCNT3 to TCNT5, TCNT6A to TCNT6D, TCNT7A to TCNT7D), if a compare-match occurs in the T2 state of a CPU write cycle when counter clearing by compare-match has been set, or when PWM mode is used, the write to TCNT has priority and TCNT clearing is not performed.

The compare-match remains valid, and writing of 1 to the interrupt status flag and waveform output to an external destination are performed in the same way as for a normal compare-match.

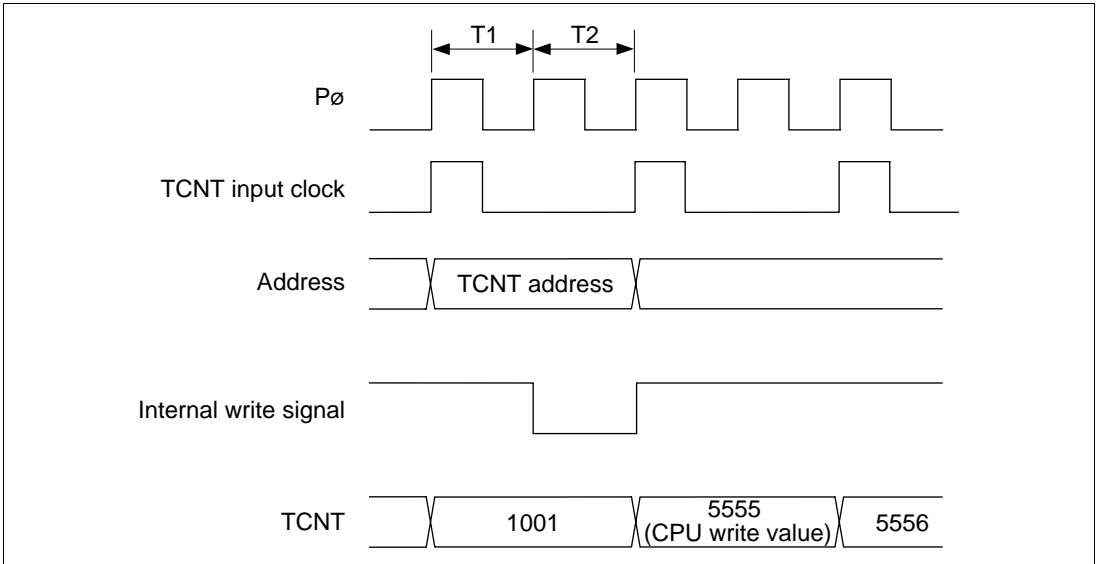
The timing in this case is shown in figure 10.64.



**Figure 10.64** Contention between TCNT Write and Clear

**Contention between TCNT Write and Increment:** If a write to a channel 0 to 11 free-running counter (TCNT0, TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3 to TCNT5, TCNT6A to TCNT6D, TCNT7A to TCNT7D, TCNT10A to TCNT10H, TCNT11), down-counter (DCNT8A to DCNT8P), or event counter 9 (ECNT9A to ECNT9F) is performed while that counter is counting up or down, the write to the counter has priority and the counter is not incremented or decremented.

The timing in this case is shown in figure 10.65 In this example, the CPU writes H'5555 at the point at which TCNT is to be incremented from H'1001 to H'1002.

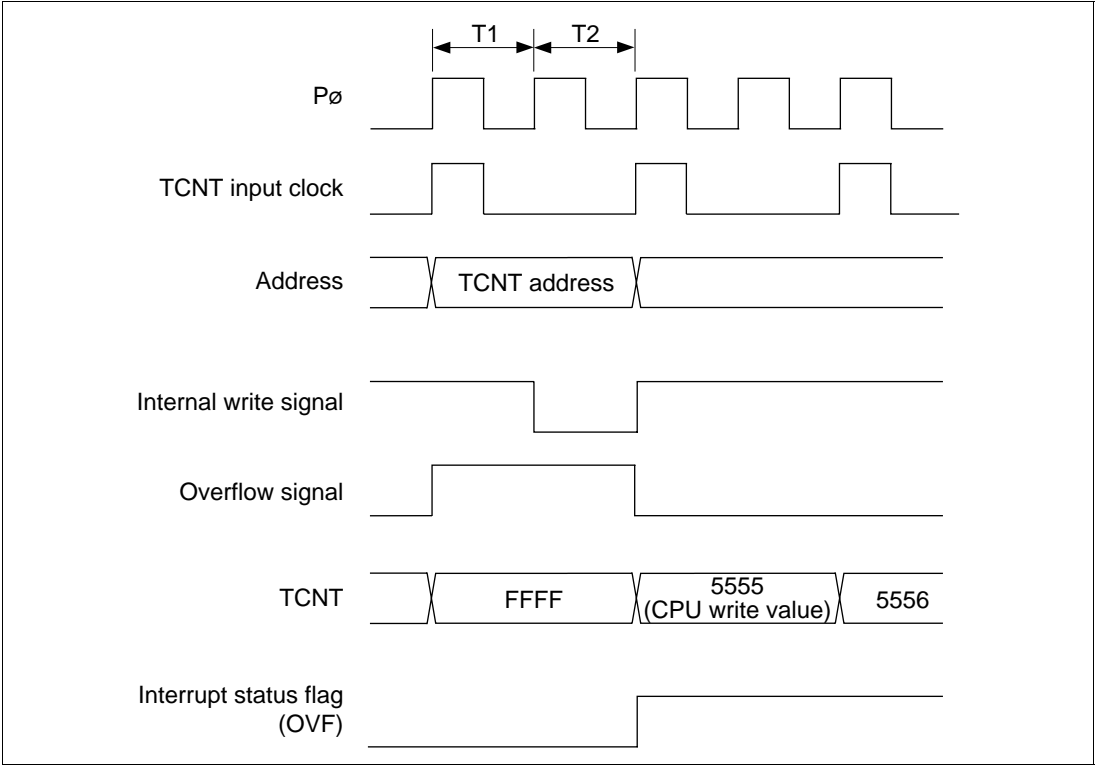


**Figure 10.65 Contention between TCNT Write and Increment**

**Contention between TCNT Write and Counter Clearing by Overflow:** With channel 0 to 5 and 11 free-running counters (TCNT0, TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3 to TCNT5, TCNT11), if overflow occurs in the T2 state of a CPU write cycle, the write to TCNT has priority and TCNT is not cleared.

Writing of 1 to the interrupt status flag (OVF) due to the overflow is performed in the same way as for normal overflow.

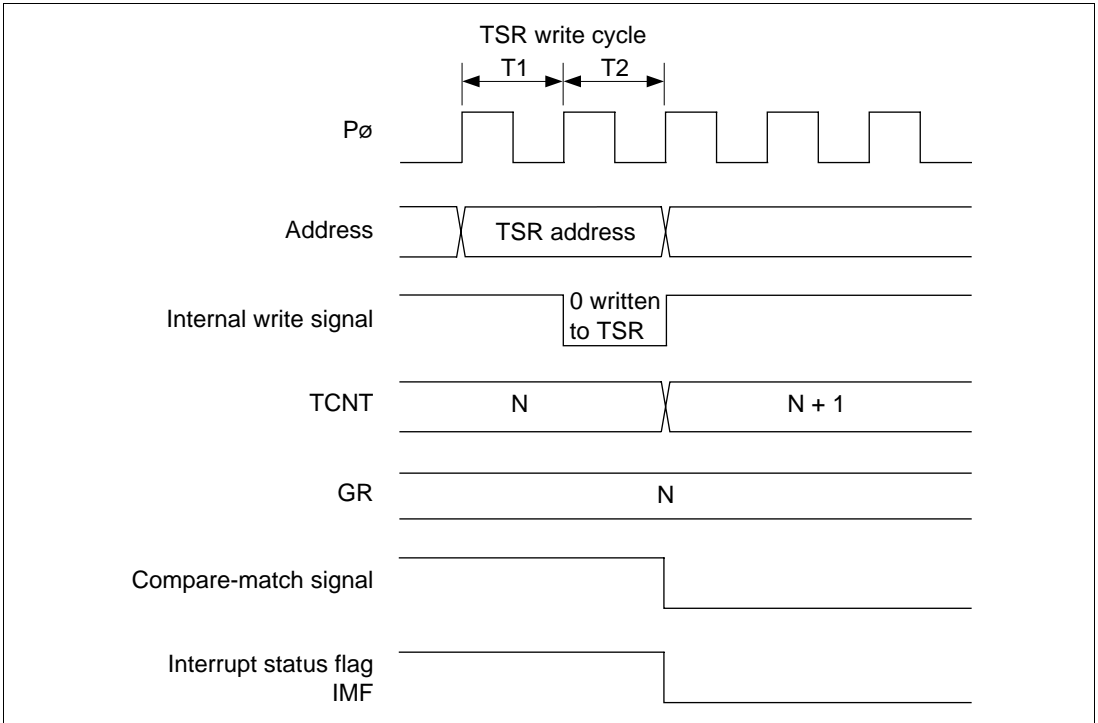
The timing in this case is shown in figure 10.66. In this example, H'5555 is written at the point at which TCNT overflows.



**Figure 10.66 Contention between TCNT Write and Overflow**

**Contention between Interrupt Status Flag Setting by Interrupt Generation and Clearing:** If an event such as input capture/compare-match or overflow/underflow occurs in the T2 state of an interrupt status flag 0 write cycle by the CPU, zeroizing by the 0 write has priority and the interrupt status flag is cleared.

The timing in this case is shown in figure 10.67.

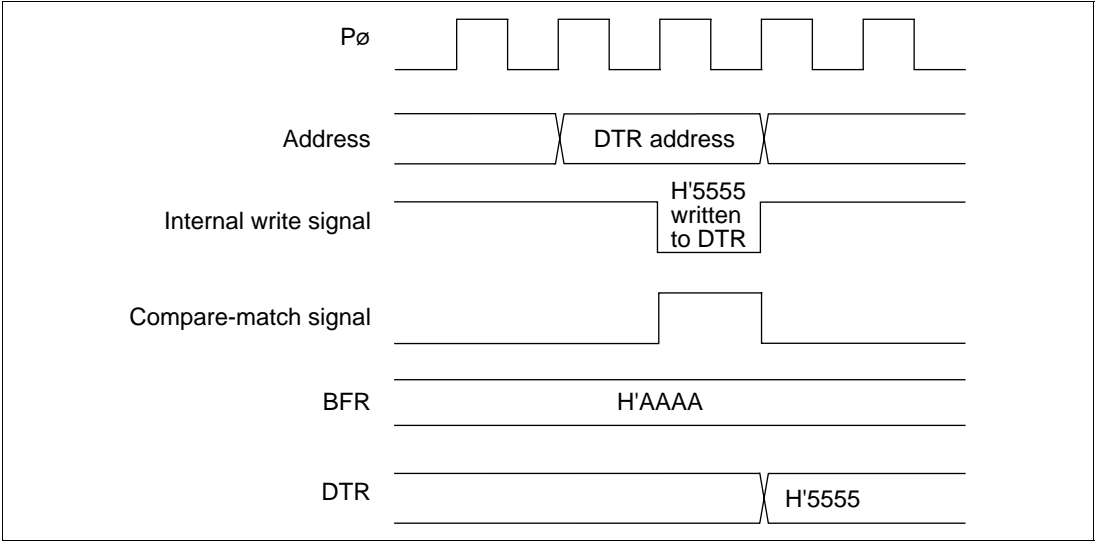


**Figure 10.67 Contention between Interrupt Status Flag Setting by Compare-Match and Clearing**



**Contention between DTR Write and BFR Value transfer by Buffer Function:** In channels 6 and 7, if there is contention between transfer of the buffer register (BFR) value to the corresponding duty register (DTR) due to a cycle register (CYLR) compare-match, and a write to DTR by the CPU, the CPU write value is written to DTR.

Figure 10.68 shows an example in which contention arises when the BFR value is H'AAAA and the value to be written to DTR is H'5555.

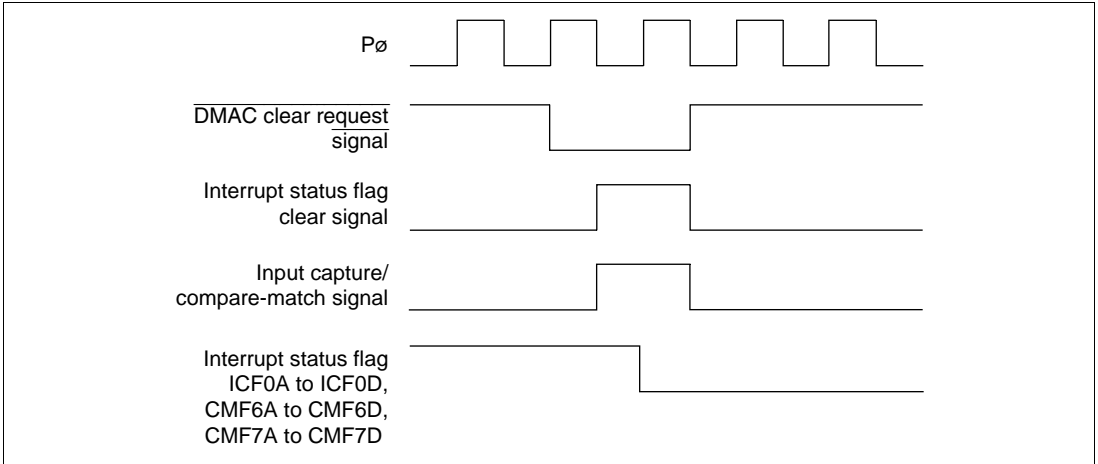


**Figure 10.68** Contention between DTR Write and BFR Value Transfer by Buffer Function

### Contention between Interrupt Status Flag Clearing by DMAC and Setting by Input

**Capture/Compare-Match:** If a clear request signal is generated by the DMAC when the interrupt status flag (ICF0A to ICF0D, CMF6A to CMF6D, CMF7A to CMF7D) is set by input capture (ICR0A to ICR0D) or compare-match (CYLR6A to CYLR6D, CYLR7A to CYLR7D), clearing by the DMAC has priority and the interrupt status flag is not set.

The timing in this case is shown in figure 10.69.

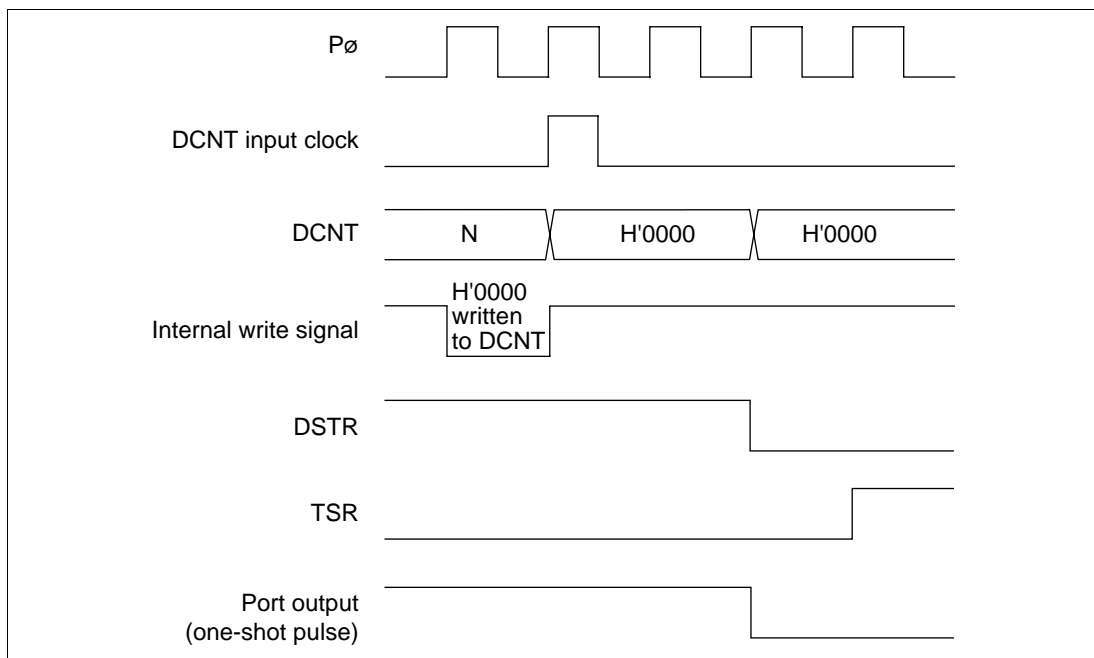


**Figure 10.69** Contention between Interrupt Status Flag Clearing by DMAC and Setting by Input Capture/Compare-Match

**Halting of a Down-Counter by the CPU:** A down-counter (DCNT) can be halted by writing H'0000 to it. The CPU cannot write 0 directly to the down-count start register (DSTR); instead, by setting DCNT to H'0000, the corresponding DSTR bit is cleared to 0 and the count is stopped. However, the OSF bit in the timer status register (TSR) is set when DCNT underflows.

Note that when H'0000 is written to DCNT, the corresponding DSTR bit is not cleared to 0 immediately; it is cleared to 0, and the down-counter is stopped, when underflow occurs following the H'0000 write.

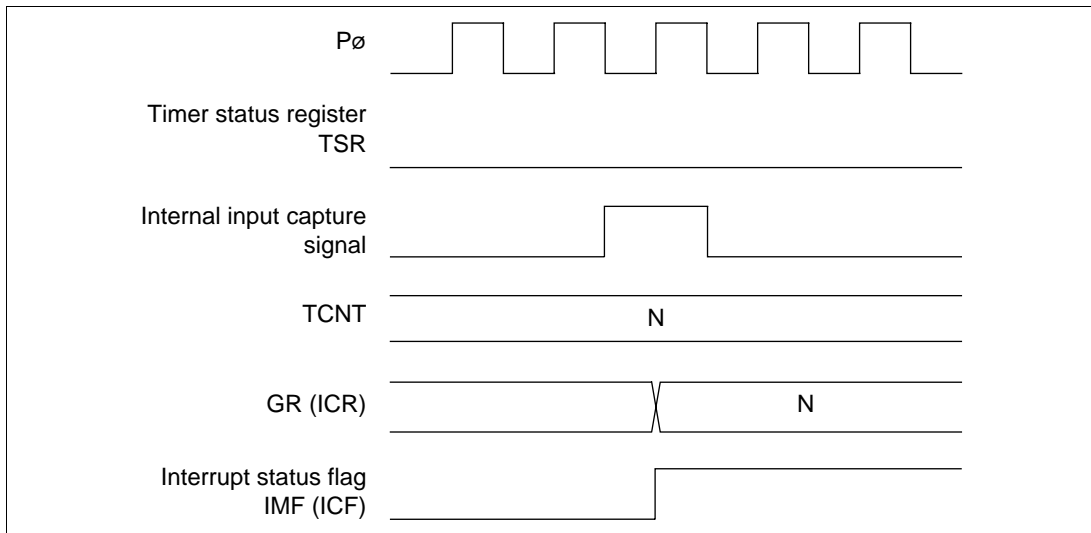
The timing in this case is shown in figure 10.70.



**Figure 10.70 Halting of a Down-Counter by the CPU**

**Input Capture Operation when Free-Running Counter is Halted:** In channels 0 to 5, channel 10, or channel 11, if input capture setting is performed and a trigger signal is input from the input pin, the TCNT value will be transferred to the corresponding general register (GR) or input capture register (ICR) irrespective of whether the free-running counter (TCNT) is running or halted, and the IMF or ICF bit will be set in the timer status register (TSR).

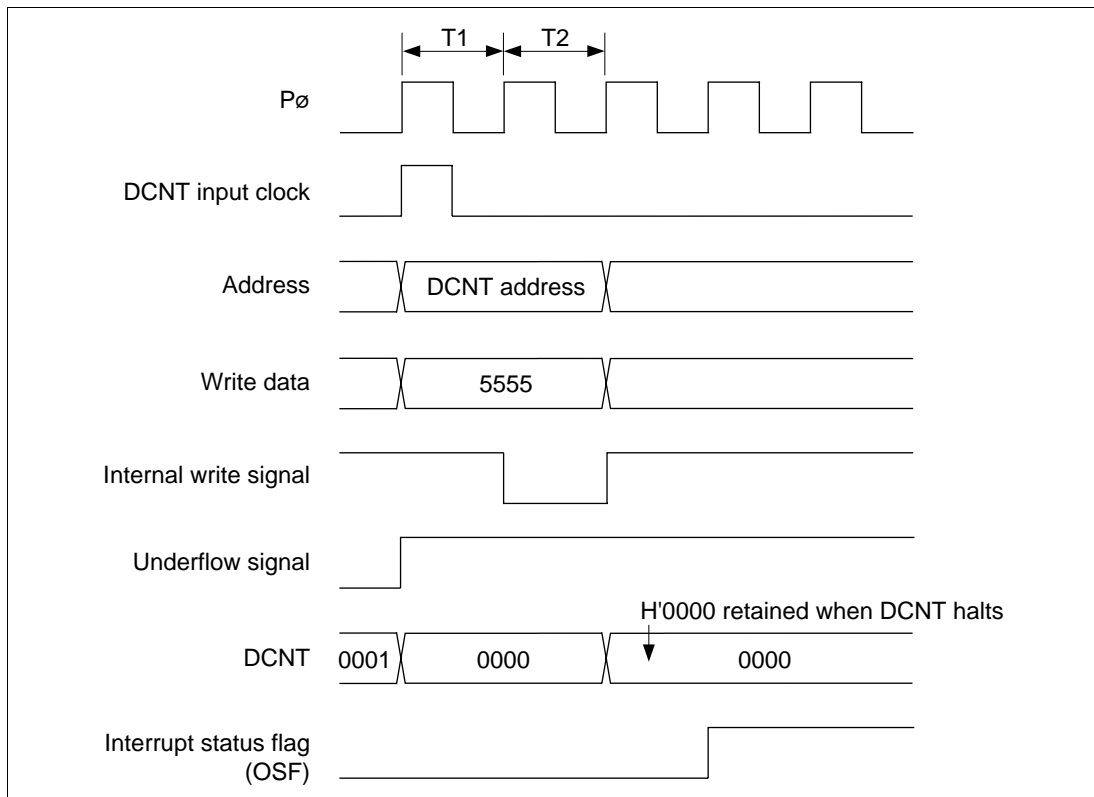
The timing in this case is shown in figure 10.71.



**Figure 10.71 Input Capture Operation before Free-Running Counter is Started**

**Contention between DCNT Write and Counter Clearing by Underflow:** With the channel 8 down-counters (DCNT8A to DCNT8P), if the count is halted due to underflow occurring in the T2 state of a down-counter write cycle by the CPU, retention of the H'0000 value has priority and the write to DCNT by the CPU is not performed. Writing of 1 to the interrupt status flag (OSF) when the underflow occurs is performed in the same way as for normal underflow.

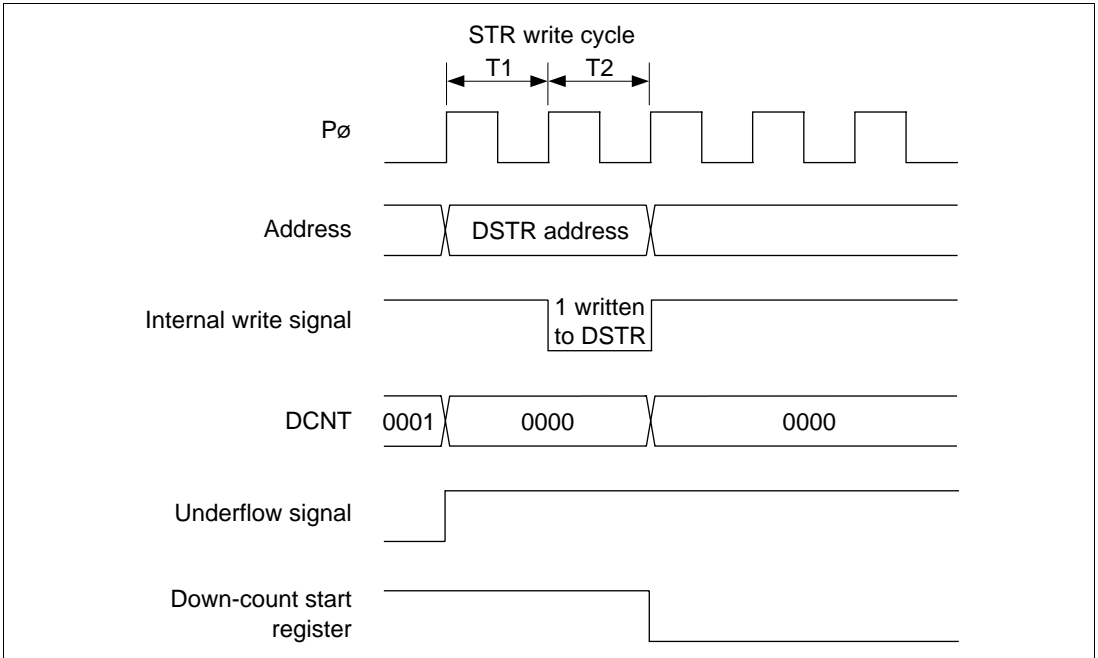
The timing in this case is shown in figure 10.72. In this example, a write of H'5555 to DCNT is attempted at the same time as DCNT underflows.



**Figure 10.72 Contention between DCNT Write and Underflow**

**Contention between DSTR Bit Setting by CPU and Clearing by Underflow:** If underflow occurs in the T2 state of a down-counter start register (DSTR) “1” write cycle by the CPU, clearing to 0 by the underflow has priority, and the corresponding bit of DSTR is not set to 1.

The timing in this case is shown in figure 10.73.



**Figure 10.73 Contention between DSTR Bit Setting by CPU and Clearing by Underflow**

**Timing of Prescaler Register (PSCR), Timer Control Register (TCR), and Timer Mode Register (TMDR) Setting:** Settings in the prescaler register (PSCR), timer control register (TCR), and timer mode register (TMDR) should be made before the counter is started. Operation is not guaranteed if these registers are modified while the counter is running.

Also, the counter must not be started until P $\phi$  has been input 32 times after setting PSCR1 to PSCR4.

**Interrupt Status Flag Clearing Procedure:** When an interrupt status flag is cleared to 0 by the CPU, it must first be read before 0 is written to it. Correct operation cannot be guaranteed if 0 is written without first reading the flag.

**Setting H'0000 in Free-Running Counters 6A to 6D, 7A to 7D (TCNT6A to TCNT6D, TCNT7A to TCNT7D):** If H'0000 is written to a channel 6 and 7 free-running counter (TCNT6A to TCNT6D, TCNT7A to TCNT7D), and the counter is started, the interval up to the first compare-match with the cycle register (CYLR) and duty register (DTR) will be a maximum of one TCNT input clock cycle longer than the set value. With subsequent compare-matches, the correct waveform will be output for the CYLR and DTR values.

**Register Values when a Free-Running Counter (TCNT) Halts:** If the timer start register (TSTR) value is set to 0 during counter operation, only incrementing of the corresponding free-running counter (TCNT) is stopped, and neither the free-running counter (TCNT) nor any other ATU registers are initialized. The external output value at the time TSTR is cleared to 0 will continue to be output.

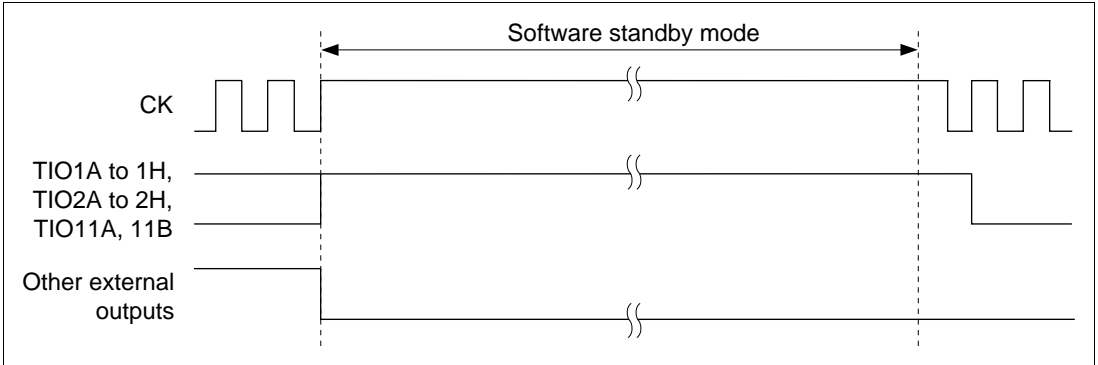
**TCNT0 Writing and Interval Timer Operation:** If the CPU program writes 1 to a bit in free-running counter 0 (TCNT0) corresponding to a bit set to 1 in the interval interrupt request register (ITVRR) when that TCNT0 bit is 0, TCNT0 bit 6, 7, 8, 9, 10, 11, 12, or 13 will be detected as having changed from 0 to 1, and an interrupt request will be sent to INTC and A/D sampling will be started. While the count is halted with the STR0 bit cleared to 0 in timer start register 1 (TSTR1), the bit transition from 0 to 1 will still be detected.

**Automatic TSR Clearing by DMAC Activation by the ATU:** Automatic clearing of TSR is performed after completion of the transfer when the DMAC is in burst mode, and each time the DMAC returns the bus in cycle steal mode.

**Interrupt Status Flag Setting/Resetting:** With TSR, a 0 write to a bit is possible even if overlapping events occur for the same bit before writing 0 after reading 1 to clear that bit. (The duplicate events are not accepted.)

**External Output Value in Software Standby Mode:** In software standby mode, the ATU register and external output values are cleared to 0. However, while the channel 1, 2, and 11 TIO1A to TIO1H, TIO2A to TIO2H external output values are cleared to 0 immediately after software standby mode is exited, other external output values and all registers are cleared to 0 immediately after a transition to software standby mode.

Also, when pin output is inverted by the pin function controller's port B invert register (PBIR) or port K invert register (PKIR), the corresponding pins are cleared to 1.



**Figure 10.74 External Output Value Transition Points in Relation to Software Standby Mode**

**Contention between TCNT Clearing from Channel 10 and TCNT Overflow:** When a channel 1 or 2 free-running counter (TCNT1A, TCNT1B, TCNT2A, TCNT2B) overflows, it is cleared to H'0000. If a clear signal from the channel 10 correction counter clear register (TCCLR) is input at the same time, a 1 write to the interrupt status flag (OVF) due to the overflow is still performed in the same way as for a normal overflow.

**Contention between Channel 10 Reload Register Transfer Timing and Write:** If there is contention between a multiplied-output transfer from the input capture register (ICR10A) to the channel 10 reload register (RLDR10C), and the timing of a CPU write to that register, the CPU write has priority and the multiplied output is ignored.

**Contention between Channel 10 Reload Timing and Write to TCNT10C:** If there is contention between a multiplied-output transfer from the input capture register (ICR10A) to the channel 10 reload register (RLDR10C), and a CPU write to the reload counter (TCNT10C), the CPU write has priority and the multiplied output is ignored.



**ATU Pin Setting:** When a port is set to the ATU pin function, the following points must be noted.

When using a port for input capture input, the corresponding TIOR register must be in the input capture disabled state when the port is set. Regarding channel 10 TI10 input, TCR10 must be in the TI10 input disabled state when the port is set. When using a port for external clock input, the STR bit for the corresponding channel must be in the count operation disabled state when the port is set. When using a port for event input, the corresponding TCR register must be in the count operation disabled state when the port is set.

Regarding TCLKB and TI10 input, although input is assigned to a number of pins, when using TCLKB and TI10 input, only one pin should be enabled.

**Writing to ROM Area Immediately after ATU Register Write:** If a write cycle for a ROM address for which address bit 11 = 0 and address bit 12 = 1 (H'00001000 to H'000017FF, H'00003000 to H'000037FF, H'00005000 to H'000057FF, ..., H'0007F000 to H'0007F7FF, ..., H'000FF000 to H'000FF7FF) occurs immediately after an ATU register write cycle, the value, or part of the value, written to ROM will be written to the ATU register. The following measures should be taken to prevent this.

- Do not perform a CPU write to a ROM address immediately after an ATU register write cycle. For example, an instruction arrangement in which an MOV instruction that writes to the ATU is located at an even-word address (4n address), and is immediately followed by an MOV instruction that writes to a ROM area, will meet the bug conditions.
- Do not perform an AUD write to any of the above ROM addresses immediately after an ATU register write cycle. For example, in the case of a write to overlap RAM when using the RAM emulation function, the write should be performed to the on-chip RAM area address, not the overlapping ROM area address.
- Do not perform a DMAC write to an ATU register when a ROM address write operation occurs.

# 10.8 ATU-II Registers And Pins

**Table 10.4 ATU-II Registers and Pins**

Register Name	Channel											
	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	Channel 9	Channel 10	Channel 11
TSTR (3)	TSTR1	TSTR1	TSTR1	TSTR1	TSTR1	TSTR1	TSTR2	TSTR2	—	—	TSTR3	TSTR1
PSCR (4)	PSCR1	PSCR1	PSCR1	PSCR1	PSCR1	PSCR1	PSCR2	PSCR3	PSCR1	—	PSCR4	PSCR1
TCNT (25)	TCNT0H, TCNT0L	TCNT1A, TCNT1B	TCNT2A, TCNT2B	TCNT3	TCNT4	TCNT5	TCNT6A to TCNT6D	TCNT7A to TCNT7D	—	—	TCNT10AH, TCNT10AL, TCNT10B to TCNT10B	TCNT11
DCNT (16)	—	—	—	—	—	—	—	—	—	DCNT8A to DCNT8P	—	—
ECNT (6)	—	—	—	—	—	—	—	—	—	ECNT9A to ECNT9F	—	—
TCR (17)	—	TCR1A, TCR1B	TCR2A, TCR2B	TCR3	TCR4	TCR5	TCR6A, TCR6B	TCR7A, TCR7B	TCR8	TCR9A to TCR9C	TCR10	TCR11
TIOR (17)	TIOR0	TIOR1A to TIOR1D	TIOR2A to TIOR2D	TIOR3A, TIOR3B	TIOR4A, TIOR4B	TIOR5A, TIOR5B	—	—	—	—	TIOR10	TIOR11
TSR (12)	TSR0	TSR1A, TSR1B	TSR2A, TSR2B	TSR3	—	—	TSR6	TSR7	TSR8	TSR9	TSR10	TSR11
TIER (12)	TIER0	TIER1A, TIER1B	TIER2A, TIER2B	TIER3	—	—	TIER6	TIER7	TIER8	TIER9	TIER10	TIER11
ITVRR (3)	ITVRR1, ITVRR2A, ITVRR2B	—	—	—	—	—	—	—	—	—	—	—
GR (37)	—	GR1A to GR1H	GR2A to GR2H	GR3A to GR3D	GR4A to GR4D	GR5A to GR5D	—	—	—	GR9A to GR9F	GR10G	GR11A, GR11B
ICR (5)	ICR0AH, ICR0AL to ICR0DH, ICR0DL	—	—	—	—	—	—	—	—	—	ICR10AH, ICR10AL	—
OCR (11)	—	OCR1	OCR2A to OCR2H	—	—	—	—	—	—	—	OCR10AH, OCR10AL, OCR10B	—
OSBR (2)	—	OSBR1	OSBR2	—	—	—	—	—	—	—	—	—
TRGMDR (1)	—	TRGMDR	—	—	—	—	—	—	—	—	—	—
TMDR (1)	—	—	—	TMDR	TMDR	TMDR	—	—	—	—	—	—

**Table 10.4 ATU-II Registers and Pins (cont)**

Register Name	Channel											
	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	Channel 9	Channel 10	Channel 11
CYLR (8)	—	—	—	—	—	—	CYLR6A to CYLR6D	CYLR7A to CYLR7D	—	—	—	—
BFR (8)	—	—	—	—	—	—	BFR6A to BFR6D	BFR7A to BFR7D	—	—	—	—
DTR (8)	—	—	—	—	—	—	DTR6A to DTR7A	DTR7A to DTR7D	—	—	—	—
PMDR (1)	—	—	—	—	—	—	PMDR	—	—	—	—	—
PLDR (1)	—	—	—	—	—	—	—	—	RLDR8	—	—	—
TCNR (1)	—	—	—	—	—	—	—	—	TCNR	—	—	—
OTR (1)	—	—	—	—	—	—	—	—	OTR	—	—	—
DSTR (1)	—	—	—	—	—	—	—	—	DSTR	—	—	—
RLDENR (1)	—	—	—	—	—	—	—	—	RLDENR	—	—	—
RLD (1)	—	—	—	—	—	—	—	—	—	—	RLD10C	—
NCR (1)	—	—	—	—	—	—	—	—	—	—	NCR10	—
TCCLR (1)	—	—	—	—	—	—	—	—	—	—	TCCLR10	—
Pins*	TIOA to D	TIO1A to D, TCLKA, TCLKB	TIO2A to H, TCLKA, TCLKB	TIO3A to D, TCLKA, TCLKB	TIO4A to D, TCLKA, TCLKB	TIO5A to D, TCLKA, TCLKB	TO6A to D	TO7A to D	TO8A to P	TI9A to F	T10	TCLKA, TCLKB

Note: \* Pin functions should be set as described in section 20, Pin Function Controller (PFC).



# Section 11 Advanced Pulse Controller (APC)

## 11.1 Overview

The SH7052F/SH7053F/SH7054F has an on-chip advanced pulse controller (APC) that can generate a maximum of eight pulse outputs, using the advanced timer unit II (ATU-II) as the time base.

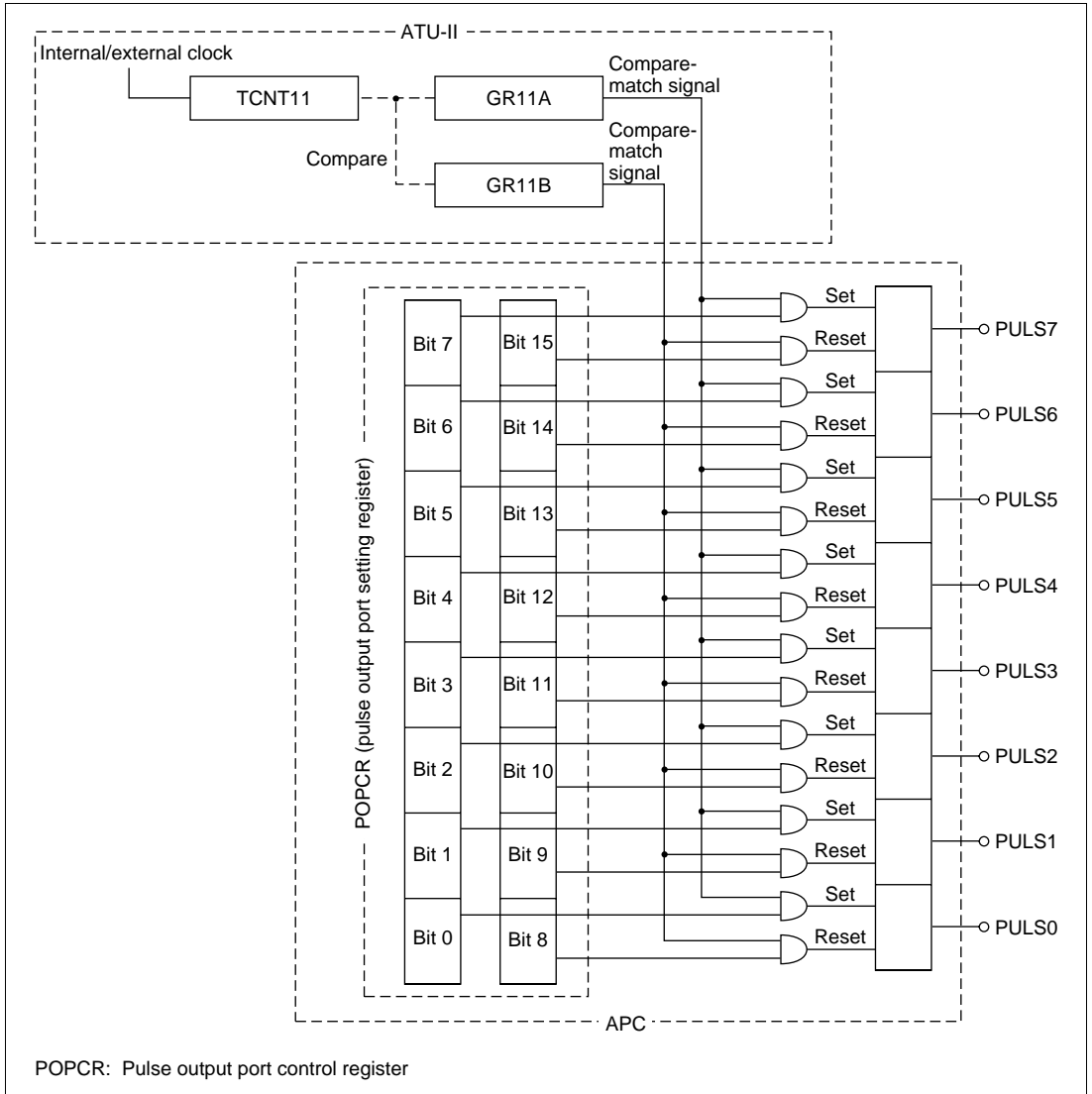
### 11.1.1 Features

The features of the APC are summarized below.

- Maximum eight pulse outputs  
The pulse output pins can be selected from among eight pins. Multiple settings are possible.
- Output trigger provided by advanced timer unit II (ATU-II) channel 2  
Pulse 0 output and 1 output is performed using the compare-match signal generated by the ATU-II channel II compare-match register as the trigger.

## 11.1.2 Block Diagram

Figure 11.1 shows a block diagram of the advanced pulse controller.



**Figure 11.1 Advanced Pulse Controller Block Diagram**

### 11.1.3 Pin Configuration

Table 11.1 summarizes the advanced pulse controller's output pins.

**Table 11.1 Advanced Pulse Controller Pins**

Pin Name	I/O	Function
PULS0	Output	APC pulse output 0
PULS1	Output	APC pulse output 1
PULS2	Output	APC pulse output 2
PULS3	Output	APC pulse output 3
PULS4	Output	APC pulse output 4
PULS5	Output	APC pulse output 5
PULS6	Output	APC pulse output 6
PULS7	Output	APC pulse output 7

### 11.1.4 Register Configuration

Table 11.2 summarizes the advanced pulse controller's register.

**Table 11.2 Advanced Pulse Controller Register**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Pulse output port control register	POPCR	R/W	H'0000	H'FFFFFF700	8, 16

Note: Register access requires 4 or 5 cycles.

## 11.2 Register Descriptions

### 11.2.1 Pulse Output Port Control Register (POPCR)

The pulse output port control register (POPCR) is a 16-bit readable/writable register.

POPCR is initialized to H'0000 by a power-on reset and in hardware standby mode. It is not initialized in software standby mode.

Bit:	15	14	13	12	11	10	9	8
	PULS7 ROE	PULS6 ROE	PULS5 ROE	PULS4 ROE	PULS3 ROE	PULS2 ROE	PULS1 ROE	PULS0 ROE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PULS7 SOE	PULS6 SOE	PULS5 SOE	PULS4 SOE	PULS3 SOE	PULS2 SOE	PULS1 SOE	PULS0 SOE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 8—PULS7 to PULS0 Reset Output Enable (PULS7ROE to PULS0ROE): These bits enable or disable 0 output to the APC pulse output pins (PULS7 to PULS0) bit by bit.

#### Bits 15 to 8:

#### PULS7ROE to PULS0ROE Description

	Description
0	0 output to APC pulse output pin (PULS7 to PULS0) is disabled (Initial value)
1	0 output to APC pulse output pin (PULS7 to PULS0) is enabled

When one of these bits is set to 1, 0 is output from the corresponding pin on a compare-match between the GR11B and TCNT11 values.



- Bits 7 to 0—PULS7 to PULS0 Set Output Enable (PULS7SOE to PULS0SOE): These bits enable or disable 1 output to the APC pulse output pins (PULS7 to PULS0) bit by bit.

#### Bits 7 to 0:

PULS7SOE to PULS0SOE	Description
0	1 output to APC pulse output pin (PULS7 to PULS0) is disabled (Initial value)
1	1 output to APC pulse output pin (PULS7 to PULS0) is enabled

When one of these bits is set to 1, 1 is output from the corresponding pin on a compare-match between the GR11A and TCNT11 values.

## 11.3 Operation

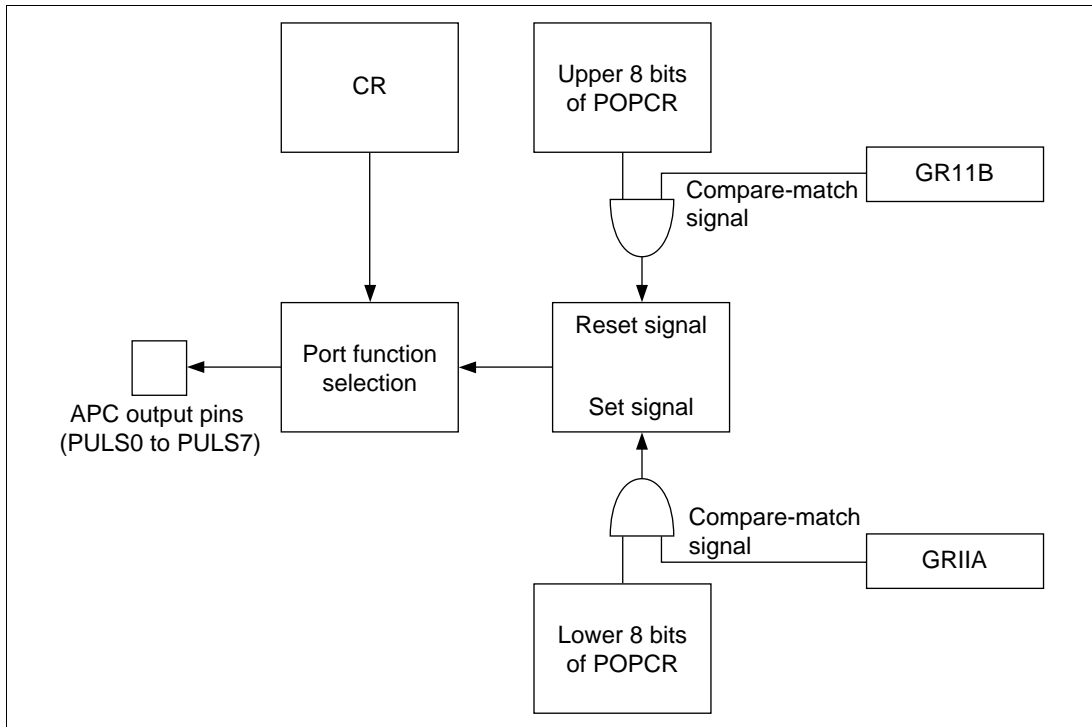
### 11.3.1 Overview

APC pulse output is enabled by designating multiplex pins for APC pulse output with the pin function controller (PFC), and setting the corresponding bits to 1 in the pulse output port control register (POPCR).

When general register 11A (GR11A) in the advanced timer unit II (ATU-II) subsequently generates a compare-match signal, 1 is output from the pins set to 1 by bits 7 to 0 in POPCR. When general register 11B (GR11B) generates a compare-match signal, 0 is output from the pins set to 1 by bits 15 to 8 in POPCR.

0 is output from the output-enabled state until the first compare-match occurs.

The advanced pulse controller output operation is shown in figure 11.2.

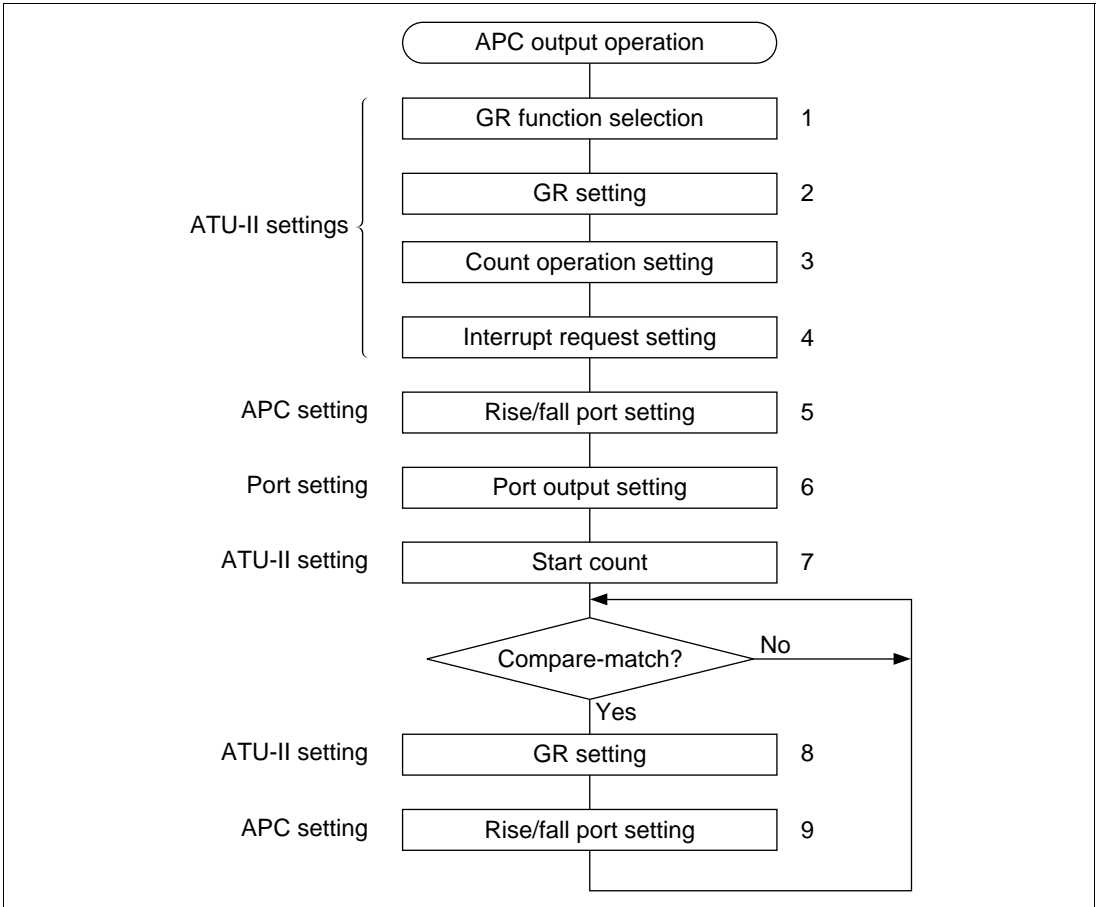


**Figure 11.2 Advanced Pulse Controller Output Operation**

### 11.3.2 Advanced Pulse Controller Output Operation

**Example of Setting Procedure for Advanced Pulse Controller Output Operation:** Figure 11.3 shows an example of the setting procedure for advanced pulse controller output operation.

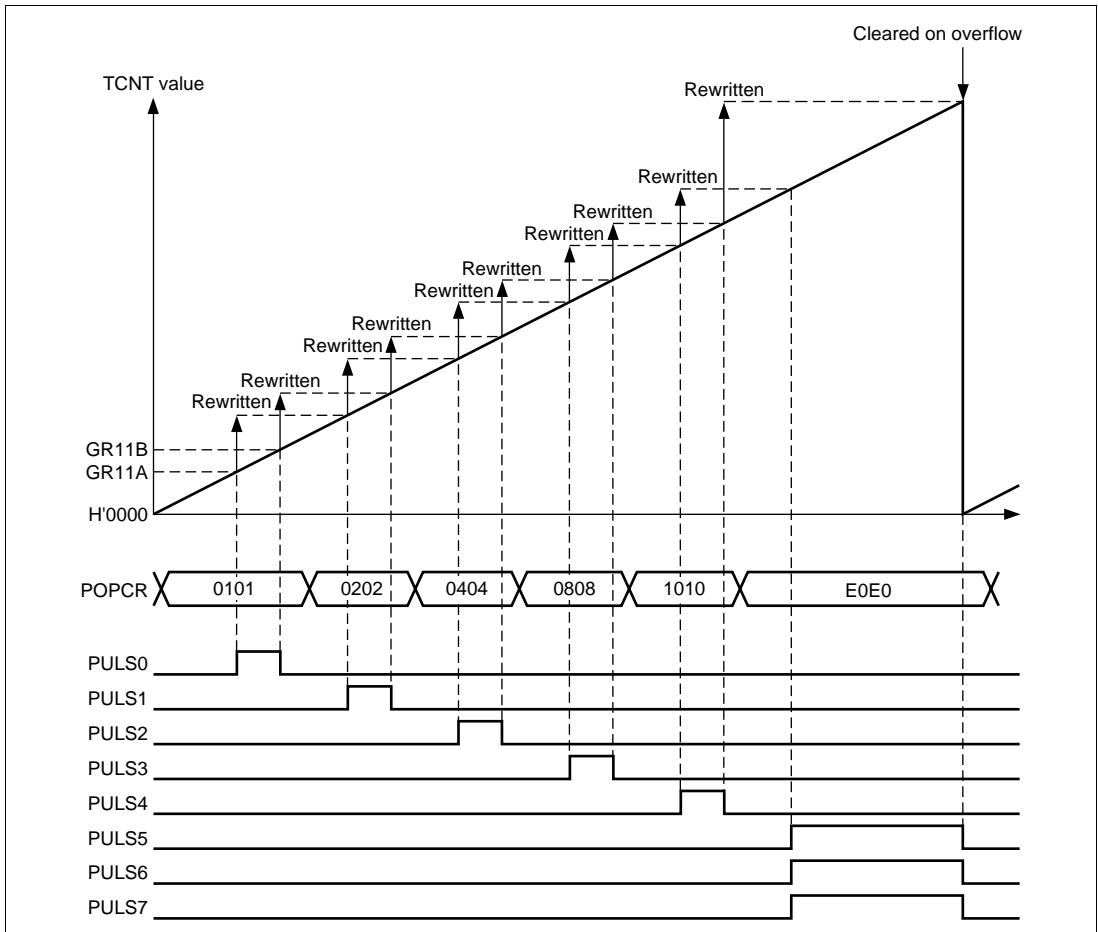
1. Set general registers GR11A and GR11B as output compare registers with the timer I/O control register (TIOR).
2. Set the pulse rise point with GR11A and the pulse fall point with GR11B.
3. Select the timer counter 11 (TCNT11) counter clock with the timer prescale register (PSCR). TCNT11 can only be cleared by an overflow.
4. Enable the respective interrupts with the timer interrupt enable register (TIER).
5. Set the pins for 1 output and 0 output with POPCR.
6. Set the control register for the port to be used by the APC to the APC output pin function.
7. Set the STR bit to 1 in the timer start register (TSTR) to start timer counter 11 (TCNT11).
8. Each time a compare-match interrupt is generated, update the GR value and set the next pulse output time.
9. Each time a compare-match interrupt is generated, update the POPCR value and set the next pin for pulse output.



**Figure 11.3 Example of Setting Procedure for Advanced Pulse Controller Output Operation**

**Example of Advanced Pulse Controller Output Operation:** Figure 11.4 shows an example of advanced pulse controller output operation.

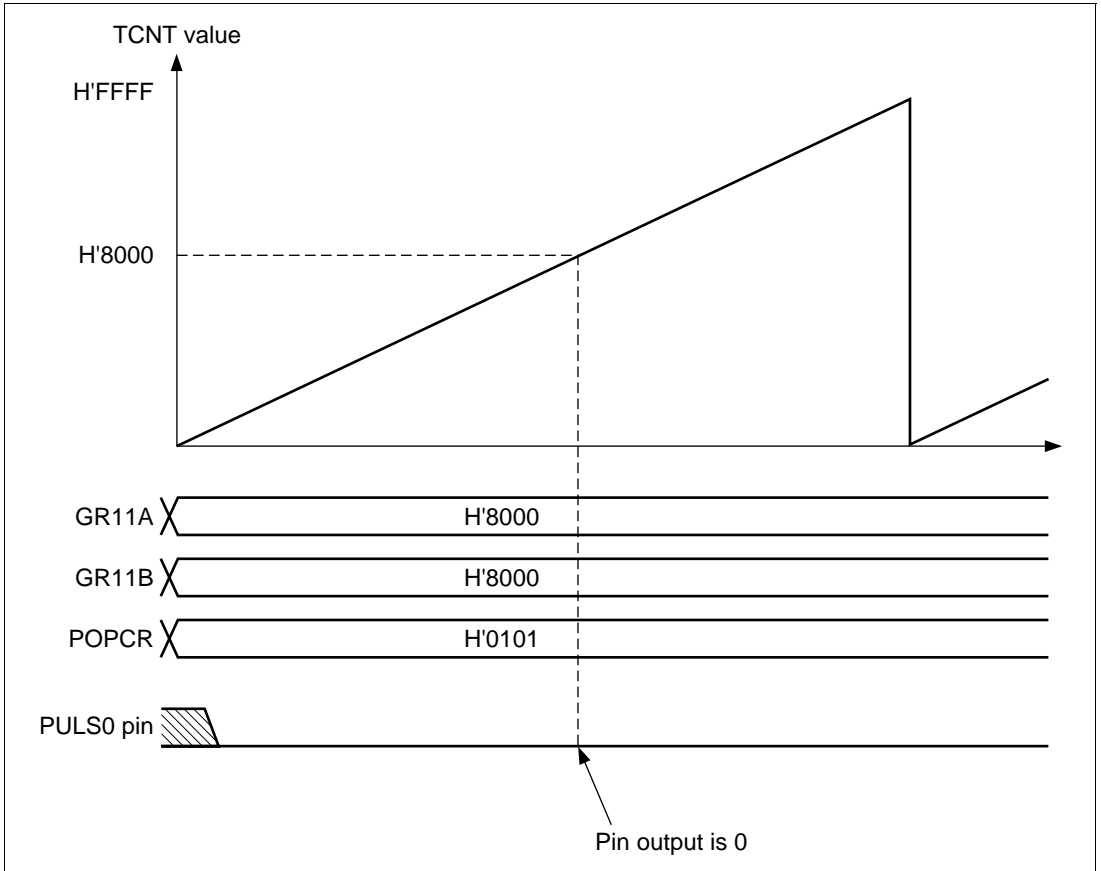
1. Set ATU-11 registers GR11A and GR11B (to be used for output trigger generation) as output compare registers. Set the rise point in GR11A and the fall point in GR11B, and enable the respective compare-match interrupts.
2. Write H'0101 to POPCR.
3. Start the ATU timer 2 count. When a GR11A compare-match occurs, 1 is output from the PULS0 pin. When a GR11B compare-match occurs, 0 is output from the PULS0 pin.
4. Pulse output widths and output pins can be continually changed by successively rewriting GR11A, GR11B, and POPCR in response to compare-match interrupts.
5. By setting POPCR to a value such as H'E0E0, pulses can be output from up to 8 pins in response to a single compare-match.



**Figure 11.4 Example of Advanced Pulse Controller Output Operation**

## 11.4 Usage Notes

**Contention between Compare-Match Signals:** If the same value is set for both GR11A and GR11B, and 0 output and 1 output are both enabled for the same pin by the POPCR settings, 0 output has priority on pins PULS0 to PULS7 when compare-matches occur.



**Figure 11.5 Example of Compare-Match Contention**



# Section 12 Watchdog Timer (WDT)

## 12.1 Overview

The watchdog timer (WDT) is a 1-channel timer for monitoring system operations. If a system encounters a problem (crashes, for example) and the timer counter overflows without being rewritten correctly by the CPU, an overflow signal ( $\overline{\text{WDTOVF}}$ ) is output externally. The WDT can simultaneously generate an internal reset signal for the entire chip.

When the watchdog function is not needed, the WDT can be used as an interval timer. In the interval timer operation, an interval timer interrupt is generated at each counter overflow. The WDT is also used in recovering from standby mode.

### 12.1.1 Features

The WDT has the following features:

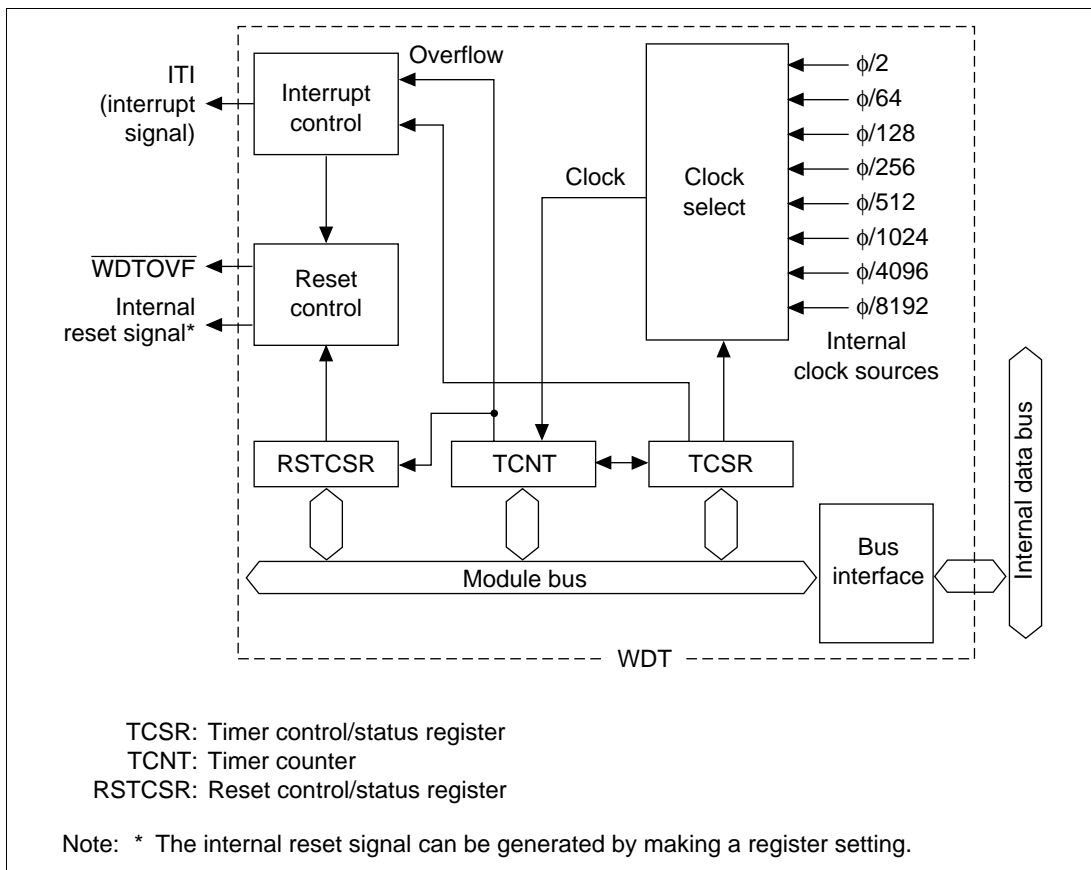
- Works in watchdog timer mode or interval timer mode
- Outputs  $\overline{\text{WDTOVF}}$  in watchdog timer mode

When the counter overflows in watchdog timer mode, overflow signal  $\overline{\text{WDTOVF}}$  is output externally. It is possible to select whether to reset the chip internally when this happens. Either the power-on reset or manual reset signal can be selected as the internal reset signal.

- Generates interrupts in interval timer mode  
When the counter overflows, it generates an interval timer interrupt.
- Clears software standby mode
- Works with eight counter input clocks

## 12.1.2 Block Diagram

Figure 12.1 is the block diagram of the WDT.



**Figure 12.1 WDT Block Diagram**

## 12.1.3 Pin Configuration

Table 12.1 shows the pin configuration.

**Table 12.1 Pin Configuration**

Pin	Abbreviation	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$	O	Outputs the counter overflow signal in watchdog timer mode



## 12.1.4 Register Configuration

Table 12.2 summarizes the three WDT registers. They are used to select the clock, switch the WDT mode, and control the reset signal.

**Table 12.2 WDT Registers**

Name	Abbreviation	R/W	Initial Value	Address	
				Write* <sup>1</sup>	Read* <sup>2</sup>
Timer control/status register	TCSR	R/(W)* <sup>3</sup>	H'18	H'FFFFEC10	H'FFFFEC10
Timer counter	TCNT	R/W	H'00		H'FFFFEC11
Reset control/status register	RSTCSR	R/(W)* <sup>3</sup>	H'1F	H'FFFFEC12	H'FFFFEC13

- Notes:
1. Write by word transfer. These registers cannot be written in byte or longword.
  2. Read by byte transfer. These registers cannot be read in word or longword.
  3. Only 0 can be written to bit 7 to clear the flag.
  4. In register access, three cycles are required for both byte access and word access.

## 12.2 Register Descriptions

### 12.2.1 Timer Counter (TCNT)

TCNT is an 8-bit readable/writable upcounter. (TCNT differs from other registers in that it is more difficult to write to. See section 12.2.4, Register Access, for details.) When the timer enable bit (TME) in the timer control/status register (TCSR) is set to 1, the watchdog timer counter starts counting pulses of an internal clock selected by clock select bits 2 to 0 (CKS2 to CKS0) in TCSR. When the value of TCNT overflows (changes from H'FF to H'00), a watchdog timer overflow signal ( $\overline{\text{WDTOVF}}$ ) or interval timer interrupt (ITI) is generated, depending on the mode selected in the  $\overline{\text{WT/IT}}$  bit of TCSR.

TCNT is initialized to H'00 by a power-on reset, in hardware and software standby modes, and when the TME bit is cleared to 0.

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## 12.2.2 Timer Control/Status Register (TCSR)

The timer control/status register (TCSR) is an 8-bit readable/writable register. (TCSR differs from other registers in that it is more difficult to write to. See section 12.2.4, Register Access, for details.) TCSR performs selection of the timer counter (TCNT) input clock and mode.

Bits 7 to 5 are initialized to 000 by a power-on reset, and in hardware standby mode and software standby mode. Bits 2 to 0 are initialized to 000 by a power-on reset and in hardware standby mode, but retain their values in software standby mode.

Bit:	7	6	5	4	3	2	1	0
	OVF	WT/ $\overline{\text{IT}}$	TME	—	—	CKS2	CKS1	CKS0
Initial value:	0	0	0	1	1	0	0	0
R/W:	R/(W)*	R/W	R/W	R	R	R/W	R/W	R/W

Note: \* The only operation permitted on the OVF bit is a write of 0 after reading 1.

- Bit 7—Overflow Flag (OVF): Indicates that TCNT has overflowed from H'FF to H'00 in interval timer mode. This flag is not set in the watchdog timer mode.

Bit 7: OVF	Description
0	No overflow of TCNT in interval timer mode (Initial value) [Clearing condition] When 0 is written to OVF after reading OVF
1	TCNT overflow in interval timer mode

- Bit 6—Timer Mode Select (WT/ $\overline{\text{IT}}$ ): Selects whether to use the WDT as a watchdog timer or interval timer. When TCNT overflows, the WDT either generates an interval timer interrupt (ITI) or generates a  $\overline{\text{WDTOVF}}$  signal, depending on the mode selected.

Bit 6: WT/ $\overline{\text{IT}}$	Description
0	Interval timer mode: interval timer interrupt (ITI) request to the CPU when TCNT overflows (Initial value)
1	Watchdog timer mode: $\overline{\text{WDTOVF}}$ signal output externally when TCNT overflows. (Section 12.2.3, Reset Control/Status Register (RSTCSR), describes in detail what happens when TCNT overflows in watchdog timer mode.)

- Bit 5—Timer Enable (TME): Enables or disables the timer.

Bit 5: TME	Description
0	Timer disabled: TCNT is initialized to H'00 and count-up stops (Initial value)
1	Timer enabled: TCNT starts counting. A $\overline{\text{WDTOVF}}$ signal or interrupt is generated when TCNT overflows.

- Bits 4 and 3—Reserved: These bits always read 1. The write value should always be 1.
- Bits 2 to 0: Clock Select 2 to 0 (CKS2 to CKS0): These bits select one of eight internal clock sources for input to TCNT. The clock signals are obtained by dividing the frequency of the system clock ( $\phi$ ).

Bit 2: CKS2	Bit 1: CKS1	Bit 0: CKS0	Description	
			Clock Source	Overflow Interval* ( $\phi = 40 \text{ MHz}$ )
0	0	0	$\phi/2$ (Initial value)	12.8 $\mu\text{s}$
0	0	1	$\phi/64$	409.6 $\mu\text{s}$
0	1	0	$\phi/128$	0.8 ms
0	1	1	$\phi/256$	1.6 ms
1	0	0	$\phi/512$	3.3 ms
1	0	1	$\phi/1024$	6.6 ms
1	1	0	$\phi/4096$	26.2 ms
1	1	1	$\phi/8192$	52.4 ms

Note: \* The overflow interval listed is the time from when the TCNT begins counting at H'00 until an overflow occurs.

### 12.2.3 Reset Control/Status Register (RSTCSR)

RSTCSR is an 8-bit readable/writable register. (RSTCSR differs from other registers in that it is more difficult to write. See section 12.2.4, Register Access, for details.) It controls output of the internal reset signal generated by timer counter (TCNT) overflow. RSTCSR is initialized to H'1F by input of a reset signal from the  $\overline{\text{RES}}$  pin, but is not initialized by the internal reset signal generated by overflow of the WDT. It is initialized to H'1F in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
	WOVF	RSTE	RSTS	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/(W)*	R/W	R/W	R	R	R	R	R

Note: Only 0 can be written to bit 7 to clear the flag.

- Bit 7—Watchdog Timer Overflow Flag (WOVF): Indicates that TCNT has overflowed (H'FF to H'00) in watchdog timer mode. This flag is not set in interval timer mode.

Bit 7: WOVF	Description
0	No TCNT overflow in watchdog timer mode (Initial value) [Clearing condition] When 0 is written to WOVF after reading WOVF
1	Set by TCNT overflow in watchdog timer mode

- Bit 6—Reset Enable (RSTE): Selects whether to reset the chip internally if TCNT overflows in watchdog timer mode.

Bit 6: RSTE	Description
0	Not reset when TCNT overflows (Initial value) LSI not reset internally, but TCNT and TCSR reset within WDT.
1	Reset when TCNT overflows

- Bit 5—Reset Select (RSTS): Selects the kind of internal reset to be generated when TCNT overflows in watchdog timer mode.

Bit 5: RSTS	Description
0	Power-on reset (Initial value)
1	Manual reset

- Bits 4 to 0—Reserved: These bits always read 1. The write value should always be 1.

## 12.2.4 Register Access

The watchdog timer's TCNT, TCSR, and RSTCSR registers differ from other registers in that they are more difficult to write to. The procedures for writing and reading these registers are given below.

**Writing to TCNT and TCSR:** These registers must be written by a word transfer instruction. They cannot be written by byte transfer instructions.

TCNT and TCSR both have the same write address. The write data must be contained in the lower byte of the written word. The upper byte must be H'5A (for TCNT) or H'A5 (for TCSR) (figure 12.2). This transfers the write data from the lower byte to TCNT or TCSR.



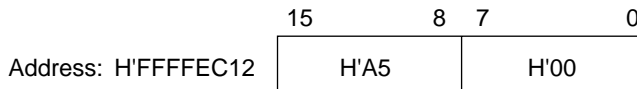
**Figure 12.2 Writing to TCNT and TCSR**

**Writing to RSTCSR:** RSTCSR must be written by a word access to address H'FFFEC12. It cannot be written by byte transfer instructions.

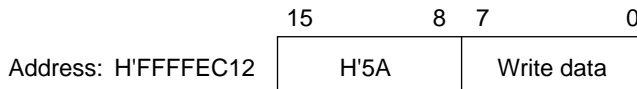
Procedures for writing 0 to WOVF (bit 7) and for writing to RSTE (bit 6) and RSTS (bit 5) are different, as shown in figure 12.3.

To write 0 to the WOVF bit, the write data must be H'A5 in the upper byte and H'00 in the lower byte. This clears the WOVF bit to 0. The RSTE and RSTS bits are not affected. To write to the RSTE and RSTS bits, the upper byte must be H'5A and the lower byte must be the write data. The values of bits 6 and 5 of the lower byte are transferred to the RSTE and RSTS bits, respectively. The WOVF bit is not affected.

### Writing 0 to the WOVF bit



### Writing to the RSTE and RSTS bits



**Figure 12.3 Writing to RSTCSR**

**Reading from TCNT, TCSR, and RSTCSR:** TCNT, TCSR, and RSTCSR are read like other registers. Use byte transfer instructions. The read addresses are H'FFFFEC10 for TCSR, H'FFFFEC11 for TCNT, and H'FFFFEC13 for RSTCSR.

## 12.3 Operation

### 12.3.1 Watchdog Timer Mode

To use the WDT as a watchdog timer, set the  $\overline{WT/IT}$  and TME bits of TCSR to 1. Software must prevent TCNT overflow by rewriting the TCNT value (normally by writing H'00) before overflow occurs. No TCNT overflows will occur while the system is operating normally, but if TCNT fails to be rewritten and overflows occur due to a system crash or the like, a  $\overline{WDTOVF}$  signal is output externally (figure 12.4). The  $\overline{WDTOVF}$  signal can be used to reset the system. The  $\overline{WDTOVF}$  signal is output for 128  $\phi$  clock cycles.

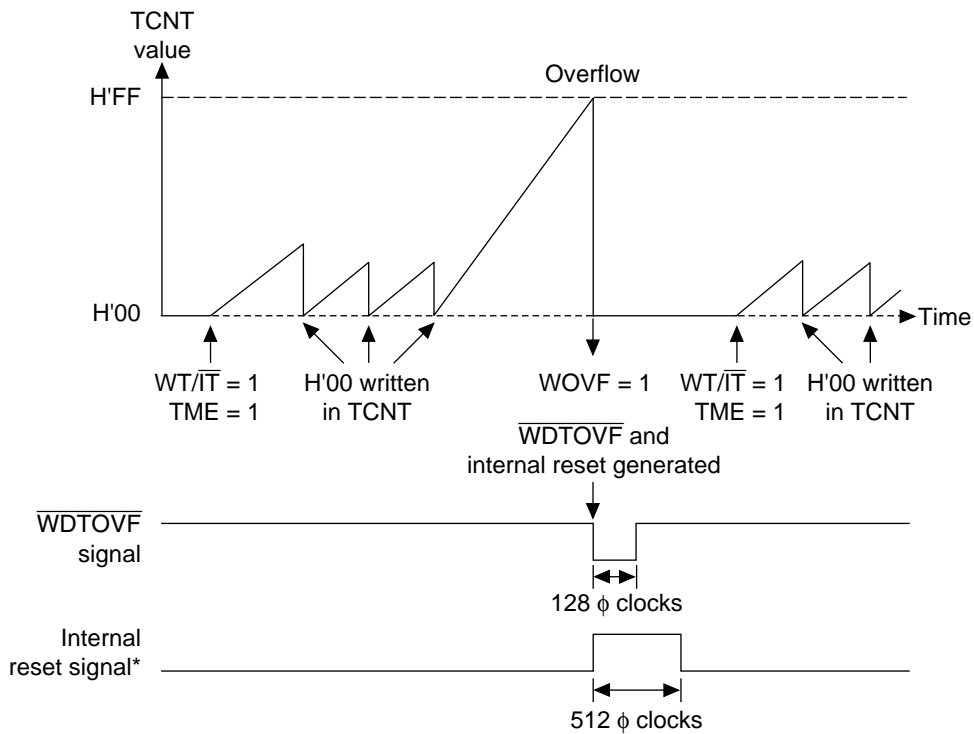
If the RSTE bit in the reset control/status register (RSTCSR) is set to 1, a signal that resets the chip internally will be generated at the same time as the  $\overline{WDTOVF}$  signal when TCNT overflows. Either a power-on reset or a manual reset can be selected by the RSTS bit in RSTCSR. The internal reset signal is output for 512  $\phi$  clock cycles.

When a WDT overflow reset is generated simultaneously with a reset input at the  $\overline{RES}$  pin, the  $\overline{RES}$  reset takes priority, and the WOVF bit in RSTCSR is cleared to 0.

The following are not initialized by a WDT reset signal:

- PFC (pin function controller) registers
- I/O port registers

These registers are initialized only by an external power-on reset.



$WT/\overline{IT}$ : Timer mode select bit  
 $TME$ : Timer enable bit

Note: \* Internal reset signal occurs only when the RSTE bit is set to 1.

**Figure 12.4 Operation in Watchdog Timer Mode**

### 12.3.2 Interval Timer Mode

To use the WDT as an interval timer, clear  $\overline{WT/IT}$  to 0 and set TME to 1 in TCSR. An interval timer interrupt (ITI) is generated each time the timer counter overflows. This function can be used to generate interval timer interrupts at regular intervals (figure 12.5).

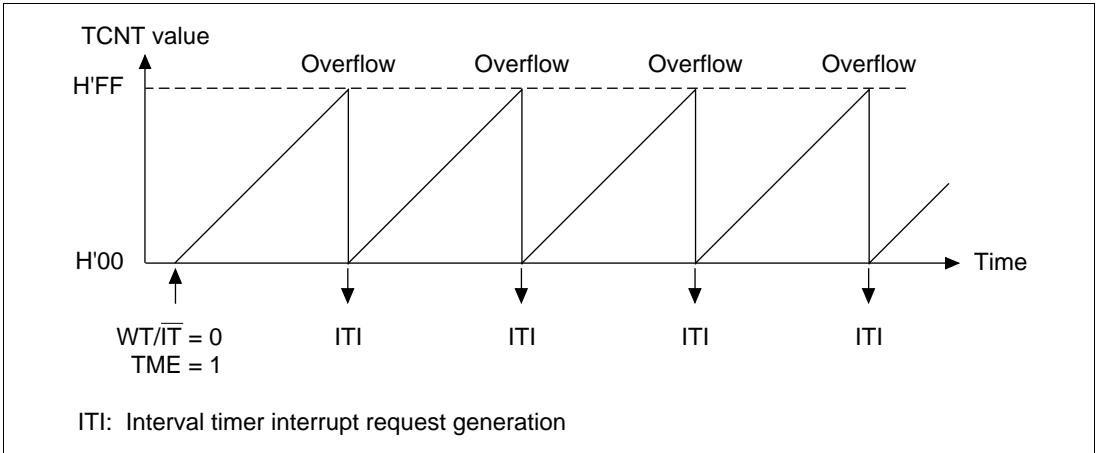


Figure 12.5 Operation in Interval Timer Mode

### 12.3.3 Clearing Software Standby Mode

The watchdog timer has a special function to clear software standby mode with an NMI interrupt. When using software standby mode, set the WDT as described below.

**Before Transition to Software Standby Mode:** The TME bit in TCSR must be cleared to 0 to stop the watchdog timer counter before entering software standby mode. The chip cannot enter software standby mode while the TME bit is set to 1. Set bits CKS2 to CKS0 in TCSR so that the counter overflow interval is equal to or longer than the oscillation settling time. See section 24.3, AC Characteristics, for the oscillation settling time.

**Recovery from Software Standby Mode:** When an NMI request signal is received in software standby mode, the clock oscillator starts running and the watchdog timer starts incrementing at the rate selected by bits CKS2 to CKS0 before software standby mode was entered. When TCNT overflows (changes from H'FF to H'00), the clock is presumed to be stable and usable; clock signals are supplied to the entire chip and software standby mode ends.

For details on software standby mode, see section 23, Power-Down State.



### 12.3.4 Timing of Setting the Overflow Flag (OVF)

In interval timer mode, when TCNT overflows, the OVF flag of TCSR is set to 1 and an interval timer interrupt (ITI) is simultaneously requested (figure 12.6).

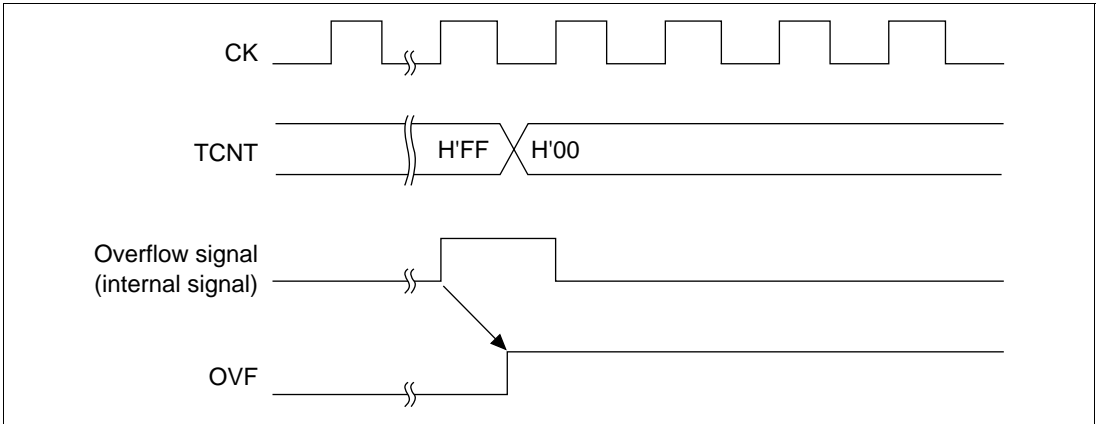


Figure 12.6 Timing of Setting OVF

### 12.3.5 Timing of Setting the Watchdog Timer Overflow Flag (WOVF)

When TCNT overflows in watchdog timer mode, the WOVF bit of RSTCSR is set to 1 and a  $\overline{\text{WDTOVF}}$  signal is output. When the RSTE bit in RSTCSR is set to 1, TCNT overflow enables an internal reset signal to be generated for the entire chip (figure 12.7).

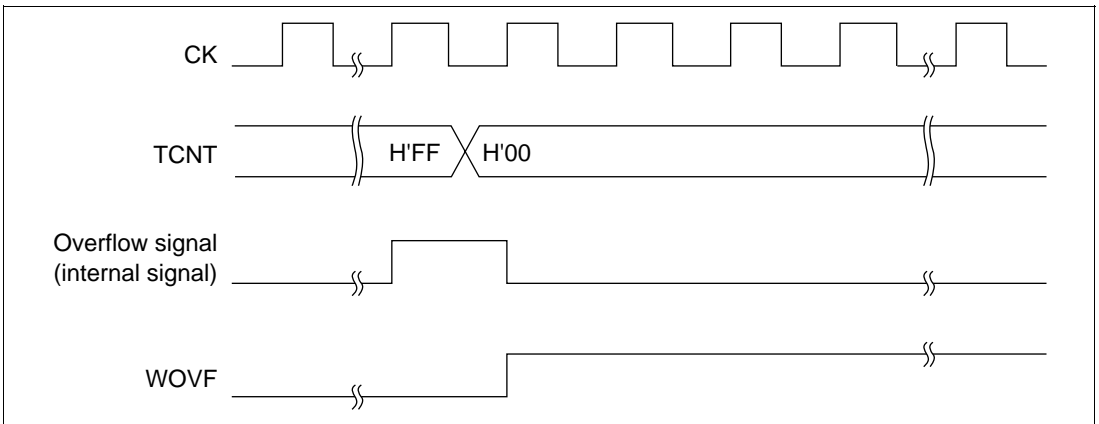
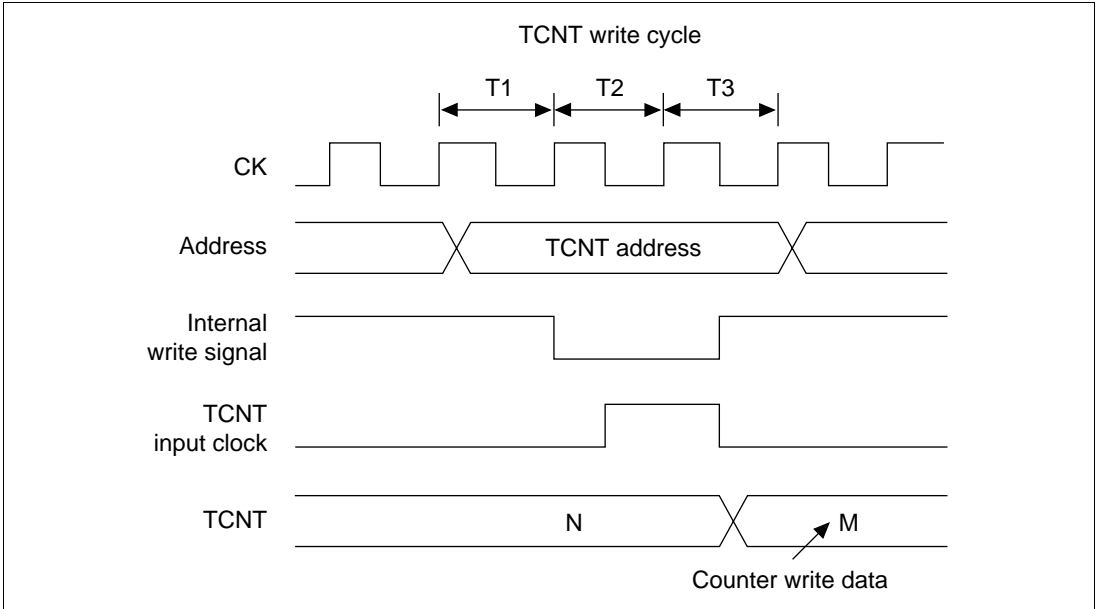


Figure 12.7 Timing of Setting WOVF

## 12.4 Usage Notes

### 12.4.1 TCNT Write and Increment Contention

If a timer counter increment clock pulse is generated during the T3 state of a write cycle to TCNT, the write takes priority and the timer counter is not incremented (figure 12.8).



**Figure 12.8 Contention between TCNT Write and Increment**

### 12.4.2 Changing CKS2 to CKS0 Bit Values

If the values of bits CKS2 to CKS0 in the timer control/status register (TCSR) are rewritten while the WDT is running, the count may not increment correctly. Always stop the watchdog timer (by clearing the TME bit to 0) before changing the values of bits CKS2 to CKS0.

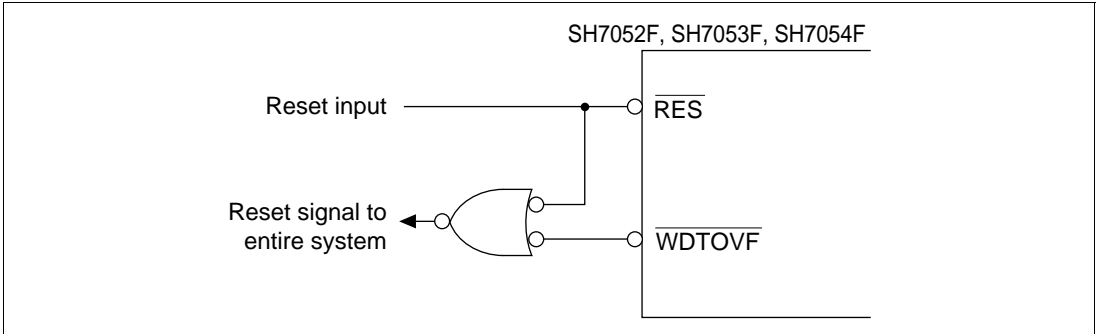
### 12.4.3 Changing between Watchdog Timer/Interval Timer Modes

To prevent incorrect operation, always stop the watchdog timer (by clearing the TME bit to 0) before switching between interval timer mode and watchdog timer mode.

#### 12.4.4 System Reset by $\overline{\text{WDTOVF}}$ Signal

If a  $\overline{\text{WDTOVF}}$  signal is input to the  $\overline{\text{RES}}$  pin, the chip cannot initialize correctly.

Avoid logical input of the  $\overline{\text{WDTOVF}}$  output signal to the  $\overline{\text{RES}}$  input pin. To reset the entire system with the  $\overline{\text{WDTOVF}}$  signal, use the circuit shown in figure 12.9.



**Figure 12.9 Example of System Reset Circuit Using  $\overline{\text{WDTOVF}}$  Signal**

#### 12.4.5 Internal Reset in Watchdog Timer Mode

If the RSTE bit is cleared to 0 in watchdog timer mode, the chip will not be reset internally when a TCNT overflow occurs, but TCNT and TCSR in the WDT will be reset.

#### 12.4.6 Manual Reset in Watchdog Timer

When an internal reset is effected by TCNT overflow in watchdog timer mode, the processor waits until the end of the bus cycle at the time of manual reset generation before making the transition to manual reset exception processing. Therefore, the bus cycle is retained in a manual reset, but if a manual reset occurs while the bus is released or during DMAC burst transfer, manual reset exception processing will be deferred until the CPU acquires the bus. However, if the interval from generation of the manual reset until the end of the bus cycle is equal to or longer than the internal manual reset interval of 512 cycles, the internal manual reset source is ignored instead of being deferred, and manual reset exception processing is not executed.



# Section 13 Compare Match Timer (CMT)

## 13.1 Overview

The SH7052F/SH7053F/SH7054F has an on-chip compare match timer (CMT) comprising two 16-bit timer channels. The CMT has 16-bit counters and can generate interrupts at set intervals.

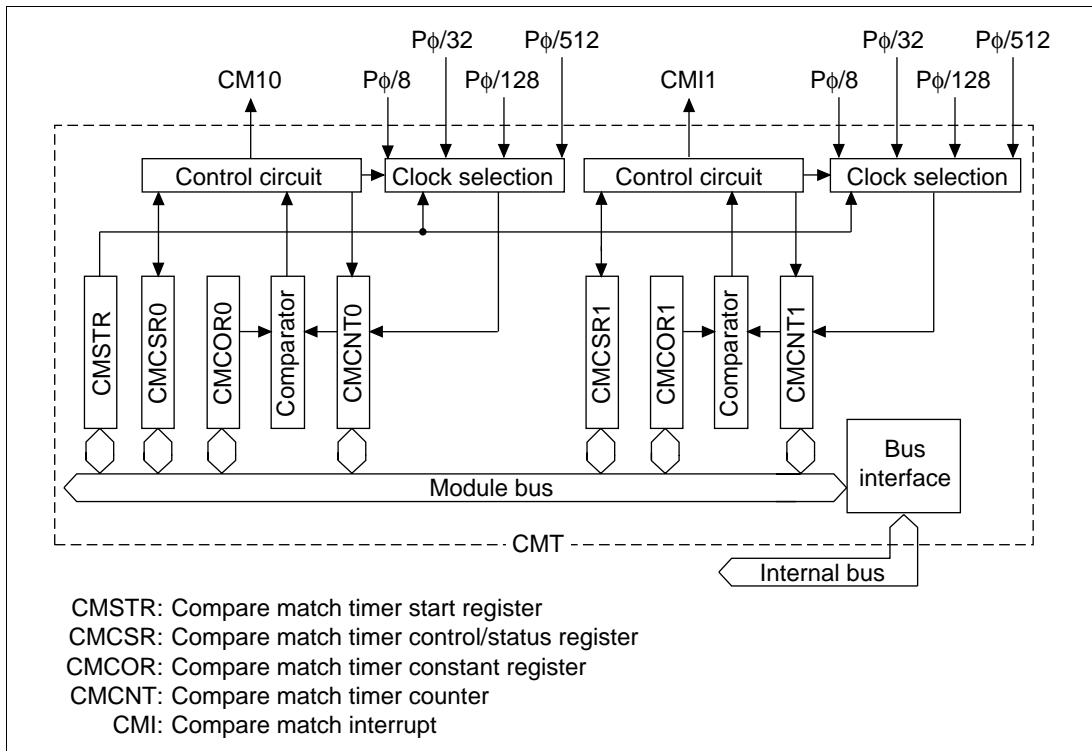
### 13.1.1 Features

The CMT has the following features:

- Four types of counter input clock can be selected
  - One of four internal clocks ( $P\phi/8$ ,  $P\phi/32$ ,  $P\phi/128$ ,  $P\phi/512$ ) can be selected independently for each channel.
- Interrupt sources
  - A compare match interrupt can be requested independently for each channel.

### 13.1.2 Block Diagram

Figure 13.1 shows a block diagram of the CMT.



**Figure 13.1 CMT Block Diagram**

### 13.1.3 Register Configuration

Table 13.1 summarizes the CMT register configuration.

**Table 13.1 Register Configuration**

Channel Name	Abbreviation	R/W	Initial Value	Address	Access Size (Bits)
Shared	Compare match timer start register	CMSTR	R/W	H'0000	H'FFFFFF710 8, 16, 32
0	Compare match timer control/status register 0	CMCSR0	R/(W)*1	H'0000	H'FFFFFF712 8, 16, 32
	Compare match timer counter 0	CMCNT0	R/W	H'0000	H'FFFFFF714 8, 16, 32
	Compare match timer constant register 0	CMCOR0	R/W	H'FFFF	H'FFFFFF716 8, 16, 32
1	Compare match timer control/status register 1	CMCSR1	R/(W)*1	H'0000	H'FFFFFF718 8, 16, 32
	Compare match timer counter 1	CMCNT1	R/W	H'0000	H'FFFFFF71A 8, 16, 32
	Compare match timer constant register 1	CMCOR1	R/W	H'FFFF	H'FFFFFF71C 8, 16, 32

- Notes:
1. The only value that can be written to the CMCSR0 and CMCSR1 CMF bits is a 0 to clear the flags.
  2. With regard to access size, four or five cycles are required for byte access and word access, and eight or nine cycles for longword access.

## 13.2 Register Descriptions

### 13.2.1 Compare Match Timer Start Register (CMSTR)

The compare match timer start register (CMSTR) is a 16-bit register that selects whether to operate or halt the channel 0 and channel 1 counters (CMCNT). It is initialized to H'0000 by a power-on reset and in the standby modes.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	STR1	STR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

- Bits 15 to 2—Reserved: These bits always read 0. The write value should always be 0.
- Bit 1—Count Start 1 (STR1): Selects whether to operate or halt compare match timer counter 1.

Bit 1: STR1	Description
0	CMCNT1 count operation halted (Initial value)
1	CMCNT1 count operation

- Bit 0—Count Start 0 (STR0): Selects whether to operate or halt compare match timer counter 0.

Bit 0: STR0	Description
0	CMCNT0 count operation halted (Initial value)
1	CMCNT0 count operation



### 13.2.2 Compare Match Timer Control/Status Register (CMCSR)

The compare match timer control/status register (CMCSR) is a 16-bit register that indicates the occurrence of compare matches, sets the enable/disable status of interrupts, and establishes the clock used for incrementation. It is initialized to H'0000 by a power-on reset and in the standby modes.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	CMF	CMIE	—	—	—	—	CKS1	CKS0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R	R	R	R	R/W	R/W

Note: \* The only value that can be written is a 0 to clear the flag.

- Bits 15 to 8 and 5 to 2—Reserved: These bits always read 0. The write value should always be 0.
- Bit 7—Compare Match Flag (CMF): This flag indicates whether or not the CMCNT and CMCOR values have matched.

Bit 7: CMF	Description
0	CMCNT and CMCOR values have not matched (Initial value) [Clearing condition] Write 0 to CMF after reading 1 from it
1	CMCNT and CMCOR values have matched

- Bit 6—Compare Match Interrupt Enable (CMIE): Selects whether to enable or disable a compare match interrupt (CMI) when the CMCNT and CMCOR values have matched (CMF = 1).

Bit 6: CMIE	Description
0	Compare match interrupt (CMI) disabled (Initial value)
1	Compare match interrupt (CMI) enabled

- Bits 1 and 0—Clock Select 1 and 0 (CKS1, CKS0): These bits select the clock input to CMCNT from among the four internal clocks obtained by dividing the peripheral clock ( $P\phi$ ). When the STR bit of CMSTR is set to 1, CMCNT begins incrementing with the clock selected by CKS1 and CKS0.

Bit 1: CKS1	Bit 0: CKS0	Description
0	0	$P\phi/8$ (Initial value)
	1	$P\phi/32$
1	0	$P\phi/128$
	1	$P\phi/512$

### 13.2.3 Compare Match Timer Counter (CMCNT)

The compare match timer counter (CMCNT) is a 16-bit register used as an up-counter for generating interrupt requests.

When an internal clock is selected with the CKS1 and CKS0 bits of the CMCSR register and the STR bit of CMSTR is set to 1, CMCNT begins incrementing with that clock. When the CMCNT value matches that of the compare match timer constant register (CMCOR), CMCNT is cleared to H'0000 and the CMF flag of CMCSR is set to 1. If the CMIE bit of CMCSR is set to 1 at this time, a compare match interrupt (CMI) is requested.

CMCNT is initialized to H'0000 by a power-on reset and in the standby modes. It is not initialized by a manual reset.

Bit:	15	14	13	12	11	10	9	8
	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## 13.2.4 Compare Match Timer Constant Register (CMCOR)

The compare match timer constant register (CMCOR) is a 16-bit register that sets the period for compare match with CMCNT.

CMCOR is initialized to H'FFFF by a power-on reset and in the standby modes. It is not initialized by a manual reset.

Bit:	15	14	13	12	11	10	9	8
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## 13.3 Operation

### 13.3.1 Cyclic Count Operation

When an internal clock is selected with the CKS1, CKS0 bits of the CMCSR register and the STR bit of CMSTR is set to 1, CMCNT begins incrementing with the selected clock. When the CMCNT counter value matches that of the compare match constant register (CMCOR), the CMCNT counter is cleared to H'0000 and the CMF flag of the CMCSR register is set to 1. If the CMIE bit of the CMCSR register is set to 1 at this time, a compare match interrupt (CMI) is requested. The CMCNT counter begins counting up again from H'0000.

Figure 13.2 shows the compare match counter operation.

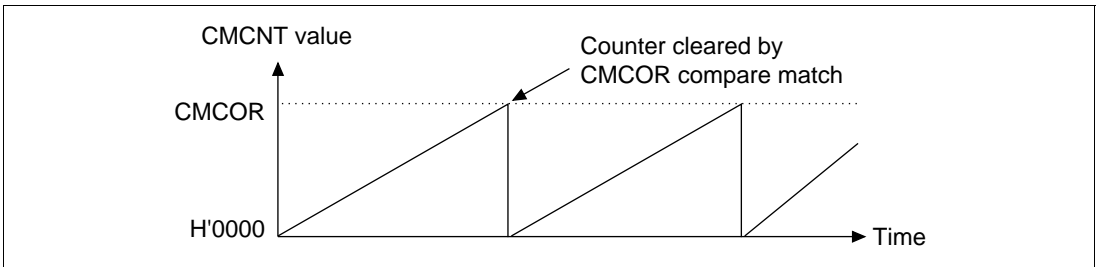


Figure 13.2 Counter Operation

### 13.3.2 CMCNT Count Timing

One of four clocks ( $P\phi/8$ ,  $P\phi/32$ ,  $P\phi/128$ ,  $P\phi/512$ ) obtained by dividing the peripheral clock ( $P\phi$ ) can be selected by the  $CKS1$  and  $CKS0$  bits of  $CMCSR$ . Figure 13.3 shows the timing.

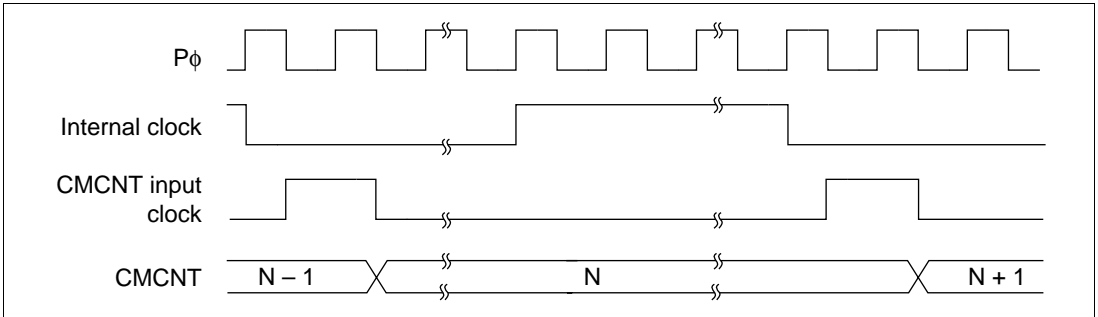


Figure 13.3 Count Timing

## 13.4 Interrupts

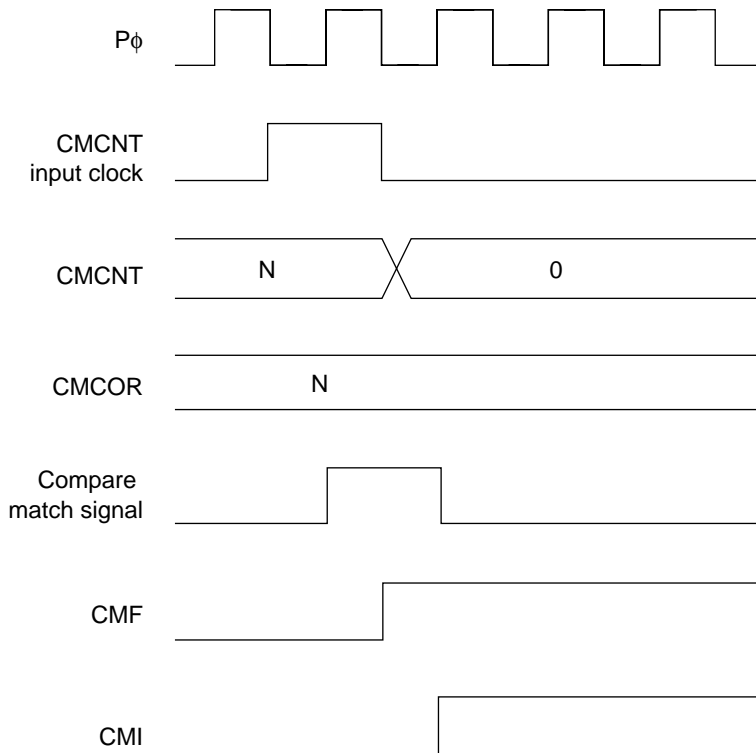
### 13.4.1 Interrupt Sources and DTC Activation

The CMT has a compare match interrupt for each channel, with independent vector addresses allocated to each of them. The corresponding interrupt request is output when interrupt request flag  $CMF$  is set to 1 and interrupt enable bit  $CMIE$  has also been set to 1.

When activating CPU interrupts by interrupt request, the priority between the channels can be changed by means of interrupt controller settings. See section 6, Interrupt Controller, for details.

### 13.4.2 Compare Match Flag Set Timing

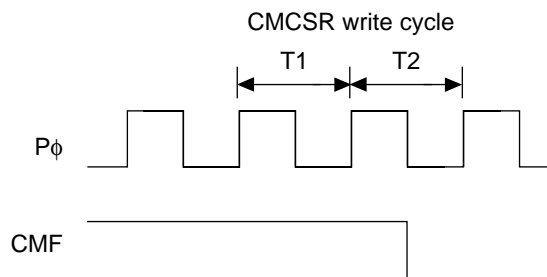
The  $CMF$  bit of the  $CMCSR$  register is set to 1 by the compare match signal generated when the  $CMCOR$  register and the  $CMCNT$  counter match. The compare match signal is generated upon the final state of the match (timing at which the  $CMCNT$  counter matching count value is updated). Consequently, after the  $CMCOR$  register and the  $CMCNT$  counter match, a compare match signal will not be generated until a  $CMCNT$  counter input clock occurs. Figure 13.4 shows the  $CMF$  bit set timing.



**Figure 13.4 CMF Set Timing**

### 13.4.3 Compare Match Flag Clear Timing

The CMF bit of the CMCSR register is cleared by writing a 0 to it after reading a 1. Figure 13.5 shows the timing when the CMF bit is cleared by the CPU.



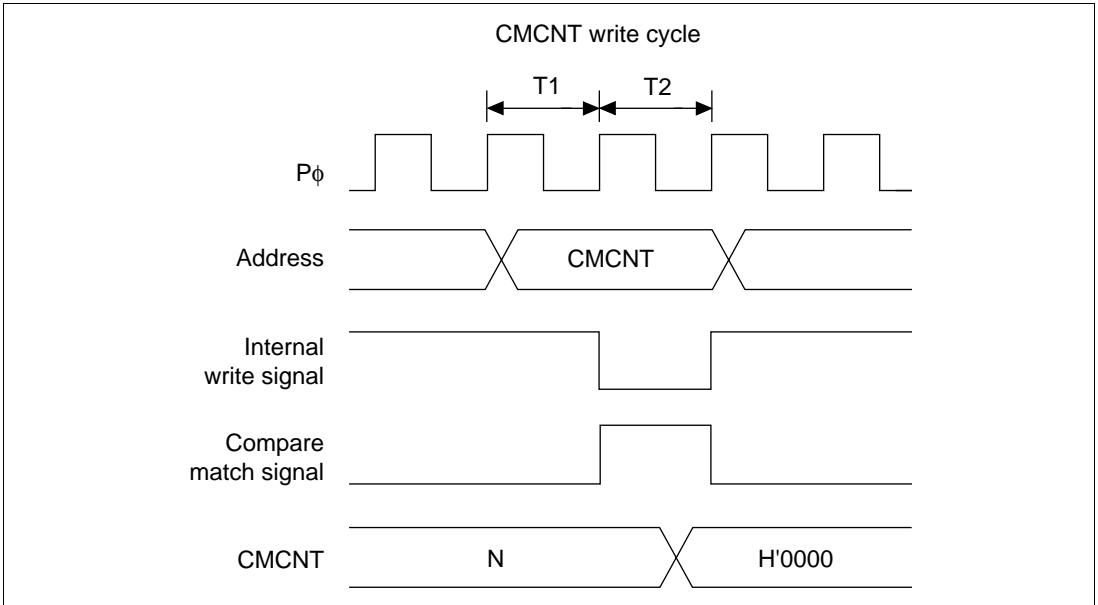
**Figure 13.5 Timing of CMF Clear by the CPU**

## 13.5 Usage Notes

Take care that the contentions described in sections 13.5.1 to 13.5.3 do not arise during CMT operation.

### 13.5.1 Contention between CMCNT Write and Compare Match

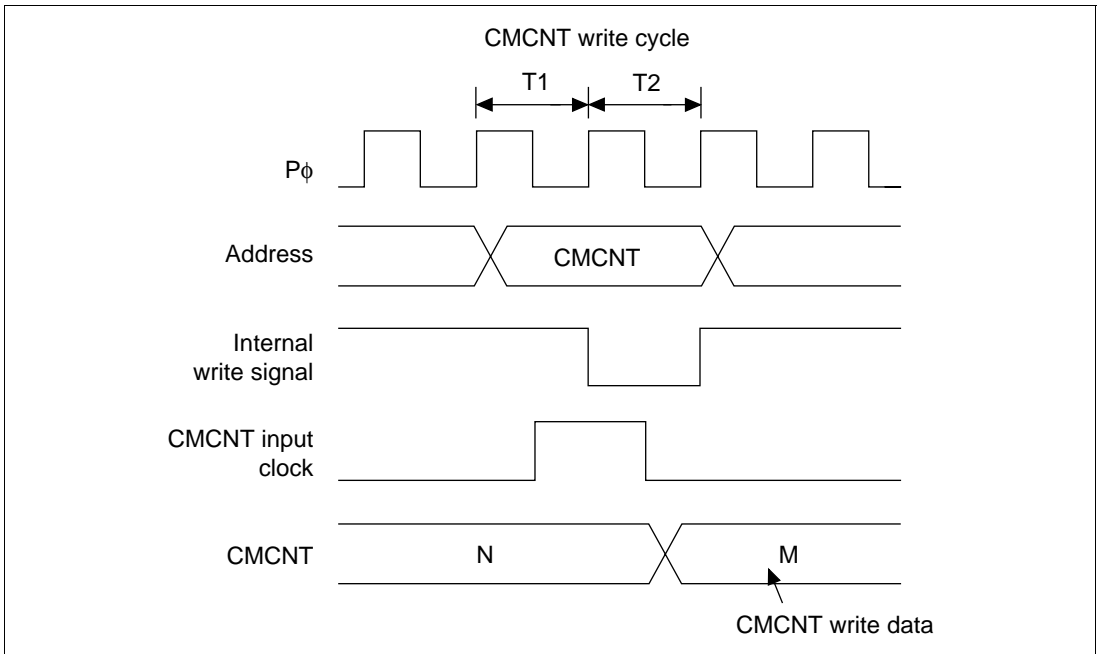
If a compare match signal is generated during the T2 state of the CMCNT counter write cycle, the CMCNT counter clear has priority, so the write to the CMCNT counter is not performed. Figure 13.6 shows the timing.



**Figure 13.6 CMCNT Write and Compare Match Contention**

### 13.5.2 Contention between CMCNT Word Write and Incrementation

If an increment occurs during the T2 state of the CMCNT counter word write cycle, the counter write has priority, so no increment occurs. Figure 13.7 shows the timing.



**Figure 13.7 CMCNT Word Write and Increment Contention**

### 13.5.3 Contention between CMCNT Byte Write and Incrementation

If an increment occurs during the T2 state of the CMCNT byte write cycle, the counter write has priority, so no increment of the write data results on the side on which the write was performed. The byte data on the side on which writing was not performed is also not incremented, so the contents are those before the write.

Figure 13.8 shows the timing when an increment occurs during the T2 state of the CMCNTH write cycle.

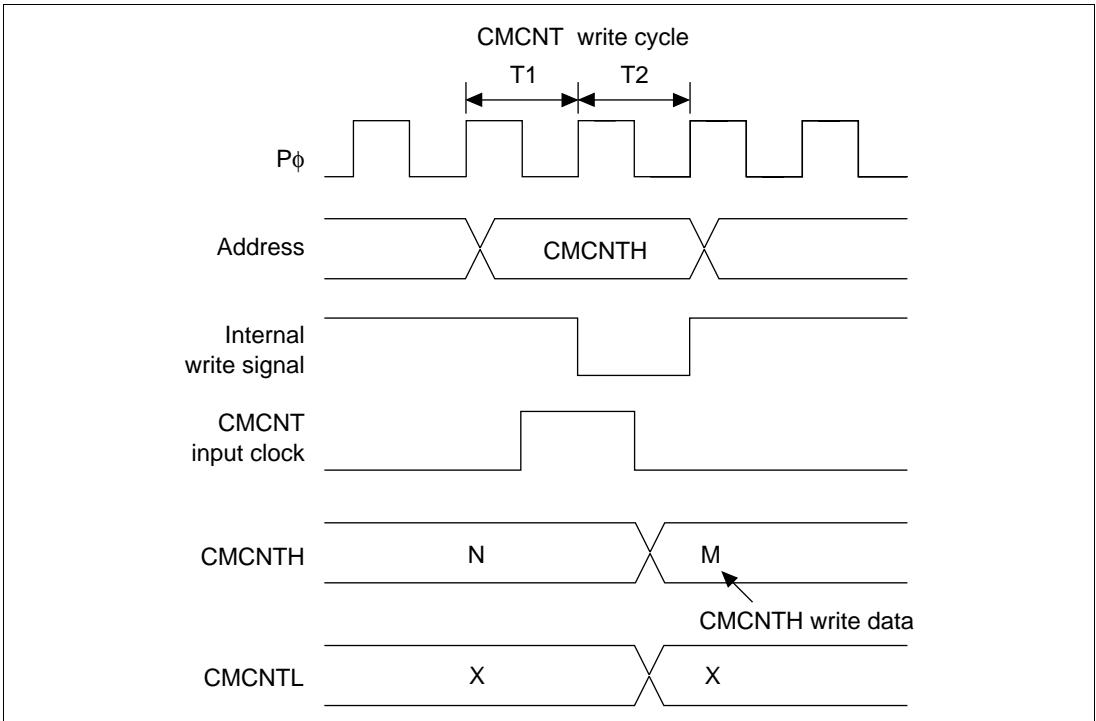


Figure 13.8 CMCNT Byte Write and Increment Contention



# Section 14 Serial Communication Interface (SCI)

## 14.1 Overview

The SH7052F/SH7053F/SH7054F has a serial communication interface (SCI) with five independent channels.

The SCI supports both asynchronous and synchronous serial communication. It also has a multiprocessor communication function for serial communication between two or more processors, and a clock inverted input/output function.

### 14.1.1 Features

The SCI has the following features:

- Selection of asynchronous or synchronous as the serial communication mode
  - Asynchronous mode

Serial data communication is synchronized in character units. The SCI can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other chip that employs standard asynchronous serial communication. It can also communicate with two or more other processors using the multiprocessor communication function. There are twelve selectable serial data communication formats.

    - Data length: seven or eight bits
    - Stop bit length: one or two bits
    - Parity: even, odd, or none
    - Multiprocessor bit: one or none
    - Receive error detection: parity, overrun, and framing errors
    - Break detection: by reading the RxD level directly when a framing error occurs
  - Synchronous mode

Serial data communication is synchronized with a clock signal. The SCI can communicate with other chips having a synchronous communication function. There is one serial data communication format.

    - Data length: eight bits
    - Receive error detection: overrun errors
    - Serial clock inverted input/output
- Full duplex communication: The transmitting and receiving sections are independent, so the SCI can transmit and receive simultaneously. Both sections use double buffering, so continuous data transfer is possible in both the transmit and receive directions.
- On-chip baud rate generator with selectable bit rates

- Internal or external transmit/receive clock source: baud rate generator (internal) or SCK pin (external)
- Four types of interrupts: Transmit-data-empty, transmit-end, receive-data-full, and receive-error interrupts are requested independently. The transmit-data-empty and receive-data-full interrupts can start the direct memory access controller (DMAC) to transfer data.
- Selection of LSB-first or MSB-first transfer (8-bit length)  
This selection is available regardless of the communication mode. (The descriptions in this section are based on LSB-first transfer.)

### 14.1.2 Block Diagram

Figure 14.1 shows a block diagram of the SCI.

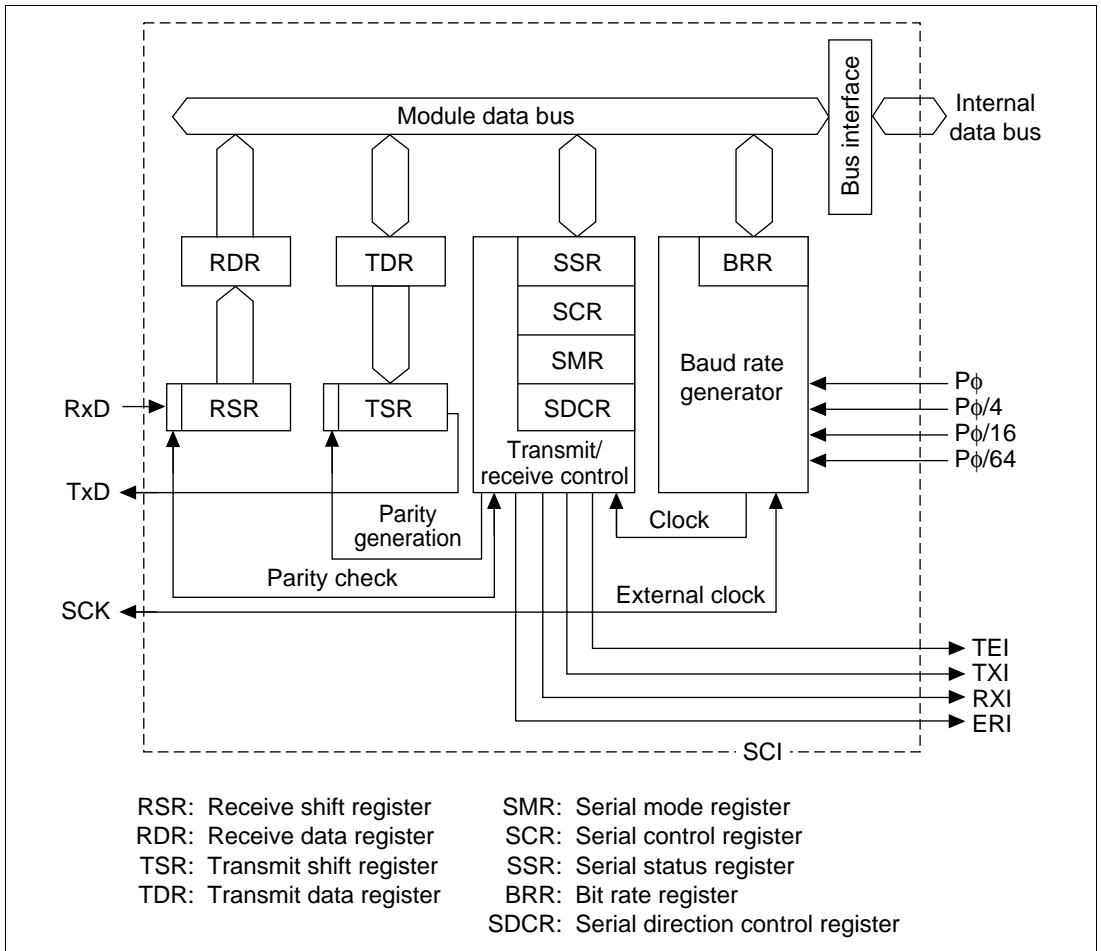


Figure 14.1 SCI Block Diagram

### 14.1.3 Pin Configuration

Table 14.1 summarizes the SCI pins by channel.

**Table 14.1 SCI Pins**

<b>Channel</b>	<b>Pin Name</b>	<b>Abbreviation</b>	<b>Input/Output</b>	<b>Function</b>
0	Serial clock pin	SCK0	Input/output	SCI0 clock input/output
	Receive data pin	RxD0	Input	SCI0 receive data input
	Transmit data pin	TxD0	Output	SCI0 transmit data output
1	Serial clock pin	SCK1	Input/output	SCI1 clock input/output
	Receive data pin	RxD1	Input	SCI1 receive data input
	Transmit data pin	TxD1	Output	SCI1 transmit data output
2	Serial clock pin	SCK2	Input/output	SCI2 clock input/output
	Receive data pin	RxD2	Input	SCI2 receive data input
	Transmit data pin	TxD2	Output	SCI2 transmit data output
3	Serial clock pin	SCK3	Input/output	SCI3 clock input/output
	Receive data pin	RxD3	Input	SCI3 receive data input
	Transmit data pin	TxD3	Output	SCI3 transmit data output
4	Serial clock pin	SCK4	Input/output	SCI4 clock input/output
	Receive data pin	RxD4	Input	SCI4 receive data input
	Transmit data pin	TxD4	Output	SCI4 transmit data output

Note: In the text the pins are referred to as SCK, RxD, and TxD, omitting the channel number.

## 14.1.4 Register Configuration

Table 14.2 summarizes the SCI internal registers. These registers select the communication mode (asynchronous or synchronous), specify the data format and bit rate, and control the transmitter and receiver sections.

**Table 14.2 Registers**

Channel	Name	Abbreviation	R/W	Initial Value	Address*2	Access Size
0	Serial mode register 0	SMR0	R/W	H'00	H'FFFFFF000	8, 16
	Bit rate register 0	BRR0	R/W	H'FF	H'FFFFFF001	
	Serial control register 0	SCR0	R/W	H'00	H'FFFFFF002	
	Transmit data register 0	TDR0	R/W	H'FF	H'FFFFFF003	
	Serial status register 0	SSR0	R/(W)*1	H'84	H'FFFFFF004	
	Receive data register 0	RDR0	R	H'00	H'FFFFFF005	
	Serial direction control register 0	SDCR0	R/W	H'F2	H'FFFFFF006	8
1	Serial mode register 1	SMR1	R/W	H'00	H'FFFFFF008	8, 16
	Bit rate register 1	BRR1	R/W	H'FF	H'FFFFFF009	
	Serial control register 1	SCR1	R/W	H'00	H'FFFFFF00A	
	Transmit data register 1	TDR1	R/W	H'FF	H'FFFFFF00B	
	Serial status register 1	SSR1	R/(W)*1	H'84	H'FFFFFF00C	
	Receive data register 1	RDR1	R	H'00	H'FFFFFF00D	
	Serial direction control register 1	SDCR1	R/W	H'F2	H'FFFFFF00E	8
2	Serial mode register 2	SMR2	R/W	H'00	H'FFFFFF010	8, 16
	Bit rate register 2	BRR2	R/W	H'FF	H'FFFFFF011	
	Serial control register 2	SCR2	R/W	H'00	H'FFFFFF012	
	Transmit data register 2	TDR2	R/W	H'FF	H'FFFFFF013	
	Serial status register 2	SSR2	R/(W)*1	H'84	H'FFFFFF014	
	Receive data register 2	RDR2	R	H'00	H'FFFFFF015	
	Serial direction control register 2	SDCR2	R/W	H'F2	H'FFFFFF016	8

**Table 14.2 Registers (cont)**

Channel	Name	Abbreviation	R/W	Initial Value	Address* <sup>2</sup>	Access Size
3	Serial mode register 3	SMR3	R/W	H'00	H'FFFFFF018	8, 16
	Bit rate register 3	BRR3	R/W	H'FF	H'FFFFFF019	
	Serial control register 3	SCR3	R/W	H'00	H'FFFFFF01A	
	Transmit data register 3	TDR3	R/W	H'FF	H'FFFFFF01B	
	Serial status register 3	SSR3	R/(W)* <sup>1</sup>	H'84	H'FFFFFF01C	
	Receive data register 3	RDR3	R	H'00	H'FFFFFF01D	
	Serial direction control register 3	SDCR3	R/W	H'F2	H'FFFFFF01E	8
4	Serial mode register 4	SMR4	R/W	H'00	H'FFFFFF020	8, 16
	Bit rate register 4	BRR4	R/W	H'FF	H'FFFFFF021	
	Serial control register 4	SCR4	R/W	H'00	H'FFFFFF022	
	Transmit data register 4	TDR4	R/W	H'FF	H'FFFFFF023	
	Serial status register 4	SSR4	R/(W)* <sup>1</sup>	H'84	H'FFFFFF024	
	Receive data register 4	RDR4	R	H'00	H'FFFFFF025	
	Serial direction control register 4	SDCR4	R/W	H'F2	H'FFFFFF026	8

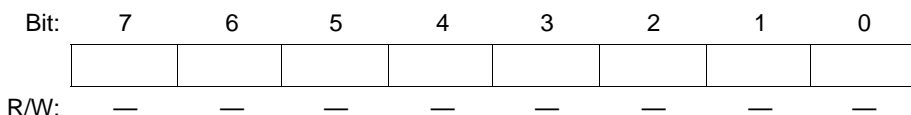
- Notes: 1. The only value that can be written is a 0 to clear the flags.  
 2. Do not access empty addresses.  
 3. In register access, four or five cycles are required for byte access, and eight or nine cycles for word access.

## 14.2 Register Descriptions

### 14.2.1 Receive Shift Register (RSR)

The receive shift register (RSR) receives serial data. Data input at the RxD pin is loaded into RSR in the order received, LSB (bit 0) first, converting the data to parallel form. When one byte has been received, it is automatically transferred to RDR.

The CPU cannot read or write to RSR directly.



### 14.2.2 Receive Data Register (RDR)

The receive data register (RDR) stores serial receive data. The SCI completes the reception of one byte of serial data by moving the received data from the receive shift register (RSR) into RDR for storage. RSR is then ready to receive the next data. This double buffering allows the SCI to receive data continuously.

The CPU can read but not write to RDR. RDR is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode. It is not initialized by a manual reset.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

### 14.2.3 Transmit Shift Register (TSR)

The transmit shift register (TSR) transmits serial data. The SCI loads transmit data from the transmit data register (TDR) into TSR, then transmits the data serially from the TxD pin, LSB (bit 0) first. After transmitting one data byte, the SCI automatically loads the next transmit data from TDR into TSR and starts transmitting again. If the TDRE bit of SSR is 1, however, the SCI does not load the TDR contents into TSR.

The CPU cannot read or write to TSR directly.

Bit:	7	6	5	4	3	2	1	0
R/W:	—	—	—	—	—	—	—	—

## 14.2.4 Transmit Data Register (TDR)

The transmit data register (TDR) is an 8-bit register that stores data for serial transmission. When the SCI detects that the transmit shift register (TSR) is empty, it moves transmit data written in TDR into TSR and starts serial transmission. Continuous serial transmission is possible by writing the next transmit data in TDR during serial transmission from TSR.

The CPU can always read and write to TDR. TDR is initialized to H'FF by a power-on reset, and in hardware standby mode and software standby mode. It is not initialized by a manual reset.

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## 14.2.5 Serial Mode Register (SMR)

The serial mode register (SMR) is an 8-bit register that specifies the SCI serial communication format and selects the clock source for the baud rate generator.

The CPU can always read and write to SMR. SMR is initialized to H'00 by a power-on reset and in hardware standby mode. It is not initialized by a manual reset, and in software standby mode.

Bit:	7	6	5	4	3	2	1	0
	$C/\bar{A}$	CHR	PE	$O/\bar{E}$	STOP	MP	CKS1	CKS0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 7—Communication Mode ( $C/\bar{A}$ ): Selects whether the SCI operates in asynchronous or synchronous mode.

Bit 7: $C/\bar{A}$	Description
0	Asynchronous mode (Initial value)
1	Synchronous mode

- Bit 6—Character Length (CHR): Selects 7-bit or 8-bit data in asynchronous mode. In synchronous mode, the data length is always eight bits, regardless of the CHR setting.

Bit 6: CHR	Description
0	Eight-bit data (Initial value)
1	Seven-bit data When 7-bit data is selected, the MSB (bit 7) of the transmit data register is not transmitted. LSB-first/MSB-first selection is not available.

- Bit 5—Parity Enable (PE): Selects whether to add a parity bit to transmit data and to check the parity of receive data, in asynchronous mode. In synchronous mode and when using a multiprocessor format, a parity bit is neither added nor checked, regardless of the PE bit setting.

Bit 5: PE	Description
0	Parity bit not added or checked (Initial value)
1	Parity bit added and checked When PE is set to 1, an even or odd parity bit is added to transmit data, depending on the parity mode ( $O/\bar{E}$ bit) setting. Receive data parity is checked according to the even/odd ( $O/\bar{E}$ bit) setting.

- Bit 4—Parity Mode ( $O/\bar{E}$ ): Selects even or odd parity when parity bits are added and checked. The  $O/\bar{E}$  setting is used only in asynchronous mode and only when the parity enable bit (PE) is set to 1 to enable parity addition and checking. The  $O/\bar{E}$  setting is invalid in synchronous mode, in asynchronous mode when parity bit addition and checking is disabled, and when using a multiprocessor format.

Bit 4: $O/\bar{E}$	Description
0	Even parity (Initial value) If even parity is selected, the parity bit is added to transmit data to make an even number of 1s in the transmitted character and parity bit combined. Receive data is checked to see if it has an even number of 1s in the received character and parity bit combined.
1	Odd parity If odd parity is selected, the parity bit is added to transmit data to make an odd number of 1s in the transmitted character and parity bit combined. Receive data is checked to see if it has an odd number of 1s in the received character and parity bit combined.



- **Bit 3—Stop Bit Length (STOP):** Selects one or two bits as the stop bit length in asynchronous mode. This setting is used only in asynchronous mode. It is ignored in synchronous mode because no stop bits are added.

In receiving, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit, but if the second stop bit is 0, it is treated as the start bit of the next incoming character.

Bit 3: STOP	Description
0	One stop bit (Initial value) In transmitting, a single bit of 1 is added at the end of each transmitted character.
1	Two stop bits In transmitting, two 1-bits are added at the end of each transmitted character.

- **Bit 2—Multiprocessor Mode (MP):** Selects multiprocessor format. When multiprocessor format is selected, settings of the parity enable (PE) and parity mode (O/ $\bar{E}$ ) bits are ignored. The MP bit setting is used only in asynchronous mode; it is ignored in synchronous mode. For the multiprocessor communication function, see section 14.3.3, Multiprocessor Communication.

Bit 2: MP	Description
0	Multiprocessor function disabled (Initial value)
1	Multiprocessor format selected

- **Bits 1 and 0—Clock Select 1 and 0 (CKS1, CKS0):** These bits select the internal clock source of the on-chip baud rate generator. Four clock sources are available:  $P\phi$ ,  $P\phi/4$ ,  $P\phi/16$ , or  $P\phi/64$  ( $P\phi$  is the peripheral clock). For further information on the clock source, bit rate register settings, and baud rate, see section 14.2.8, Bit Rate Register.

Bit 1: CKS1	Bit 0: CKS0	Description
0	0	$P\phi$ (Initial value)
	1	$P\phi/4$
1	0	$P\phi/16$
	1	$P\phi/64$

## 14.2.6 Serial Control Register (SCR)

The serial control register (SCR) operates the SCI transmitter/receiver, selects the serial clock output in asynchronous mode, enables/disables interrupt requests, and selects the transmit/receive clock source. The CPU can always read and write to SCR. SCR is initialized to H'00 by a power-on reset, and in hardware standby mode. It is not initialized by a manual reset, and in software standby mode.

Bit:	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 7—Transmit Interrupt Enable (TIE): Enables or disables the transmit-data-empty interrupt (TXI) requested when the transmit data register empty bit (TDRE) in the serial status register (SSR) is set to 1 by transfer of serial transmit data from TDR to TSR.

### Bit 7: TIE

### Description

0	Transmit-data-empty interrupt request (TXI) is disabled (Initial value) The TXI interrupt request can be cleared by reading TDRE after it has been set to 1, then clearing TDRE to 0, or by clearing TIE to 0.
1	Transmit-data-empty interrupt request (TXI) is enabled

- Bit 6—Receive Interrupt Enable (RIE): Enables or disables the receive-data-full interrupt (RXI) requested when the receive data register full bit (RDRF) in the serial status register (SSR) is set to 1 by transfer of serial receive data from RSR to RDR. It also enables or disables receive-error interrupt (ERI) requests.

### Bit 6: RIE

### Description

0	Receive-data-full interrupt (RXI) and receive-error interrupt (ERI) requests are disabled (Initial value) RXI and ERI interrupt requests can be cleared by reading the RDRF flag or error flag (FER, PER, or ORER) after it has been set to 1, then clearing the flag to 0, or by clearing RIE to 0.
1	Receive-data-full interrupt (RXI) and receive-error interrupt (ERI) requests are enabled

- Bit 5—Transmit Enable (TE): Enables or disables the SCI serial transmitter.

<b>Bit 5: TE</b>	<b>Description</b>
0	Transmitter disabled (Initial value) The transmit data register empty bit (TDRE) in the serial status register (SSR) is locked at 1.
1	Transmitter enabled Serial transmission starts when the transmit data register empty (TDRE) bit in the serial status register (SSR) is cleared to 0 after writing of transmit data into TDR. Select the transmit format in SMR before setting TE to 1.

- Bit 4—Receive Enable (RE): Enables or disables the SCI serial receiver.

<b>Bit 4: RE</b>	<b>Description</b>
0	Receiver disabled (Initial value) Clearing RE to 0 does not affect the receive flags (RDRF, FER, PER, ORER). These flags retain their previous values.
1	Receiver enabled Serial reception starts when a start bit is detected in asynchronous mode, or synchronous clock input is detected in synchronous mode. Select the receive format in SMR before setting RE to 1.

- Bit 3—Multiprocessor Interrupt Enable (MPIE): Enables or disables multiprocessor interrupts. The MPIE setting is used only in asynchronous mode, and only if the multiprocessor mode bit (MP) in the serial mode register (SMR) is set to 1 during reception. The MPIE setting is ignored in synchronous mode or when the MP bit is cleared to 0.

Bit 3: MPIE	Description
0	Multiprocessor interrupts are disabled (normal receive operation) (Initial value)  [Clearing conditions] <ul style="list-style-type: none"> <li>• When the MPIE bit is cleared to 0</li> <li>• When data with MPB = 1 is received</li> </ul>
1	Multiprocessor interrupts are enabled. Receive-data-full interrupt requests (RXI), receive-error interrupt requests (ERI), and setting of the RDRF, FER, and ORER status flags in the serial status register (SSR) are disabled until data with the multiprocessor bit set to 1 is received.  The SCI does not transfer receive data from RSR to RDR, does not detect receive errors, and does not set the RDRF, FER, and ORER flags in the serial status register (SSR). When it receives data that includes MPB = 1, MPB is set to 1, and the SCI automatically clears MPIE to 0, generates RXI and ERI interrupts (if the TIE and RIE bits in SCR are set to 1), and allows the FER and ORER bits to be set.

- Bit 2—Transmit-End Interrupt Enable (TEIE): Enables or disables the transmit-end interrupt (TEI) requested if TDR does not contain valid transmit data when the MSB is transmitted.

Bit 2: TEIE	Description
0	Transmit-end interrupt (TEI) requests are disabled* (Initial value)
1	Transmit-end interrupt (TEI) requests are enabled*

Note: \* The TEI request can be cleared by reading the TDRE bit in the serial status register (SSR) after it has been set to 1, then clearing TDRE to 0 and clearing the transmit end (TEND) bit to 0; or by clearing the TEIE bit to 0.

- Bits 1 and 0—Clock Enable 1 and 0 (CKE1, CKE0): These bits select the SCI clock source and enable or disable clock output from the SCK pin. Depending on the combination of CKE1 and CKE0, the SCK pin can be used for serial clock output, or serial clock input. Select the SCK pin function by using the pin function controller (PFC).

The CKE0 setting is valid only in asynchronous mode, and only when the SCI is internally clocked (CKE1 = 0). The CKE0 setting is ignored in synchronous mode, or when an external clock source is selected (CKE1 = 1). For further details on selection of the SCI clock source, see table 14.9 in section 14.3, Operation.

**Bit 1: Bit 0:**

**CKE1 CKE0 Description\*<sup>1</sup>**

CKE1	CKE0	Description* <sup>1</sup>	
0	0	Asynchronous mode	Internal clock, SCK pin used for input pin (input signal is ignored) or output pin (output level is undefined)* <sup>2</sup>
		Synchronous mode	Internal clock, SCK pin used for synchronous clock output <sup>2</sup>
0	1	Asynchronous mode	Internal clock, SCK pin used for clock output* <sup>3</sup>
		Synchronous mode	Internal clock, SCK pin used for synchronous clock output
1	0	Asynchronous mode	External clock, SCK pin used for clock input* <sup>4</sup>
		Synchronous mode	External clock, SCK pin used for synchronous clock input
1	1	Asynchronous mode	External clock, SCK pin used for clock input* <sup>4</sup>
		Synchronous mode	External clock, SCK pin used for synchronous clock input

- Notes: 1. The SCK pin is multiplexed with other functions. Use the pin function controller (PFC) to select the SCK function for this pin, as well as the I/O direction.
2. Initial value.
3. The output clock frequency is the same as the bit rate.
4. The input clock frequency is 16 times the bit rate.

## 14.2.7 Serial Status Register (SSR)

The serial status register (SSR) is an 8-bit register containing multiprocessor bit values, and status flags that indicate the SCI operating status.

The CPU can always read and write to SSR, but cannot write 1 in the status flags (TDRE, RDRF, ORER, PER, and FER). These flags can be cleared to 0 only if they have first been read (after being set to 1). Bits 2 (TEND) and 1 (MPB) are read-only bits that cannot be written. SSR is initialized to H'84 by a power-on reset, and in hardware standby mode and software standby mode. It is not initialized by a manual reset.

Bit:	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value:	1	0	0	0	0	1	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: \* The only value that can be written is a 0 to clear the flag.

- Bit 7—Transmit Data Register Empty (TDRE): Indicates that the SCI has loaded transmit data from TDR into TSR and new serial transmit data can be written in TDR.

Bit 7: TDRE	Description
0	TDR contains valid transmit data [Clearing conditions] <ul style="list-style-type: none"> <li>• When 0 is written to TDRE after reading TDRE = 1</li> <li>• When the DMAC writes data in TDR</li> </ul>
1	TDR does not contain valid transmit data (Initial value) [Setting conditions] <ul style="list-style-type: none"> <li>• Power-on reset, hardware standby mode, or software standby mode</li> <li>• When the TE bit in SCR is 0</li> <li>• When data is transferred from TDR to TSR, enabling new data to be written in TDR</li> </ul>

- Bit 6—Receive Data Register Full (RDRF): Indicates that RDR contains received data.

Bit 6: RDRF	Description
0	RDR does not contain valid receive data (Initial value) [Clearing conditions] <ul style="list-style-type: none"> <li>• Power-on reset, hardware standby mode, or software standby mode</li> <li>• When 0 is written to RDRF after reading RDRF = 1</li> <li>• When the DMAC reads data from RDR</li> </ul>
1	RDR contains valid received data [Setting condition] RDRF is set to 1 when serial data is received normally and transferred from RSR to RDR

Note: RDR and RDRF are not affected by detection of receive errors or by clearing of the RE bit to 0 in the serial control register. They retain their previous contents. If RDRF is still set to 1 when reception of the next data ends, an overrun error (ORER) occurs and the receive data is lost.

- Bit 5—Overrun Error (ORER): Indicates that data reception ended abnormally due to an overrun error.

Bit 5: ORER	Description
0	Receiving is in progress or has ended normally (Initial value) Clearing the RE bit to 0 in the serial control register does not affect the ORER bit, which retains its previous value. [Clearing conditions] <ul style="list-style-type: none"> <li>• Power-on reset, hardware standby mode, or software standby mode</li> <li>• When 0 is written to ORER after reading ORER = 1</li> </ul>
1	A receive overrun error occurred RDR continues to hold the data received before the overrun error, so subsequent receive data is lost. Serial receiving cannot continue while ORER is set to 1. In synchronous mode, serial transmitting is disabled. [Setting condition] ORER is set to 1 if reception of the next serial data ends when RDRF is set to 1

- Bit 4—Framing Error (FER): Indicates that data reception ended abnormally due to a framing error in asynchronous mode.

Bit 4: FER	Description
0	<p>Receiving is in progress or has ended normally (Initial value)</p> <p>Clearing the RE bit to 0 in the serial control register does not affect the FER bit, which retains its previous value.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Power-on reset, hardware standby mode, or software standby mode</li> <li>• When 0 is written to FER after reading FER = 1</li> </ul>
1	<p>A receive framing error occurred</p> <p>When the stop bit length is two bits, only the first bit is checked to see if it is a 1. The second stop bit is not checked. When a framing error occurs, the SCI transfers the receive data into RDR but does not set RDRF. Serial receiving cannot continue while FER is set to 1. In synchronous mode, serial transmitting is also disabled.</p> <p>[Setting condition]</p> <p>FER is set to 1 if the stop bit at the end of receive data is checked and found to be 0</p>

- Bit 3—Parity Error (PER): Indicates that data reception (with parity) ended abnormally due to a parity error in asynchronous mode.

Bit 3: PER	Description
0	<p>Receiving is in progress or has ended normally (Initial value)</p> <p>Clearing the RE bit to 0 in the serial control register does not affect the PER bit, which retains its previous value.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Power-on reset, hardware standby mode, or software standby mode</li> <li>• When 0 is written to PER after reading PER = 1</li> </ul>
1	<p>A receive parity error occurred</p> <p>When a parity error occurs, the SCI transfers the receive data into RDR but does not set RDRF. Serial receiving cannot continue while PER is set to 1.</p> <p>[Setting condition]</p> <p>PER is set to 1 if the number of 1s in receive data, including the parity bit, does not match the even or odd parity setting of the parity mode bit (O/E) in the serial mode register (SMR)</p>



- **Bit 2—Transmit End (TEND):** Indicates that when the last bit of a serial character was transmitted, TDR did not contain valid data, so transmission has ended. TEND is a read-only bit and cannot be written.

<b>Bit 2: TEND</b>	<b>Description</b>
0	Transmission is in progress [Clearing conditions] <ul style="list-style-type: none"> <li>• When 0 is written to TDRE after reading TDRE = 1</li> <li>• When the DMAC writes data in TDR</li> </ul>
1	End of transmission (Initial value) [Setting conditions] <ul style="list-style-type: none"> <li>• Power-on reset, hardware standby mode, or software standby mode</li> <li>• When the TE bit in SCR is 0</li> <li>• If TDRE = 1 when the last bit of a one-byte serial transmit character is transmitted</li> </ul>

- **Bit 1—Multiprocessor Bit (MPB):** Stores the value of the multiprocessor bit in receive data when a multiprocessor format is selected for receiving in asynchronous mode. MPB is a read-only bit and cannot be written.

<b>Bit 1: MPB</b>	<b>Description</b>
0	Multiprocessor bit value in receive data is 0 (Initial value) If RE is cleared to 0 when a multiprocessor format is selected, the MPB retains its previous value.
1	Multiprocessor bit value in receive data is 1

- **Bit 0—Multiprocessor Bit Transfer (MPBT):** Stores the value of the multiprocessor bit added to transmit data when a multiprocessor format is selected for transmitting in asynchronous mode. The MPBT setting is ignored in synchronous mode, when a multiprocessor format is not selected, or when the SCI is not transmitting.

<b>Bit 0: MPBT</b>	<b>Description</b>
0	Multiprocessor bit value in transmit data is 0 (Initial value)
1	Multiprocessor bit value in transmit data is 1

## 14.2.8 Bit Rate Register (BRR)

The bit rate register (BRR) is an 8-bit register that, together with the baud rate generator clock source selected by the CKS1 and CKS0 bits in the serial mode register (SMR), determines the serial transmit/receive bit rate.

The CPU can always read and write to BRR. BRR is initialized to H'FF by a power-on reset and in hardware standby mode. It is not initialized by a manual reset, and in software standby mode. Each channel has independent baud rate generator control, so different values can be set for each channel.

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 14.3 lists examples of BRR settings in the asynchronous mode; table 14.4 lists examples of BRR settings in the clock synchronous mode.

The BRR setting is calculated as follows:

Asynchronous mode:

$$N = \frac{P\phi}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

Synchronous mode:

$$N = \frac{P\phi}{8 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B: Bit rate (bits/s)

N: Baud rate generator BRR setting ( $0 \leq N \leq 255$ )

$P\phi$ : Peripheral module operating frequency (MHz) (1/2 of system clock)

n: Baud rate generator input clock ( $n = 0$  to 3)

(See the following table for the clock sources and value of n.)

n	Clock Source	SMR Settings	
		CKS1	CKS2
0	$P\phi$	0	0
1	$P\phi/4$	0	1
2	$P\phi/16$	1	0
3	$P\phi/64$	1	1

The bit rate error in asynchronous mode is calculated as follows:

$$\text{Error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

**Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode**

Bit Rate (Bits/s)	P $\phi$ (MHz)								
	10			11.0592			12		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	177	-0.25	2	195	0.19	2	212	0.03
150	2	129	0.16	2	143	0.00	2	155	0.16
300	2	64	0.16	2	71	0.00	2	77	0.16
600	1	129	0.16	1	143	0.00	1	155	0.16
1200	1	64	0.16	1	71	0.00	1	77	0.16
2400	0	129	0.16	0	143	0.00	0	155	0.16
4800	0	64	0.16	0	71	0.00	0	77	0.16
9600	0	32	-1.36	0	35	0.00	0	28	0.16
14400	0	21	-1.36	0	23	0.00	0	25	0.16
19200	0	15	1.73	0	19	0.00	0	19	-2.34
28800	0	10	-1.36	0	11	0.00	0	12	0.16
31250	0	9	0.00	0	10	0.54	0	11	0.00
38400	0	7	1.73	0	8	0.00	0	9	-2.34

**Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)**

Bit Rate (Bits/s)	P $\phi$ (MHz)								
	12.288			14			14.7456		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	217	0.08	2	248	-0.17	3	64	0.70
150	2	159	0.00	2	181	0.16	2	191	0.00
300	2	79	0.00	2	90	0.16	2	95	0.00
600	1	159	0.00	1	181	0.16	1	191	0.00
1200	1	79	0.00	1	90	0.16	1	95	0.00
2400	0	159	0.00	0	181	0.16	0	191	0.00
4800	0	79	0.00	0	90	0.16	0	95	0.00
9600	0	39	0.00	0	45	-0.93	0	47	0.00
14400	0	26	-1.23	0	29	1.27	0	31	0.00
19200	0	19	0.00	0	22	-0.93	0	23	0.00
28800	0	12	2.56	0	14	1.27	0	15	0.00
31250	0	11	2.40	0	13	0.00	0	14	-1.70
38400	0	9	0.00	0	10	3.57	0	11	0.00

**Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)**

Bit Rate (Bits/s)	P $\phi$ (MHz)								
	16			17.2032			18		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	70	0.03	3	75	0.48	3	79	-0.12
150	2	207	0.16	2	223	0.00	2	233	0.16
300	2	103	0.16	2	111	0.00	2	116	0.16
600	1	207	0.16	1	223	0.00	1	233	0.16
1200	1	103	0.16	1	111	0.00	1	116	0.16
2400	0	207	0.16	0	223	0.00	0	233	0.16
4800	0	103	0.16	0	111	0.00	0	116	0.16
9600	0	51	0.16	0	55	0.00	0	58	-0.69
14400	0	34	-0.79	0	36	0.90	0	38	0.16
19200	0	25	0.16	0	27	0.00	0	28	1.02
28800	0	16	2.12	0	18	-1.75	0	19	-2.34
31250	0	15	0.00	0	16	1.20	0	17	0.00
38400	0	12	0.16	0	13	0.00	0	14	-2.34

**Table 14.3 Bit Rates and BRR Settings in Asynchronous Mode (cont)**

Bit Rate (Bits/s)	$\phi$ (MHz)								
	18.432			19.6608			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	81	-0.22	3	86	0.31	3	88	-0.25
150	2	239	0.00	2	255	0.00	3	64	0.16
300	2	119	0.00	2	127	0.00	2	129	0.16
600	1	239	0.00	1	255	0.00	2	64	0.16
1200	1	119	0.00	1	127	0.00	1	129	0.16
2400	0	239	0.00	0	255	0.00	1	64	0.16
4800	0	119	0.00	0	127	0.00	0	129	0.16
9600	0	59	0.00	0	63	0.00	0	64	0.16
14400	0	39	0.00	0	42	-0.78	0	42	0.94
19200	0	29	0.00	0	31	0.00	0	32	-1.36
28800	0	19	0.00	0	20	1.59	0	21	-1.36
31250	0	17	2.40	0	19	-1.70	0	19	0.00
38400	0	14	0.00	0	15	0.00	0	15	1.73

**Table 14.4 Bit Rates and BRR Settings in Synchronous Mode**

Bit Rate (Bits/s)	P $\phi$ (MHz)							
	10		12		16		20	
	n	N	n	N	n	N	n	N
250	—	—	3	187	3	249		
500	—	—	3	93	3	124	—	—
1 k	—	—	2	187	2	249	—	—
2.5 k	1	249	2	74	2	99	2	124
5 k	1	124	1	149	1	199	2	249
10 k	0	249	1	74	1	99	1	124
25 k	0	99	0	119	0	159	1	199
50 k	0	49	0	59	0	79	0	99
100 k	0	24	0	29	0	39	0	49
250 k	0	9	0	11	0	15	0	19
500 k	0	4	0	5	0	7	0	9
1 M			0	2	0	3	0	4
2.5 M	0	0*	0	0*	—	—	0	1
5 M							0	0*

Note: Settings with an error of 1% or less are recommended.

Legend

Blank: No setting available

—: Setting possible, but error occurs

\*: Continuous transmission/reception not possible

Table 14.5 indicates the maximum bit rates in asynchronous mode when the baud rate generator is being used for various frequencies. Tables 14.6 and 14.7 show the maximum rates for external clock input.

**Table 14.5 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (Asynchronous Mode)**

P $\phi$ (MHz)	Maximum Bit Rate (Bits/s)	Settings	
		n	N
10	312500	0	0
11.0592	345600	0	0
12	375000	0	0
12.288	384000	0	0
14	437500	0	0
14.7456	460800	0	0
16	500000	0	0
17.2032	537600	0	0
18	562500	0	0
18.432	576000	0	0
19.6608	614400	0	0
20	625000	0	0

**Table 14.6 Maximum Bit Rates during External Clock Input (Asynchronous Mode)**

P $\phi$ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (Bits/s)
10	2.5000	156250
11.0592	2.7648	172800
12	3.0000	187500
12.288	3.0720	192000
14	3.5000	218750
14.7456	3.6864	230400
16	4.0000	250000
17.2032	4.3008	268800
18	4.5000	281250
18.432	4.6080	288000
19.6608	4.9152	307200
20	5.0000	312500



**Table 14.7 Maximum Bit Rates during External Clock Input (Clock Synchronous Mode)**

<b>P<math>\phi</math> (MHz)</b>	<b>External Input Clock (MHz)</b>	<b>Maximum Bit Rate (Bits/s)</b>
10	1.6667	1666666.7
12	2.0000	2000000.0
14	2.3333	2333333.3
16	2.6667	2666666.7
18	3.0000	3000000.0
20	3.3333	3333333.3

**14.2.9 Serial Direction Control Register (SDCR)**

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	DIR	—	—	—
Initial value:	1	1	1	1	0	0	1	0
R/W:	R	R	R	R	R/W	R	R	R

The DIR bit in the serial direction control register (SDCR) selects LSB-first or MSB-first transfer. With an 8-bit data length, LSB-first/MSB-first selection is available regardless of the communication mode. With a 7-bit data length, LSB-first transfer must be selected. The description in this section assumes LSB-first transfer.

SDCR is initialized to H'F2 by a power-on reset and in the hardware standby mode. It is not initialized by a manual reset, and in software standby mode.

- Bits 7 to 4—Reserved: The write value must always be 1. Operation cannot be guaranteed if 0 is written.
- Bit 3—Data Transfer Direction (DIR): Selects the serial/parallel conversion format. Valid for an 8-bit transmit/receive format.

<b>Bit 3: DIR</b>	<b>Description</b>
0	TDR contents are transmitted in LSB-first order (Initial value) Receive data is stored in RDR in LSB-first order
1	TDR contents are transmitted in MSB-first order Receive data is stored in RDR in MSB-first order

- Bit 2—Reserved: This bit always reads 0. Operation cannot be guaranteed if 1 is written.
- Bit 1—Reserved: This bit always reads 1, and cannot be modified.

- Bit 0—Reserved: This bit always reads 0. Operation cannot be guaranteed if 1 is written.

### 14.2.10 Inversion of SCK Pin Signal

The signal input from the SCK pin and the signal output from the SCK pin can be inverted by means of a port control register setting. See the section on port function control for details.

## 14.3 Operation

### 14.3.1 Overview

For serial communication, the SCI has an asynchronous mode in which characters are synchronized individually, and a synchronous mode in which communication is synchronized with clock pulses. Selection of asynchronous or synchronous mode and the transmission format is made in the serial mode register (SMR) as shown in table 14.8. The SCI clock source is selected by the  $C/\bar{A}$  bit in the serial mode register (SMR) and the CKE1 and CKE0 bits in the serial control register (SCR), as shown in table 14.9.

#### Asynchronous Mode:

- Data length is selectable: seven or eight bits.
- Parity and multiprocessor bits are selectable, as well as the stop bit length (one or two bits). These selections determine the transmit/receive format and character length.
- In receiving, it is possible to detect framing errors (FER), parity errors (PER), overrun errors (ORER), and the break state.
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the on-chip baud rate generator clock, and can output a clock with a frequency matching the bit rate.
  - When an external clock is selected, the external clock input must have a frequency 16 times the bit rate. (The on-chip baud rate generator is not used.)

#### Synchronous Mode:

- The communication format has a fixed 8-bit data length.
- In receiving, it is possible to detect overrun errors (ORER).
- An internal or external clock can be selected as the SCI clock source.
  - When an internal clock is selected, the SCI operates using the on-chip baud rate generator clock, and outputs a serial clock signal to external devices.
  - When an external clock is selected, the SCI operates on the input serial clock. The on-chip baud rate generator is not used.

**Table 14.8 Serial Mode Register Settings and SCI Communication Formats**

Mode	SMR Settings					SCI Communication Format			
	Bit 7 C/A	Bit 6 CHR	Bit 5 PE	Bit 2 MP	Bit 3 STOP	Data Length	Parity Bit	Multipro- cessor Bit	Stop Bit Length
Asynchronous	0	0	0	0	0	8-bit	Absent	Absent	1 bit
					1				2 bits
			1	0	0	7-bit	Absent	1 bit	
					1				2 bits
	1	0	1	0	0	7-bit	Absent	Present	1 bit
					1				2 bits
		1	0	1	0	0	7-bit	Present	1 bit
						1			
Asynchronous (multiprocessor format)	0	*	1	0	8-bit	Absent	Present	1 bit	
				1				2 bits	
	1	*	1	0	7-bit	1 bit			
				1			2 bits		
Synchronous	1	*	*	*	8-bit		Absent	None	

Note: Asterisks (\*) in the table indicate don't care bits.

**Table 14.9 SMR and SCR Settings and SCI Clock Source Selection**

Mode	SMR	SCR Settings		SCI Transmit/Receive Clock		
	Bit 7 C/A	Bit 1 CKE1	Bit 0 CKE0	Clock Source	SCK Pin Function*	
Asynchronous	0	0	0	Internal	SCI does not use the SCK pin	
			1		Outputs a clock with frequency matching the bit rate	
			1	0	External	Inputs a clock with frequency 16 times the bit rate
Synchronous	1	0	0	Internal	Outputs the serial clock or the inverted serial clock	
			1			
			1	0	External	Inputs the serial clock or the inverted serial clock

Note: \* Select the function in combination with the pin function controller (PFC).

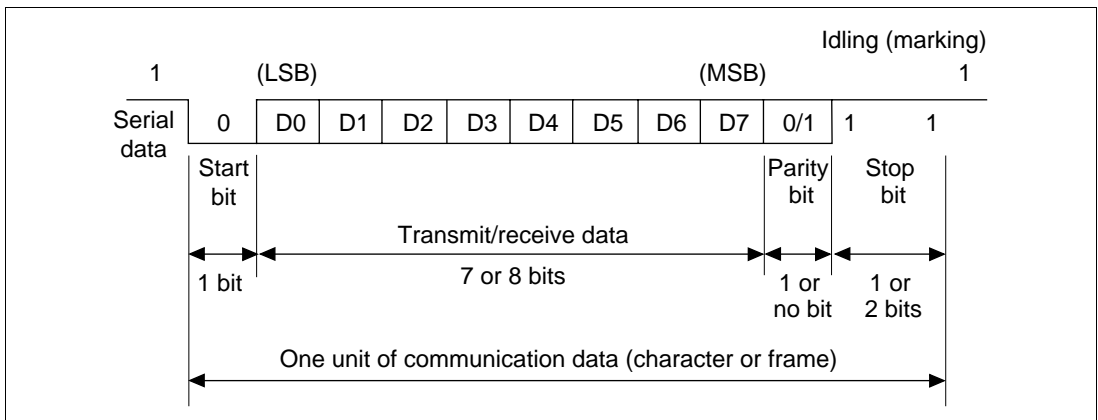
### 14.3.2 Operation in Asynchronous Mode

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCI are independent, so full duplex communication is possible. The transmitter and receiver are both double buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving.

Figure 14.2 shows the general format of asynchronous serial communication. In asynchronous serial communication, the communication line is normally held in the marking (high) state. The SCI monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCI synchronizes on the falling edge of the start bit. The SCI samples each data bit on the eighth pulse of a clock with a frequency 16 times the bit rate. Receive data is latched at the center of each bit.



**Figure 14.2 Data Format in Asynchronous Communication (Example: 8-bit Data with Parity and Two Stop Bits)**

**Transmit/Receive Formats:** Table 14.10 shows the 12 communication formats that can be selected in asynchronous mode. The format is selected by settings in the serial mode register (SMR).

**Table 14.10 Serial Communication Formats (Asynchronous Mode)**

SMR Bits				Serial Transmit/Receive Format and Frame Length												
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12	
0	0	0	0	START	8-bit data							STOP				
0	0	0	1	START	8-bit data							STOP	STOP			
0	1	0	0	START	8-bit data							P	STOP			
0	1	0	1	START	8-bit data							P	STOP	STOP		
1	0	0	0	START	7-bit data						STOP					
1	0	0	1	START	7-bit data						STOP	STOP				
1	1	0	0	START	7-bit data						P	STOP				
1	1	0	1	START	7-bit data						P	STOP	STOP			
0	—	1	0	START	8-bit data							MPB	STOP			
0	—	1	1	START	8-bit data							MPB	STOP	STOP		
1	—	1	0	START	7-bit data						MPB	STOP				
1	—	1	1	START	7-bit data						MPB	STOP	STOP			

—: Don't care bits.

START: Start bit

STOP: Stop bit

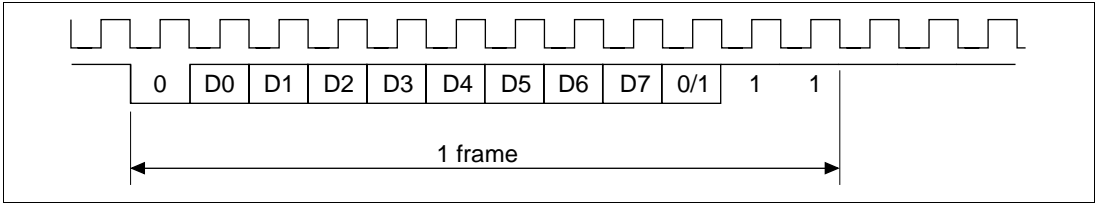
P: Parity bit

MPB: Multiprocessor bit

**Clock:** An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCI transmit/receive clock. The clock source is selected by the  $C/\bar{A}$  bit in the serial mode register (SMR) and bits CKE1 and CKE0 in the serial control register (SCR) (table 14.9).

When an external clock is input at the SCK pin, it must have a frequency equal to 16 times the desired bit rate.

When the SCI operates on an internal clock, it can output a clock signal at the SCK pin. The frequency of this output clock is equal to the bit rate. The phase is aligned as in figure 14.3 so that the rising edge of the clock occurs at the center of each transmit data bit.



**Figure 14.3 Output Clock and Communication Data Phase Relationship (Asynchronous Mode)**

### Data Transmit/Receive Operation

**SCI Initialization (Asynchronous Mode):** Before transmitting or receiving, clear the TE and RE bits to 0 in the serial control register (SCR), then initialize the SCI as follows.

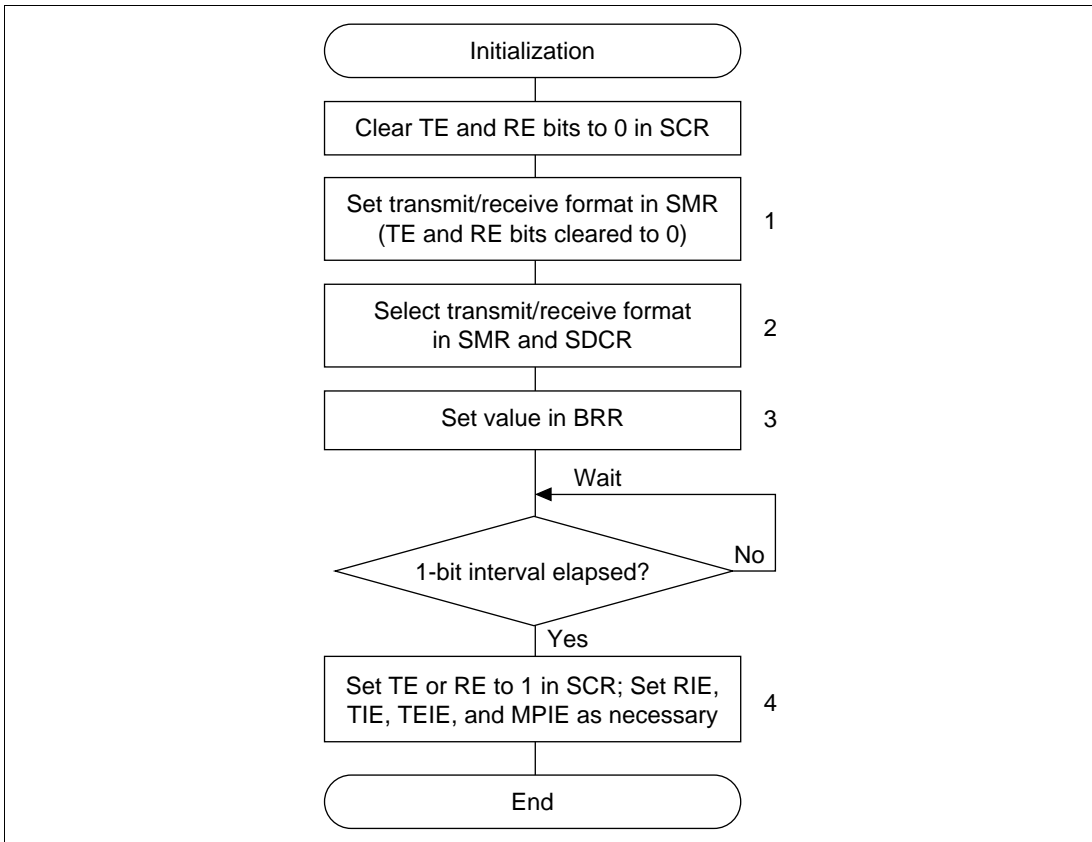
When changing the operation mode or communication format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets TDRE to 1 and initializes the transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags and receive data register (RDR), which retain their previous contents.

When an external clock is used, the clock should not be stopped during initialization or subsequent operation. SCI operation becomes unreliable if the clock is stopped.

Figure 14.4 is a sample flowchart for initializing the SCI. The procedure is as follows (the steps correspond to the numbers in the flowchart):

1. Select the clock source in the serial control register (SCR). Leave RIE, TIE, TEIE, MPIE, TE and RE cleared to 0. If clock output is selected in asynchronous mode, clock output starts immediately after the setting is made in SCR.
2. Select the communication format in the serial mode register (SMR) and serial direction control register (SDCR).
3. Write the value corresponding to the bit rate in the bit rate register (BRR) (unless an external clock is used).
4. Wait for at least the interval required to transmit or receive one bit, then set TE or RE in the serial control register (SCR) to 1.\* Also set RIE, TIE, TEIE and MPIE as necessary. Setting TE or RE enables the SCI to use the TxD or RxD pin.

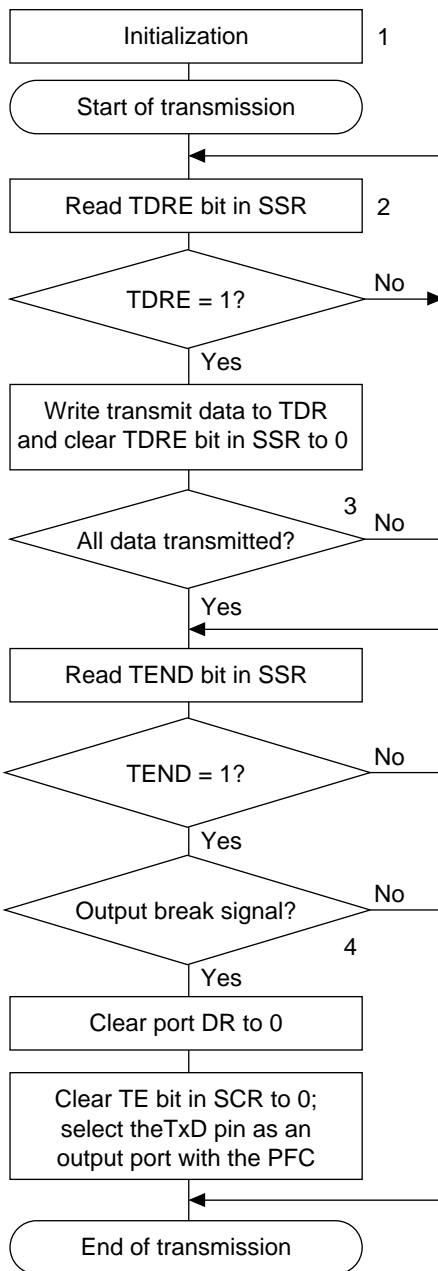
Note: \* In simultaneous transmit/receive operation, the TE bit and RE bit must be cleared to 0 or set to 1 simultaneously.



**Figure 14.4 Sample Flowchart for SCI Initialization**

**Transmitting Serial Data (Asynchronous Mode):** Figure 14.5 shows a sample flowchart for transmitting serial data. The procedure is as follows (the steps correspond to the numbers in the flowchart):

1. SCI initialization: Set the TxD pin using the PFC.
2. SCI status check and transmit data write: Read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0.
3. Continue transmitting serial data: Read the TDRE bit to check whether it is safe to write (if it reads 1); if so, write data in TDR, then clear TDRE to 0. When the DMAC is started by a transmit-data-empty interrupt request (TXI) in order to write data in TDR, the TDRE bit is checked and cleared automatically.
4. To output a break at the end of serial transmission, first clear the port data register (DR) to 0, then clear the TE bit to 0 in SCR and use the PFC to establish the TxD pin as an output port.



**Figure 14.5 Sample Flowchart for Transmitting Serial Data**



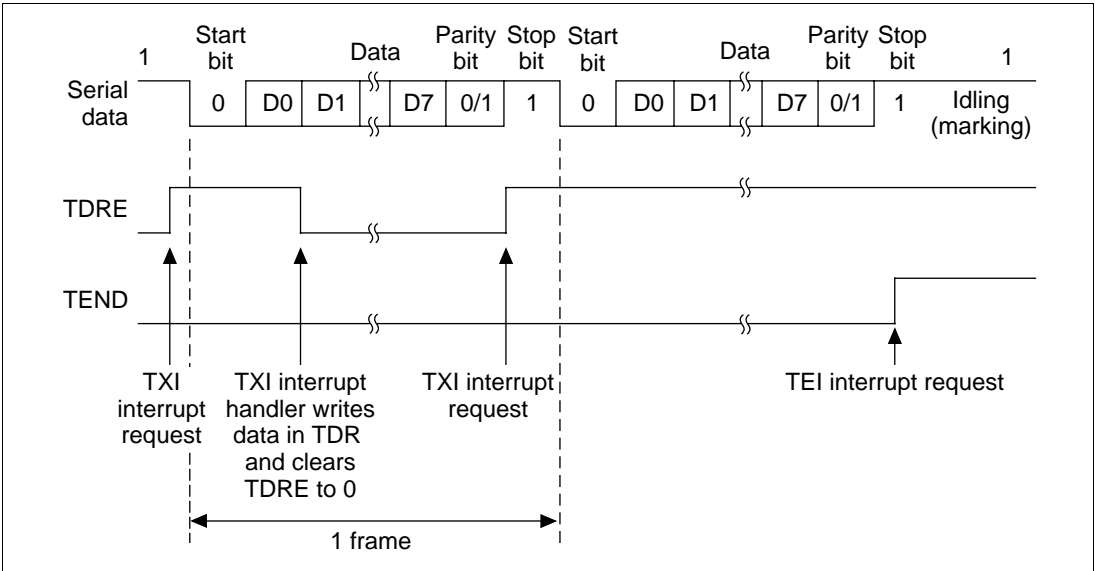
In transmitting serial data, the SCI operates as follows:

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0, the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).
2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) is set to 1 in SCR, the SCI requests a transmit-data-empty interrupt (TXI) at this time.

Serial transmit data is transmitted in the following order from the TxD pin:

- a. Start bit: one 0-bit is output.
  - b. Transmit data: seven or eight bits of data are output, LSB first.
  - c. Parity bit or multiprocessor bit: one parity bit (even or odd parity) or one multiprocessor bit is output. Formats in which neither a parity bit nor a multiprocessor bit is output can also be selected.
  - d. Stop bit: one or two 1-bits (stop bits) are output.
  - e. Marking: output of 1-bits continues until the start bit of the next transmit data.
3. The SCI checks the TDRE bit when it outputs the stop bit. If TDRE is 0, the SCI loads new data from TDR into TSR, outputs the stop bit, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit to 1 in SSR, outputs the stop bit, then continues output of 1-bits (marking). If the transmit-end interrupt enable bit (TEIE) in SCR is set to 1, a transmit-end interrupt (TEI) is requested.

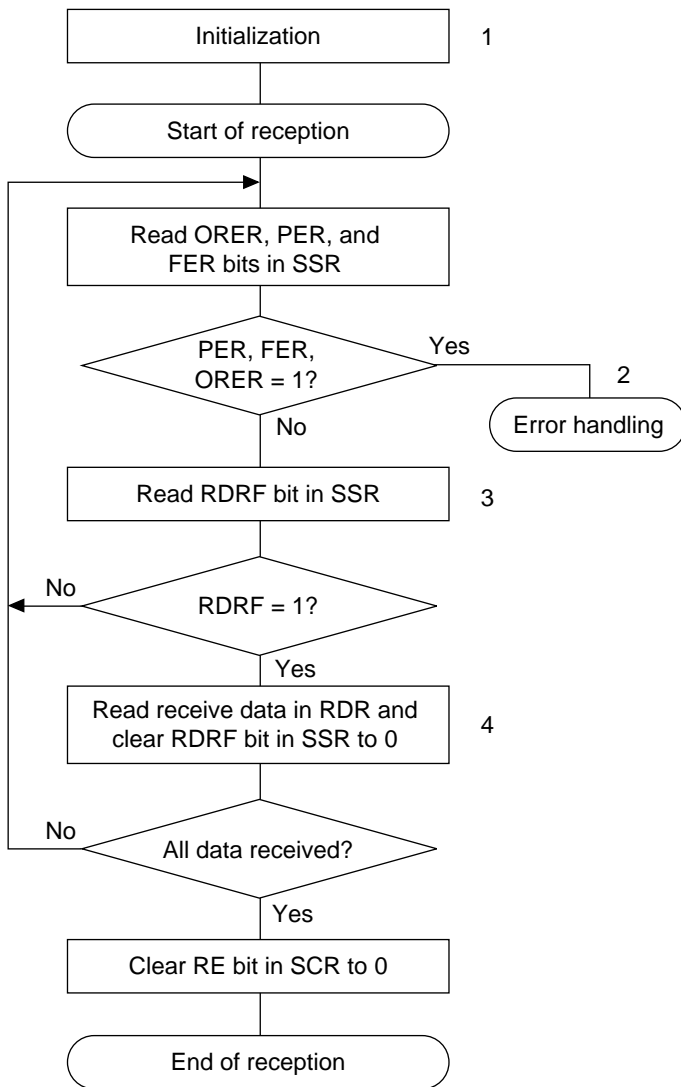
Figure 14.6 shows an example of SCI transmit operation in asynchronous mode.



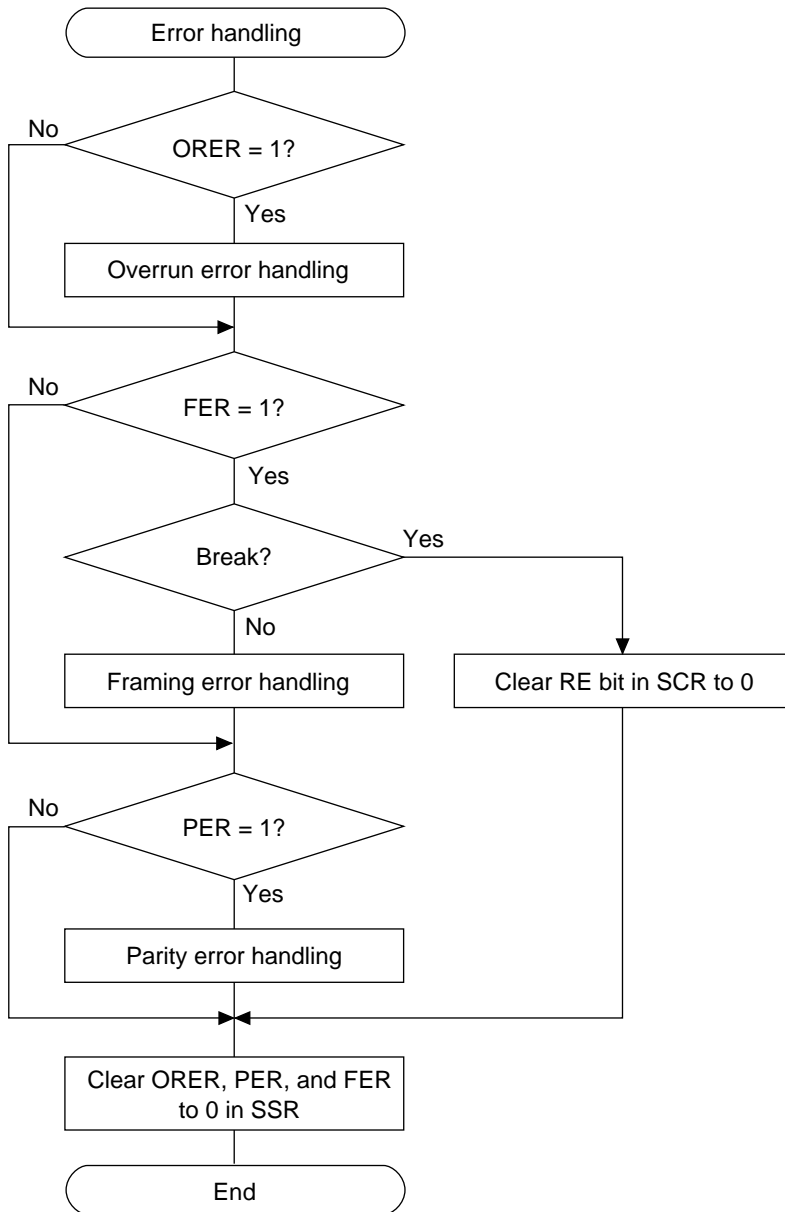
**Figure 14.6 SCI Transmit Operation in Asynchronous Mode  
(Example: 8-Bit Data with Parity and One Stop Bit)**

**Receiving Serial Data (Asynchronous Mode):** Figures 14.7 and 14.8 show a sample flowchart for receiving serial data. The procedure is as follows (the steps correspond to the numbers in the flowchart).

1. SCI initialization: Set the RxD pin using the PFC.
2. Receive error handling and break detection: If a receive error occurs, read the ORER, PER, and FER bits of SSR to identify the error. After executing the necessary error handling, clear ORER, PER, and FER all to 0. Receiving cannot resume if ORER, PER or FER remain set to 1. When a framing error occurs, the RxD pin can be read to detect the break state.
3. SCI status check and receive-data read: Read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. The RXI interrupt can also be used to determine if the RDRF bit has changed from 0 to 1.
4. Continue receiving serial data: Read RDR and the RDRF bit and clear RDRF to 0 before the stop bit of the current frame is received. If the DMAC is started by a receive-data-full interrupt (RXI) to read RDR, the RDRF bit is cleared automatically so this step is unnecessary.



**Figure 14.7 Sample Flowchart for Receiving Serial Data (1)**



**Figure 14.8 Sample Flowchart for Receiving Serial Data (2)**

In receiving, the SCI operates as follows:

1. The SCI monitors the communication line. When it detects a start bit (0), the SCI synchronizes internally and starts receiving.
2. Receive data is shifted into RSR in order from the LSB to the MSB.
3. The parity bit and stop bit are received. After receiving these bits, the SCI makes the following checks:
  - a. Parity check. The number of 1s in the receive data must match the even or odd parity setting of the O/E bit in SMR.
  - b. Stop bit check. The stop bit value must be 1. If there are two stop bits, only the first stop bit is checked.
  - c. Status check. RDRF must be 0 so that receive data can be loaded from RSR into RDR.

If the data passes these checks, the SCI sets RDRF to 1 and stores the receive data in RDR. If one of the checks fails (receive error), the SCI operates as indicated in table 14.11.

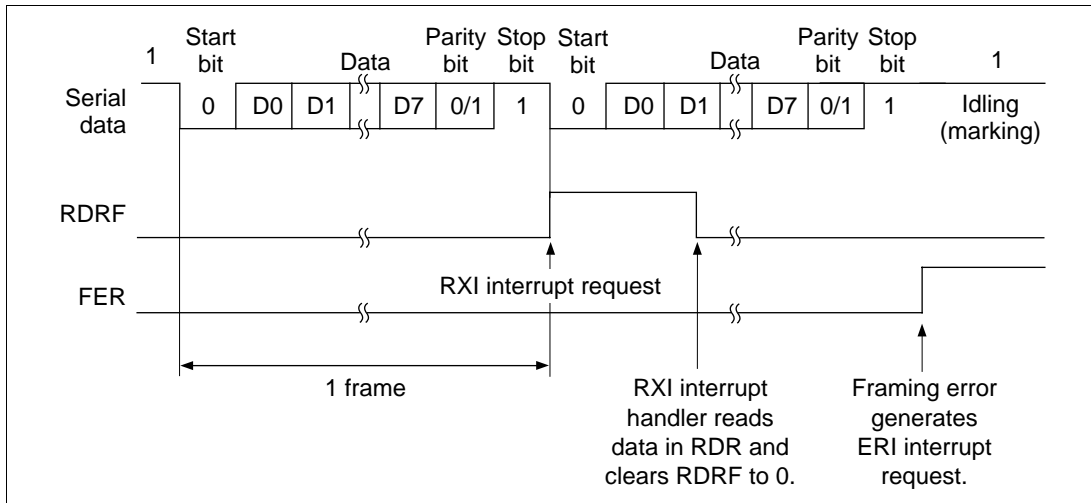
Note: When a receive error occurs, further receiving is disabled. While receiving, the RDRF bit is not set to 1, so be sure to clear the error flags.

4. After setting RDRF to 1, if the receive-data-full interrupt enable bit (RIE) is set to 1 in SCR, the SCI requests a receive-data-full interrupt (RXI). If one of the error flags (ORER, PER, or FER) is set to 1 and the receive-data-full interrupt enable bit (RIE) in SCR is also set to 1, the SCI requests a receive-error interrupt (ERI).

**Table 14.11 Receive Error Conditions and SCI Operation**

Receive Error	Abbreviation	Condition	Data Transfer
Overrun error	ORER	Receiving of next data ends while RDRF is still set to 1 in SSR	Receive data not loaded from RSR into RDR
Framing error	FER	Stop bit is 0	Receive data loaded from RSR into RDR
Parity error	PER	Parity of receive data differs from even/odd parity setting in SMR	Receive data loaded from RSR into RDR

Figure 14.9 shows an example of SCI receive operation in asynchronous mode.



**Figure 14.9 SCI Receive Operation**  
**(Example: 8-Bit Data with Parity and One Stop Bit)**

### 14.3.3 Multiprocessor Communication

The multiprocessor communication function enables several processors to share a single serial communication line for sending and receiving data. The processors communicate in the asynchronous mode using a format with an additional multiprocessor bit (multiprocessor format).

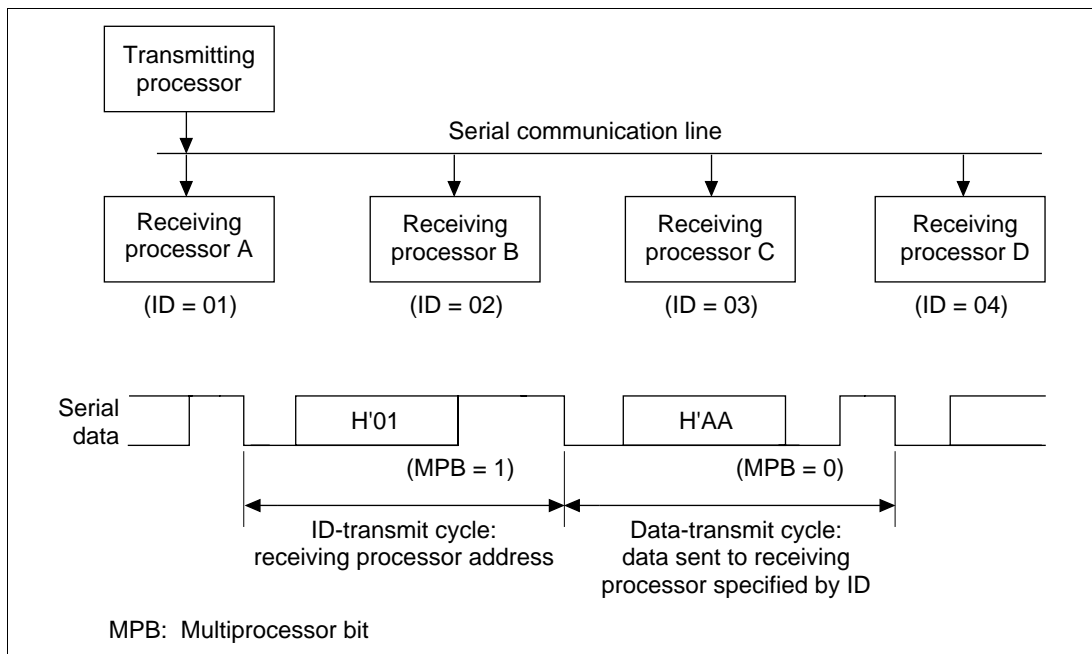
In multiprocessor communication, each receiving processor is addressed by a unique ID. A serial communication cycle consists of an ID-sending cycle that identifies the receiving processor, and a data-sending cycle. The multiprocessor bit distinguishes ID-sending cycles from data-sending cycles. The transmitting processor starts by sending the ID of the receiving processor with which it wants to communicate as data with the multiprocessor bit set to 1. Next the transmitting processor sends transmit data with the multiprocessor bit cleared to 0.

Receiving processors skip incoming data until they receive data with the multiprocessor bit set to 1. When they receive data with the multiprocessor bit set to 1, receiving processors compare the data with their IDs. The receiving processor with a matching ID continues to receive further incoming data. Processors with IDs not matching the received data skip further incoming data until they again receive data with the multiprocessor bit set to 1. Multiple processors can send and receive data in this way.

Figure 14.10 shows an example of communication among processors using the multiprocessor format.

**Communication Formats:** Four formats are available. Parity-bit settings are ignored when the multiprocessor format is selected. For details see table 14.8.

**Clock:** See the description in the asynchronous mode section.

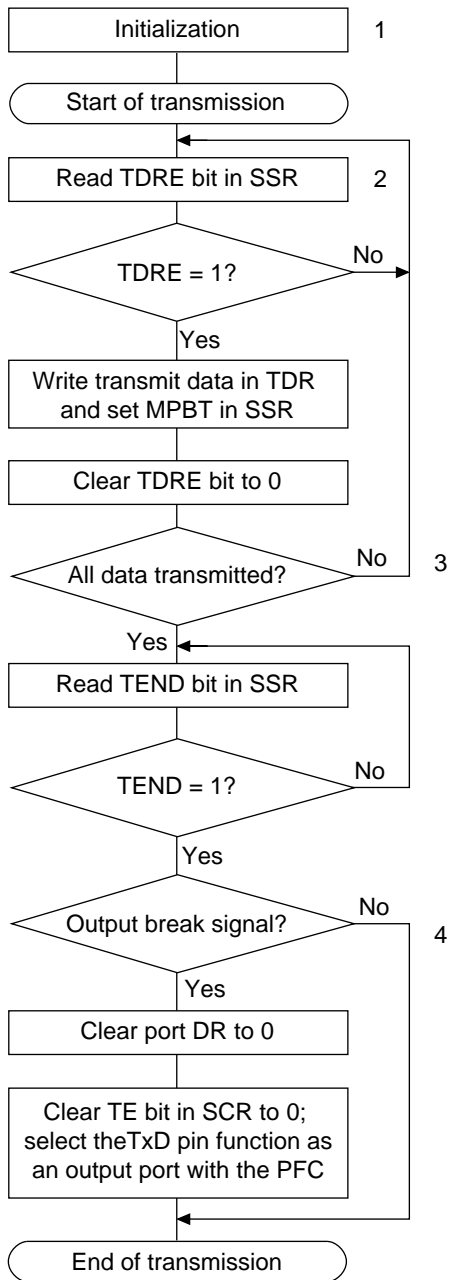


**Figure 14.10 Communication Among Processors Using Multiprocessor Format  
(Example: Sending Data H'AA to Receiving Processor A)**

### Data Transmit/Receive Operation

**Transmitting Multiprocessor Serial Data:** Figure 14.11 shows a sample flowchart for transmitting multiprocessor serial data. The procedure is as follows (the steps correspond to the numbers in the flowchart):

1. SCI initialization: Set the TxD pin using the PFC.
2. SCI status check and transmit data write: Read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR). Also set MPBT (multiprocessor bit transfer) to 0 or 1 in SSR. Finally, clear TDRE to 0.
3. Continue transmitting serial data: Read the TDRE bit to check whether it is safe to write (if it reads 1); if so, write data in TDR, then clear TDRE to 0. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically.
4. Output a break at the end of serial transmission: Set the data register (DR) of the port to 0, then clear TE to 0 in SCR and set the TxD pin function as output port with the PFC.



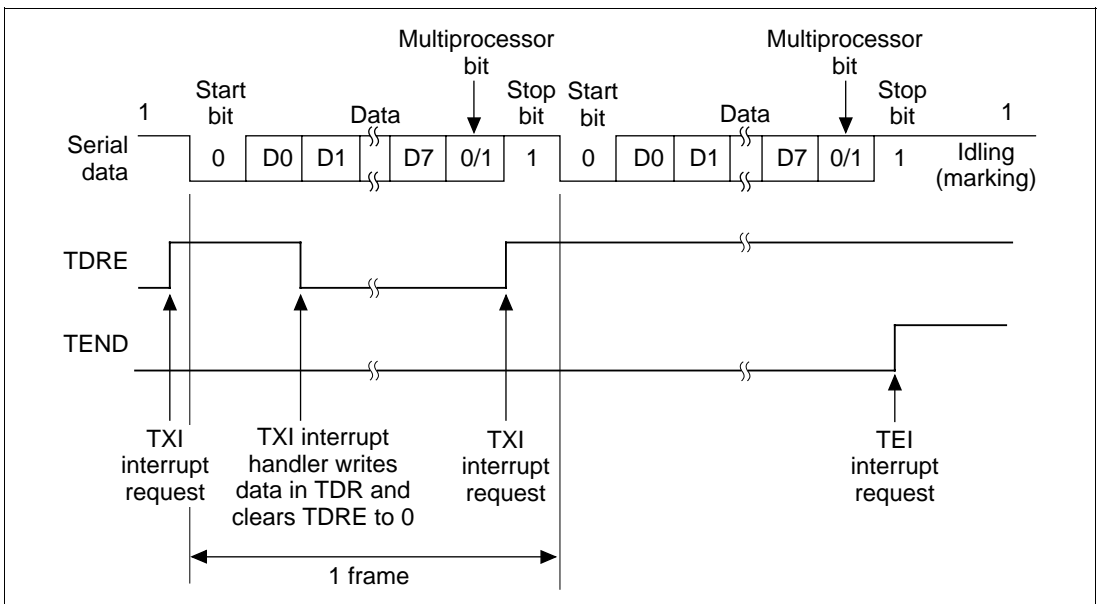
**Figure 14.11 Sample Flowchart for Transmitting Multiprocessor Serial Data**



In transmitting serial data, the SCI operates as follows:

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data, and loads this data from TDR into the transmit shift register (TSR).
2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) in SCR is set to 1, the SCI requests a transmit-data-empty interrupt (TXI) at this time.  
Serial transmit data is transmitted in the following order from the TxD pin:
  - a. Start bit: one 0-bit is output.
  - b. Transmit data: seven or eight bits are output, LSB first.
  - c. Multiprocessor bit: one multiprocessor bit (MPBT value) is output.
  - d. Stop bit: one or two 1-bits (stop bits) are output.
  - e. Marking: output of 1-bits continues until the start bit of the next transmit data.
3. The SCI checks the TDRE bit when it outputs the stop bit. If TDRE is 0, the SCI loads data from TDR into TSR, outputs the stop bit, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in SSR to 1, outputs the stop bit, then continues output of 1-bits in the marking state. If the transmit-end interrupt enable bit (TEIE) in SCR is set to 1, a transmit-end interrupt (TEI) is requested at this time.

Figure 14.12 shows an example of SCI receive operation in the multiprocessor format.



**Figure 14.12 SCI Multiprocessor Transmit Operation**  
(Example: 8-Bit Data with Multiprocessor Bit and One Stop Bit)

**Receiving Multiprocessor Serial Data:** Figures 14.13 and 14.14 show sample flowcharts for receiving multiprocessor serial data. The procedure for receiving multiprocessor serial data is as follows (the steps correspond to the numbers in the flowchart):

1. SCI initialization: Set the RxD pin using the PFC.
2. ID receive cycle: Set the MPIE bit in the serial control register (SCR) to 1.
3. SCI status check and compare to ID reception: Read the serial status register (SSR), check that RDRF is set to 1, then read data from the receive data register (RDR) and compare with the processor's own ID. If the ID does not match the receive data, set MPIE to 1 again and clear RDRF to 0. If the ID matches the receive data, clear RDRF to 0.
4. Receive error handling and break detection: If a receive error occurs, read the ORER and FER bits in SSR to identify the error. After executing the necessary error handling, clear both ORER and FER to 0. Receiving cannot resume if ORER or FER remain set to 1. When a framing error occurs, the RxD pin can be read to detect the break state.
5. SCI status check and data receiving: Read SSR, check that RDRF is set to 1, then read data from the receive data register (RDR).

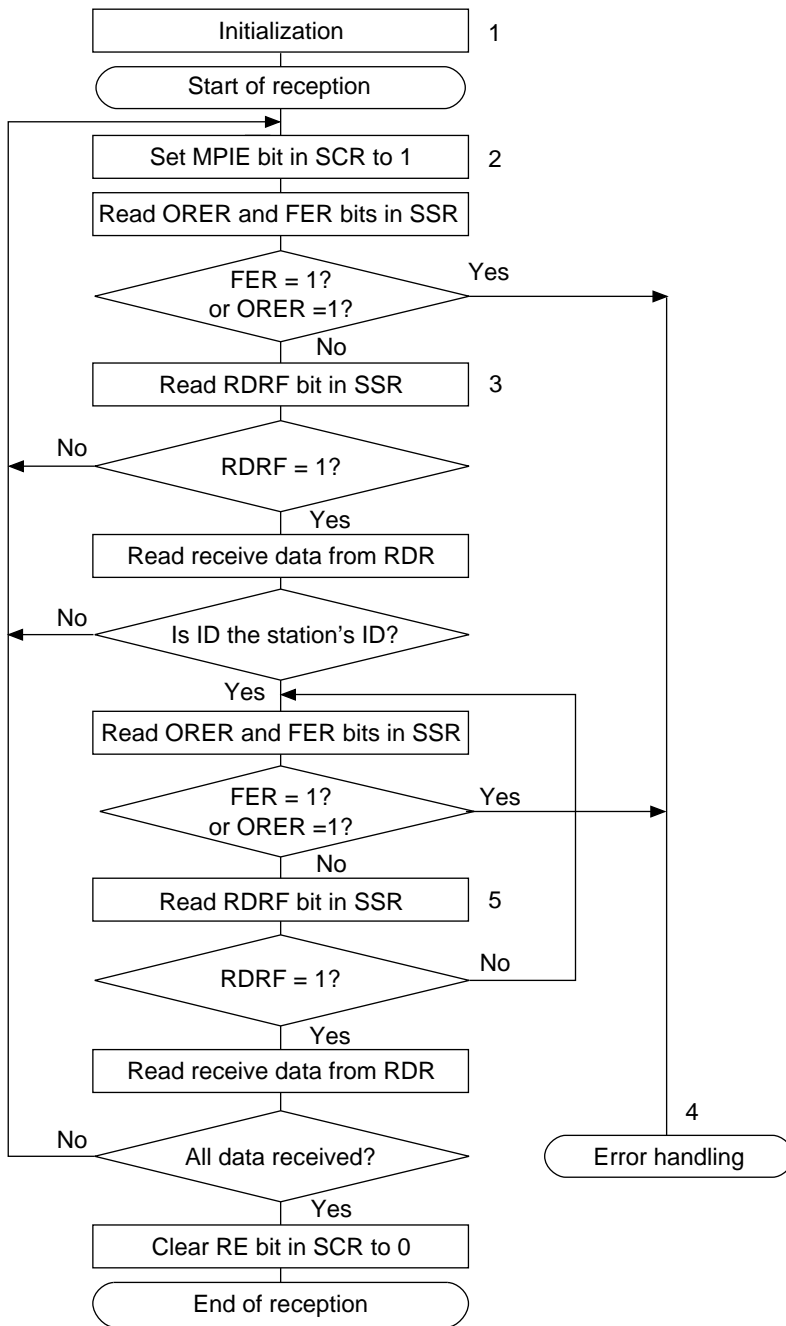
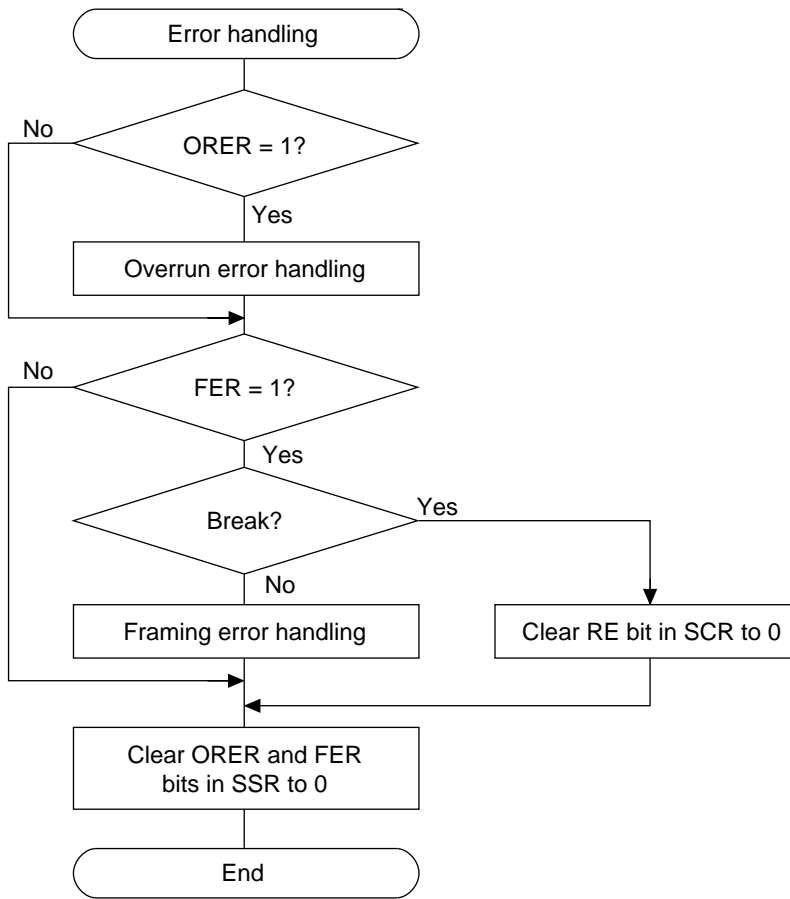
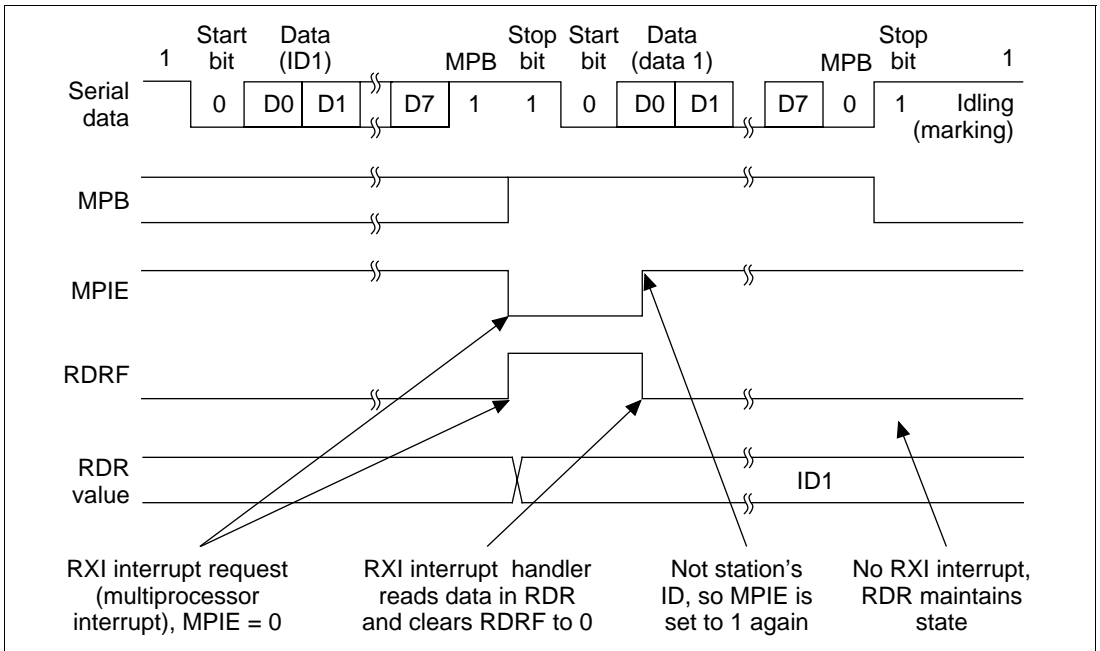


Figure 14.13 Sample Flowchart for Receiving Multiprocessor Serial Data (1)

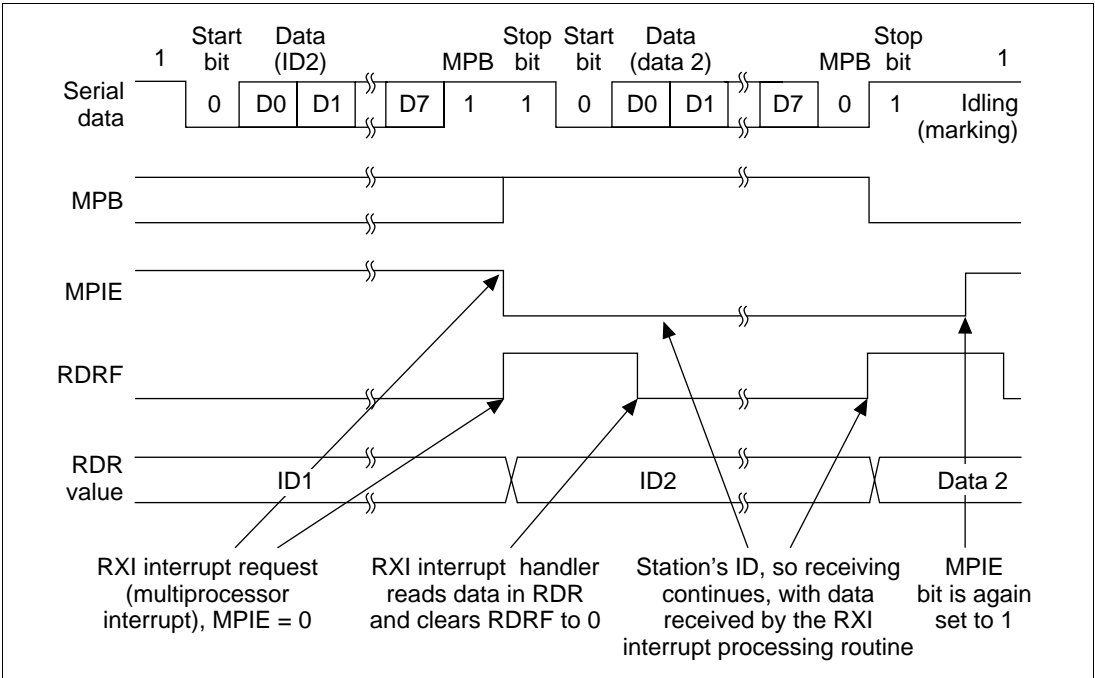


**Figure 14.14 Sample Flowchart for Receiving Multiprocessor Serial Data (2)**

Figures 14.15 and 14.16 show examples of SCI receive operation using a multiprocessor format.



**Figure 14.15 SCI Receive Operation (ID Does Not Match)**  
**(Example: 8-Bit Data with Multiprocessor Bit and One Stop Bit)**



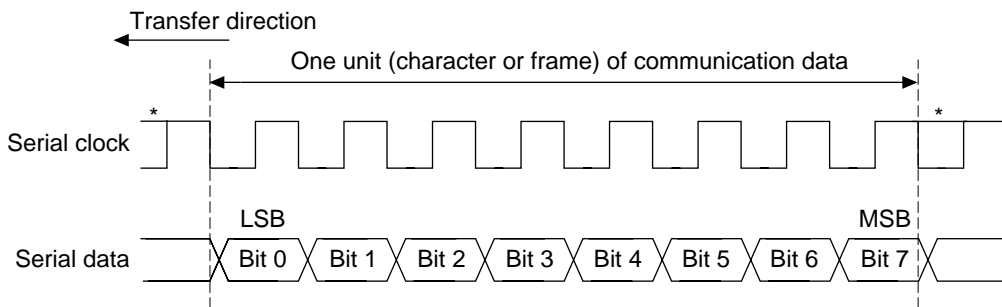
**Figure 14.16 Example of SCI Receive Operation (ID Matches)  
(Example: 8-Bit Data with Multiprocessor Bit and One Stop Bit)**

### 14.3.4 Synchronous Operation

In synchronous mode, the SCI transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communication.

The SCI transmitter and receiver are independent, so full duplex communication is possible while sharing the same clock. The transmitter and receiver are also double buffered, so continuous transmitting or receiving is possible by reading or writing data while transmitting or receiving is in progress.

Figure 14.17 shows the general format in synchronous serial communication.



Note: \* High except in continuous transmitting or receiving.

**Figure 14.17 Data Format in Synchronous Communication**

In synchronous serial communication, each data bit is output on the communication line from one falling edge of the serial clock to the next. Data is guaranteed valid at the rising edge of the serial clock. In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB. In synchronous mode, the SCI transmits or receives data by synchronizing with the rise of the serial clock.

**Communication Format:** The data length is fixed at eight bits. No parity bit or multiprocessor bit can be added.

**Clock:** An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCI transmit/receive clock. The clock source is selected by the  $C/\bar{A}$  bit in the serial mode register (SMR) and bits CKE1 and CKE0 in the serial control register (SCR). See table 14.9.

When the SCI operates on an internal clock, it outputs the clock signal at the SCK pin. Eight clock pulses are output per transmitted or received character. When the SCI is not transmitting or receiving, the clock signal remains in the high state. An overrun error occurs only during the receive operation, and the serial clock is output until the RE bit is cleared to 0. To perform a receive operation in one-character units, select an external clock for the clock source.

## Transmitting and Receiving Data

**SCI Initialization (Synchronous Mode):** Before transmitting or receiving, software must clear the TE and RE bits to 0 in the serial control register (SCR), then initialize the SCI as follows.

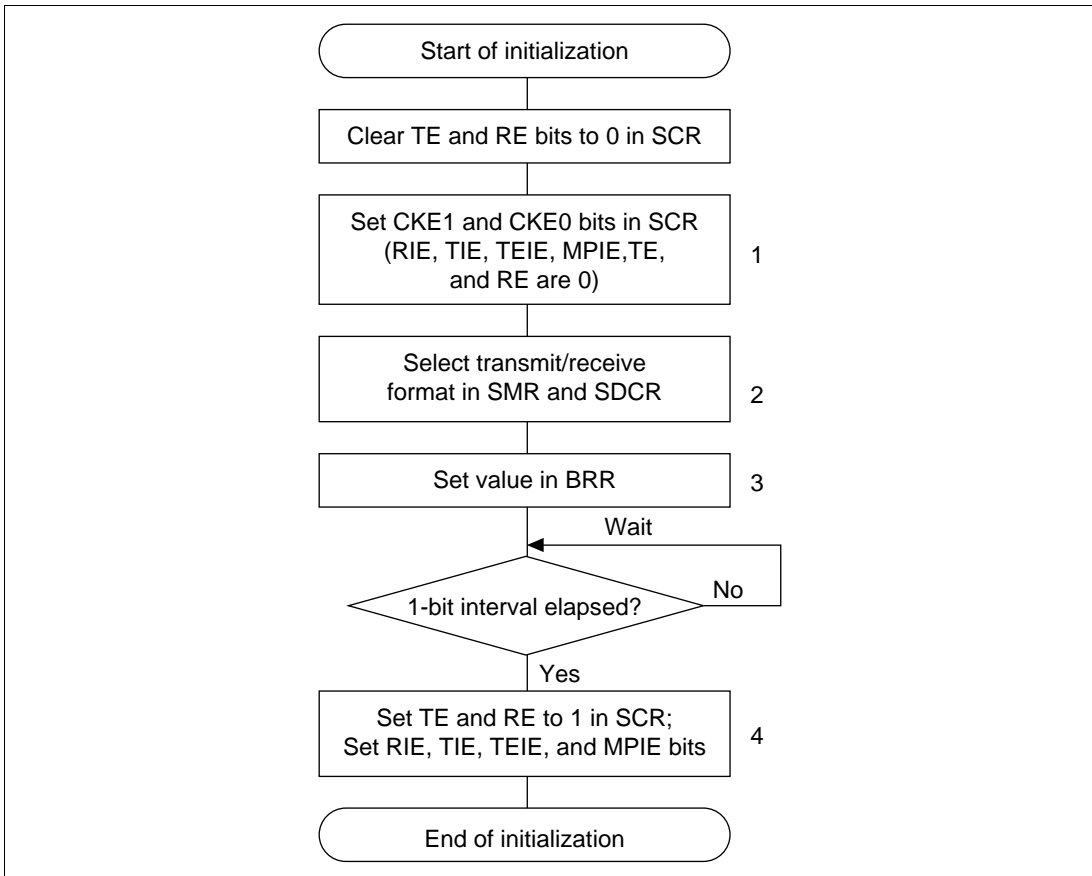
When changing the mode or communication format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets TDRE to 1 and initializes the transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags and receive data register (RDR), which retain their previous contents.

Figure 14.18 is a sample flowchart for initializing the SCI.

1. Select the clock source in the serial control register (SCR). Leave RIE, TIE, TEIE, MPIE, TE, and RE cleared to 0.
2. Select the communication format in the serial mode register (SMR) and serial direction control register (SDCR).
3. Write the value corresponding to the bit rate in the bit rate register (BRR) (unless an external clock is used).
4. Wait for at least the interval required to transmit or receive one bit, then set TE or RE in the serial control register (SCR) to 1.\* Also set RIE, TIE, TEIE, and MPIE. The TxD, RxD pins becomes usable in response to the PFC corresponding bits and the TE, RE bit settings.

Note: \* In simultaneous transmit/receive operation, the TE bit and RE bit must be cleared to 0 or set to 1 simultaneously.

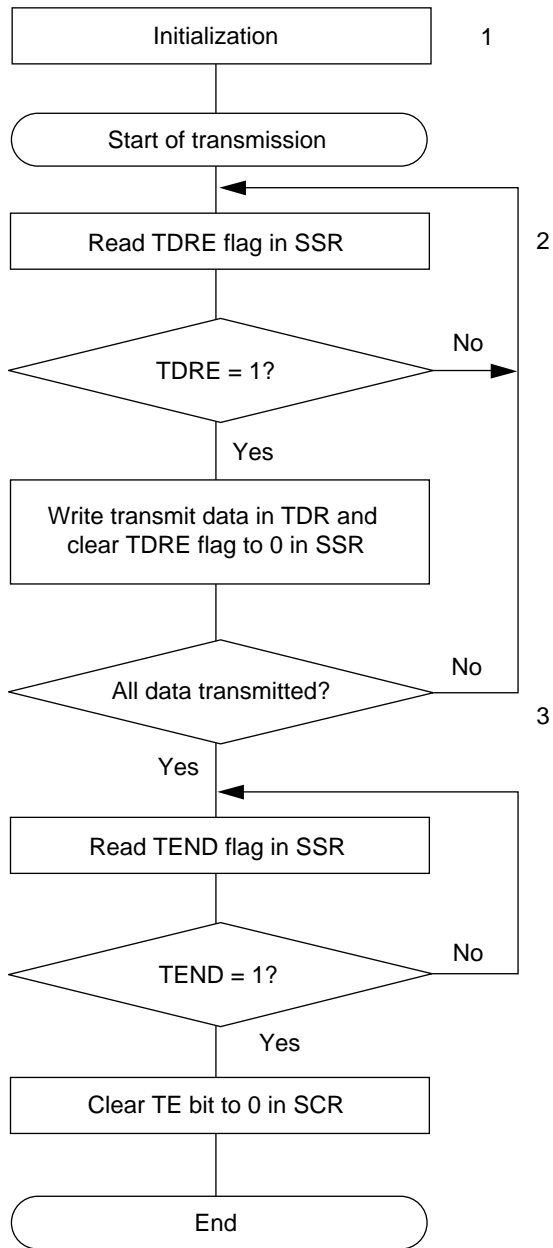




**Figure 14.18 Sample Flowchart for SCI Initialization**

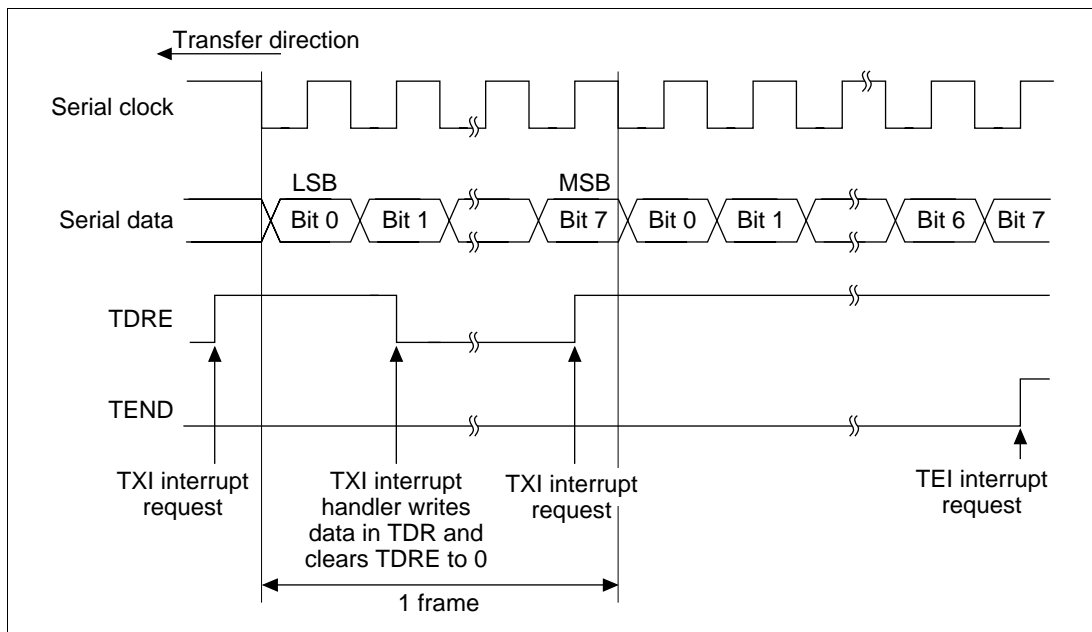
**Transmitting Serial Data (Synchronous Mode):** Figure 14.19 shows a sample flowchart for transmitting serial data. The procedure is as follows (the steps correspond to the numbers in the flowchart):

1. SCI initialization: Set the TxD pin function with the PFC.
2. SCI status check and transmit data write: Read SSR, check that the TDRE flag is 1, then write transmit data in TDR and clear the TDRE flag to 0.
3. To continue transmitting serial data: After checking that the TDRE flag is 1, indicating that data can be written, write data in TDR, then clear the TDRE flag to 0. When the DMAC is activated by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE flag is checked and cleared automatically.



**Figure 14.19 Sample Flowchart for Serial Transmitting**

Figure 14.20 shows an example of SCI transmit operation.



**Figure 14.20 Example of SCI Transmit Operation**

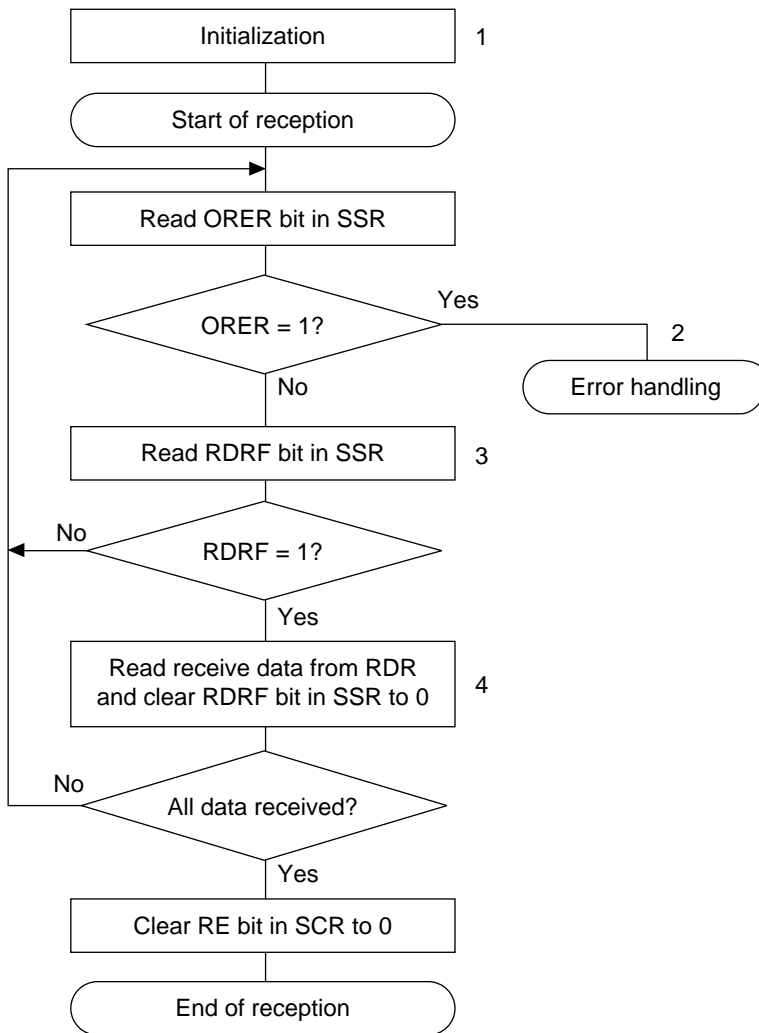
SCI serial transmission operates as follows.

1. The SCI monitors the TDRE bit in SSR. When TDRE is cleared to 0 the SCI recognizes that the transmit data register (TDR) contains new data and loads this data from TDR into the transmit shift register (TSR).
2. After loading the data from TDR into TSR, the SCI sets the TDRE bit to 1 and starts transmitting. If the transmit-data-empty interrupt enable bit (TIE) in SCR is set to 1, the SCI requests a transmit-data-empty interrupt (TXI) at this time.  
If clock output mode is selected, the SCI outputs eight serial clock pulses. If an external clock source is selected, the SCI outputs data in synchronization with the input clock. Data is output from the TxD pin in order from the LSB (bit 0) to the MSB (bit 7).
3. The SCI checks the TDRE bit when it outputs the MSB (bit 7). If TDRE is 0, the SCI loads data from TDR into TSR, then begins serial transmission of the next frame. If TDRE is 1, the SCI sets the TEND bit in SSR to 1, transmits the MSB, then holds the transmit data pin (TxD) in the MSB state. If the transmit-end interrupt enable bit (TEIE) in SCR is set to 1, a transmit-end interrupt (TEI) is requested at this time.
4. After the end of serial transmission, the SCK pin is held in the high state.

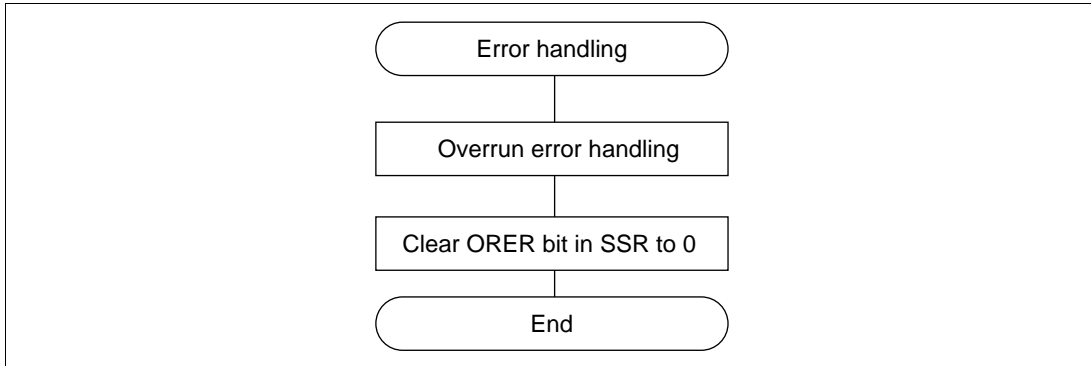
**Receiving Serial Data (Synchronous Mode):** Figures 14.21 and 14.22 show sample flowcharts for receiving serial data. When switching from asynchronous mode to synchronous mode, make sure that ORER, PER, and FER are cleared to 0. If PER or FER is set to 1, the RDRF bit will not be set and both transmitting and receiving will be disabled.

The procedure for receiving serial data is as follows (the steps correspond to the numbers in the flowchart):

1. SCI initialization: Set the RxD pin using the PFC.
2. Receive error handling: If a receive error occurs, read the ORER bit in SSR to identify the error. After executing the necessary error handling, clear ORER to 0. Transmitting/receiving cannot resume if ORER remains set to 1.
3. SCI status check and receive data read: Read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. The RXI interrupt can also be used to determine if the RDRF bit has changed from 0 to 1.
4. Continue receiving serial data: Read RDR, and clear RDRF to 0 before the MSB (bit 7) of the current frame is received. If the DMAC is started by a receive-data-full interrupt (RXI) to read RDR, the RDRF bit is cleared automatically so this step is unnecessary.

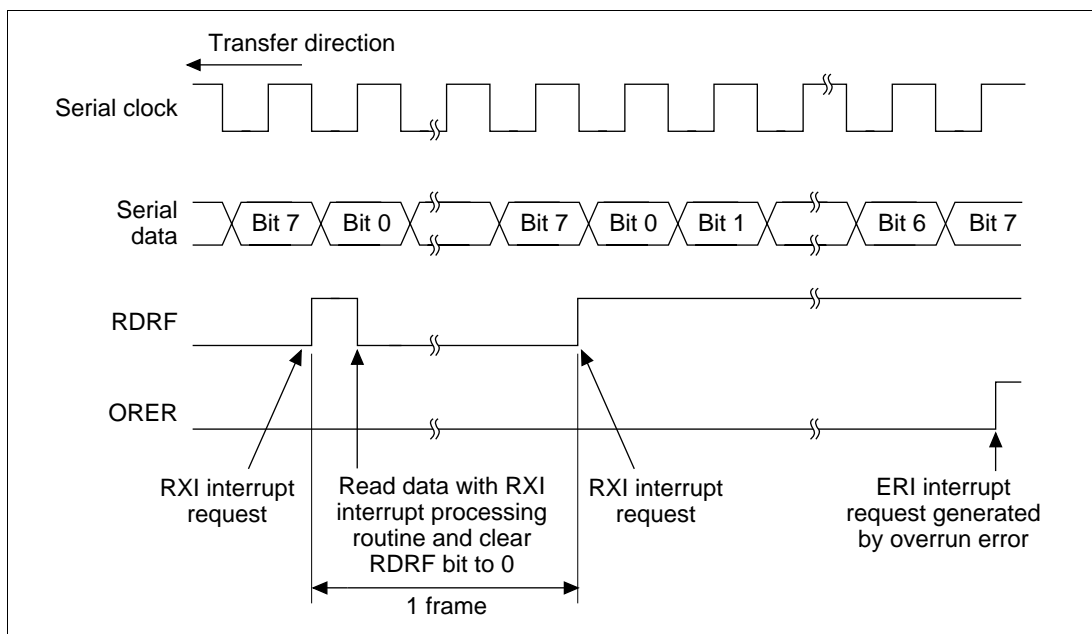


**Figure 14.21 Sample Flowchart for Serial Receiving (1)**



**Figure 14.22 Sample Flowchart for Serial Receiving (2)**

Figure 14.23 shows an example of the SCI receive operation.



**Figure 14.23 Example of SCI Receive Operation**

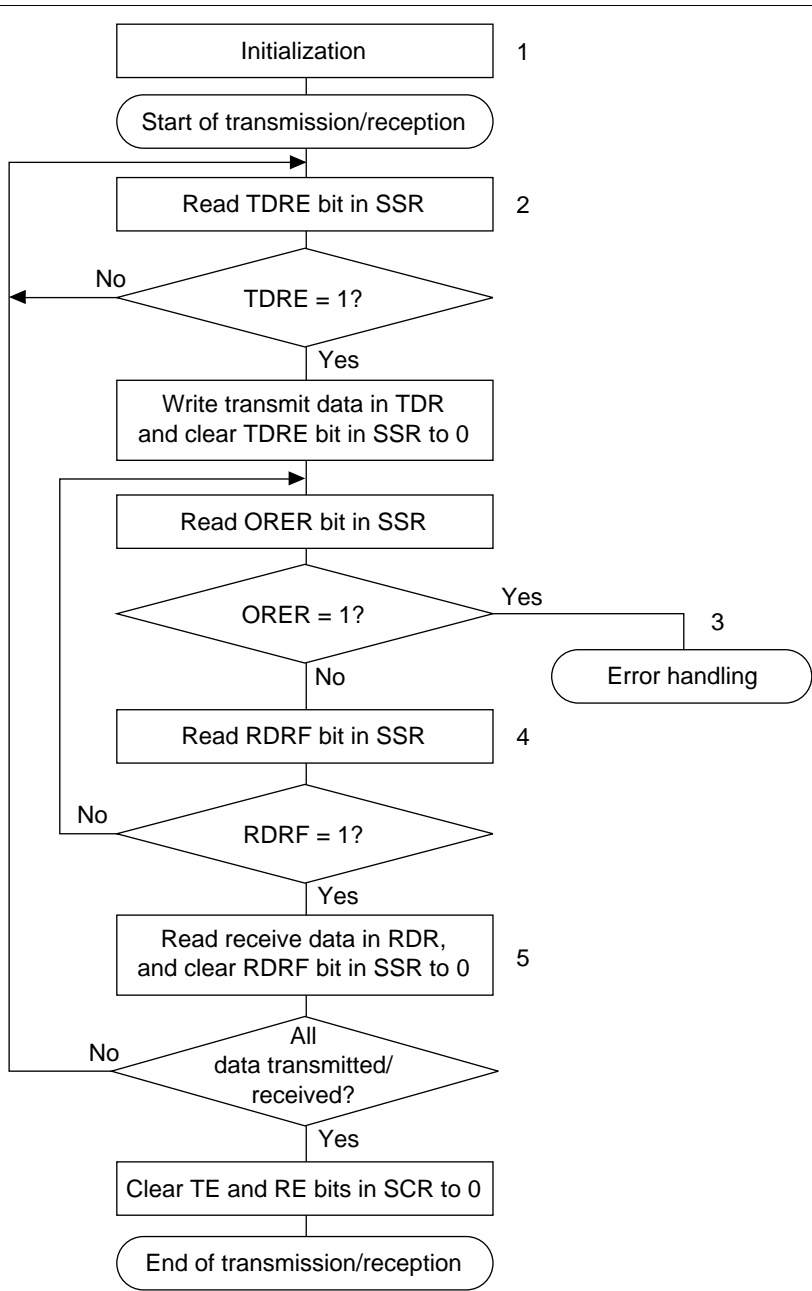
In receiving, the SCI operates as follows:

1. The SCI synchronizes with serial clock input or output and initializes internally.
2. Receive data is shifted into RSR in order from the LSB to the MSB. After receiving the data, the SCI checks that RDRF is 0 so that receive data can be loaded from RSR into RDR. If this check passes, the SCI sets RDRF to 1 and stores the receive data in RDR. If the check does not pass (receive error), the SCI operates as indicated in table 14.11 and no further transmission or reception is possible. If the error flag is set to 1, the RDRF bit is not set to 1 during reception, even if the RDRF bit is 0 cleared. When restarting reception, be sure to clear the error flag.
3. After setting RDRF to 1, if the receive-data-full interrupt enable bit (RIE) is set to 1 in SCR, the SCI requests a receive-data-full interrupt (RXI). If the ORER bit is set to 1 and the receive-data-full interrupt enable bit (RIE) in SCR is also set to 1, the SCI requests a receive-error interrupt (ERI).

**Transmitting and Receiving Serial Data Simultaneously (Synchronous Mode):** Figure 14.24 shows a sample flowchart for transmitting and receiving serial data simultaneously. The procedure is as follows (the steps correspond to the numbers in the flowchart):

1. SCI initialization: Set the TxD and RxD pins using the PFC.
2. SCI status check and transmit data write: Read the serial status register (SSR), check that the TDRE bit is 1, then write transmit data in the transmit data register (TDR) and clear TDRE to 0. The TXI interrupt can also be used to determine if the TDRE bit has changed from 0 to 1.
3. Receive error handling: If a receive error occurs, read the ORER bit in SSR to identify the error. After executing the necessary error handling, clear ORER to 0. Transmitting/receiving cannot resume if ORER remains set to 1.
4. SCI status check and receive data read: Read the serial status register (SSR), check that RDRF is set to 1, then read receive data from the receive data register (RDR) and clear RDRF to 0. The RXI interrupt can also be used to determine if the RDRF bit has changed from 0 to 1.
5. Continue transmitting and receiving serial data: Read the RDRF bit and RDR, and clear RDRF to 0 before the MSB (bit 7) of the current frame is received. Also read the TDRE bit to check whether it is safe to write (if it reads 1); if so, write data in TDR, then clear TDRE to 0 before the MSB (bit 7) of the current frame is transmitted. When the DMAC is started by a transmit-data-empty interrupt request (TXI) to write data in TDR, the TDRE bit is checked and cleared automatically. When the DMAC is started by a receive-data-full interrupt (RXI) to read RDR, the RDRF bit is cleared automatically.

Note: In switching from transmitting or receiving to simultaneous transmitting and receiving, clear both TE and RE to 0, then set both TE and RE to 1 simultaneously.



**Figure 14.24 Sample Flowchart for Serial Transmission and Reception**



## 14.4 SCI Interrupt Sources and the DMAC

The SCI has four interrupt sources: transmit-end (TEI), receive-error (ERI), receive-data-full (RXI), and transmit-data-empty (TXI). Table 14.12 lists the interrupt sources and indicates their priority. These interrupts can be enabled and disabled by the TIE, RIE, and TEIE bits in the serial control register (SCR). Each interrupt request is sent separately to the interrupt controller.

TXI is requested when the TDRE bit in SSR is set to 1. TXI can start the direct memory access controller (DMAC) to transfer data. TDRE is automatically cleared to 0 when the DMAC writes data in the transmit data register (TDR).

RXI is requested when the RDRF bit in SSR is set to 1. RXI can start the DMAC to transfer data. RDRF is automatically cleared to 0 when the DMAC reads the receive data register (RDR).

ERI is requested when the ORER, PER, or FER bit in SSR is set to 1. ERI cannot start the DMAC.

TEI is requested when the TEND bit in SSR is set to 1. TEI cannot start the DMAC. Where the TXI interrupt indicates that transmit data writing is enabled, the TEI interrupt indicates that the transmit operation is complete.

**Table 14.12 SCI Interrupt Sources**

<b>Interrupt Source</b>	<b>Description</b>	<b>DMAC Activation</b>	<b>Priority</b>
ERI	Receive error (ORER, PER, or FER)	No	High
RXI	Receive data full (RDRF)	Yes	↑ ↓
TXI	Transmit data empty (TDRE)	Yes	
TEI	Transmit end (TEND)	No	Low

## 14.5 Usage Notes

Sections 14.5.1 through 14.5.9 provide information concerning use of the SCI.

### 14.5.1 TDR Write and TDRE Flag

The TDRE bit in the serial status register (SSR) is a status flag indicating loading of transmit data from TDR into TSR. The SCI sets TDRE to 1 when it transfers data from TDR to TSR. Data can be written to TDR regardless of the TDRE bit status. If new data is written in TDR when TDRE is 0, however, the old data stored in TDR will be lost because the data has not yet been transferred to TSR. Before writing transmit data to TDR, be sure to check that TDRE is set to 1.

### 14.5.2 Simultaneous Multiple Receive Errors

Table 14.13 indicates the state of the SSR status flags when multiple receive errors occur simultaneously. When an overrun error occurs, the RSR contents cannot be transferred to RDR, so receive data is lost.

**Table 14.13 SSR Status Flags and Transfer of Receive Data**

Receive Error Status	SSR Status Flags				Receive Data Transfer
	RDRF	ORER	FER	PER	RSR → RDR
Overrun error	1	1	0	0	X
Framing error	0	0	1	0	O
Parity error	0	0	0	1	O
Overrun error + framing error	1	1	1	0	X
Overrun error + parity error	1	1	0	1	X
Framing error + parity error	0	0	1	1	O
Overrun error + framing error + parity error	1	1	1	1	X

Note: O: Receive data is transferred from RSR to RDR.

X: Receive data is not transferred from RSR to RDR.

### **14.5.3 Break Detection and Processing (Asynchronous Mode Only)**

Break signals can be detected by reading the RxD pin directly when a framing error (FER) is detected. In the break state, the input from the RxD pin consists of all 0s, so FER is set and the parity error flag (PER) may also be set. In the break state, the SCI receiver continues to operate, so if the FER bit is cleared to 0, it will be set to 1 again.

### **14.5.4 Sending a Break Signal (Asynchronous Mode Only)**

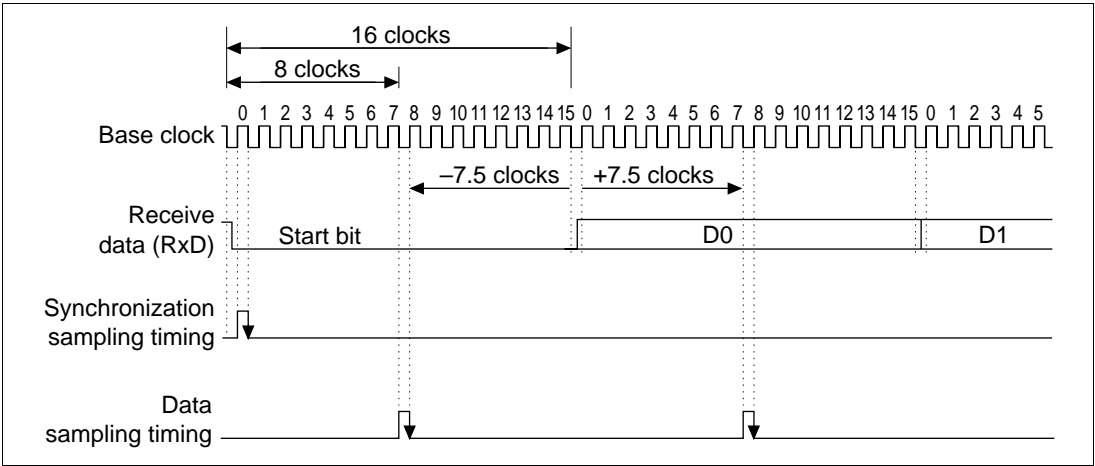
The TxD pin becomes a general I/O pin with the I/O direction and level determined by the I/O port data register (DR) and pin function controller (PFC) control register (CR). These conditions allow break signals to be sent. The DR value is substituted for the marking status until the PFC is set. Consequently, the output port is set to initially output a 1. To send a break in serial transmission, first clear the DR to 0, then establish the TxD pin as an output port using the PFC. When TE is cleared to 0, the transmission section is initialized regardless of the present transmission status.

### **14.5.5 Receive Error Flags and Transmitter Operation (Synchronous Mode Only)**

When a receive error flag (ORER, PER, or FER) is set to 1, the SCI will not start transmitting even if TDRE is set to 1. Be sure to clear the receive error flags to 0 before starting to transmit. Note that clearing RE to 0 does not clear the receive error flags.

### **14.5.6 Receive Data Sampling Timing and Receive Margin in Asynchronous Mode**

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times the transfer rate. In receiving, the SCI synchronizes internally with the falling edge of the start bit, which it samples on the base clock. Receive data is latched on the rising edge of the eighth base clock pulse (figure 14.25).



**Figure 14.25 Receive Data Sampling Timing in Asynchronous Mode**

The receive margin in asynchronous mode can therefore be expressed as:

$$M = \left| \left( 0.5 - \frac{1}{2N} \right) - (L - 0.5) F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\%$$

M : Receive margin (%)

N : Ratio of clock frequency to bit rate (N = 16)

D : Clock duty cycle (D = 0 to 1.0)

L : Frame length (L = 9 to 12)

F : Absolute deviation of clock frequency

From the equation above, if F = 0 and D = 0.5 the receive margin is 46.875%:

$$D = 0.5, F = 0$$

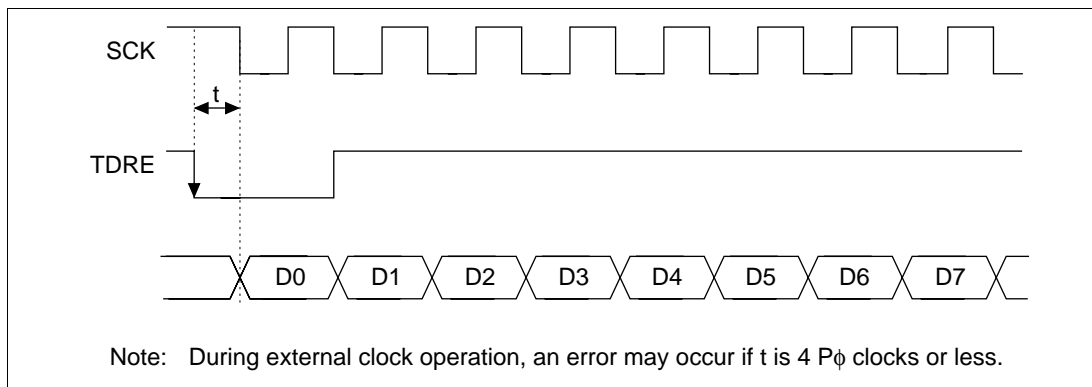
$$M = (0.5 - 1/(2 \times 16)) \times 100\%$$

$$= 46.875\%$$

This is a theoretical value. A reasonable margin to allow in system designs is 20 to 30%.

### 14.5.7 Constraints on DMAC Use

- When using an external clock source for the serial clock, update TDR with the DMAC, and then after the elapse of five peripheral clocks ( $P\phi$ ) or more, input a transmit clock. If a transmit clock is input in the first four  $P\phi$  clocks after TDR is written, an error may occur (figure 14.26).
- Before reading the receive data register (RDR) with the DMAC, select the receive-data-full (RXI) interrupt of the SCI as a start-up source.



**Figure 14.26 Example of Synchronous Transmission with DMAC**

### 14.5.8 Cautions on Synchronous External Clock Mode

- Set  $TE = RE = 1$  only when external clock SCK is 1.
- Do not set  $TE = RE = 1$  until at least four  $P\phi$  clocks after external clock SCK has changed from 0 to 1.
- When receiving, RDRF is 1 when RE is cleared to zero 2.5 to 3.5  $P\phi$  clocks after the rising edge of the RxD D7 bit SCK input, but copying to RDR is not possible.

### 14.5.9 Caution on Synchronous Internal Clock Mode

When receiving, RDRF is 1 when RE is cleared to zero 1.5  $P\phi$  clocks after the rising edge of the RxD D7 bit SCK output, but copying to RDR is not possible.



# Section 15 Hitachi Controller Area Network (HCAN)

## 15.1 Overview

The HCAN is a module for controlling a controller area network (CAN) for realtime communication in automotive and industrial equipment systems, etc. The SH7052F/SH7053F/SH7054F has a 1-channel on-chip HCAN module.

Reference: Bosch CAN Specification Version 2.0 1991, Robert Bosch GmbH

### 15.1.1 Features

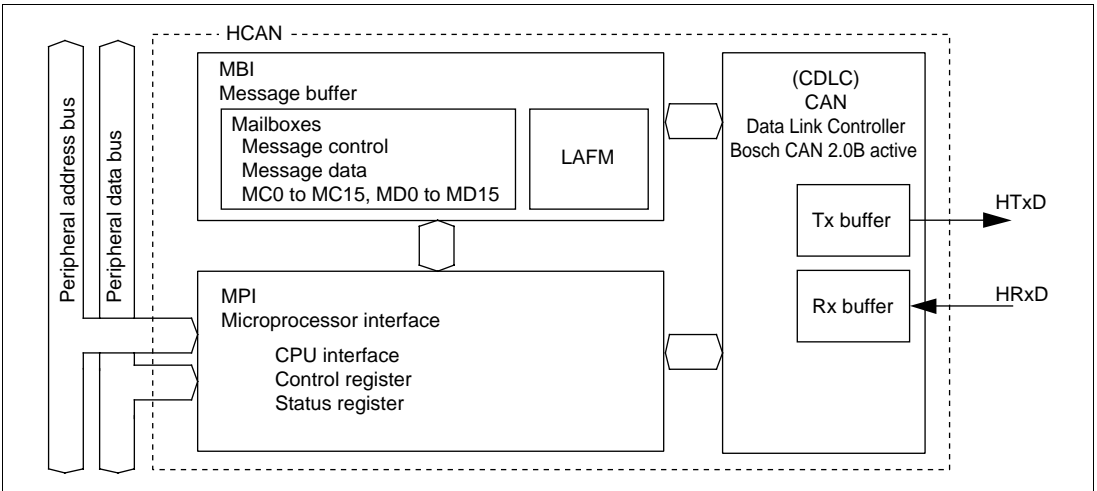
The HCAN has the following features:

- CAN version: Bosch 2.0B active compatible
  - Communication systems:
    - NRZ (Non-Return to Zero) system (with bit-stuffing function)
    - Broadcast communication system
  - Transmission path: Bidirectional 2-wire serial communication
  - Communication speed: Max. 1 Mbps (at 40 MHz operation)
  - Data length: 0 to 8 bytes
- Number of channels: 1
- Data buffers: 16 (one receive-only buffer and 15 buffers settable for transmission/reception)
- Data transmission: Choice of two methods:
  - Mailbox (buffer) number order (low-to-high)
  - Message priority (identifier) high-to-low order
- Data reception: Two methods:
  - Message identifier match (transmit/receive-setting buffers)
  - Reception with message identifier masked (receive-only)
- CPU interrupts: Four independent interrupt vectors:
  - Error interrupt
  - Reset processing interrupt
  - Message reception interrupt
  - Message transmission interrupt
- HCAN operating modes: Support for various modes:
  - Hardware reset
  - Software reset
  - Normal status (error-active, error-passive)

- Bus off status
- HCAN configuration mode
- HCAN sleep mode
- HCAN halt mode
- Other features: DMAC can be activated by message reception mailbox (HCAN mailbox 0 only)

### 15.1.2 Block Diagram

Figure 15.1 shows a block diagram of the HCAN.



**Figure 15.1 HCAN Block Diagram**

**Message Buffer Interface (MBI):** The MBI, consisting of mailboxes and a local acceptance filter mask (LAFM), stores CAN transmit/receive messages (identifiers, data, etc.). Transmit messages are written by the CPU. For receive messages, the data received by the CDLC is stored automatically.

**Microprocessor Interface (MPI):** The MPI, consisting of a bus interface, control register, status register, etc., controls HCAN internal data, statuses, and so forth.

**CAN Data Link Controller (CDLC):** The CDLC performs transmission and reception of messages conforming to the Bosch CAN Ver. 2.0B active standard (data frames, remote frames, error frames, overload frames, inter-frame spacing), as well as CRC checking, bus arbitration, and other functions.



### 15.1.3 Pin Configuration

Table 15.1 shows the HCAN's pins. When using the functions of these external pins, the pin function controller (PFC) must also be set in line with the HCAN settings.

When using HCAN pins, settings must be made in the HCAN configuration mode (during initialization: MCR0 = 1 and GSR3 = 1).

**Table 15.1 HCAN Pins**

<b>Name</b>	<b>Abbreviation</b>	<b>Input/Output</b>	<b>Function</b>
HCAN transmit data pin	HTxD	Output	CAN bus transmission pin
HCAN receive data pin	HRxD	Input	CAN bus reception pin

A bus driver is necessary between the pins and the CAN bus. A Philips PCA82C250 compatible model is recommended.

## 15.1.4 Register Configuration

Table 15.2 lists the HCAN's registers.

**Table 15.2 HCAN Registers**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Master control register	MCR	R/W	H'01	H'FFFF E400	8 bits 16 bits
General status register	GSR	R	H'0C	H'FFFF E401	8 bits
Bit configuration register	BCR	R/W	H'0000	H'FFFF E402	8/16 bits
Mailbox configuration register	MBCR	R/W	H'0100	H'FFFF E404	8/16 bits
Transmit wait register	TXPR	R/W	H'0000	H'FFFF E406	8/16 bits
Transmit wait cancel register	TXCR	R/W	H'0000	H'FFFF E408	8/16 bits
Transmit acknowledge register	TXACK	R/W	H'0000	H'FFFF E40A	8/16 bits
Abort acknowledge register	ABACK	R/W	H'0000	H'FFFF E40C	8/16 bits
Receive complete register	RXPR	R/W	H'0000	H'FFFF E40E	8/16 bits
Remote request register	RFPR	R/W	H'0000	H'FFFF E410	8/16 bits
Interrupt register	IRR	R/W	H'0100	H'FFFF E412	8/16 bits
Mailbox interrupt mask register	MBIMR	R/W	H'FFFF	H'FFFF E414	8/16 bits
Interrupt mask register	IMR	R/W	H'FEFF	H'FFFF E416	8/16 bits
Receive error counter	REC	R	H'00	H'FFFF E418	8 bits 16 bits
Transmit error counter	TEC	R	H'00	H'FFFF E419	8 bits
Unread message status register	UMSR	R/W	H'0000	H'FFFF E41A	8/16 bits
Local acceptance filter mask L	LAFML	R/W	H'0000	H'FFFF E41C	8/16 bits
Local acceptance filter mask H	LAFMH	R/W	H'0000	H'FFFF E41E	8/16 bits

**Table 15.2 HCAN Registers (cont)**

<b>Name</b>	<b>Abbreviation</b>	<b>R/W</b>	<b>Initial Value</b>	<b>Address</b>	<b>Access Size</b>
Message control 0 [1:8]	MC0 [1:8]	R/W	Undefined	H'FFFF E420	8/16 bits
Message control 1 [1:8]	MC1 [1:8]	R/W	Undefined	H'FFFF E428	8/16 bits
Message control 2 [1:8]	MC2 [1:8]	R/W	Undefined	H'FFFF E430	8/16 bits
Message control 3 [1:8]	MC3 [1:8]	R/W	Undefined	H'FFFF E438	8/16 bits
Message control 4 [1:8]	MC4 [1:8]	R/W	Undefined	H'FFFF E440	8/16 bits
Message control 5 [1:8]	MC5 [1:8]	R/W	Undefined	H'FFFF E448	8/16 bits
Message control 6 [1:8]	MC6 [1:8]	R/W	Undefined	H'FFFF E450	8/16 bits
Message control 7 [1:8]	MC7 [1:8]	R/W	Undefined	H'FFFF E458	8/16 bits
Message control 8 [1:8]	MC8 [1:8]	R/W	Undefined	H'FFFF E460	8/16 bits
Message control 9 [1:8]	MC9 [1:8]	R/W	Undefined	H'FFFF E468	8/16 bits
Message control 10 [1:8]	MC10 [1:8]	R/W	Undefined	H'FFFF E470	8/16 bits
Message control 11 [1:8]	MC11 [1:8]	R/W	Undefined	H'FFFF E478	8/16 bits
Message control 12 [1:8]	MC12 [1:8]	R/W	Undefined	H'FFFF E480	8/16 bits
Message control 13 [1:8]	MC13 [1:8]	R/W	Undefined	H'FFFF E488	8/16 bits
Message control 14 [1:8]	MC14 [1:8]	R/W	Undefined	H'FFFF E490	8/16 bits
Message control 15 [1:8]	MC15 [1:8]	R/W	Undefined	H'FFFF E498	8/16 bits
Message data 0 [1:8]	MD0 [1:8]	R/W	Undefined	H'FFFF E4B0	8/16 bits
Message data 1 [1:8]	MD1 [1:8]	R/W	Undefined	H'FFFF E4B8	8/16 bits
Message data 2 [1:8]	MD2 [1:8]	R/W	Undefined	H'FFFF E4C0	8/16 bits
Message data 3 [1:8]	MD3 [1:8]	R/W	Undefined	H'FFFF E4C8	8/16 bits
Message data 4 [1:8]	MD4 [1:8]	R/W	Undefined	H'FFFF E4D0	8/16 bits
Message data 5 [1:8]	MD5 [1:8]	R/W	Undefined	H'FFFF E4D8	8/16 bits
Message data 6 [1:8]	MD6 [1:8]	R/W	Undefined	H'FFFF E4E0	8/16 bits
Message data 7 [1:8]	MD7 [1:8]	R/W	Undefined	H'FFFF E4E8	8/16 bits
Message data 8 [1:8]	MD8 [1:8]	R/W	Undefined	H'FFFF E4F0	8/16 bits
Message data 9 [1:8]	MD9 [1:8]	R/W	Undefined	H'FFFF E4F8	8/16 bits
Message data 10 [1:8]	MD10 [1:8]	R/W	Undefined	H'FFFF E500	8/16 bits
Message data 11 [1:8]	MD11 [1:8]	R/W	Undefined	H'FFFF E508	8/16 bits
Message data 12 [1:8]	MD12 [1:8]	R/W	Undefined	H'FFFF E510	8/16 bits
Message data 13 [1:8]	MD13 [1:8]	R/W	Undefined	H'FFFF E518	8/16 bits
Message data 14 [1:8]	MD14 [1:8]	R/W	Undefined	H'FFFF E520	8/16 bits
Message data 15 [1:8]	MD15 [1:8]	R/W	Undefined	H'FFFF E528	8/16 bits

## 15.2 Register Descriptions

### 15.2.1 Master Control Register (MCR)

The master control register (MCR) is an 8-bit readable/writable register that controls the CAN interface.

Bit:	7	6	5	4	3	2	1	0
	MCR7	—	MCR5	—	—	MCR2	MCR1	MCR0
Initial value:	0	0	0	0	0	0	0	1
R/W:	R/W	—	R/W	—	—	R/W	R/W	R/W

- Bit 7—HCAN Sleep Mode Release (MCR7): Enables or disables HCAN sleep mode release by bus operation.

Bit 7: MCR7	Description
0	HCAN sleep mode release by CAN bus operation disabled (Initial value)
1	HCAN sleep mode release by CAN bus operation enabled

- Bit 6—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 5—HCAN Sleep Mode (MCR5): Enables or disables HCAN sleep mode transition.

Bit 5: MCR5	Description
0	HCAN sleep mode released (Initial value)
1	Transition to HCAN sleep mode enabled

- Bits 4 and 3—Reserved: These bits always read 0. The write value should always be 0.
- Bit 2—Message Transmission Method (MCR2): Selects the transmission method for transmit messages.

Bit 2: MCR2	Description
0	Transmission order determined by message identifier priority (Initial value)
1	Transmission order determined by mailbox (buffer) number priority (TXPR1 > TXPR15)

- Bit 1—Halt Request (MCR1): Controls halting of the HCAN module.

Bit 1: MCR1	Description
0	Normal operating mode (Initial value)
1	Halt mode transition request

- Bit 0—Reset Request (MCR0): Controls resetting of the HCAN module.

Bit 0: MCR0	Description
0	Normal operating mode (MCR0 = 0 and GSR3 = 0) [Setting condition] When 0 is written after an HCAN reset
1	Reset mode transition request (Initial value)

In order for GSR3 to change from 1 to 0 after 0 is written to MCR0, time is required before the HCAN is internally reset. There is consequently a delay before GSR3 is cleared to 0 after MCR0 is cleared to 0.

### 15.2.2 General Status Register (GSR)

The general status register (GSR) is an 8-bit readable/writable register that indicates the status of the CAN bus.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	GSR3	GSR2	GSR1	GSR0
Initial value:	0	0	0	0	1	1	0	0
R/W:	R	R	R	R	R	R	R	R

- Bits 7 to 4—Reserved: These bits always read 0. The write value should always be 0.
- Bit 3—Reset Status Bit (GSR3): Indicates whether the HCAN module is in the normal operating state or the reset state. This bit cannot be modified.

Bit 3: MCR3	Description
0	Normal operating state [Setting condition] After an HCAN internal reset
1	Configuration mode (Initial value) [Reset condition] MCR0-initiated reset state or sleep mode

- Bit 2—Message Transmission Status Flag (GSR2): Flag that indicates whether the module is currently in the message transmission period. The “message transmission period” is the period from the start of message transmission (SOF) until the end of a 3-bit intermission interval after EOF (End of Frame). This bit cannot be modified.

Bit 2: GSR2	Description
0	Transmission in progress
1	[Reset condition] Idle period (Initial value)

- Bit 1—Transmit/Receive Warning Flag (GSR1): Flag that indicates an error warning. This bit cannot be modified.

Bit 1: GSR1	Description
0	[Reset condition] When TEC < 96 and REC < 96 or TEC ≥ 256 (Initial value)
1	When TEC ≥ 96 or REC ≥ 96

- Bit 0—Bus Off Flag (GSR0): Flag that indicates the bus off state. This bit cannot be modified.

Bit 0: GSR0	Description
0	[Reset condition] Recovery from bus off state (Initial value)
1	When TEC ≥ 256 (bus off state)

### 15.2.3 Bit Configuration Register (BCR)

The bit configuration register (BCR) is a 16-bit readable/writable register that is used to set CAN bit timing parameters and the baud rate prescaler.

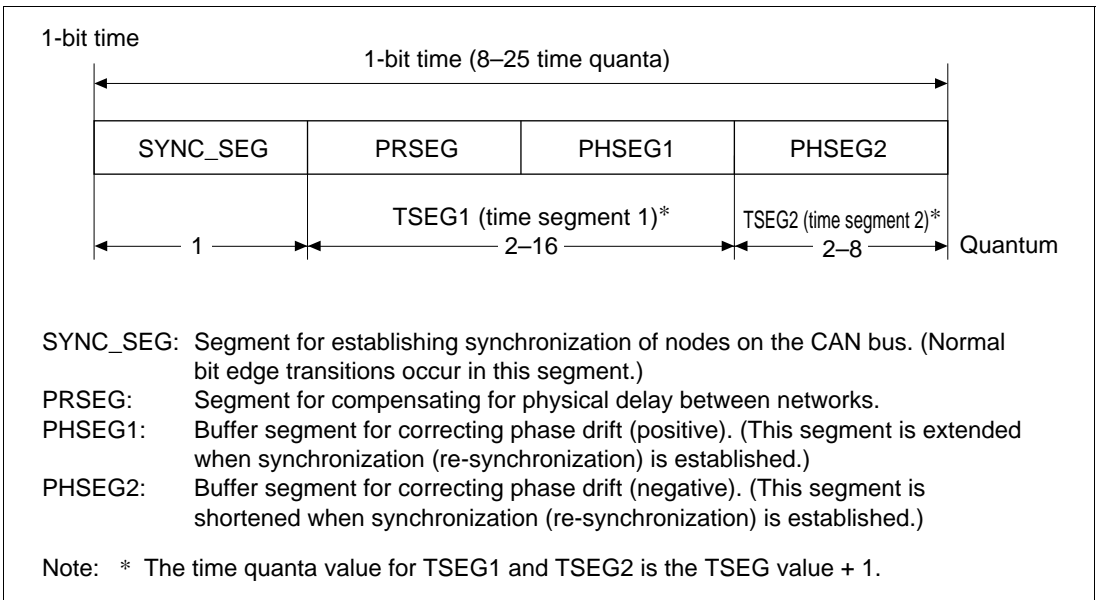
Bit:	15	14	13	12	11	10	9	8
	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	BCR15	BCR14	BCR13	BCR12	BCR11	BCR10	BCR9	BCR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 and 14—Re-synchronization Jump Width (SJW): These bits set the maximum bit synchronization range.

Bit 15: BCR7	Bit 14: BCR6	Description
0	0	Maximum bit synchronization width = 1 time quantum
	1	Maximum bit synchronization width = 2 time quanta
1	0	Maximum bit synchronization width = 3 time quanta
	1	Maximum bit synchronization width = 4 time quanta

- Bits 13 to 8—Baud Rate Prescale (BRP): These bits are used to set the CAN bus baud rate.

Bit 13: BCR5	Bit 12: BCR4	Bit 11: BCR3	Bit 10: BCR2	Bit 9: BCR1	Bit 8: BCR0	Description
0	0	0	0	0	0	2 × system clock (Initial value)
0	0	0	0	0	1	4 × system clock
0	0	0	0	1	0	6 × system clock
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	128 × system clock



**Figure 15.2 Detailed Description of One Bit**

HCAN bit rate calculation:

$$\text{Bit rate [b/s]} = \frac{f_{\text{CLK}}}{2 \times (\text{BRP} + 1) \times (3 + \text{TSEG1} + \text{TSEG2})}$$

Note:  $f_{\text{CLK}} = P\phi$  (peripheral clock ( $\phi/2$ ))

The BCR values are used for BRP, TSEG1, and TSEG2.

### BCR Setting Constraints

$$\text{TSEG1} > \text{TSEG2} \geq \text{SJW} \quad (\text{SJW} = 1 \text{ to } 4)$$

$$3 + \text{TSEG1} + \text{TSEG2} = 8 \text{ to } 25 \text{ time quanta}$$

$$\text{TSEG2} > \text{B}'001 \text{ (BRP} = \text{B}'000000)$$

$$\text{TSEG2} > \text{B}'000 \text{ (BRP} > \text{B}'000000)$$

These constraints allow the setting range shown in table 15.3 for TSEG1 and TSEG2 in BCR.

**Table 15.3 Setting Range for TSEG1 and TSEG2 in BCR**

		TSEG2 (BCR [14:12])						
		001	010	011	100	101	110	111
TSEG1 (BCR [11:8])	0011	No	Yes	No	No	No	No	No
	0100	Yes*	Yes	Yes	No	No	No	No
	0101	Yes*	Yes	Yes	Yes	No	No	No
	0110	Yes*	Yes	Yes	Yes	Yes	No	No
	0111	Yes*	Yes	Yes	Yes	Yes	Yes	No
	1000	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
	1001	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
	1010	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
	1011	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
	1100	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
	1101	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
	1110	Yes*	Yes	Yes	Yes	Yes	Yes	Yes
1111	Yes*	Yes	Yes	Yes	Yes	Yes	Yes	

Notes: The time quanta value for TSEG1 and TSEG2 is the TSEG value + 1.

\* Setting is enabled except when BRP[13:8] = B'000000.



- Bit 7—Bit Sample Point (BSP): Sets the point at which data is sampled.

Bit 7: BCR15	Description
0	Bit sampling at one point (end of time segment 1) (Initial value)
1	Bit sampling at three points (end of time segment 1, and 1 time quantum before and after)

- Bits 6 to 4—Time Segment 2 (TSEG2): These bits are used to set the segment for correcting 1-bit time error. A value from 2 to 8 can be set.

Bit 6: BCR14	Bit 5: BCR13	Bit 4: BCR12	Description
0	0	0	Setting prohibited (Initial value)
		1	TSEG2 (PHSEG2) = 2 time quanta
1	1	0	TSEG2 (PHSEG2) = 3 time quanta
		1	TSEG2 (PHSEG2) = 4 time quanta
	0	0	TSEG2 (PHSEG2) = 5 time quanta
		1	TSEG2 (PHSEG2) = 6 time quanta
1	1	0	TSEG2 (PHSEG2) = 7 time quanta
		1	TSEG2 (PHSEG2) = 8 time quanta

- Bits 3 to 0—Time Segment 1 (TSEG1): These bits are used to set the segment for absorbing output buffer, CAN bus, and input buffer delay. A value from 1 to 16 can be set.

Bit 3: BCR11	Bit 2: BCR10	Bit 1: BCR9	Bit 0: BCR8	Description
0	0	0	0	Setting prohibited (Initial value)
0	0	0	1	Setting prohibited
0	0	1	0	Setting prohibited
0	0	1	1	TSEG1 (PRSEG + PHSEG1) = 4 time quanta
0	1	0	0	TSEG1 (PRSEG + PHSEG1) = 5 time quanta
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	1	1	TSEG1 (PRSEG + PHSEG1) = 16 time quanta

## 15.2.4 Mailbox Configuration Register (MBCR)

The mailbox configuration register (MBCR) is a 16-bit readable/writable register that is used to set mailbox (buffer) transmission/reception.

Bit:	15	14	13	12	11	10	9	8
	MBCR7	MBCR6	MBCR5	MBCR4	MBCR3	MBCR2	MBCR1	—
Initial value:	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Bit:	7	6	5	4	3	2	1	0
	MBCR15	MBCR14	MBCR13	MBCR12	MBCR11	MBCR10	MBCR9	MBCR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9 and 7 to 0—Mailbox Setting Register (MBCR7 to 1, MBCR15 to 8): These bits set the polarity of the corresponding mailboxes (buffers).

Bit x: MBCRx	Description
0	Corresponding mailbox is set for transmission (Initial value)
1	Corresponding mailbox is set for reception

- Bit 8—Reserved: This bit always reads 1. The write value should always be 1.

## 15.2.5 Transmit Wait Register (TXPR)

The transmit wait register (TXPR) is a 16-bit readable/writable register that is used to set a transmit wait after a transmit message is stored in a mailbox (buffer) (CAN bus arbitration wait).

Bit:	15	14	13	12	11	10	9	8
	TXPR7	TXPR6	TXPR5	TXPR4	TXPR3	TXPR2	TXPR1	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Bit:	7	6	5	4	3	2	1	0
	TXPR15	TXPR14	TXPR13	TXPR12	TXPR11	TXPR10	TXPR9	TXPR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9 and 7 to 0—Transmit Wait Register (TXPR7 to 1, TXPR15 to 8): These bits set a CAN bus arbitration wait for the corresponding mailboxes (buffers).

Bit x: TXPRx	Description
0	Transmit message idle state in corresponding mailbox (Initial value) [Clearing condition] Message transmission completion and cancellation completion
1	Transmit message transmit wait in corresponding mailbox (CAN bus arbitration)

- Bit 8—Reserved: This bit always reads 0. The write value should always be 0.

### 15.2.6 Transmit Wait Cancel Register (TXCR)

The transmit wait cancel register (TXCR) is a 16-bit readable/writable register that controls cancellation of transmit wait messages in mailboxes (buffers).

Bit:	15	14	13	12	11	10	9	8
	TXCR7	TXCR6	TXCR5	TXCR4	TXCR3	TXCR2	TXCR1	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	7	6	5	4	3	2	1	0
	TXCR15	TXCR14	TXCR13	TXCR12	TXCR11	TXCR10	TXCR9	TXCR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9 and 7 to 0—Transmit Wait Cancel Register (TXCR7 to 1, TXCR15 to 8): These bits control cancellation of transmit wait messages in the corresponding HCAN mailboxes (buffers).

Bit x: TXCRx	Description
0	Transmit message cancellation idle state in corresponding mailbox (Initial value) [Clearing condition] Completion of TXPR clearing (when transmit message is canceled normally)
1	TXPR cleared for corresponding mailbox (transmit message cancellation)

- Bit 8—Reserved: This bit always reads 0. The write value should always be 0.

## 15.2.7 Transmit Acknowledge Register (TXACK)

The transmit acknowledge register (TXACK) is a 16-bit readable/writable register containing status flags that indicate normal transmission of mailbox (buffer) transmit messages.

Bit:	15	14	13	12	11	10	9	8
	TXACK7	TXACK6	TXACK5	TXACK4	TXACK3	TXACK2	TXACK1	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	7	6	5	4	3	2	1	0
	TXACK15	TXACK14	TXACK13	TXACK12	TXACK11	TXACK10	TXACK9	TXACK8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9 and 7 to 0—Transmit Acknowledge Register (TXACK7 to 1, TXACK15 to 8): These bits indicate that a transmit message in the corresponding HCAN mailbox (buffer) has been transmitted normally.

Bit x: TXACKx	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Completion of message transmission for corresponding mailbox

- Bit 8—Reserved: This bit always reads 0. The write value should always be 0.

## 15.2.8 Abort Acknowledge Register (ABACK)

The abort acknowledge register (ABACK) is a 16-bit readable/writable register containing status flags that indicate normal cancellation (aborting) of a mailbox (buffer) transmit messages.

Bit:	15	14	13	12	11	10	9	8
	ABACK7	ABACK6	ABACK5	ABACK4	ABACK3	ABACK2	ABACK1	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Bit:	7	6	5	4	3	2	1	0
	ABACK15	ABACK14	ABACK13	ABACK12	ABACK11	ABACK10	ABACK9	ABACK8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 9 and 7 to 0—Abort Acknowledge Register (ABACK7 to 1, ABACK15 to 8): These bits indicate that a transmit message in the corresponding mailbox (buffer) has been canceled (aborted) normally.

Bit x: ABACKx	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Completion of transmit message cancellation for corresponding mailbox

- Bit 8—Reserved: This bit always reads 0. The write value should always be 0.

## 15.2.9 Receive Complete Register (RXPR)

The receive complete register (RXPR) is a 16-bit readable/writable register containing status flags that indicate normal reception of messages (data frame or remote frame) in mailboxes (buffers). In the case of remote frame reception, the corresponding bit in the remote request register (RFPR) is also set.

Bit:	15	14	13	12	11	10	9	8
	RXPR7	RXPR6	RXPR5	RXPR4	RXPR3	RXPR2	RXPR1	RXPR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	RXPR15	RXPR14	RXPR13	RXPR12	RXPR11	RXPR10	RXPR9	RXPR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 0—Receive Complete Register (RXPR7 to 0, RXPR15 to 8): These bits indicate that a receive message has been received normally in the corresponding mailbox (buffer).

Bit x: RXPRx	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Completion of message (data frame or remote frame) reception in corresponding mailbox

## 15.2.10 Remote Request Register (RFPR)

The remote request register (RFPR) is a 16-bit readable/writable register containing status flags that indicate normal reception of remote frames in mailboxes (buffers). When a bit in this register is set, the corresponding bit in the receive complete register (RXPR) is also set.

Bit:	15	14	13	12	11	10	9	8
	RFPR7	RFPR6	RFPR5	RFPR4	RFPR3	RFPR2	RFPR1	RFPR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	RFPR15	RFPR14	RFPR13	RFPR12	RFPR11	RFPR10	RFPR9	RFPR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 0—Remote Request Register (RFPR7 to 0, RFPR15 to 8): These bits indicate that a remote frame has been received normally in the corresponding mailbox (buffer).

Bit x: RFPRx	Description
0	[Clearing condition] Writing 1 <span style="float: right;">(Initial value)</span>
1	Completion of remote frame reception in corresponding mailbox

## 15.2.11 Interrupt Register (IRR)

The interrupt register (IRR) is a 16-bit readable/writable register containing status flags for the various interrupt sources.

Bit:	15	14	13	12	11	10	9	8
	IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0
Initial value:	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	—	—	IRR12	—	—	IRR9	IRR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W

- Bit 15—Overload Frame/Bus Off Recovery Interrupt Flag (IRR7): Status flag indicating that the HCAN has transmitted an overload frame or recovered from the bus off state.

Bit 15: IRR7	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Overload frame transmission or recovery from bus off state [Setting conditions] Error active/error passive state <ul style="list-style-type: none"> <li>• When overload frame is transmitted</li> </ul> Bus off state <ul style="list-style-type: none"> <li>• When 11 recessive bits is received 128 times (<math>REC \geq 128</math>)</li> </ul>

- Bit 14—Bus Off Interrupt Flag (IRR6): Status flag indicating the bus off state caused by the transmit error counter.

Bit 14: IRR6	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Bus off state caused by transmit error [Setting condition] When $TEC \geq 256$

- Bit 13—Error Passive Interrupt Flag (IRR5): Status flag indicating the error passive state caused by the transmit/receive error counter.

Bit 13: IRR5	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Error passive state caused by transmit/receive error [Setting condition] When $TEC \geq 128$ or $REC \geq 128$



- Bit 12—Receive Overload Warning Interrupt Flag (IRR4): Status flag indicating the error warning state caused by the receive error counter.

Bit 12: IRR4	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Error warning state caused by receive error [Setting condition] When REC ≥ 96

- Bit 11—Transmit Overload Warning Interrupt Flag (IRR3): Status flag indicating the error warning state caused by the transmit error counter.

Bit 11: IRR3	Description
0	[Clearing condition] Writing 1 (Initial value)
1	Error warning state caused by transmit error [Setting condition] When TEC ≥ 96

- Bit 10—Remote Frame Request Interrupt Flag (IRR2): Status flag indicating that a remote frame has been received in a mailbox (buffer).

Bit 10: IRR2	Description
0	[Clearing condition] Clearing of all bits in RFPR (remote request wait register) (Initial value)
1	Remote frame received and stored in mailbox [Setting conditions] When remote frame reception is completed. When corresponding MBIMR = 0.

- Bit 9—Receive Message Interrupt Flag (IRR1): Status flag indicating that a mailbox (buffer) receive message has been received normally.

Bit 9: IRR1	Description
0	[Clearing condition] Clearing of all bits in RXPR (receive complete register) when MBIMR is 0 (Initial value)
1	Data frame or remote frame received and stored in mailbox [Setting conditions] When data frame or remote frame reception is completed. When corresponding MBIMR = 0.

- Bit 8—Reset Interrupt Flag (IRR0): Status flag indicating that the HCAN module has been reset. This bit cannot be masked in the interrupt mask register (IMR). If this bit is not cleared after a power-on reset or a transition to software standby mode, the program will jump to the interrupt vector as soon as interrupts are enabled by the interrupt controller.

Bit 8: IRR0	Description
0	[Clearing condition] Writing 1
1	Interrupt request by power-on reset or transition to software standby mode (OVR) (Initial value) [Setting condition] When reset processing is completed after power-on reset or software standby mode transition

- Bits 7 to 5, 3, and 2—Reserved: These bits always read 0. The write value should always be 0.
- Bit 4—Bus Operation Interrupt Flag (IRR12): Status flag indicating detection of a dominant bit due to bus operation when the HCAN module is in HCAN sleep mode.

Bit 4: IRR12	Description
0	CAN bus idle state (Initial value) [Clearing condition] Writing 1
1	CAN bus operation in HCAN sleep mode [Setting condition] Bus operation (dominant bit detection) in HCAN sleep mode

- Bit 1—Unread Interrupt Flag (IRR9): Status flag indicating that a receive message has been overwritten while still unread.

Bit 1: IRR9	Description
0	[Clearing condition] Clearing of all bits in UMSR (unread message status register) (Initial value)
1	Unread message overwrite [Setting condition] When UMSR (unread message status register) is set

- Bit 0—Mailbox Empty Interrupt Flag (IRR8): Status flag indicating that the next transmit message can be stored in the mailbox.

Bit 0: IRR8	Description
0	[Clearing condition] Writing 1 <span style="float: right;">(Initial value)</span>
1	Transmit message has been transmitted or aborted, and new message can be stored  [Setting condition] When TXPR (transmit wait register) is cleared by completion of transmission or completion of transmission abort

### 15.2.12 Mailbox Interrupt Mask Register (MBIMR)

The mailbox interrupt mask register (MBIMR) is a 16-bit readable/writable register containing flags that enable or disable individual mailbox (buffer) interrupt requests.

Bit:	15	14	13	12	11	10	9	8
	MBIMR7	MBIMR6	MBIMR5	MBIMR4	MBIMR3	MBIMR2	MBIMR1	MBIMR0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	MBIMR15	MBIMR14	MBIMR13	MBIMR12	MBIMR11	MBIMR10	MBIMR9	MBIMR8
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 0—Mailbox Interrupt Mask (MBIMR7 to 0, MBIMR15 to 8): Flags that enable or disable individual mailbox interrupt requests.

Bit x: MBIMRx	Description
0	[Transmitting] Interrupt request to CPU due to TXPR clearing  [Receiving] Interrupt request to CPU due to RXPR setting
1	Interrupt requests to CPU disabled <span style="float: right;">(Initial value)</span>

### 15.2.13 Interrupt Mask Register (IMR)

The interrupt mask register (IMR) is a 16-bit readable/writable register containing flags that enable or disable requests by individual interrupt sources.

Bit:	15	14	13	12	11	10	9	8
	IMR7	IMR6	IMR5	IMR4	IMR3	IMR2	IMR1	—
Initial value:	1	1	1	1	1	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
Bit:	7	6	5	4	3	2	1	0
	—	—	—	IMR12	—	—	IMR9	IMR8
Initial value:	1	1	1	1	1	1	1	1
R/W:	R	R	R	R/W	R	R	R/W	R/W

- Bit 15—Overload Frame/Bus Off Recovery Interrupt Mask (IMR7): Enables or disables overload frame/bus off recovery interrupt requests.

Bit 15: IMR7	Description
0	Overload frame/bus off recovery interrupt request (OVR) by IRR7 to CPU enabled
1	Overload frame/bus off recovery interrupt request (OVR) by IRR7 to CPU disabled
(Initial value)	

- Bit 14—Bus Off Interrupt Mask (IMR6): Enables or disables bus off interrupt requests caused by the transmit error counter.

Bit 14: IMR6	Description
0	Bus off interrupt request (ERS) by IRR6 to CPU enabled
1	Bus off interrupt request (ERS) by IRR6 to CPU disabled
(Initial value)	

- Bit 13—Error Passive Interrupt Mask (IMR5): Enables or disables error passive interrupt requests caused by the transmit/receive error counter.

Bit 13: IMR5	Description
0	Error passive interrupt request (ERS) by IRR5 to CPU enabled
1	Error passive interrupt request (ERS) by IRR5 to CPU disabled (Initial value)

- Bit 12—Receive Overload Warning Interrupt Mask (IMR4): Enables or disables error warning interrupt requests caused by the receive error counter.

Bit 12: IMR4	Description
0	REC error warning interrupt request (OVR) by IRR4 to CPU enabled
1	REC error warning interrupt request (OVR) by IRR4 to CPU disabled (Initial value)

- Bit 11—Transmit Overload Warning Interrupt Mask (IMR3): Enables or disables error warning interrupt requests caused by the transmit error counter.

Bit 11: IMR3	Description
0	TEC error warning interrupt request (OVR) by IRR3 to CPU enabled
1	TEC error warning interrupt request (OVR) by IRR3 to CPU disabled (Initial value)

- Bit 10—Remote Frame Request Interrupt Mask (IMR2): Enables or disables remote frame reception interrupt requests.

Bit 10: IMR2	Description
0	Remote frame reception interrupt request (OVR) by IRR2 to CPU enabled
1	Remote frame reception interrupt request (OVR) by IRR2 to CPU disabled (Initial value)

- Bit 9—Receive Message Interrupt Mask (IMR1): Enables or disables message reception interrupt requests.

Bit 9: IMR1	Description
0	Message reception interrupt request (RM) by IRR1 to CPU enabled
1	Message reception interrupt request (RM) by IRR1 to CPU disabled (Initial value)

- Bit 8—Reserved: This bit always reads 0. The write value should always be 0.
- Bits 7 to 5, 3, and 2—Reserved: These bits always read 1. The write value should always be 1.

- Bit 4—Bus Operation Interrupt Mask (IMR12): Enables or disables interrupt requests due to bus operation in sleep mode.

Bit 4: IMR12	Description
0	Bus operation interrupt request (OVR) by IRR12 to CPU enabled
1	Bus operation interrupt request (OVR) by IRR12 to CPU disabled (Initial value)

- Bit 1—Unread Interrupt Mask (IMR9): Enables or disables unread receive message overwrite interrupt requests.

Bit 1: IMR9	Description
0	Unread message overwrite interrupt request (OVR) by IRR9 to CPU enabled
1	Unread message overwrite interrupt request (OVR) by IRR9 to CPU disabled (Initial value)

- Bit 0—Mailbox Empty Interrupt Mask (IMR8): Enables or disables mailbox empty interrupt requests.

Bit 0: IMR8	Description
0	Mailbox empty interrupt request (SLE) by IRR8 to CPU enabled
1	Mailbox empty interrupt request (SLE) by IRR8 to CPU disabled (Initial value)

#### 15.2.14 Receive Error Counter (REC)

The receive error counter (REC) is an 8-bit read-only register that functions as a counter indicating the number of receive message errors on the CAN bus. The count value is stipulated in the CAN protocol.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

## 15.2.15 Transmit Error Counter (TEC)

The transmit error counter (TEC) is an 8-bit read-only register that functions as a counter indicating the number of transmit message errors on the CAN bus. The count value is stipulated in the CAN protocol.

Bit:	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

## 15.2.16 Unread Message Status Register (UMSR)

The unread message status register (UMSR) is a 16-bit readable/writable register containing status flags that indicate, for individual mailboxes (buffers), that a received message has been overwritten by a new receive message before being read. When an unread message is overwritten by a new receive message, the old data is lost.

Bit:	15	14	13	12	11	10	9	8
	UMSR7	UMSR6	UMSR5	UMSR4	UMSR3	UMSR2	UMSR1	UMSR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	UMSR15	UMSR14	UMSR13	UMSR12	UMSR11	UMSR10	UMSR9	UMSR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 to 0—Unread Message Status Flags (UMSR7 to 0, UMSR15 to 8): Status flags indicating that an unread receive message has been overwritten.

Bit x: UMSRx	Description
0	[Clearing condition] Writing 1 <span style="float: right;">(Initial value)</span>
1	Unread receive message is overwritten by a new message [Setting condition] When a new message is received before RXPR is cleared

### 15.2.17 Local Acceptance Filter Masks (LAFML, LAFMH)

The local acceptance filter masks (LAFML, LAFMH) are 16-bit readable/writable registers that filter receive messages to be stored in the receive-only mailbox (MC0, MD0) according to the identifier. In these registers, consist of LAFMH15: MSB to LAFMH5: LSB are 11 standard/extended identifier bits, and LAFMH1: MSB to LAFML0: LSB are 18 extended identifier bits.

#### LAFML

Bit:	15	14	13	12	11	10	9	8
	LAFML7	LAFML6	LAFML5	LAFML4	LAFML3	LAFML2	LAFML1	LAFML0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	LAFML15	LAFML14	LAFML13	LAFML12	LAFML11	LAFML10	LAFML9	LAFML8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

#### LAFMH

Bit:	15	14	13	12	11	10	9	8
	LAFMH7	LAFMH6	LAFMH5	—	—	—	LAFMH1	LAFMH0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	LAFMH15	LAFMH14	LAFMH13	LAFMH12	LAFMH11	LAFMH10	LAFMH9	LAFMH8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- LAFMH Bits 7 to 0 and 15 to 13—11-Bit Identifier Filter (LAFMH7 to 5, LAFMH15 to 8): Filter mask bits for the first 11 bits of the receive message identifier (for both standard and extended identifiers).



Bit x: LAFMHx	Description
0	Stored in MC0 and MD0 (receive-only mailbox) depending on bit match between MC0 message identifier and receive message identifier (Initial value)
1	Stored in MC0 and MD0 (receive-only mailbox) regardless of bit match between MC0 message identifier and receive message identifier

- LAFMH Bits 12 to 10—Reserved: These bits always read 0. The write value should always be 0.
- LAFMH Bits 9 and 8, LAFML bits 15 to 0—18-Bit Identifier Filter (LAFMH1, 0, LAFML15 to 0): Filter mask bits for the 18 bits of the receive message identifier (extended).

Bit x: LAFMHx LAFMLx	Description
0	Stored in MC0 and MD0 (receive-only mailbox) depending on bit match between MC0 message identifier and receive message identifier (Initial value)
1	Stored in MC0 and MD0 (receive-only mailbox) regardless of bit match between MC0 message identifier and receive message identifier

### 15.2.18 Message Control (MC0 to MC15)

The message control register sets (MC0 to MC15) consist of eight 8-bit readable/writable registers (MCx[1] to MCx[8]). The HCAN has 16 sets of these registers (MC0 to MC15).

The initial value of these registers is undefined, so they must be initialized (by writing 0 or 1).

#### MCx [1]

Bit:	7	6	5	4	3	2	1	0
					DLC3	DLC2	DLC1	DLC0
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

#### MCx [2]

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**MCx [3]**

Bit: 7 6 5 4 3 2 1 0

--	--	--	--	--	--	--	--

Initial value: — — — — — — — —  
 R/W: R/W R/W R/W R/W R/W R/W R/W R/W

**MCx [4]**

Bit: 7 6 5 4 3 2 1 0

--	--	--	--	--	--	--	--

Initial value: — — — — — — — —  
 R/W: R/W R/W R/W R/W R/W R/W R/W R/W

**MCx [5]**

Bit: 7 6 5 4 3 2 1 0

STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16
---------	---------	---------	-----	-----	--	----------	----------

Initial value: — — — — — — — —  
 R/W: R/W R/W R/W R/W R/W R/W R/W R/W

**MCx [6]**

Bit: 7 6 5 4 3 2 1 0

STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3
----------	---------	---------	---------	---------	---------	---------	---------

Initial value: — — — — — — — —  
 R/W: R/W R/W R/W R/W R/W R/W R/W R/W

**MCx [7]**

Bit: 7 6 5 4 3 2 1 0

EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0
---------	---------	---------	---------	---------	---------	---------	---------

Initial value: — — — — — — — —  
 R/W: R/W R/W R/W R/W R/W R/W R/W R/W

**MCx [8]**

Bit: 7 6 5 4 3 2 1 0

EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8
----------	----------	----------	----------	----------	----------	---------	---------

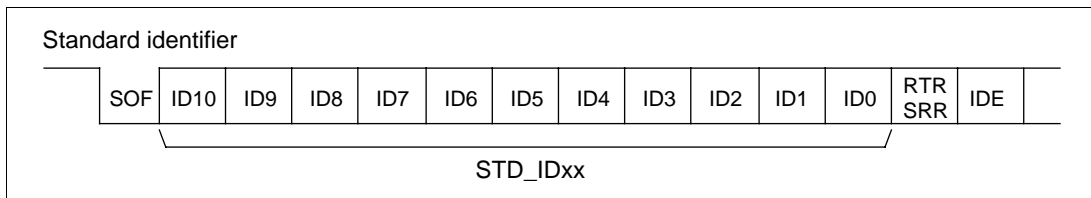
Initial value: — — — — — — — —  
 R/W: R/W R/W R/W R/W R/W R/W R/W R/W

- MCx[1] Bits 7 to 4—Reserved: The initial value of these bits is undefined; they must be initialized (by writing 0 or 1).
- MCx[1] Bits 3 to 0: Data Length Code (DLC3 to 0): These bits indicate the required length of data frames and remote frames.

Bit 3: DLC3	Bit 2: DLC2	Bit 1: DLC1	Bit 0: DLC0	Description
0	0	0	0	Data length = 0 bytes
			1	Data length = 1 byte
		1	0	Data length = 2 bytes
			1	Data length = 3 bytes
	1	0	0	Data length = 4 bytes
			1	Data length = 5 bytes
		1	0	Data length = 6 bytes
			1	Data length = 7 bytes
1	*	*	*	Data length = 8 bytes

\*: Don't care

- MCx[2] Bits 7 to 0—Reserved: The initial value of these bits is undefined; they must be initialized (by writing 0 or 1).
- MCx[3] Bits 7 to 0—Reserved: The initial value of these bits is undefined; they must be initialized (by writing 0 or 1).
- MCx[4] Bits 7 to 0—Reserved: The initial value of these bits is undefined; they must be initialized (by writing 0 or 1).
- MCx[6] Bits 7 to 0: Standard Identifier (STD\_ID10 to STD\_ID3)  
MCx[5] Bits 7 to 5: Standard Identifier (STD\_ID2 to STD\_ID0)  
These bits set the identifier (standard identifier) of data frames and remote frames.



**Figure 15.3 Standard Identifier**

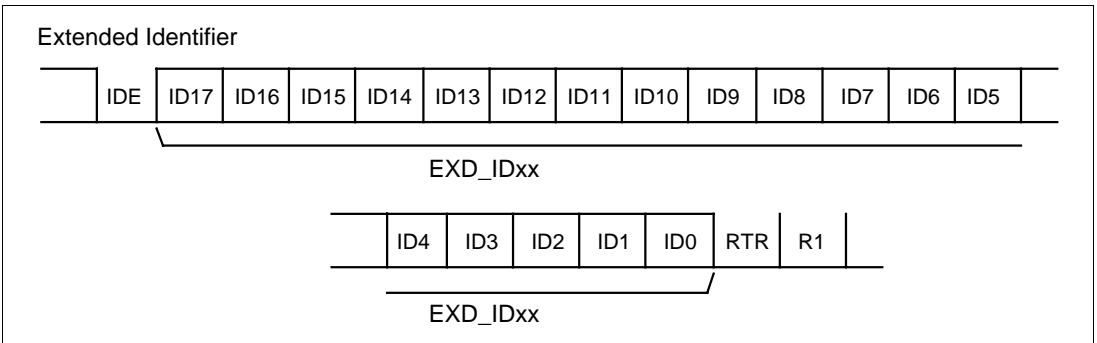
- MCx[5] Bit 4: Remote Transmission Request (RTR): Used to distinguish between data frames and remote frames.

Bit 4: RTR	Description
0	Data frame
1	Remote frame

- MCx[5] Bit 3: Identifier Extension (IDE): Used to distinguish between the standard format and extended format of data frames and remote frames.

Bit 3: IDE	Description
0	Standard format
1	Extended format

- MCx[5] Bit 2—Reserved: The initial value of this bit is undefined; it must be initialized (by writing 0 or 1).
- MCx[5] Bits 1 and 0: Extended Identifier (EXD\_ID17, EXD\_ID16)  
 MCx[8] Bits 7 to 0: Extended Identifier (EXD\_ID15 to EXD\_ID8)  
 MCx[7] Bits 7 to 0: Extended Identifier (EXD\_ID7 to EXD\_ID0)  
 These bits set the identifier (extended identifier) of data frames and remote frames.



**Figure 15.4 Extended Identifier**

## 15.2.19 Message Data (MD0 to MD15)

The message data register sets (MD0 to MD15) consist of eight 8-bit readable/writable registers (MDx[1] to MDx[8]). The HCAN has 16 sets of these registers (MD0 to MD15).

The initial value of these registers is undefined, so they must be initialized (by writing 0 or 1).

### MDx[1] Message Data 1

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### MDx[2] Message Data 2

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### MDx[3] Message Data 3

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### MDx[4] Message Data 4

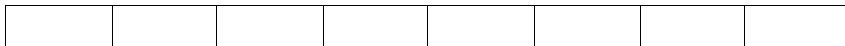
Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### MDx[5] Message Data 5

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### MDx[6] Message Data 6

Bit: 7 6 5 4 3 2 1 0

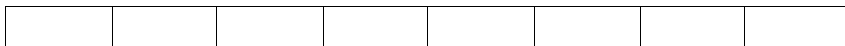


Initial value: — — — — — — — —

R/W: R/W R/W R/W R/W R/W R/W R/W R/W

### MDx[7] Message Data 7

Bit: 7 6 5 4 3 2 1 0



Initial value: — — — — — — — —

R/W: R/W R/W R/W R/W R/W R/W R/W R/W

### MDx[8] Message Data 8

Bit: 7 6 5 4 3 2 1 0



Initial value: — — — — — — — —

R/W: R/W R/W R/W R/W R/W R/W R/W R/W

## 15.3 Operation

### 15.3.1 Hardware Reset and Software Reset

There are two ways of resetting the HCAN: Hardware reset, software reset

**Hardware Reset (power-on reset or hardware/software standby):** The MCR reset request bit (MCR0) in MCR and the reset state bit (GSR3) in GSR within the HCAN are automatically set and initialization is performed. At the same time, all internal registers are initialized. However mailbox (RAM) contents are not initialized. A flowchart of this reset is shown in figure 15.5.

**Software Reset:** In normal operation, HCAN is initialized by setting the MCR reset request bit (MCR0) in MCR. With this kind of reset, if the CAN controller is performing a communication operation (transmission or reception), the initialization state is not entered until the message has been completed. During initialization, the reset state bit (GSR3) in GSR is set. In this kind of initialization, the error counters (TEC and REC) are initialized but other registers and RAM are not. A flowchart of this reset is shown in figure 15.6.

Hardware reset

MCR0 = 1 (automatic)

IRR0 = 1 (automatic)  
GSR3 = 1 (automatic)

Initialization of HCAN module

Clear IRR0  
HCAN port setting  
BCR setting  
MBCR setting  
Mailbox initialization  
Message transmission method initialization

MCR0 = 0

GSR3 = 0?

No

Yes

IMR setting (interrupt mask setting)  
MBIMR setting (interrupt mask setting)  
MC[x] setting (receive identifier setting)  
LAFM setting (receive identifier mask setting)

GSR3 = 0 & 11  
recessive bits received?

No

Yes

CAN bus communication enabled

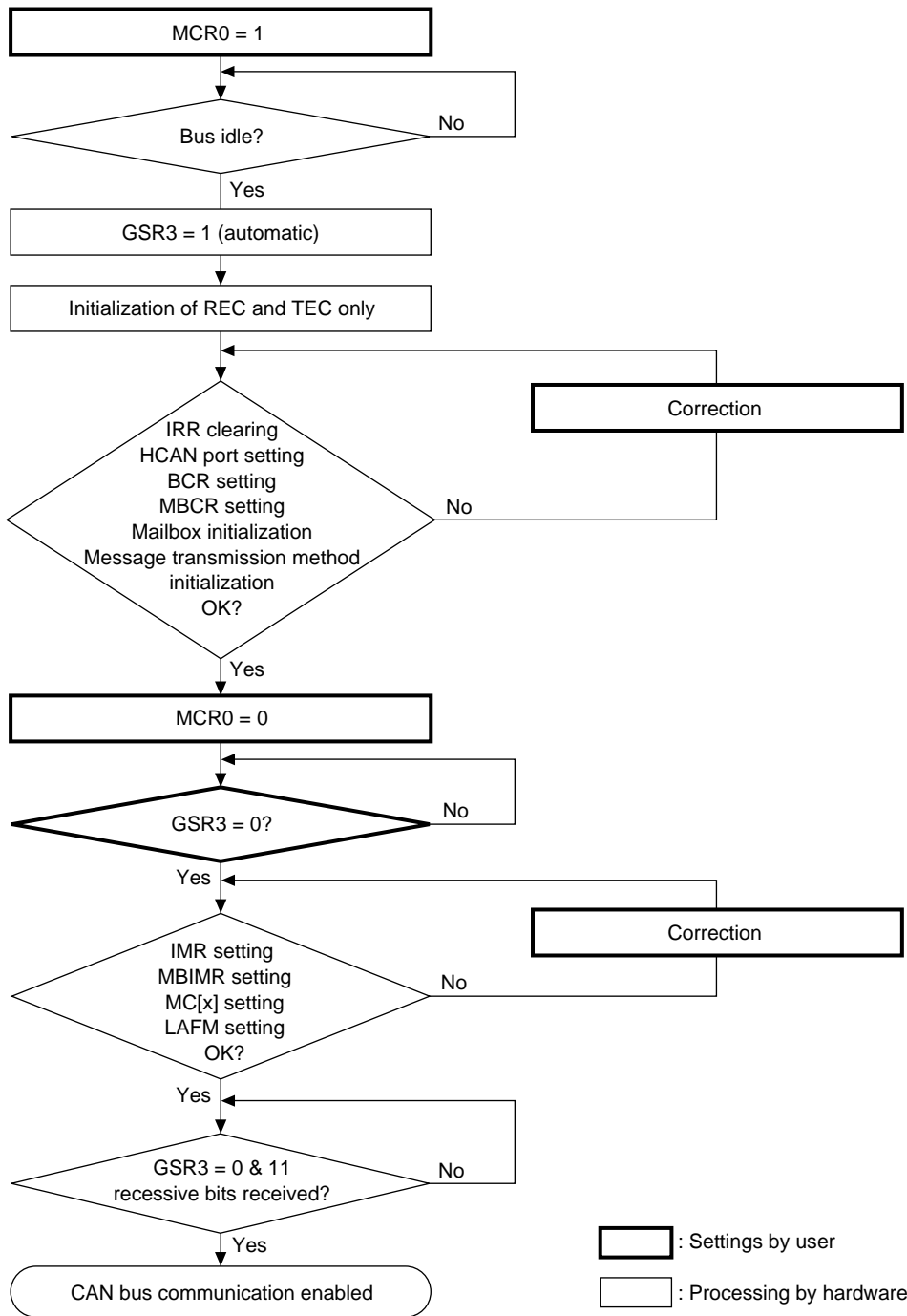
Bit configuration mode  
Period in which BCR, MBCR, etc.,  
are initialized

**▭** : Settings by user

**▭** : Processing by hardware

**Figure 15.5 Hardware Reset Flowchart**





**Figure 15.6 Software Reset Flowchart**

### 15.3.2 Initialization after a Hardware Reset

After a hardware reset, the following initialization processing should be carried out:

1. IRR0 clearing
2. HCAN pin port settings
3. Bit rate setting
4. Mailbox transmit/receive settings
5. Mailbox (RAM) initialization
6. Message transmission method setting

These initial settings must be made while the HCAN is in bit configuration mode. Configuration mode is a state in which the reset request bit (MCR0) in the master control register (MCR) is 1 and the reset status bit in the general status register (GSR) is also 1 ( $GSR3 = 1$ ). Configuration mode is exited by clearing the reset request bit in MCR to 0; when MCR0 is cleared to 0, the HCAN automatically clears the reset state bit (GSR3) in the general status register (GSR). The power-up sequence then begins, and communication with the CAN bus is possible as soon as the sequence ends. The power-up sequence consists of the detection of 11 consecutive recessive bits.

**IRR0 Clearing:** The reset interrupt flag (IRR0) is always set after a power-on reset or recovery from software standby mode. As an HCAN interrupt is initiated immediately when interrupts are enabled, IRR0 should be cleared.

**HCAN Pin Port Settings:** HCAN pin port settings must be made during or before bit configuration. Refer to the section 18, Pin Function Controller (PFC), for details of the setting method.

**Bit Rate Settings:** As bit rate settings, a baud rate setting and bit timing setting must be made each time a CAN node begins communication. The baud rate and bit timing settings are made in the bit configuration register (BCR).

- Notes:
1. BCR can be written to at all times, but should only be modified in configuration mode.
  2. Settings should be made so that all CAN controllers connected to the CAN bus have the same baud rate and bit width.
  3. Limits for the settable variables (TSEG1, TSEG2, BRP, sample point, and SJW) are shown in table 15.4.

**Table 15.4 BCR Setting Limits**

Name	Abbreviation	Min. Value	Max. Value	Unit
Time segment 1	TSEG1	4	16	TQ
Time segment 2	TSEG2	2	8	TQ
Baud rate prescaler	BRP	2	128	System clock
Sample point	SAM	1	3	Point
Re-synchronization jump width	SJW	1	4	TQ

#### Settable Variable Limits

- The bit width consists of the total of the settable time quanta (TQ). TQ (number of system clocks) is determined by the baud rate prescaler (BRP).

$$TQ = (2 * (BRP + 1)) / (f_{CLK})$$

$$f_{CLK} = P\phi$$

- The minimum value of SJW is stipulated in the CAN specifications.

$$4 \geq SJW \geq 1$$

- The minimum value of TSEG1 is stipulated in the CAN specifications.

$$TSEG1 \geq TSEG2$$

- The minimum value of TSEG2 is stipulated in the CAN specifications.

$$TSEG2 \geq (1 + SJW)$$

The following formula is used to calculate the baud rate.

$$\text{Bit rate [b/s]} = \frac{f_{CLK}}{2 \times (BRP + 1) \times (3 + TSEG1 + TSEG2)}$$

Note:  $f_{CLK} = P\phi$  (peripheral clock:  $\phi/2$ )  
The BCR values are used for BRP, TSEG1, and TSEG2.

Example: With a 1 Mb/s baud rate and a 40 MHz input clock:

$$1 \text{ Mb/s} = \frac{20 \text{ MHz}}{2 \times (0 + 1) \times (3 + 4 + 3)}$$

	Set Values	Actual Values
$f_{\text{CLK}}$	40 MHz/2	—
BRP	0 (B'000000)	System clock $\times$ 2
TSEG1	4 (B'0100)	5TQ
TSEG2	3 (B'011)	4TQ

**Mailbox Transmit/Receive Settings:** HCAN0 and HCAN1 each have 16 mailboxes. Mailbox 0 is receive-only, while mailboxes 1 to 15 can be set for transmission or reception. Mailboxes that can be set for transmission or reception must be designated either for transmission use or for reception use before communication begins. The Initial status of mailboxes 1 to 15 is for transmission (while mailbox 0 is for reception only). Mailbox transmit/receive settings are not initialized by a software reset.

- Setting for transmission

Transmit mailbox setting (mailboxes 1 to 15)

Clearing a bit to 0 in the mailbox configuration register (MBCR) designates the corresponding mailbox for transmission use. After a reset, mailboxes are initialized for transmission use, so this setting is not necessary.

- Setting for reception

Transmit/receive mailbox setting (mailboxes 1 to 15)

Setting a bit to 1 in the mailbox configuration register (MBCR) designates the corresponding mailbox for reception use. When setting mailboxes for reception, to improve message transmission efficiency, high-priority messages should be set in low-to-high mailbox order (priority order: mailbox 1 (MCx[1]) > mailbox 15 (MCx[15])).

- Receive-only mailbox (mailbox 0)

No setting is necessary, as this mailbox is always used for reception.

**Mailbox (Message Control/Data (MCx[x], MDx[x]) Initial Settings:** After power is supplied, all registers and RAM (message control/data, control registers, status registers, etc.) are initialized. Message control/data (MCx[x], MDx[x]) only are in RAM, and so their values are undefined. Initial values must therefore be set in all the mailboxes (by writing 0s or 1s).

**Setting the Message Transmission Method:** Either of the following message transmission methods can be selected with the message transmission method bit (MCR2) in the master control register (MCR):

1. Transmission order determined by mailbox number priority
2. Transmission order determined by message identifier priority

When the mailbox number priority method is selected, if a number of messages are designated as waiting for transmission (TXPR = 1), messages are stored in the transmit buffer in low-to-high mailbox order (priority order: mailbox 1 > 15). CAN bus arbitration is then carried out for the messages in the transmit buffer, and message transmission is performed when the bus is acquired.

When the message identifier priority method is selected, if a number of messages are designated as waiting for transmission (TXPR = 1), the message with the highest priority set in the message identifier (MCx[5] to MCx[8]) is stored in the transmit buffer. CAN bus arbitration is then carried out for the message in the transmit buffer, and message transmission is performed when the transmission right is acquired. When the TXPR bit is set, internal arbitration is performed again, and the highest-priority message is found and stored in the transmit buffer.

### 15.3.3 Transmit Mode

Message transmission is performed using mailboxes 1 to 15. The transmission procedure is described below, and a transmission flowchart is shown in figure 15.7.

1. Initialization (after hardware reset only)
  - a. Clearing of IRR0 bit in interrupt register (IRR)
  - b. HCAN pin port settings
  - c. Bit rate settings
  - d. Mailbox transmit/receive settings
  - e. Mailbox initialization
  - f. Message transmission method setting
2. Interrupt and transmit data settings
  - a. Interrupt setting
  - b. Arbitration field setting
  - c. Control field setting
  - d. Data field setting
3. Message transmission and interrupts
  - a. Message transmission wait
  - b. Message transmission completion and interrupt
  - c. Message transmission abort
  - d. Message retransmission

**Initialization (after Hardware Reset Only):** These settings should be made while the HCAN is in bit configuration mode.

1. IRR0 clearing

The reset interrupt flag (IRR0) is always set after a power-on reset or recovery from software standby mode. As an HCAN interrupt is initiated immediately when interrupts are enabled, IRR0 should be cleared.

2. HCAN pin port settings

To prevent erroneous identification of CAN bus data, HCAN pin port settings should be made first. See section 15.3.2, HCAN Pin Port Settings, and section 18, Pin Function Controller, for details.

3. Bit rate settings

Set values relating to the CAN bus communication speed and re-synchronization. See section 15.3.2, Bit Rate Settings, for details.

4. Mailbox transmit/receive settings

Mailbox transmit/receive settings should be made in advance. A total of 30 mailbox can be set for transmission or reception (mailboxes 1 to 15 in HCAN0 and HCAN1). To set a mailbox for transmission, clear the corresponding bit to 0 in the mailbox configuration register (MBCR). See section 15.3.2, Mailbox Transmit/Receive Settings, for details.

5. Mailbox initialization

As message control/data registers (MCx[x], MDx[x]) are configured in RAM, their initial values after powering on are undefined, and so bit initialization is necessary. Write 0s or 1s to the mailboxes. See section 15.3.2, Mailbox Transmit/Receive Settings, for details.

6. Message transmission method setting

Set the transmission method for mailboxes designated for transmission. The following two transmission methods can be used. See section 15.3.2, Setting the Message Transmission Method, for details.

- a. Transmission order determined by message identifier priority
- b. Transmission order determined by mailbox number priority

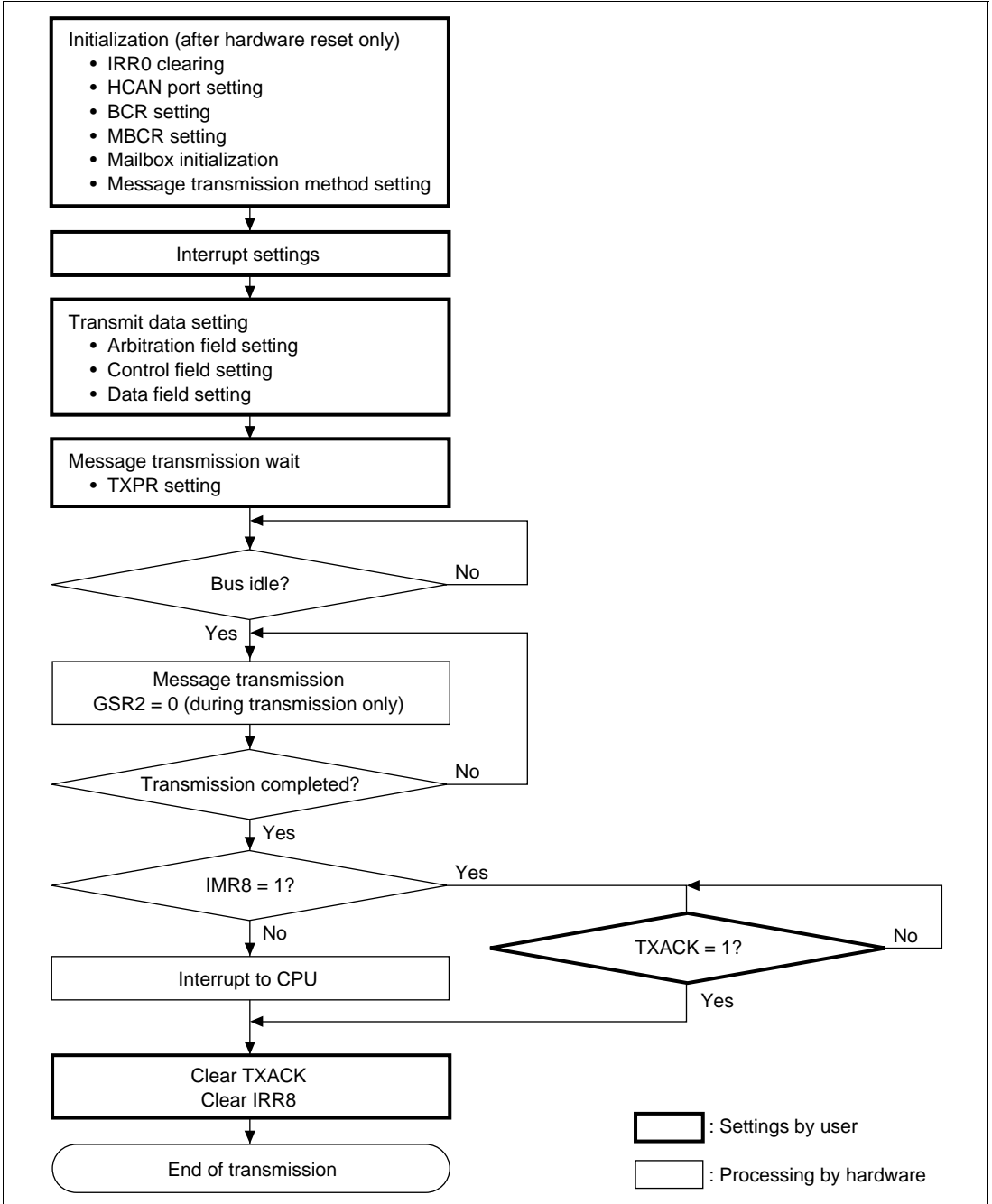


Figure 15.7 Transmission Flowchart

**Interrupt and Transmit Data Settings:** When mailbox initialization is finished, CPU interrupt source settings and data settings must be made. Interrupt source settings are made in the mailbox interrupt mask register (MBIMR) and interrupt mask register (IMR), while transmit data settings are made by writing the following three kinds of necessary data in the message control registers (MCx[1] to MCx[8]) and message data registers (MDx[1] to MDx[8]).

1. CPU interrupt source settings

Transmission acknowledge and transmission abort acknowledge interrupts can be masked for individual mailboxes in the mailbox interrupt mask register (MBIMR). Interrupt register (IRR) interrupts can be masked in the interrupt mask register (IMR).

2. Arbitration field

In the arbitration field, the 11-bit identifier (STD\_ID0 to STD\_ID10) and RTR bit (standard format) or 29-bit identifier (STD\_ID0 to STD\_ID10, EXT\_ID0 to EXT\_ID17) and IDE.RTR bit (extended format) are set. The registers to be set are MCx[5] to MCx[8].

3. Control field

In the control field, the byte length of the data to be transmitted is set in DLC0 to DLC3. The register to be set is MCx[1].

4. Data field

In the data field, the data to be transmitted is set in byte units in the range of 0 to 8 bytes. The registers to be set are MDx[1] to MDx[8].

The number of bytes in the data actually transmitted depends on the data length code (DLC) in the control field. If a value exceeding the value set in DLC is set in the data field, only the number of bytes set in DLC will actually be transmitted.



## Message Transmission and Interrupts:

### 1. Message transmission wait

If message transmission is to be performed after completion of the message control (MCx[1] to MCx[8]) and message data (MDx[1] to MDx[8]) settings, transmission is started by setting the corresponding mailbox transmit wait bit (TXPR1 to TXPR15) to 1 in the transmit wait register (TXPR). The following two transmission methods can be used:

- a. Transmission order determined by mailbox number priority
- b. Transmission order determined by message identifier priority

When the message identifier priority method is selected, if a number of messages are designated as waiting for transmission (TXPR = 1), messages are stored in the transmit buffer in low-to-high mailbox order (priority order: mailbox 1 > mailbox 15). CAN bus arbitration is then carried out for the messages in the transmit buffer, and message transmission is performed when the bus is acquired.

When the mailbox number priority method is selected, if a number of messages are designated as waiting for transmission (TXPR = 1), the message with the highest priority set in the message identifier (MCx[5] to MCx[8]) is stored in the transmit buffer. CAN bus arbitration is then carried out for the message in the transmit buffer, and message transmission is performed when the transmission right is acquired. When the TXPR bit is set, internal arbitration is performed again, the highest-priority message is found and stored in the transmit buffer, CAN bus arbitration is carried out in the same way, and message transmission is performed when the transmission right is acquired.

### 2. Message transmission completion and interrupt

When a message is transmitted error-free using the above procedure, The corresponding acknowledge bit (TXACK1 to TXACK15) in the transmit acknowledge register (TXACK) and transmit wait bit (TXPR1 to TXPR15) in the transmit wait register (TXPR) are automatically initialized. If the corresponding bit (MBIMR1 to MBIMR15) in the mailbox interrupt mask register (MBIMR) and the mailbox empty interrupt bit (IRR8) in the interrupt mask register (IMR) are set to the interrupt enable value at this time, an interrupt can be sent to the CPU.

### 3. Message transmission cancellation

Transmission cancellation can be specified for a message stored in a mailbox as a transmit wait message. A transmit wait message is canceled by setting the bit for the corresponding mailbox (TXCR1 to TXCR15) to 1 in the transmit cancel register (TXCR). When cancellation is executed, the transmit wait register (TXPR) is automatically reset, and the corresponding bit is set to 1 in the abort acknowledge register (ABACK). An interrupt can be requested. If the corresponding bit (MBIMR1 to MBIMR15) in the mailbox interrupt mask register (MBIMR) and the mailbox empty interrupt bit (IRR8) in the interrupt mask register (IMR) are set to the interrupt enable value at this time, an interrupt can be sent to the CPU.

However, a transmit wait message cannot be canceled at the following times:

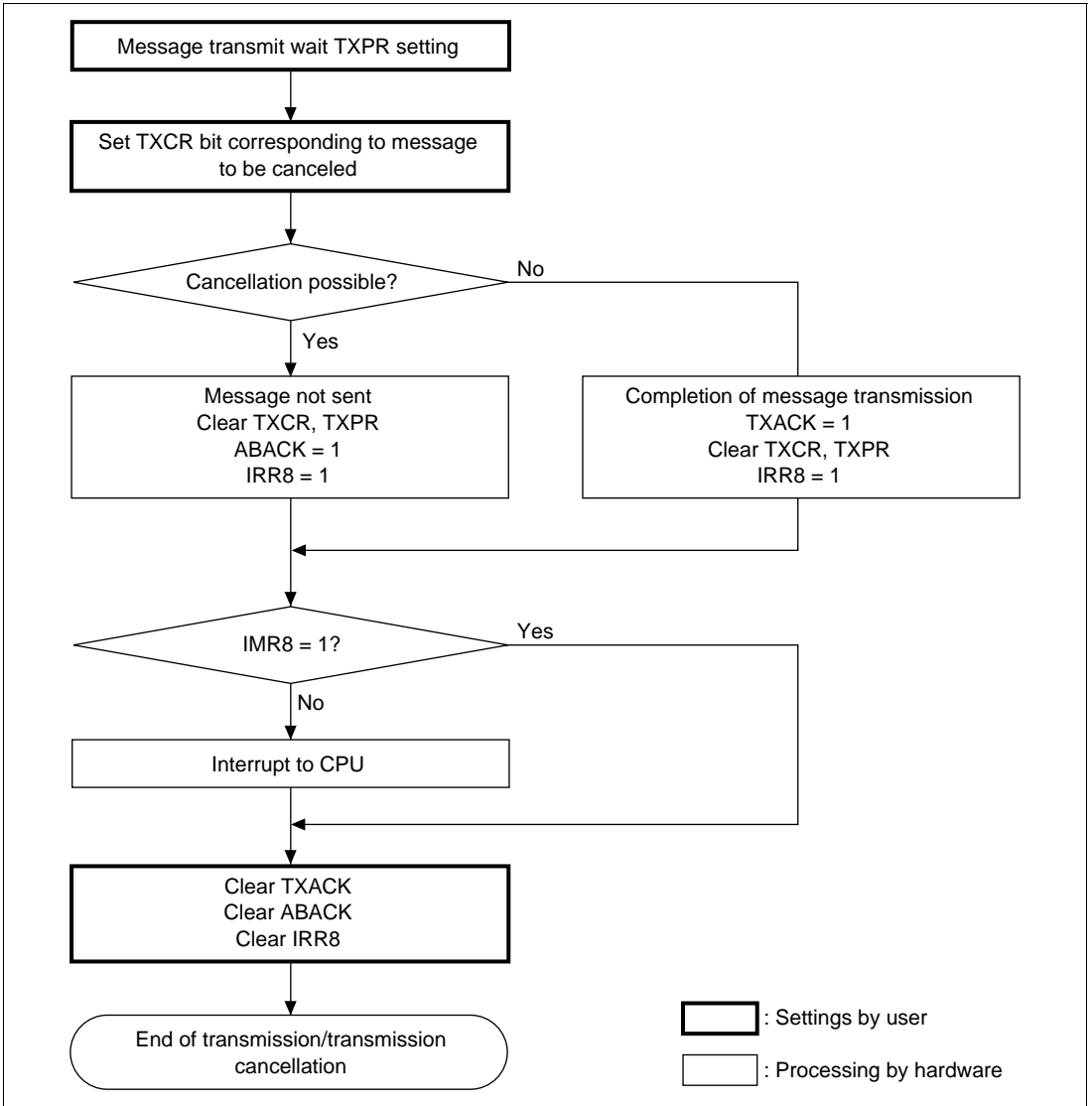
- a. During internal arbitration or CAN bus arbitration
- b. During data frame or remote frame transmission

Also, transmission cannot be canceled by clearing the transmit wait register (TXPR). Figure 15.8 shows a flowchart of transmit message cancellation.

#### 4. Message retransmission

If transmission of a transmit message is aborted in the following cases, the message is retransmitted automatically:

- a. CAN bus arbitration failure (failure to acquire the bus)
- b. Error during transmission (bit error, stuff error, CRC error, frame error, ACK error)



**Figure 15.8 Transmit Message Cancellation Flowchart**

### 15.3.4 Receive Mode

Message reception is performed using mailboxes 0 and 1 to 15. The reception procedure is described below, and a reception flowchart is shown in figure 15.9.

1. Initialization (after hardware reset only)
  - a. Clearing of IRR0 bit in interrupt register (IRR)
  - b. HCAN pin port settings
  - c. Bit rate settings
  - d. Mailbox transmit/receive settings
  - e. Mailbox initialization
2. Interrupt and receive message settings
  - a. Interrupt setting
  - b. Arbitration field setting
  - c. Local acceptance filter mask (LAFM) settings
3. Message reception and interrupts
  - a. Message reception CRC check
  - b. Data frame reception
  - c. Remote frame reception
  - d. Unread message reception

**Initialization (after Hardware Reset Only):** These settings should be made while the HCAN is in bit configuration mode.

1. IRR0 clearing

The reset interrupt flag (IRR0) is always set after a power-on reset or recovery from software standby mode. As an HCAN interrupt is initiated immediately when interrupts are enabled, IRR0 should be cleared.

2. HCAN pin port settings

To prevent erroneous identification of CAN bus data, HCAN pin port settings should be made first. See section 15.3.2, HCAN Pin Port Settings, and section 18, Pin Function Controller, for details.

3. Bit rate settings

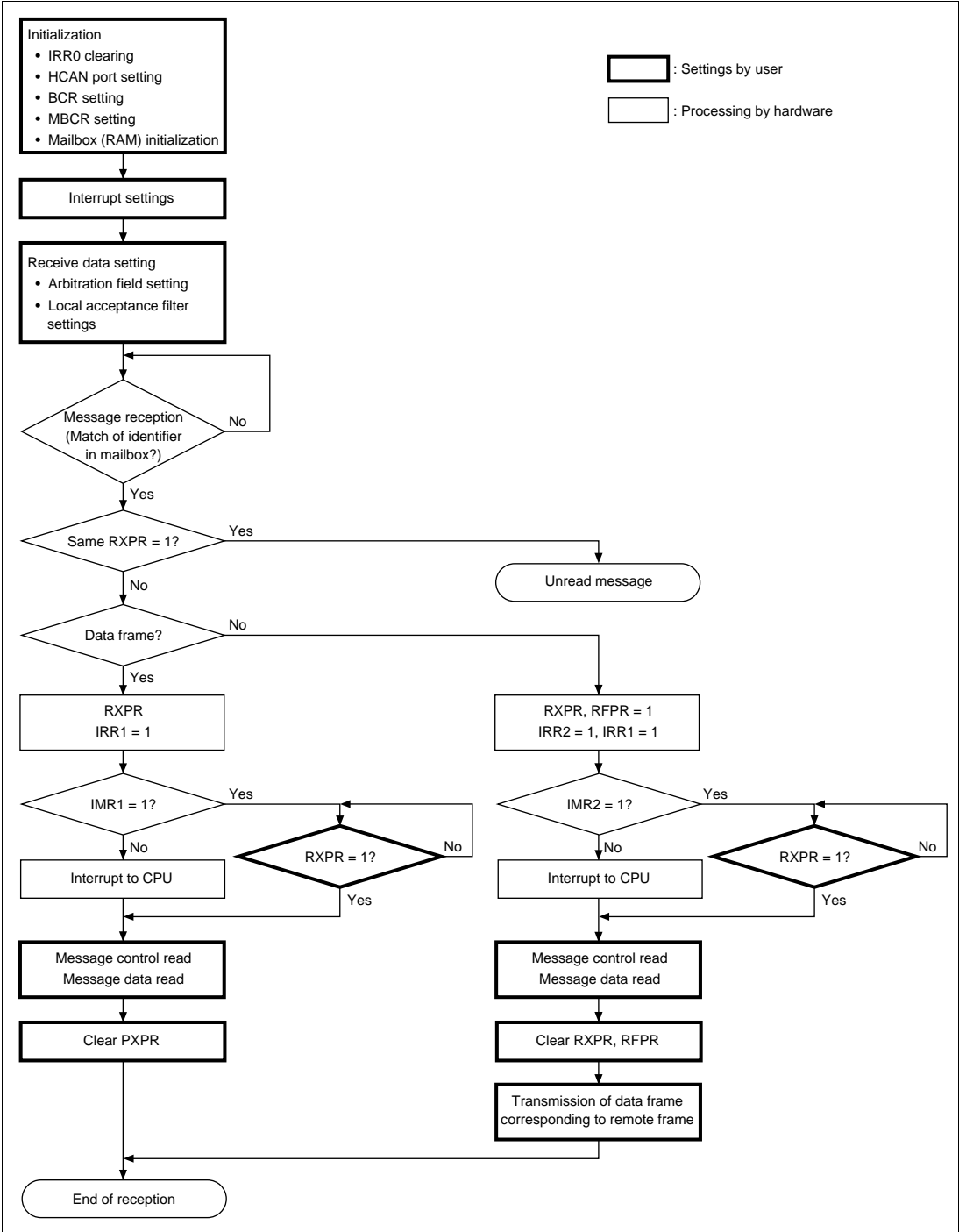
Set values relating to the CAN bus communication speed and re-synchronization. See section 15.3.2, Bit Rate Settings, for details.

4. Mailbox transmit/receive settings

Each channel has one receive-only mailbox (mailbox 0) and 15 mailboxes that can be set for reception. Thus a total of 32 mailboxes can be used for reception. To set a mailbox for reception, set the corresponding bit to 1 in the mailbox configuration register (MBCR). The initial setting for mailboxes is 0, designating transmission use. See section 15.3.2, Mailbox Transmit/Receive Settings, for details.

5. Mailbox (RAM) initialization

As message control/data registers (MCx[x], MDx[x]) are configured in RAM, their initial values after powering on are undefined, and so bit initialization is necessary. Write 0s or 1s to the mailboxes. See section 15.3.2, Mailbox (Message Control/Data (MCx[x], MDx[x]) Initial Settings, for details.



**Figure 15.9 Reception Flowchart**

**Interrupt and Receive Message Settings:** When mailbox initialization is finished, CPU interrupt source settings and receive message specifications must be made. Interrupt source settings are made in the mailbox interrupt mask register (MBIMR) and interrupt mask register (IMR). To receive a message, the identifier must be set in advance in the message control (MCx[1] to MCx[8]) for the receiving mailbox. When a message is received, all the bits in the receive message identifier are compared, and if a 100% match is found, the message is stored in the matching mailbox. Mailbox 0 (MC0[x], MD0[x]) has a local acceptance filter mask (LAFM) that allows Don't Care settings to be made.

#### 1. CPU interrupt source settings

When transmitting, transmission acknowledge and transmission abort acknowledge interrupts can be masked for individual mailboxes in the mailbox interrupt mask register (MBIMR).

When receiving, data frame and remote frame receive wait interrupts can be masked. Interrupt register (IRR) interrupts can be masked in the interrupt mask register (IMR).

#### 2. Arbitration field setting

In the arbitration field, the identifier (STD\_ID0 to STD\_ID10, EXT\_ID0 to EXT\_ID17) of the message to be received is set. If all the bits in the set identifier do not match, the message is not stored in a mailbox.

Example: Mailbox 1    010\_1010\_1010 (standard identifier)

Only one kind of message identifier can be received by MB1

Identifier 1:    010\_1010\_1010

#### 3. Local acceptance filter mask (LAFM) setting

The local acceptance filter mask is provided for mailbox 0 (MC0[x], MD0[x]) only, enabling a Don't Care specification to be made for all bits in the received identifier. This allows various kinds of messages to be received.

Example: Mailbox 0    010\_1010\_1010 (standard identifier)

LAFM                000\_0000\_0011 (0: Care, 1: Don't Care)

A total of four kinds of message identifiers can be received by MB0

Identifier 1:    010\_1010\_1000

Identifier 2:    010\_1010\_1001

Identifier 3:    010\_1010\_1010

Identifier 4:    010\_1010\_1011

## Message Reception and Interrupts:

### 1. Message reception CRC check

When a message is received, a CRC check is performed automatically (by hardware). If the result of the CRC check is normal, ACK is transmitted in the ACK field irrespective of whether or not the message can be received.

### 2. Data frame reception

If the received message is confirmed to be error-free by the CRC check, etc., the identifier in the mailbox (and also LAFM in the case of mailbox 0 only) and the identifier of the receive message are compared, and if a complete match is found, the message is stored in the mailbox. The message identifier comparison is carried out on each mailbox in turn, starting with mailbox 0 and ending with mailbox 15. If a complete match is found, the comparison ends at that point, the message is stored in the matching mailbox, and the corresponding receive complete bit (RXPR0 to RXPR15) is set in the receive complete register (RXPR). However, when a mailbox 0 LAFM comparison is carried out, even if the identifier matches, the mailbox comparison sequence does not end at that point, but continues with mailbox 1 and then the remaining mailboxes. It is therefore possible for a message matching mailbox 0 to be received by another mailbox (however, the same message cannot be stored in more than one of mailboxes 1 to 15). If the corresponding bit (MBIMR0 to MBIMR15) in the mailbox interrupt mask register (MBIMR) and the receive message interrupt mask (IMR1) in the interrupt mask register (IMR) are set to the interrupt enable value at this time, an interrupt can be sent to the CPU.

### 3. Remote frame reception

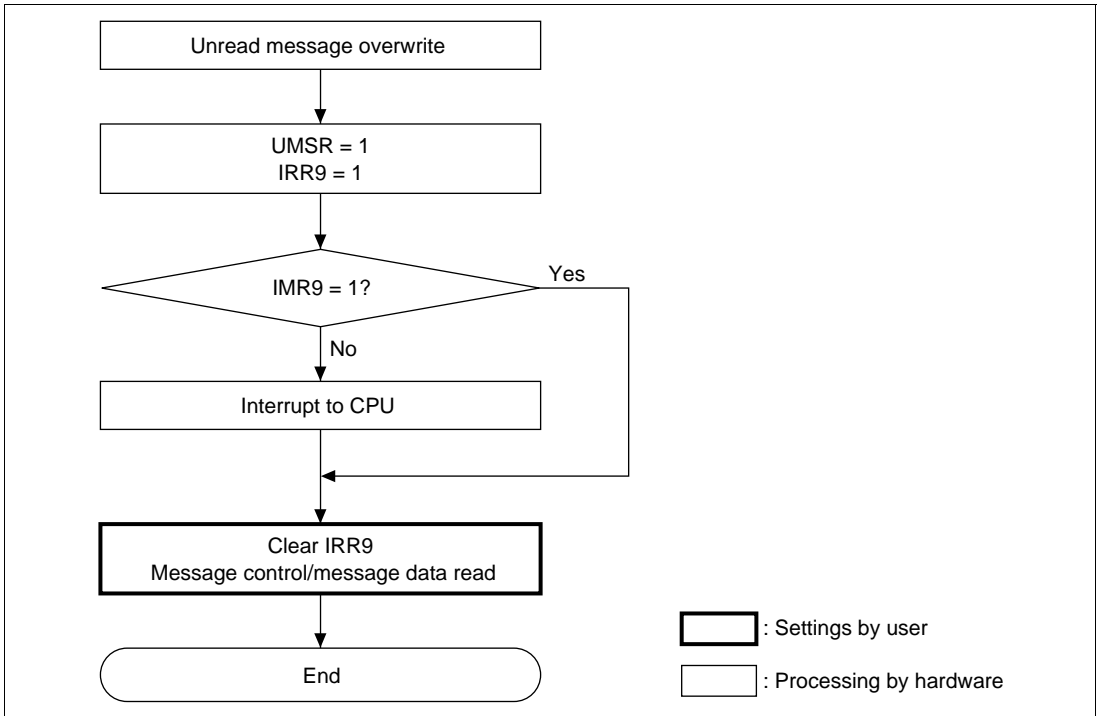
Two kinds of messages—data frames and remote frames—can be stored in mailboxes. A remote frame differs from a data frame in that the remote reception request bit (RTR) in the message control register (MC[x]5) and the data field are 0 bytes. The data length to be returned in a data frame must be stored in the data length code (DLC) in the control field.

When a remote frame (RTR = recessive) is received, the corresponding bit is set in the remote request wait register (RFPR). If the corresponding bit (MBIMR0 to MBIMR15) in the mailbox interrupt mask register (MBIMR) and the remote frame request interrupt mask (IRR2) in the interrupt mask register (IMR) are set to the interrupt enable value at this time, an interrupt can be sent to the CPU.



#### 4. Unread message reception

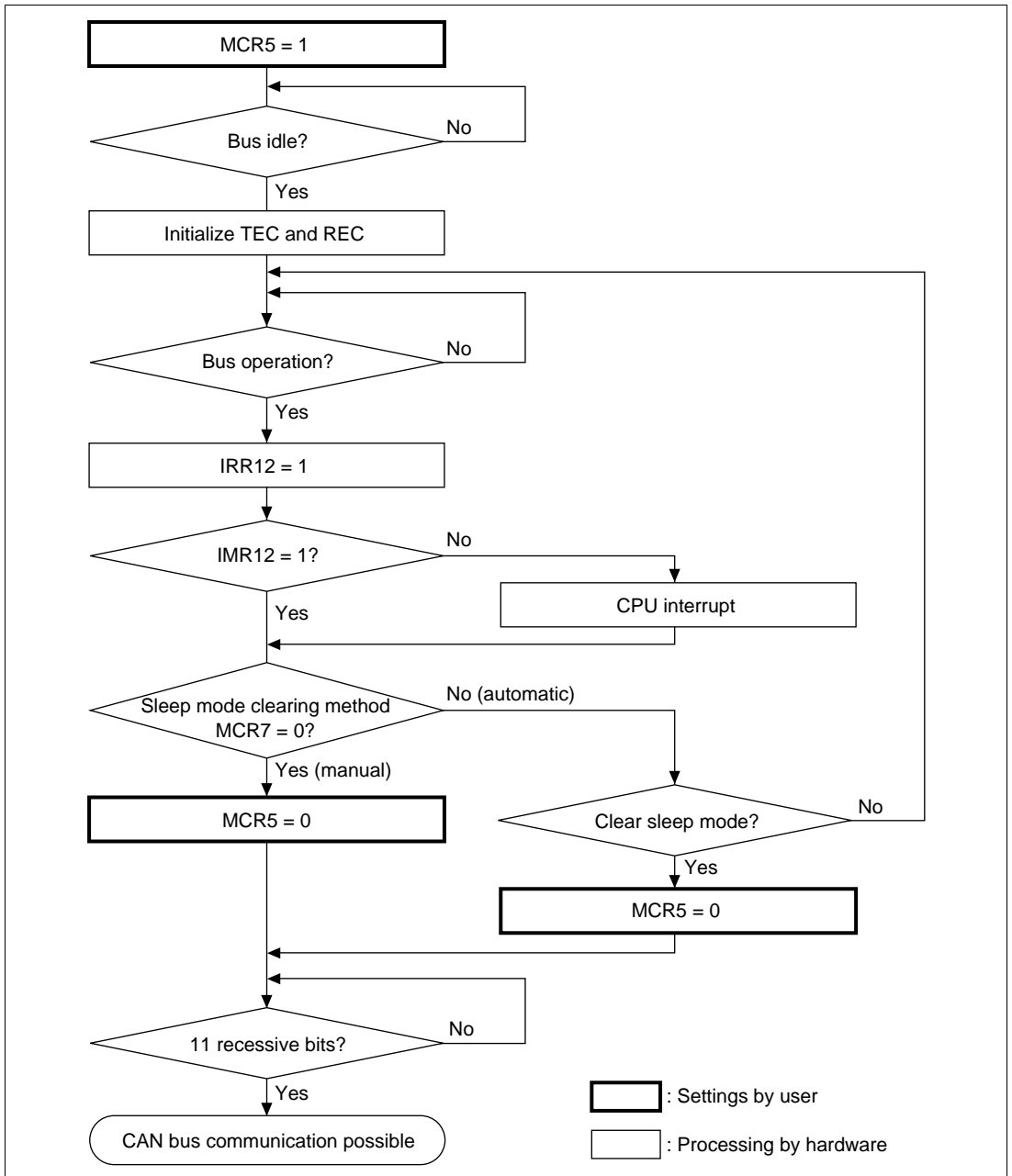
When the identifier in a mailbox matches a receive message, the message is stored in the mailbox. If a message overwrite occurs before the CPU reads the message, the corresponding bit (UMSR0 to UMSR15) is set in the unread message register (UMSR). In overwriting of an unread message, when a new message is received before the corresponding bit in the receive complete register (RXPR) has been cleared, the unread message register (UMSR) is set. If the unread interrupt flag (IRR9) in the interrupt mask register (IMR) is set to the interrupt enable value at this time, an interrupt can be sent to the CPU. Figure 15.10 shows a flowchart of unread message overwriting.



**Figure 15.10 Unread Message Overwrite Flowchart**

### 15.3.5 HCAN Sleep Mode

The HCAN is provided with an HCAN sleep mode that places the HCAN module in the sleep state to reduce current dissipation. Figure 15.11 shows a flowchart of the HCAN sleep mode.



**Figure 15.11 HCAN Sleep Mode Flowchart**

HCAN sleep mode is entered by setting the HCAN sleep mode bit (MCR5) to 1 in the master control register (MCR). If the CAN bus is operating, the transition to HCAN sleep mode is delayed until the bus becomes idle.

Either of the following methods of clearing HCAN sleep mode can be selected by making a setting in the MCR7 bit.

1. Clearing by software
2. Clearing by CAN bus operation

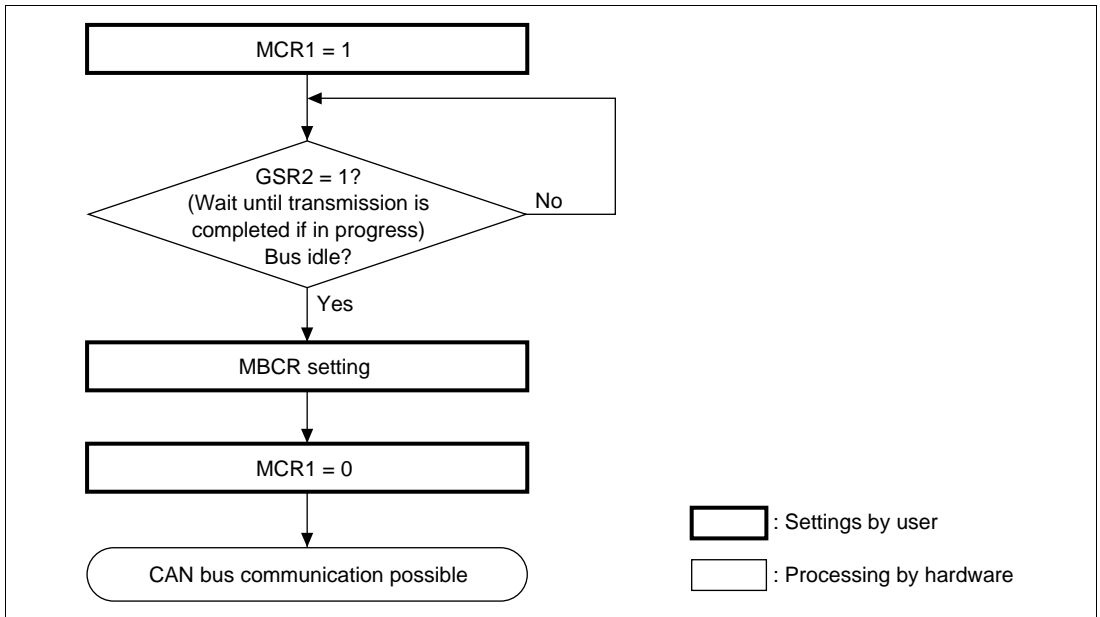
Eleven recessive bits must be received after HCAN sleep mode is cleared before CAN bus communication is enabled again.

**Clearing by Software:** Clearing by software is performed by having the CPU write 0 to MCR5.

**Clearing by CAN Bus Operation:** Clearing by CAN bus operation occurs automatically when the CAN bus performs an operation and this change is detected. In this case, the first message is not received in the message box; normal reception starts with the second message. When a change is detected on the CAN bus in HCAN sleep mode, the bus operation interrupt flag (IRR12) is set in the interrupt register (IRR). If the bus interrupt mask (IMR12) in the interrupt mask register (IMR) is set to the interrupt enable value at this time, an interrupt can be sent to the CPU.

### 15.3.6 HCAN Halt Mode

The HCAN halt mode is provided to enable mailbox settings to be changed without performing an HCAN hardware or software reset. Figure 15.12 shows a flowchart of the HCAN halt mode.



**Figure 15.12 HCAN Halt Mode Flowchart**

HCAN halt mode is entered by setting the halt request bit (MCR1) to 1 in the master control register (MCR). If the CAN bus is operating, the transition to HCAN halt mode is delayed until the bus becomes idle.

HCAN halt mode is cleared by clearing MCR1 to 0.

### 15.3.7 Interrupt Interface

There are 12 interrupt sources for each HCAN channel. Four independent interrupt vectors are assigned to each channel. Table 15.5 lists the HCAN interrupt sources.

With the exception of the power-on reset processing vector (IRR0), these sources can be masked. Masking is implemented using the mailbox interrupt mask register (MBIMR) and interrupt mask register (IMR).

**Table 15.5 HCAN Interrupt Sources**

Channel	IPR Bits	Vector	Vector Number	IRR Bit	Description
HCAN	IPRL (11 to 8)  (initial value)	ERS	220	IRR5	Error passive interrupt (TEC $\geq$ 128 or REC $\geq$ 128)
				IRR6	Bus off interrupt (TEC $\geq$ 256)
	OVR	221	IRR0	Power-on reset processing interrupt	
			IRR2	Remote frame reception interrupt	
			IRR3	Error warning interrupt (TEC $\geq$ 96)	
			IRR4	Error warning interrupt (REC $\geq$ 96)	
			IRR7	Overload frame transmission interrupt/bus off recovery interrupt (11 recessive bits $\times$ 128 times)	
			IRR9	Unread message overwrite interrupt	
	RM0	222	IRR1	Mailbox 0 message reception interrupt	
			IRR1	Mailbox 1 to 15 message reception interrupt	
	SLE0	223	IRR8	Message transmission/cancellation interrupt	

### 15.3.8 DMAC Interface

The DMAC can be activated by reception of a message in HCAN's mailbox 0. When DMAC transfer ends after DMAC activation has been set, the RXPR0 and RFPR0 flags are acknowledge signal automatically. An interrupt request due to a receive interrupt from the HCAN cannot be sent to the CPU in this case. Figure 15.13 shows a DMAC transfer flowchart.

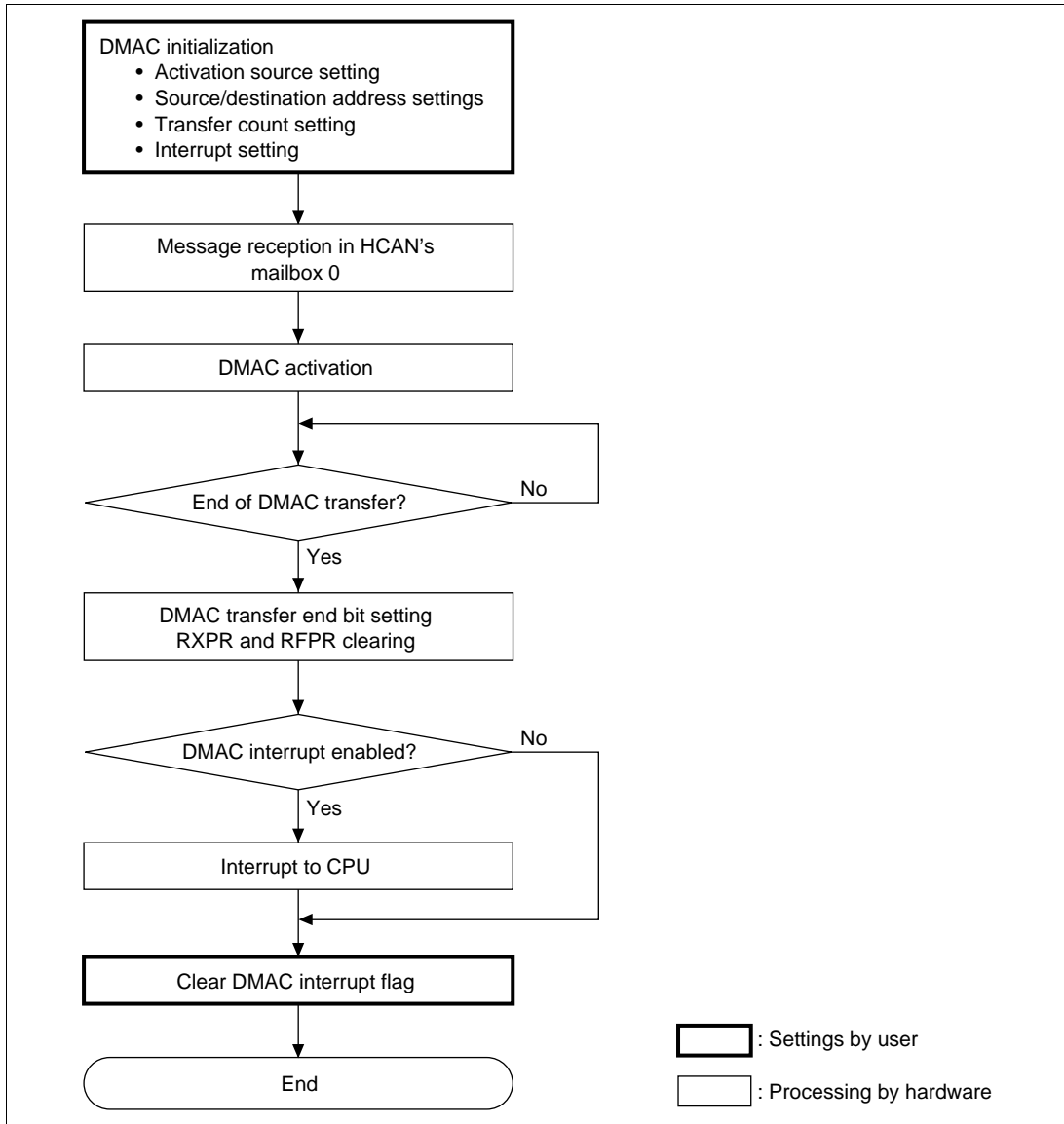


Figure 15.13 DMAC Transfer Flowchart

# 15.4 CAN Bus Interface

A bus transceiver IC is necessary to connect the SH7052F/SH7053F/SH7054F chip to a CAN bus. A Philips PCA82C250 transceiver IC, or compatible device, is recommended. Figure 15.14 shows a sample connection diagram.

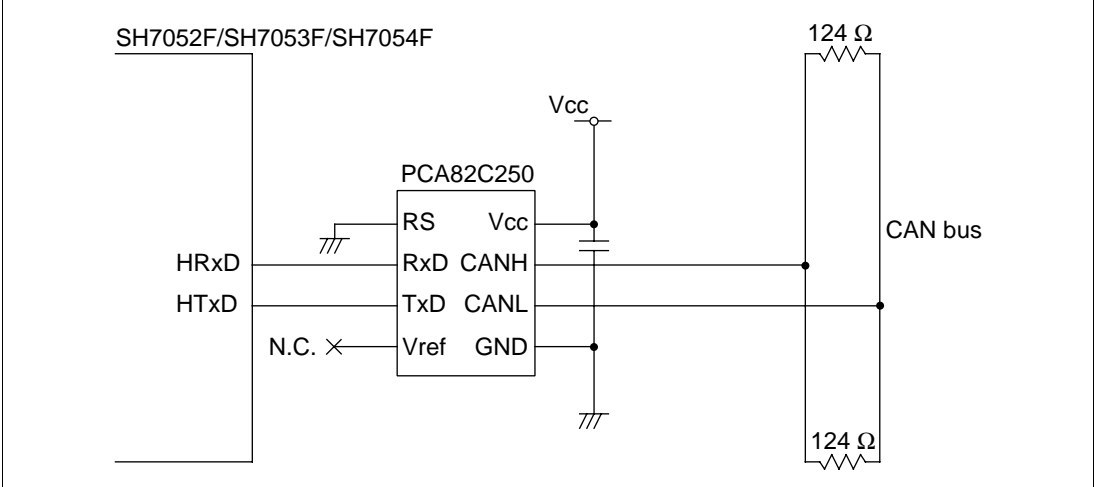


Figure 15.14 Example of High-Speed Interface Using PCA82C250

## 15.5 Usage Notes

### 1. Reset

The HCAN is reset by a power-on reset, and in hardware standby mode and software standby mode. All the registers are initialized in a reset, but mailboxes (message control (MCx[x])/message data (MDx[x])) are not. However, after powering on, mailboxes (message control (MCx[x])/message data (MDx[x])) are initialized, and their values are undefined. Therefore, mailbox initialization must always be carried out after a power-on reset or a transition to hardware standby mode or software standby mode. The reset interrupt flag (IRR0) is always set after a power-on reset or recovery from software standby mode. As this bit cannot be masked in the interrupt mask register (IMR), if HCAN interrupt enabling is set in the interrupt controller without clearing the flag, an HCAN interrupt will be initiated immediately. IRR0 should therefore be cleared during initialization.

### 2. HCAN sleep mode

The bus operation interrupt flag (IRR12) in the interrupt register (IRR) is set by bus operation in HCAN sleep mode. Therefore, this flag is not used by the HCAN to indicate sleep mode release. Also note that the reset status bit (GSR3) in the general status register (GSR) is set in sleep mode.

### 3. Port settings

Port settings must be made with the PFC before the HCAN begins CAN bus communication. When using the two HCAN pins in a 2-channel/32-buffer configuration (wired-AND), set the other two HCAN pin locations as non-HCAN.

### 4. DMAC activation

When the DMAC is activated automatically by reception of a message in HCAN0's mailbox 0 (receive-only mailbox), a signal is not sent to the INTC.

### 5. Interrupts

When the mailbox interrupt mask register (MBIMR) is set, the interrupt register (IRR8.2.1) is not set by reception completion, transmission completion, or transmission cancellation for the set mailboxes.

### 6. Error counters

In the case of error active and error passive, REC and TEC normally count up and down. In the bus off state, 11-bit recessive sequences are counted (REC + 1) using REC. If REC reaches 96 during the count, IRR4 and GSR1 are set, and if REC reaches 128, IRR7 is set.

### 7. Register access

Byte or word access can be used on all HCAN registers. Longword access cannot be used.

### 8. Register initialization in standby modes

All HCAN registers are initialized in hardware standby mode and software standby mode.



# Section 16 A/D Converter

## 16.1 Overview

The SH7052F/SH7053F/SH7054F includes a 10-bit successive-approximation A/D converter, with software selection of up to 32 analog input channels.

The A/D converter is composed of two independent modules, A/D0 and A/D1. A/D0 comprises three groups and A/D1 comprises one group.

Module	Analog Groups	Channels
A/D0	Analog group 0	AN0 to AN3
	Analog group 1	AN4 to AN7
	Analog group 2	AN8 to AN11
A/D1	Analog group 3	AN12 to AN15

### 16.1.1 Features

The features of the A/D converter are summarized below.

- 10-bit resolution  
16 input channels (A/D0: 12 channels, A/D1: 4 channels)
- High-speed conversion  
Conversion time: minimum 13.4  $\mu$ s per channel (when  $\phi = 40$  MHz)
- Two conversion modes
  - Single mode: A/D conversion on one channel
  - Scan mode: cotinuous scan mode, single-cycle scan mode (AN0 to AN3, AN4 to AN7, AN8 to AN11, AN12 to AN15)
    - Continuous conversion on 1 to 12 channels (A/D0)
    - Continuous conversion on 1 to 4 channels (A/D1)
- Sixteen 10-bit A/D data registers  
A/D conversion results are transferred for storage into data registers corresponding to the channels.
- Two sample-and-hold circuits  
A sample-and-hold circuit is built into each A/D converter module (A/D0 and A/D1), simplifying the configuration of external analog input circuitry.
- A/D conversion interrupts and DMA function supported

An A/D conversion interrupt request (ADI) can be sent to the CPU at the end of A/D conversion (ADI0: A/D0 interrupt request; ADI1: A/D1 interrupt request). Also, the DMAC can be activated by an ADI interrupt request.

- Two kinds of conversion activation
  - Software or external trigger ( $\overline{\text{ADTER0}}$ , ATU-II (ITVRR2A)) can be selected (A/D0)
  - Software or external trigger ( $\overline{\text{ADTGR0}}$ , ATU-II (ITVRR2B)) can be selected (A/D1)

## 16.1.2 Block Diagram

Figure 16.1 shows a block diagram of the A/D converter.

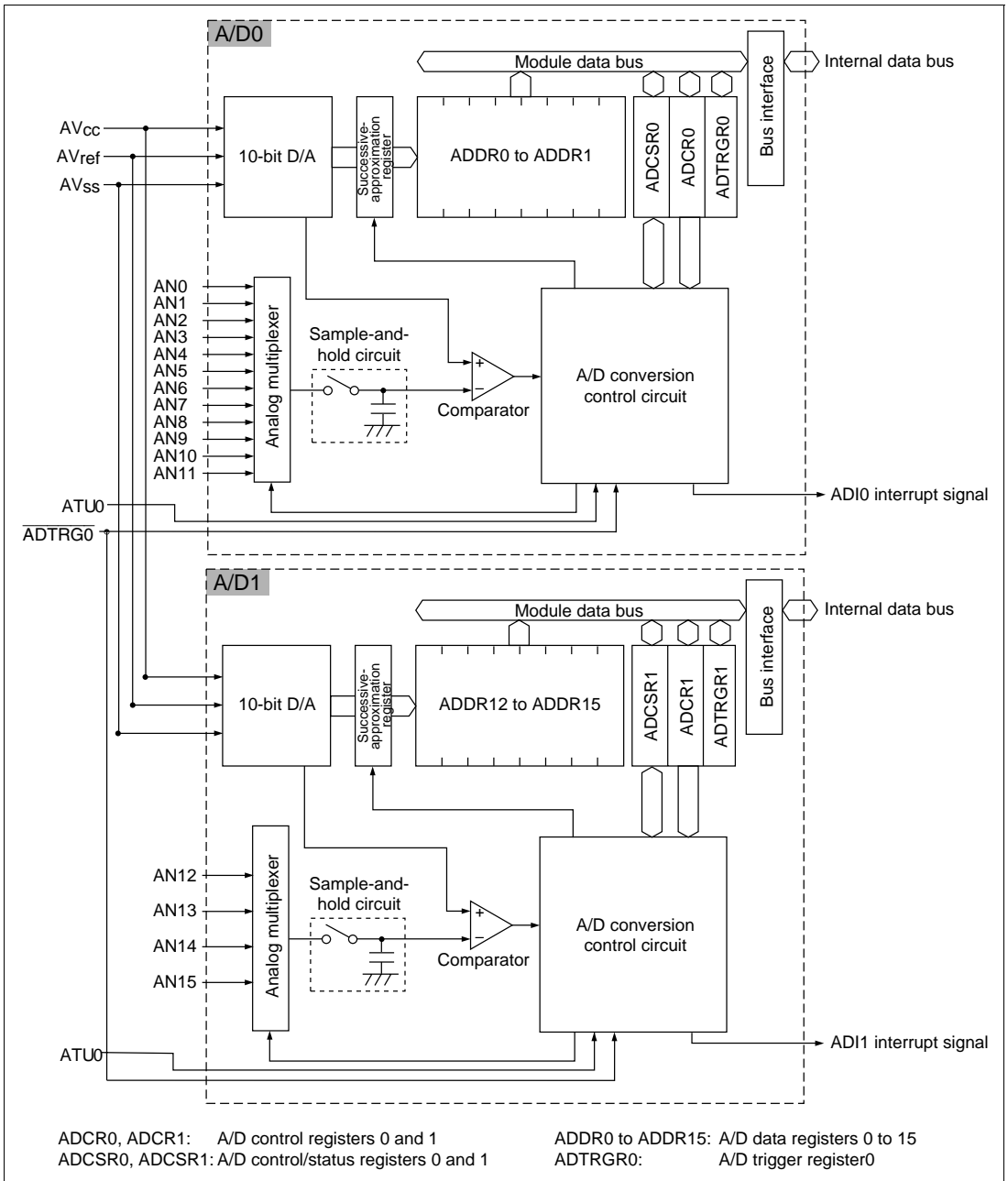


Figure 16.1 A/D Converter Block Diagram

### 16.1.3 Pin Configuration

Table 16.1 summarizes the A/D converter's input pins. There are 16 analog input pins, AN0 to AN15. The 12 pins AN0 to AN11 are A/D0 analog inputs, divided into three groups: AN0 to AN3 (group 0), AN4 to AN7 (group 1), and AN8 to AN11 (group 2). The 4 pins AN12 to AN15 are A/D1 analog inputs, which is one group: AN12 to AN15 (group 3).

The  $\overline{\text{ADTRG0}}$  pin is used to provide A/D conversion start timing from off-chip. When a low level is applied to one of these pins, A/D0 or A/D1 starts conversion.

The  $\text{AV}_{\text{CC}}$  and  $\text{AV}_{\text{SS}}$  pins are power supply voltage pins for the analog section in A/D converter modules A/D0 and A/D1. The  $\text{AV}_{\text{ref}}$  pin is the A/D converter module A/D0 and A/D1 reference voltage pin.

To maintain chip reliability, ensure that  $\text{AV}_{\text{CC}} = 5 \text{ V} \pm 0.5 \text{ V}$  and  $\text{AV}_{\text{SS}} = \text{V}_{\text{SS}}$  during normal operation, and never leave the  $\text{AV}_{\text{CC}}$  and  $\text{AV}_{\text{SS}}$  pins open, even when the A/D converter is not being used.

The voltage applied to the analog input pins should be in the range  $\text{AV}_{\text{SS}} \leq \text{ANn} \leq \text{AV}_{\text{ref}}$ .

**Table 16.1 A/D Converter Pins**

<b>Pin Name</b>	<b>Abbreviation</b>	<b>I/O</b>	<b>Function</b>
Analog power supply pin	$AV_{CC}$	Input	A/D0, A/D1 analog section power supply
Analog ground pin	$AV_{SS}$	Input	A/D0, A/D1 analog section ground and reference voltage
Analog reference power supply pin	$AV_{ref}$	Input	A/D0, A/D1 analog section reference voltage
Analog input pin 0	AN0	Input	A/D0 analog inputs 0 to 3 (analog group 0)
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	A/D0 analog inputs 4 to 7 (analog group 1)
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
Analog input pin 8	AN8	Input	A/D0 analog inputs 8 to 11 (analog group 2)
Analog input pin 9	AN9	Input	
Analog input pin 10	AN10	Input	
Analog input pin 11	AN11	Input	
Analog input pin 12	AN12	Input	A/D1 analog inputs 12 to 15 (analog group 3)
Analog input pin 13	AN13	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	
A/D conversion trigger input pin 0	$\overline{ADTRG0}$	Input	A/D0 and A/D1 A/D conversion trigger input

## 16.1.4 Register Configuration

Table 16.2 summarizes the A/D converter's registers.

**Table 16.2 A/D Converter Registers**

Name	Abbreviation	R/W	Initial Value	Address	Access Size* <sup>1</sup>
A/D data register 0 (H/L)	ADDR0 (H/L)	R	H'0000	H'FFFFFF800	8, 16
A/D data register 1 (H/L)	ADDR1 (H/L)	R	H'0000	H'FFFFFF802	8, 16
A/D data register 2 (H/L)	ADDR2 (H/L)	R	H'0000	H'FFFFFF804	8, 16
A/D data register 3 (H/L)	ADDR3 (H/L)	R	H'0000	H'FFFFFF806	8, 16
A/D data register 4 (H/L)	ADDR4 (H/L)	R	H'0000	H'FFFFFF808	8, 16
A/D data register 5 (H/L)	ADDR5 (H/L)	R	H'0000	H'FFFFFF80A	8, 16
A/D data register 6 (H/L)	ADDR6 (H/L)	R	H'0000	H'FFFFFF80C	8, 16
A/D data register 7 (H/L)	ADDR7 (H/L)	R	H'0000	H'FFFFFF80E	8, 16
A/D data register 8 (H/L)	ADDR8 (H/L)	R	H'0000	H'FFFFFF810	8, 16
A/D data register 9 (H/L)	ADDR9 (H/L)	R	H'0000	H'FFFFFF812	8, 16
A/D data register 10 (H/L)	ADDR10 (H/L)	R	H'0000	H'FFFFFF814	8, 16
A/D data register 11 (H/L)	ADDR11 (H/L)	R	H'0000	H'FFFFFF816	8, 16
A/D data register 12 (H/L)	ADDR12 (H/L)	R	H'0000	H'FFFFFF820	8, 16
A/D data register 13 (H/L)	ADDR13 (H/L)	R	H'0000	H'FFFFFF822	8, 16
A/D data register 14 (H/L)	ADDR14 (H/L)	R	H'0000	H'FFFFFF824	8, 16
A/D data register 15 (H/L)	ADDR15 (H/L)	R	H'0000	H'FFFFFF826	8, 16
A/D control/status register 0	ADCSR0	R/(W)* <sup>2</sup>	H'00	H'FFFFFF818	8, 16
A/D control register 0	ADCR0	R/W	H'0F	H'FFFFFF819	8, 16
A/D trigger register 0	ADTRGR0	R/W	H'FF	H'FFFFFF76E	8
A/D control/status register 1	ADCSR1	R/(W)* <sup>2</sup>	H'00	H'FFFFFF838	8, 16
A/D control register 1	ADCR1	R/W	H'0F	H'FFFFFF839	8, 16
A/D trigger register 1	ADTRGR1	R/W	H'FF	H'FFFFFF72E	8

Notes: Register accesses consist of 6 or 7 cycles for byte access and 12 or 13 cycles for word access.

1. A 16-bit access must be made on a word boundary.
2. Only 0 can be written to bit 7, to clear the flag.

## 16.2 Register Descriptions

### 16.2.1 A/D Data Registers 0 to 15 (ADDR0 to ADDR15)

A/D data registers 0 to 15 (ADDR0 to ADDR15) are 16-bit read-only registers that store the results of A/D conversion. There are 31 registers, corresponding to analog inputs 0 to 15 (AN0 to AN15).

The ADDR registers are initialized to H'0000 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
ADDRnH (upper byte)	AD9	AD8	AD7	AD6	AD5	ADR	AD3	AD2
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
ADDRnL (lower byte)	AD1	AD0	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

(n = 0 to 15)

The A/D converter converts analog input to a 10-bit digital value. The upper 8 bits of this data are stored in the upper byte of the ADDR corresponding to the selected channel, and the lower 2 bits in the lower byte of that ADDR. Only the most significant 2 bits of the ADDR lower byte data are valid.

Table 16.3 shows correspondence between the analog input channels and A/D data registers.

**Table 16.3 Analog Input Channels and A/D Data Registers**

Analog Input Channel	A/D Data Register	Analog Input Channel	A/D Data Register
AN0	ADDR0	AN8	ADDR8
AN1	ADDR1	AN9	ADDR9
AN2	ADDR2	AN10	ADDR10
AN3	ADDR3	AN11	ADDR11
AN4	ADDR4	AN12	ADDR12
AN5	ADDR5	AN13	ADDR13
AN6	ADDR6	AN14	ADDR14
AN7	ADDR7	AN15	ADDR15

### 16.2.2 A/D Control/Status Register 0 (ADCSR0)

A/D control/status register 0 (ADCSR0) is 8-bit readable/writable register whose function includes selection of the A/D conversion mode for A/D0.

ADCSR0 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
	ADF	ADIE	ADM1	ADM0	CH3	CH2	CH1	CH0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: \* Only 0 can be written, to clear the flag.

- Bit 7—A/D End Flag (ADF): Indicates the end of A/D conversion.

#### Bit 7:

ADF	Description
0	Indicates that A/D0 is performing A/D conversion, or is in the idle state (Initial value) [Clearing conditions] <ul style="list-style-type: none"> <li>• When ADF is read while set to 1, then 0 is written to ADF</li> <li>• When the DMAC is activated by ADI0</li> </ul>
1	Indicates that A/D0 has finished A/D conversion, and the digital value has been transferred to ADDR [Setting conditions] <ul style="list-style-type: none"> <li>• Single mode: When A/D conversion ends</li> <li>• Scan mode: When all set A/D conversions end</li> </ul>



The operation of the A/D converter after ADF is set to 1 differs between single mode and scan mode.

In single mode, after the A/D converter transfers the digital value to ADDR, ADF is set to 1 and the A/D converter enters the idle state. In scan mode (continuous scanning), after all the set conversions end ADF is set to 1 and conversion is continued. For example, in the case of 12-channel scanning, ADF is set to 1 immediately after the end of conversion for AN8 to AN11 (group 2).

In scan mode (single-cycle scanning), after all the set analog conversions end ADF is set to 1 and conversion is terminated. For example, in the case of 12-channel scanning, ADF is set to 1 immediately after the end of conversion for AN0 to AN11.

- Bit 6—A/D Interrupt Enable (ADIE): Enables or disables the A/D interrupt (ADI).  
To prevent incorrect operation, ensure that the ADST bit in A/D control registers 0 and 1 (ADCR0) is cleared to 0 before switching the operating mode.

**Bit 6:**

<b>ADIE</b>	<b>Description</b>	
0	A/D interrupt (ADI0) is disabled	(Initial value)
1	A/D interrupt (ADI0) is enabled	

When A/D conversion ends and the ADF bit is set to 1, an A/D0 or A/D1 A/D interrupt (ADI0, ADI1) will be generated. If the ADIE bit is 1, ADI0 and ADI1 are cleared by clearing ADF or ADIE to 0.

- Bits 5 and 4: A/D Mode 1 and 0 (ADM1, ADM0): These bits select the A/D conversion mode from single mode, 4-channel scan mode, 8-channel scan mode, and 12-channel scan mode.  
To prevent incorrect operation, ensure that the ADST bit in A/D control registers 1 and 0 (ADCR1, ADCR0) is cleared to 0 before switching the operating mode.

<b>Bit 5: ADM1</b>	<b>Bit 4: ADM0</b>	<b>Description</b>	
0	0	Single mode	(Initial value)
	1	4-channel scan mode (analog groups 0, 1, 2)	
1	0	8-channel scan mode (analog groups 0, 1)	
	1	12-channel scan mode (analog groups 0, 1, 2)	

When ADM1 and ADM0 are set to 00, single mode is set. In single mode, operation ends after A/D conversion has been performed once on the analog channels selected with bits CH3 to CH0 in ADCSR.

When ADM1 and ADM0 are set to 01, 4-channel scan mode is set. In scan mode, A/D conversion is performed continuously on a number of channels. The channels on which A/D conversion is to be performed in scan mode are set with bits CH3 to CH0 in ADCSR0. In 4-channel scan mode, conversion is performed continuously on the channels in one of analog groups 0 (AN0 to AN3), 1 (AN4 to AN7), 2 (AN8 to AN11).

When the ADCS bit is cleared to 0, selecting scanning of all channels within the group (AN0 to AN3, AN4 to AN7, AN8 to AN11), conversion is performed continuously, once only for each channel within the group, and operation stops on completion of conversion for the last (highest-numbered) channel.

When ADM1 and ADM0 are set to 10, 8-channel scan mode is set. In 8-channel scan mode, conversion is performed continuously on the 8 channels in analog groups 0 (AN0 to AN3) and 1 (AN4 to AN7). When the ADCS bit is cleared to 0, selecting scanning of all channels within the groups (AN0 to AN7), conversion is performed continuously, once only for each channel within the groups, and operation stops on completion of conversion for the last (highest-numbered) channel.

When ADM1 and ADM0 are set to 11, 12-channel scan mode is set. In 12-channel scan mode, conversion is performed continuously on the 12 channels in analog groups 0 (AN0 to AN3), 1 (AN4 to AN7), and 2 (AN8 to AN11). When the ADCS bit is cleared to 0, selecting scanning of all channels within the groups (AN0 to AN11), conversion is performed continuously, once only for each channel within the groups, and operation stops on completion of conversion for the last (highest-numbered) channel.

For details of the operation in single mode and scan mode, see section 16.4, Operation.

- Bits 3 to 0—Channel Select 3 to 0 (CH3 to CH0): These bits, together with the ADM1 and ADM0 bits, select the analog input channels.

To prevent incorrect operation, ensure that the ADST bit in A/D control registers 1 and 0 (ADCR1, ADCR0) is cleared to 0 before changing the analog input channel selection.

### Analog Input Channels

Bit 3: CH3	Bit 2: CH2	Bit 1: CH1	Bit 0: CH0	Single Mode	4-Channel Scan Mode		
				A/D0	A/D0		
0	0	0	0	AN0 (Initial value)	AN0		
			1	AN1	AN0, AN1		
			1	0	AN2	AN0 to AN2	
				1	AN3	AN0 to AN3	
			1	0	0	AN4	AN4
					1	AN5	AN4, AN5
					1	0	AN6
1	AN7	AN4 to AN7					
1	0*	0	0	AN8	AN8		
			1	AN9	AN8, AN9		
			1	0	AN10	AN8 to AN10	
				1	AN11	AN8 to AN11	

Note: \* Must be cleared to 0.

### Analog Input Channels

Bit 3: CH3	Bit 2: CH2	Bit 1: CH1	Bit 0: CH0	8-Channel Scan Mode	12-Channel Scan Mode	
				A/D0	A/D0	
0	0	0	0	AN0, AN4	AN0, AN4, AN8	
			1	AN0, AN1, AN4, AN5	AN0, AN1, AN4, AN5, AN8, AN9	
			1	0	AN0 to AN2, AN4 to AN6	AN0 to AN2, AN4 to AN6, AN8 to AN10
				1	AN0 to AN7	AN0 to AN11
			1	0	0	0
1	AN0, AN1, AN4, AN5	AN0, AN1, AN4, AN5, AN8, AN9				
1	0	AN0 to AN2, AN4 to AN6				AN0 to AN2, AN4 to AN6, AN8 to AN10
	1	AN0 to AN7				AN0 to AN11
1	0*1	0	0	Reserved*2	AN0, AN4, AN8	
			1		AN0, AN1, AN4, AN5, AN8, AN9	
			1	0		AN0 to AN2, AN4 to AN6, AN8 to AN10
				1		AN0 to AN11

Notes: 1. Must be cleared to 0.

2. These modes are provided for future expansion, and cannot be used at present.

### 16.2.3 A/D Control Registers 0 and 1 (ADCR0, ADCR1)

A/D control registers 0 and 1 (ADCR0 and ADCR1) are 8-bit readable/writable registers that control the start of A/D conversion and selects the operating clock for A/D0 and A/D1.

ADCR0 and ADCR1 are initialized to H'0F by a power-on reset, and in hardware standby mode and software standby mode.

Bits 3 to 0 of ADCR0 and ADCR1 are reserved. These bits cannot be written to, and always return 1 if read.

Bit:	7	6	5	4	3	2	1	0
	TRGE	CKS	ADST	ADCS	—	—	—	—
Initial value:	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R	R	R	R

- Bit 7—Trigger Enable (TRGE): Enables or disables triggering of A/D conversion by external input or the ATU-II.

#### Bit 7:

TRGE	Description
0	A/D conversion triggering by external input or ATU-II is disabled (Initial value)
1	A/D conversion triggering by external input or ATU-II is enabled

For details of external or ATU-II trigger selection, see section 16.2.5, A/D Trigger Register 0 and 1.

When ATU triggering is selected, clear bit 7 of registers ADTRGR0 and ADTRGR1 to 0.

When external triggering is selected, upon input of a low level to the  $\overline{\text{ADTRG0}}$  pin after TRGE has been set to 1, the A/D converter detects the low level, and sets the ADST bit to 1 in ADCR.

The same operation is subsequently performed when 1 is written in the ADST bit by software.

External triggering of A/D conversion is only enabled when the ADST bit is cleared to 0.

When external triggering is used, the low level input to the  $\overline{\text{ADTRG0}}$  pin must be at least 1.5 P $\phi$  clock cycles in width. For details, see section 16.4.4, External Triggering of A/D Converter.

- Bit 6—Clock Select (CKS): Selects the A/D conversion time. A/D conversion is executed in a maximum of 532 states when CKS is 0, and a maximum of 268 states when 1. To prevent incorrect operation, ensure that the ADST bit A/D control registers 0 and 1 (ADCR0 and ADCR1) is cleared to 0 before changing the A/D conversion time. For details, see section 16.4.3, Analog Input Sampling and A/D Conversion Time.

**Bit 6:**

CKS	Description
0	Conversion time = 532 states (maximum) (Initial value)
1	Conversion time = 268 states (maximum)

- Bit 5—A/D Start (ADST): Starts or stops A/D conversion. A/D conversion is started when ADST is set to 1, and stopped when ADST is cleared to 0.

**Bit 5:**

ADST	Description
0	A/D conversion is stopped (Initial value)
1	A/D conversion is being executed [Clearing conditions] <ul style="list-style-type: none"> <li>• Single mode: Automatically cleared to 0 when A/D conversion ends</li> <li>• Scan mode: Automatically cleared to 0 on completion of one round of conversion on all set channels (single-cycle scan)</li> </ul>

Note that the operation of the ADST bit differs between single mode and scan mode.

In single mode, ADST is automatically cleared to 0 when A/D conversion ends on one channel. In scan mode (continuous scan), when all conversions have ended for the selected analog inputs, ADST remains set to 1 in order to start A/D conversion again for all the channels. Therefore, in scan mode (continuous scan), the ADST bit must be cleared to 0, stopping A/D conversion, before changing the conversion time or the analog input channel selection. However, in scan mode (single-cycle scan), the ADST bit is automatically cleared to 0, stopping A/D conversion, when one round of conversion ends on all the set channels.

Ensure that the ADST bit in ADCR0 and ADCR1 is cleared to 0 before switching the operating mode.

Also, make sure that A/D conversion is stopped (ADST is cleared to 0) before changing A/D interrupt enabling (bit ADIE in ADCSR0 and ADCSR1), the A/D conversion time (bit CKS in ADCR0 and ADCR1), the operating mode (bits ADM1 and ADM0 in ADSCR0 and ADCSR1), or the analog input channel selection (bits CH3 to CH0 in ADCSR0 and ADCSR1). The A/D data register contents will not be guaranteed if these changes are made while the A/D converter is operating (ADST is set to 1).

- Bit 4—A/D Continuous Scan (ADCS): Selects either single-cycle scan or continuous scan in scan mode. This bit is valid only when scan mode is selected. See section 16.4.2, Scan Mode, for details.

**Bit 4:**

ADCS	Description
0	Single-cycle scan (Initial value)
1	Continuous scan

- Bits 3 to 0—Reserved: These bits are always read as 1, and should only be written with 1.

### 16.2.4 A/D Control/Status Register 1 (ADCSR1)

A/D control/status register 1 (ADCSR1) is an 8-bit readable/writable register whose functions include selection of the A/D conversion mode for A/D1.

ADCSR1 is initialized to H'00 by a power-on reset, and in hardware standby mode and software standby mode.

Bit:	7	6	5	4	3	2	1	0
	ADF	ADIE	ADM1	ADM0	CH3	CH2	CH1	CH0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: \* Only 0 can be written, to clear the flag.

- Bit 7—A/D End Flag (ADF): Indicates the end of A/D conversion.

**Bit 7:**

ADF	Description
0	Indicates that A/D1 is performing A/D conversion, or is in the idle state (Initial value) [Clearing conditions] <ul style="list-style-type: none"> <li>• When ADF is read while set to 1, then 0 is written to ADF</li> <li>• When the DMAC is activated by ADI2</li> </ul>
1	Indicates that A/D1 has finished A/D conversion, and the digital value has been transferred to ADDR [Setting conditions] <ul style="list-style-type: none"> <li>• Single mode: When A/D conversion ends</li> <li>• Scan mode: When all set A/D conversions end</li> </ul>

The operation of the A/D converter after ADF is set to 1 differs between single mode and scan mode.

In single mode, after the A/D converter transfers the digital value to ADDR, ADF is set to 1 and the A/D converter enters the idle state. In scan mode (continuous scanning), after all the set conversions end ADF is set to 1 and conversion is continued. For example, in the case of 4-channel scanning, ADF is set to 1 immediately after the end of conversion for AN12 to AN15 (group 3).

In scan mode (single-cycle scanning), after all the set analog conversions end ADF is set to 1 and conversion is terminated. For example, in the case of 4-channel scanning, ADF is set to 1 immediately after the end of conversion for AN12 to AN15.

- Bit 6—A/D Interrupt Enable (ADIE): Enables or disables the A/D interrupt (ADI).

To prevent incorrect operation, ensure that the ADST bit in A/D control register 2 (ADCR2) is cleared to 0 before switching the operating mode.

**Bit 6:**

<b>ADIE</b>	<b>Description</b>	
0	A/D interrupt (ADI1) is disabled	(Initial value)
1	A/D interrupt (ADI1) is enabled	

When A/D conversion ends and the ADF bit in ADCSR2 is set to 1, an A/D1 A/D interrupt (ADI1) will be generated if the ADIE bit is 1. ADI1 is cleared by clearing ADF or ADIE to 0.

- Bits 5 and 4: A/D Mode 1 and 0 (ADM1, ADM0): These bits select the A/D conversion mode from single mode, 4-channel scan mode, 8-channel scan mode, 12-channel scan mode.

To prevent incorrect operation, ensure that the ADST bit in A/D control register 1, 0 (ADCR1, 0) is cleared to 0 before switching the operating mode.

<b>Bit 5:</b> <b>ADM1</b>	<b>Bit 4:</b> <b>ADM0</b>	<b>Description</b>	
0	0	Single mode	(Initial value)
	1	4-channel scan mode (analog groups 3)	
1	0	Reserved	
	1	Reserved	

When ADM1 and ADM0 are set to 00, single mode is set. In single mode, operation ends after A/D conversion has been performed once on the analog channels selected with bits CH3 to CH0 in ADCSR.

When ADM1 and ADM0 are set to 01, 4-channel scan mode is set. In scan mode, A/D conversion is performed continuously on a number of channels. The channels on which A/D conversion is to be performed in scan mode are set with bits CH3 to CH0 in ADCSR1. In 4-channel scan mode, conversion is performed continuously on the channels in one of analog groups 3 (AN12 to AN15).

When the ADCS bit is cleared to 0, selecting scanning of all channels within the group (AN12 to AN15), conversion is performed continuously, once only for each channel within the group, and operation stops on completion of conversion for the last (highest-numbered) channel.

For details of the operation in single mode and scan mode, see section 16.4, Operation.

- Bits 3 to 0—Channel Select 3 to 0 (CH3 to CH0): These bits, together with the ADM1 and ADM0 bits, select the analog input channels.

To prevent incorrect operation, ensure that the ADST bit in A/D control register 1 (ADCR1) is cleared to 0 before changing the analog input channel selection.

				<b>Analog Input Channels</b>	
<b>Bit:</b>	<b>Bit:</b>	<b>Bit:</b>	<b>Bit:</b>	<b>Single Mode</b>	<b>4-Channel Scan Mode</b>
<b>CH3</b>	<b>CH2</b>	<b>CH1</b>	<b>CH0</b>	<b>A/D1</b>	<b>A/D1</b>
0*1	0*1	0	0	AN12 (Initial value)	AN12
			1	AN13	AN12, AN13
		1	0	AN14	AN12 to AN14
			1	AN15	AN12 to AN15

- Notes
1. These bits must be set to 0.
  2. Other modes, which are not described in this table are, for future use. Be sure not to use the modes.



## 16.2.5 A/D Trigger Registers 0 and 1 (ADTRGR0, ADTRGR1)

The A/D trigger registers (ADTRGR0 and ADTRGR1) are 8-bit readable/writable registers that select the A/D0 and A/D1 triggers. Either external pin ( $\overline{\text{ADTRG0}}$ ) or ATU-II (ATU-II interval timer A/D conversion request) triggering can be selected.

ADTRG0 and ADTRG1 are initialized to H'FF by a power-on reset and in hardware standby mode. They are not initialized in software standby mode.

Bit:	7	6	5	4	3	2	1	0
	EXTRG	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R	R	R	R	R	R	R

- Bit 7—Trigger Enable (EXTRG): Selects external pin input ( $\overline{\text{ADTRG0}}$ ) or the ATU-II interval timer A/D conversion request.

### Bit 7:

EXTRG	Description
0	A/D conversion is triggered by the ATU-II channel 0 interval timer A/D conversion request
1	A/D conversion is triggered by external pin input ( $\overline{\text{ADTRG}}$ ) (Initial value)

In order to select external triggering or ATU-II triggering, the TGRE bit in ADCR0 and ADCR1 must be set to 1. For details, see section 16.2.3, A/D Control Registers 0 and 1.

- Bits 6 to 0—Reserved: These bits are always read as 1, and should only be written with 1.

## 16.3 CPU Interface

A/D data registers 0 to 15 (ADDR0 to ADDR15) are 16-bit registers, but they are connected to the CPU by an 8-bit data bus. Therefore, the upper and lower bytes must be read separately.

To prevent the data being changed between the reads of the upper and lower bytes of an A/D data register, the lower byte is read via a temporary register (TEMP). The upper byte can be read directly.

Data is read from an A/D data register as follows. When the upper byte is read, the upper-byte value is transferred directly to the CPU and the lower-byte value is transferred into TEMP. Next, when the lower byte is read, the TEMP contents are transferred to the CPU.

When performing byte-size reads on an A/D data register, always read the upper byte before the lower byte. It is possible to read only the upper byte, but if only the lower byte is read, incorrect data may be obtained. If a word-size read is performed on an A/D data register, reading is performed in upper byte, lower byte order automatically.

Figure 16.2 shows the data flow for access to an A/D data register.

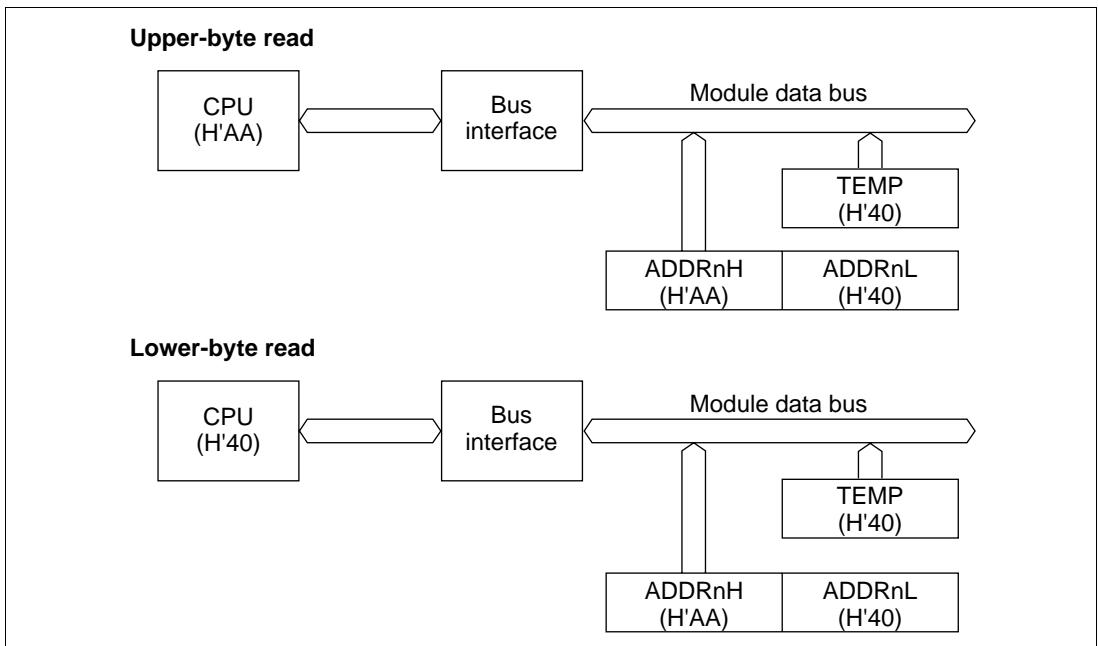


Figure 16.2 A/D Data Register Access Operation (Reading H'AA40)

## 16.4 Operation

The A/D converter operates by successive approximations with 10-bit resolution. It has two operating modes: single mode and scan mode. There are two kinds of scan mode: continuous and single-cycle. In single mode, conversion is performed once on one specified channel, then ends. In continuous scan mode, A/D conversion continues on one or more specified channels until the ADST bit is cleared to 0. In single-cycle scan mode, A/D conversion ends after being performed once on one or more channels.

### 16.4.1 Single Mode

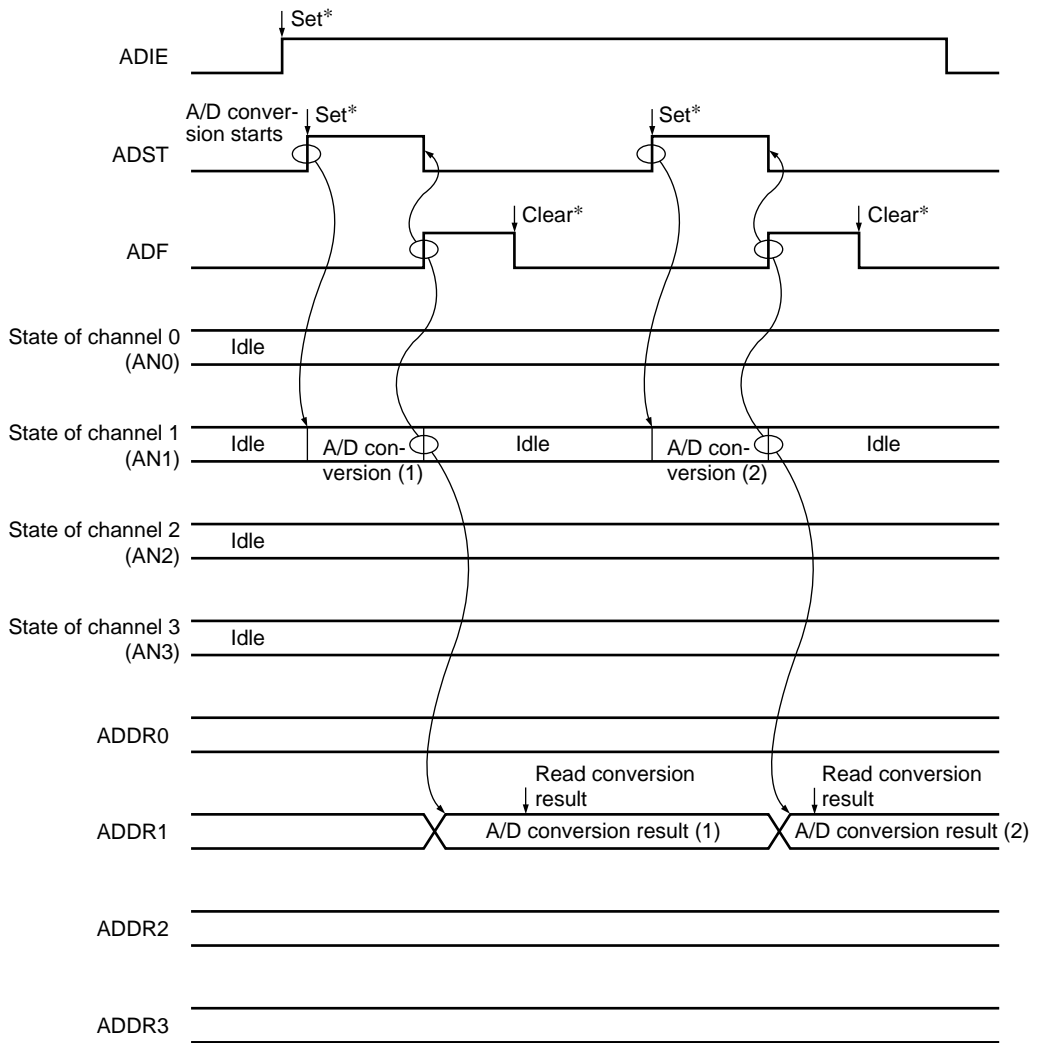
Single mode, should be selected when only one A/D conversion on one channel is required. Single mode is selected by setting the ADM1 and ADM0 bits in the A/D control/status register (ADCSR) to 00. When the ADST bit in the A/D control register (ADCR) is set to 1, A/D conversion is started in single mode.

The ADST bit remains set to 1 during A/D conversion, and is automatically cleared to 0 when conversion ends.

When conversion ends, the ADF flag in ADCSR is set to 1. If the ADIE bit in ADCSR is also 1, an ADI interrupt is requested. To clear the ADF flag, first read ADF when set to 1, then write 0 to ADF. If the DMAC is activated by the ADI interrupt, ADF is cleared automatically.

An example of the operation when analog input channel 1 (AN1) is selected and A/D conversion is performed in single mode is described next. Figure 16.3 shows a timing diagram for this example.

1. Single mode is selected ( $ADM1 = ADM0 = 0$ ), input channel AN1 is selected ( $CH3 = CH2 = CH1 = 0, CH0 = 1$ ), the A/D interrupt is enabled ( $ADIE = 1$ ), and A/D conversion is started ( $ADST = 1$ ).
2. When A/D conversion is completed, the result is transferred to ADDR1. At the same time the ADF flag is set to 1, the ADST bit is cleared to 0, and the A/D converter becomes idle.
3. Since  $ADF = 1$  and  $ADIE = 1$ , an ADI interrupt is requested.
4. The A/D interrupt handling routine is started.
5. The routine reads ADF set to 1, then writes 0 to ADF.
6. The routine reads and processes the conversion result (ADDR1).
7. Execution of the A/D interrupt handling routine ends. After this, if the ADST bit is set to 1, A/D conversion starts again and steps 2 to 7 are repeated.



Note: \* Vertical arrows (↓) indicate instructions executed by software.

**Figure 16.3 Example of A/D Converter Operation (Single Mode, Channel 1 Selected)**

## 16.4.2 Scan Mode

Scan mode is useful for monitoring analog inputs in a group of one or more channels. Scan mode is selected for A/D0 by setting the ADM1 and ADM0 bits in A/D control/status register 0 or 1 (ADSCR0) to 01 (4-channel scan mode), or 11 (12-channel scan mode).

For A/D1, scan mode is selected by setting the ADM1 and ADM0 bits in A/D control/status register 1 (ADCSR1) to 01 (4-channel scan mode). When the ADCS bit is cleared to 0 and the ADST bit is set to 1 in the A/D control register (ADCR), single-cycle scanning is performed. When the ADCS bit is set to 1 and the ADST bit is set to 1, continuous scanning is performed.

In scan mode, A/D conversion is performed in low-to-high analog input channel number order (AN0, AN1 ... AN11, AN12, AN13 ... AN15).

In single-cycle scanning, the ADF bit in ADCSR is set to 1 when conversion has been performed once on all the set channels, and the ADST bit is automatically cleared to 0.

In continuous scanning, the ADF bit in ADCSR is set to 1 when conversion ends on all the set channels. To stop A/D conversion, write 0 to the ADST bit.

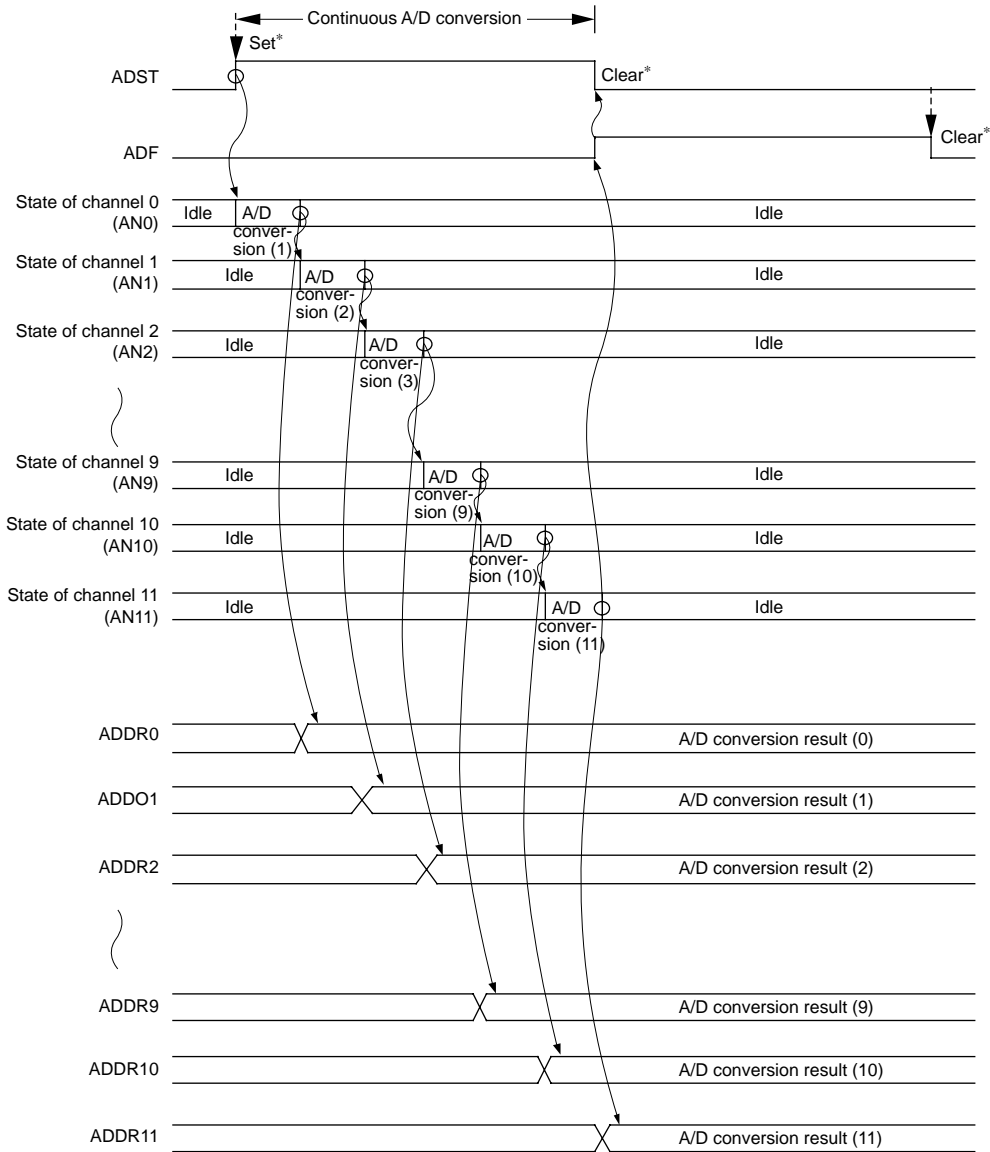
If the ADIE bit in ADCSR is set to 1 when ADF is set to 1, an ADI interrupt (ADI0, ADI1, or ADI2) is requested. To clear the ADF flag, first read ADF when set to 1, then write 0 to ADF. If the DMAC is activated by the ADI interrupt, ADF is cleared to 0 automatically.

An example of the operation when analog inputs 0 to 11 (AN0 to AN11) are selected and A/D conversion is performed in single-cycle scan mode is described below. Figure 16.4 shows the operation timing for this example.

1. 12-channel scan mode is selected (ADM1 = 1, ADM0 = 1), single-cycle scan mode is selected (ADCS = 0), analog input channels AN0 to AN11 are selected (CH3 = 0, CH2 = 0, CH1 = 1, CH0 = 1), and A/D conversion is started.
2. When conversion of the first channel (AN0) is completed, the result is transferred to ADDR0. Next, conversion of the second channel (AN1) starts automatically.
3. Conversion proceeds in the same way through the 12th channel (AN11).
4. When conversion is completed for all the selected channels (AN0 to AN11), the ADF flag is set to 1, the ADST bit is cleared to 0 automatically, and A/D conversion stops. If the ADIE bit is 1, an ADI interrupt is requested after A/D conversion ends.

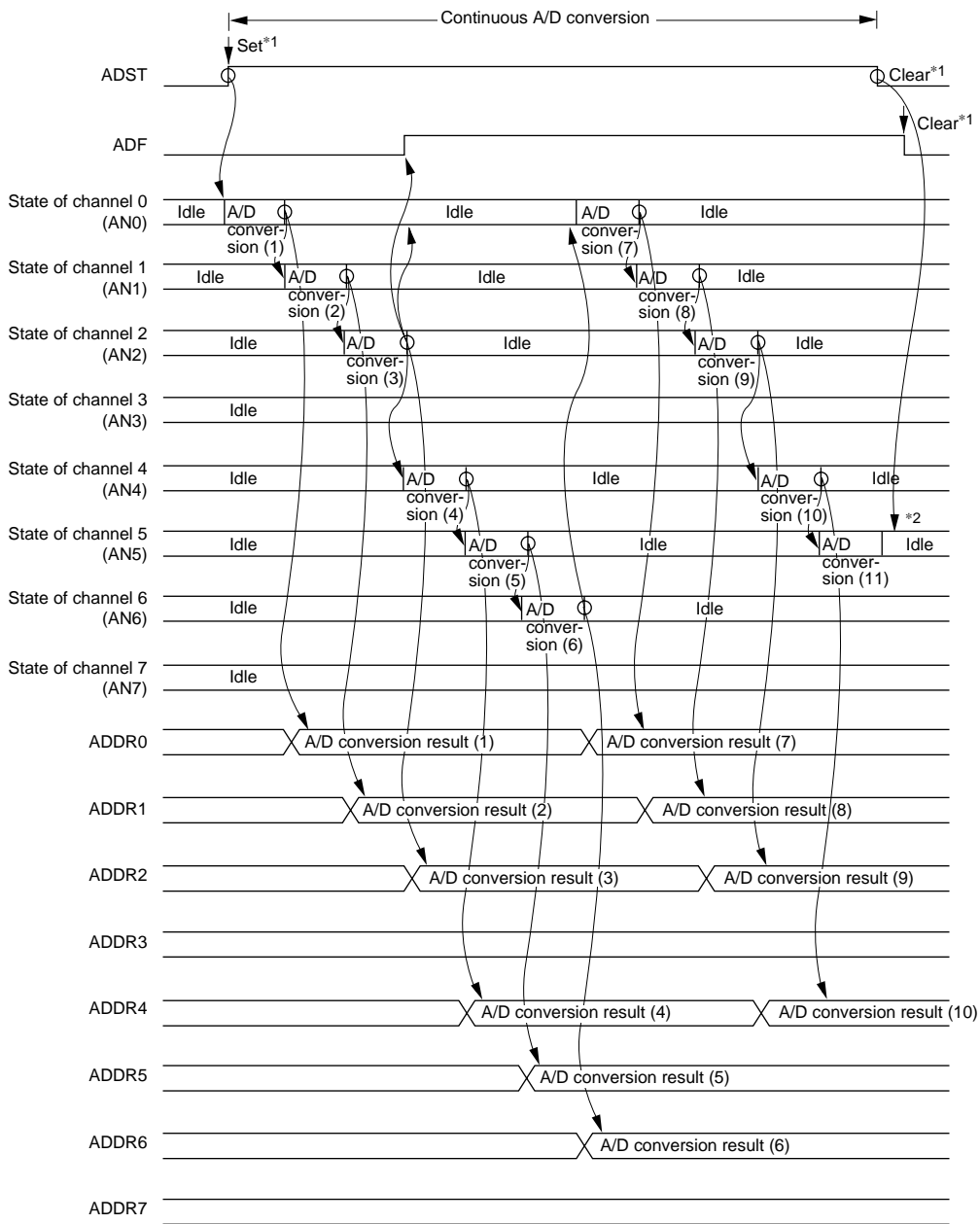
An example of the operation when analog inputs 0 to 2 and 4 to 6 (AN0 to AN2 and AN4 to AN6) are selected and A/D conversion is performed in 8-channel scan mode is described below. Figure 16.5 shows the operation timing.

1. 8-channel scan mode is selected ( $ADM1 = 1$ ,  $ADM0 = 0$ ) continuous scan mode is selected ( $ADCS = 1$ ), analog input channels AN0 to AN2 and AN4 to AN6 are selected ( $CH3 = 0$ ,  $CH2 = 0$ ,  $CH1 = 1$ ,  $CH0 = 0$ ), and A/D conversion is started.
2. When conversion of the first channel (AN0) is completed, the result is transferred to ADDR0. Next, conversion of the second channel (AN1) starts automatically.
3. Conversion proceeds in the same way through the third channel (AN2).
4. Conversion of the fourth channel (AN4) starts automatically.
5. Conversion proceeds in the same way through the sixth channel (AN6)
6. When conversion is completed for all the selected channels (AN0 to AN2 and AN4 to AN6), the ADF flag is set to 1. If the ADIE bit is also 1, an ADI interrupt is requested.
7. Steps 2 to 6 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops. After this, if the ADST bit is set to 1, A/D conversion starts again from the first channel (AN0).



Note: \* Vertical arrows (↓) indicate instructions executed by software.

**Figure 16.4 Example of A/D Converter Operation (Scan Mode (Single-Cycle Scan), Channels AN0 to AN11 Selected)**



Notes: 1. Vertical arrows ( $\downarrow$ ) indicate instructions executed by software.  
 2. Data currently being converted is ignored.

**Figure 16.5 Example of A/D Converter Operation (Scan Mode (Continuous Scan), Channels AN0 to AN2 and AN4 to AN6 Selected)**



### 16.4.3 Analog Input Sampling and A/D Conversion Time

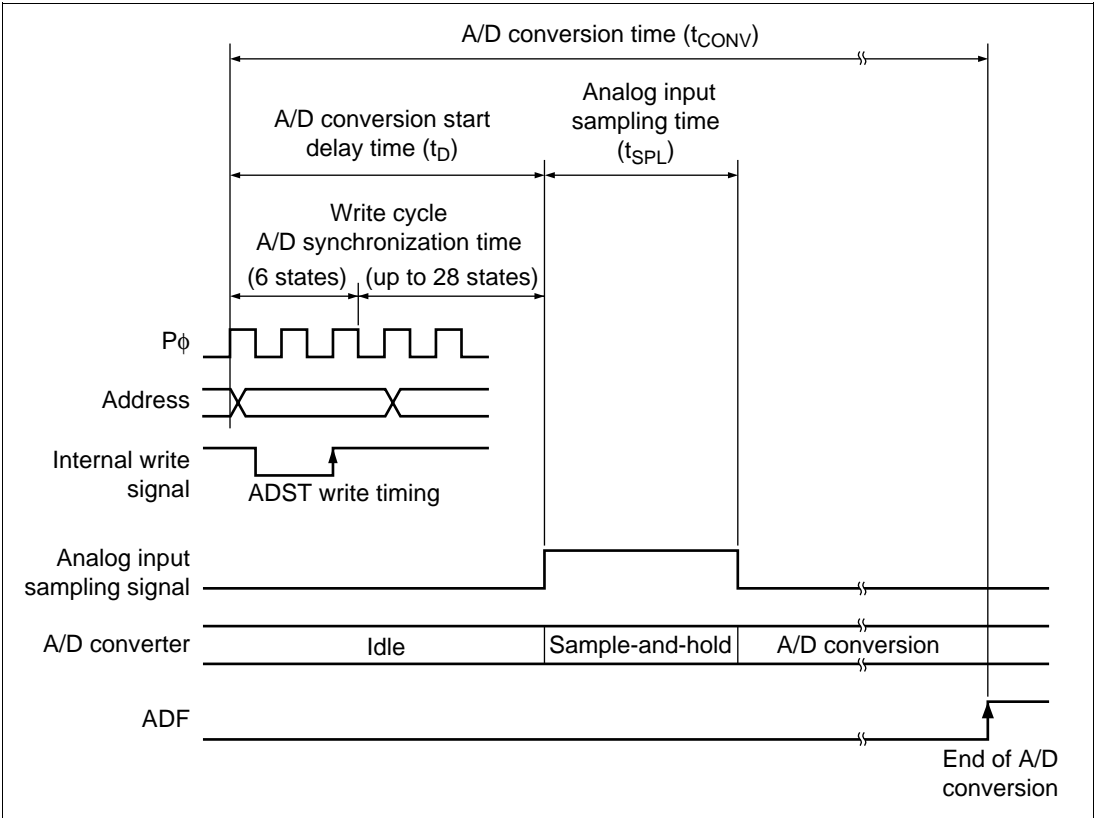
The A/D converter has a built-in sample-and-hold circuit in A/D0, A/D1, and A/D2. The A/D converter samples the analog input at time  $t_D$  (A/D conversion start delay time) after the ADST bit is set to 1, then starts conversion. Figure 16.6 shows the A/D conversion timing.

The A/D conversion time ( $t_{CONV}$ ) includes  $t_D$  and the analog input sampling time ( $t_{SPL}$ ). The length of  $t_D$  is not fixed, since it includes the time required for synchronization of the A/D conversion operation. The total conversion time therefore varies within the ranges shown in table 16.4.

In scan mode, the  $t_{CONV}$  values given in table 16.4 apply to the first conversion. In the second and subsequent conversions,  $t_{CONV}$  is fixed at 512 states when CKS = 0 or 256 states when CKS = 1.

**Table 16.4 A/D Conversion Time (Single Mode)**

Item	Symbol	CKS = 0			CKS = 1			Unit
		Min	Typ	Max	Min	Typ	Max	
A/D conversion start delay time	$t_D$	20	—	34	12	—	18	States ( $\phi$ base)
Input sampling time	$t_{SPL}$	—	128	—	—	64	—	
A/D conversion time	$t_{CONV}$	518	—	532	262	—	268	

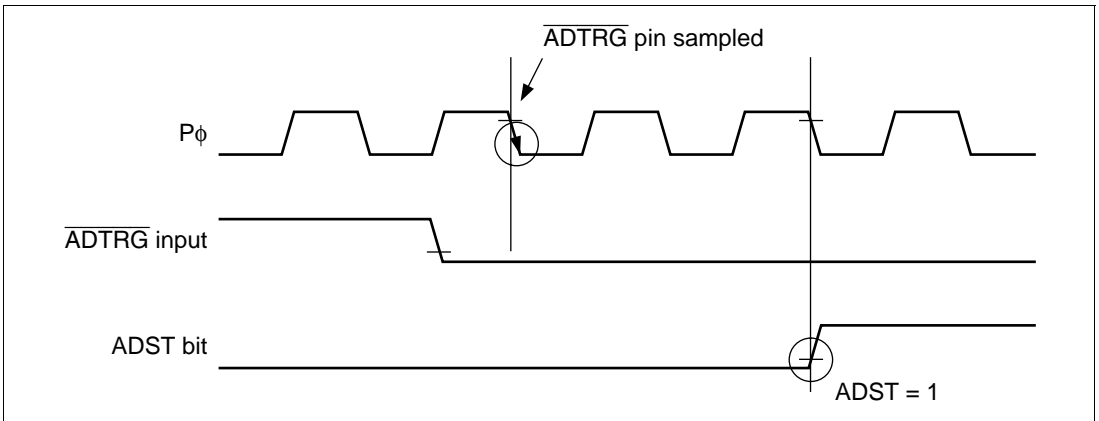


**Figure 16.6 A/D Conversion Timing**

## 16.4.4 External Triggering of A/D Converter

A/D conversion can be externally triggered. To activate the A/D converter with an external trigger, first set the pin functions with the PFC (pin function controller) and input a high level to the  $\overline{\text{ADTRG}}$  pin, then set the TRGE bit to 1 and clear the ADST bit to 0 in the A/D control register (ADCR), and set the EXTRG bit to 1 in the A/D trigger register (ADTRGR). When a low level is input to the  $\overline{\text{ADTRG}}$  pin after these settings have been made, the A/D converter detects the low level and sets the ADST bit to 1. If a low level is being input to the  $\overline{\text{ADTRG}}$  pin when A/D conversion ends, the ADST bit is set to 1 again, and A/D conversion is started. Figure 16.7 shows the timing for external trigger input.

The ADST bit is set to 1 two states after the A/D converter samples the low level on the  $\overline{\text{ADTRG}}$  pin. The timing from setting of the ADST bit until the start of A/D conversion is the same as when 1 is written into the ADST bit by software.



**Figure 16.7 External Trigger Input Timing**

## 16.4.5 A/D Converter Activation by ATU-II

The A/D0 and A/D1 converter modules can be activated by an A/D conversion request from the ATU-II's channel 0 interval timer.

To activate the A/D converter by means of the ATU-II, set the TRGE bit to 1 in the A/D control register (ADCR) and clear the EXTRG bit to 0 in the A/D trigger register (ADTRGR). When an ATU-II channel 0 interval timer A/D conversion request is generated after these settings have been made, the ADST bit set to 1. The timing from setting of the ADST bit until the start of A/D conversion is the same as when 1 is written into the ADST bit by software.

## 16.5 Interrupt Sources and DMA Transfer Requests

The A/D converter can generate an A/D conversion end interrupt request (ADI0 or ADI1) upon completion of A/D conversions. The ADI interrupt can be enabled by setting the ADIE bit in the A/D control/status register (ADCSR) to 1, or disabled by clearing the ADIE bit to 0.

The DMAC can be activated by an ADI interrupt. In this case an interrupt request is not sent to the CPU.

When the DMAC is activated by an ADI interrupt, the ADF bit in ADCSR is automatically cleared when data is transferred by the DMAC.

See section 9.4.2, Example of DMA Transfer between A/D Converter and On-Chip Memory, for an example of this operation.

## 16.6 Usage Notes

The following points should be noted when using the A/D converter.

### 1. Analog input voltage range

The voltage applied to analog input pins during A/D conversion should be in the range  $AV_{SS} \leq AN_n \leq AV_{ref}$ .

### 2. Relation between $AV_{SS}$ , $AV_{CC}$ and $V_{SS}$ , $V_{CC}$

When using the A/D converter, set  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ , and  $AV_{SS} = V_{SS}$ . When the A/D converter is not used, set  $AV_{SS} = V_{SS}$ , and do not leave the  $AV_{CC}$  pin open.

### 3. $AV_{ref}$ input range

Set  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$  when the A/D converter is used, and  $AV_{ref} \leq AV_{CC}$  when not used.

If conditions above are not met, the reliability of the device may be adversely affected.

#### 4. Notes on board design

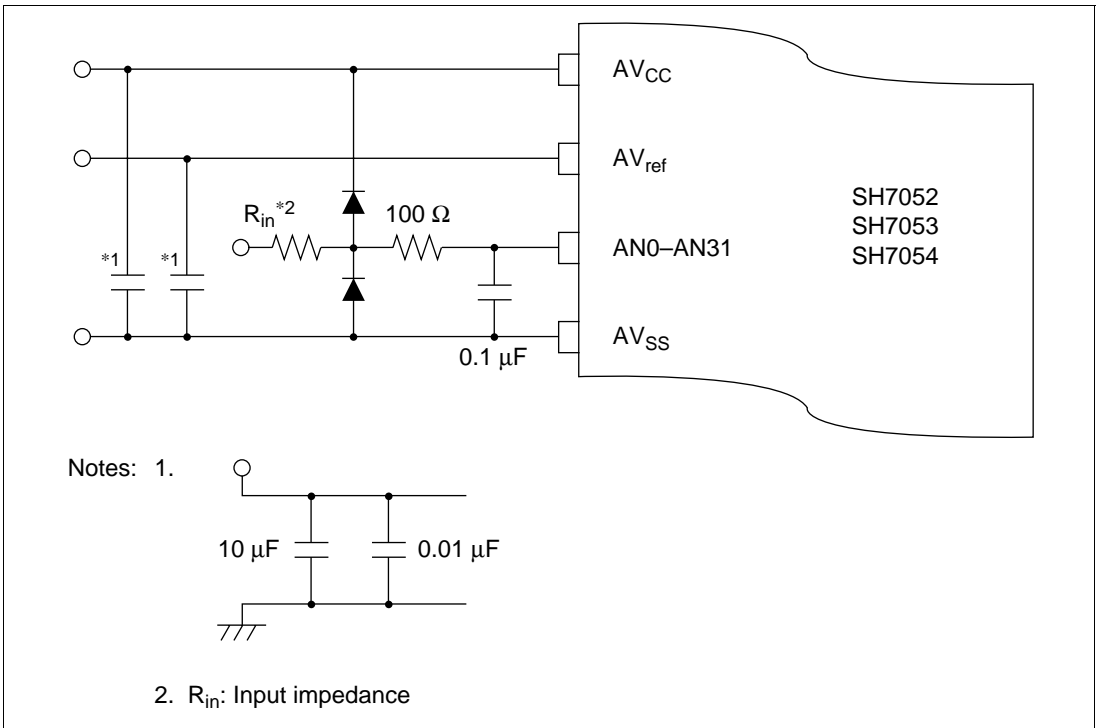
In board design, digital circuitry and analog circuitry should be as mutually isolated as possible, and layout in which digital circuit signal lines and analog circuit signal lines cross or are in close proximity should be avoided as far as possible. Failure to do so may result in incorrect operation of the analog circuitry due to inductance, adversely affecting A/D conversion values.

Also, digital circuitry must be isolated from the analog input signals ( $AN_n$ ), analog reference voltage ( $AV_{ref}$ ), and analog power supply ( $AV_{CC}$ ) by the analog ground ( $AV_{SS}$ ).  $AV_{SS}$  should be connected at one point to a stable digital ground ( $V_{SS}$ ) on the board.

#### 5. Notes on noise countermeasures

A protection circuit connected to prevent damage due to an abnormal voltage such as an excessive surge at the analog input pins ( $AN_n$ ) and analog reference voltage ( $AV_{ref}$ ) should be connected between  $AV_{CC}$  and  $AV_{SS}$  as shown in figure 16.8.

Also, the bypass capacitors connected to  $AV_{CC}$  and  $AV_{ref}$  and the filter capacitor connected to  $AN_n$  must be connected to  $AV_{SS}$ . If a filter capacitor is connected as shown in figure 16.8, the input currents at the analog input pins ( $AN_n$ ) are averaged, and so an error may arise. Careful consideration is therefore required when deciding the circuit constants.



**Figure 16.8 Example of Analog Input Pin Protection Circuit**

**Table 16.5 Analog Pin Specifications**

Item	Min	Max	Unit
Analog input capacitance	—	20	pF
Permissible signal source impedance	—	3	k $\Omega$

### 16.6.1 A/D conversion accuracy definitions

A/D conversion accuracy definitions are given below.

1. Resolution

The number of A/D converter digital conversion output codes

2. Offset error

The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001 (does not include quantization error) (see figure 16.9).

3. Full-scale error

The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111 (does not include quantization error) (see figure 16.9).

4. Quantization error

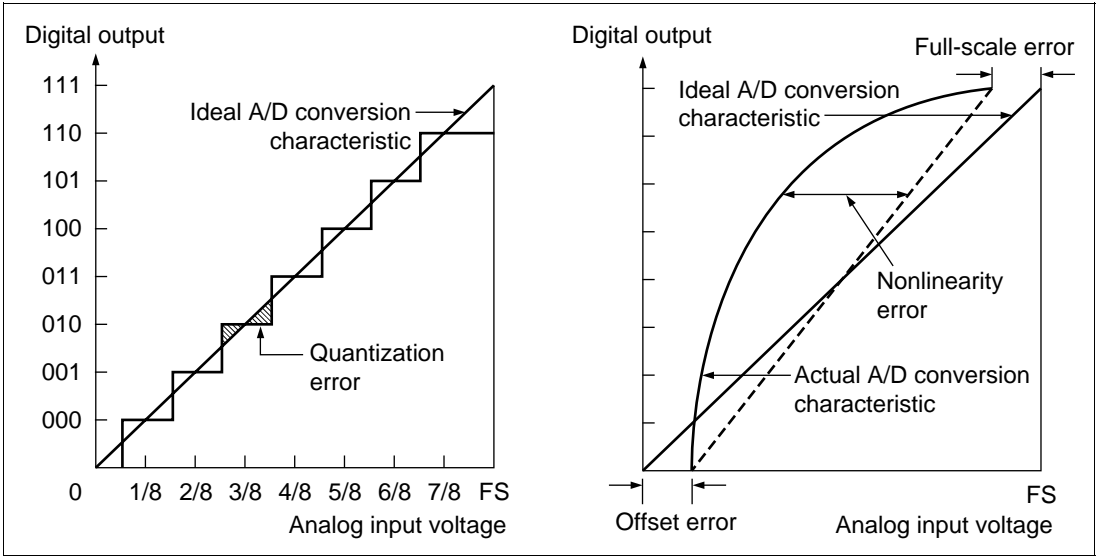
The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 16.9).

5. Nonlinearity error

The error with respect to the ideal A/D conversion characteristic between the zero voltage and the full-scale voltage. Does not include the offset error, full-scale error, or quantization error.

6. Absolute accuracy

The deviation between the digital value and the analog input value. Includes the offset error, full-scale error, quantization error, and nonlinearity error.



**Figure 16.9 A/D Conversion Accuracy Definitions**





# Section 17 Advanced User Debugger (AUD)

## 17.1 Overview

The SH7052F/SH7053F/SH7054F has an on-chip advanced user debugger (AUD). Use of the AUD simplifies the construction of a simple emulator, with functions such as acquisition of branch trace data and monitoring/tuning of on-chip RAM data.

### 17.1.1 Features

The AUD has the following features:

- Eight input/output pins
  - Data bus (AUDATA3 to AUDATA0)
  - AUD reset ( $\overline{\text{AUDRST}}$ )
  - AUD sync signal ( $\overline{\text{AUDSYNC}}$ )
  - AUD clock (AUDCK)
  - AUD mode (AUDMD)

- Two modes

Branch trace mode or RAM monitor mode can be selected by switching AUDMD.

- Branch trace mode

When the PC branches on execution of a branch instruction or generation of an interrupt in the user program, the branch is detected by the AUD and the branch destination address is output from AUDATA. The address is compared with the previously output address, and 4-, 8-, 16-, or 32-bit output is selected automatically according to the upper address matching status.

- RAM monitor mode

When an address is written to AUDATA from off-chip, the data corresponding to that address is output. If an address and data are written to AUDATA, the data is transferred to that address.

## 17.1.2 Block Diagram

Figure 17.1 shows a block diagram of the AUD.

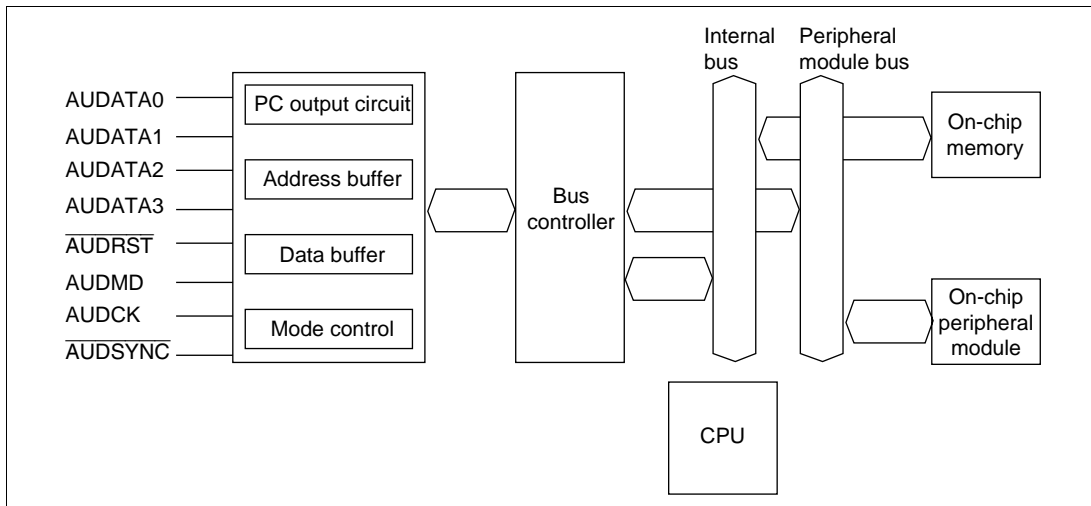


Figure 17.1 AUD Block Diagram

## 17.2 Pin Configuration

Table 17.1 shows the AUD's input/output pins.

Table 17.1 AUD Pins

Name	Abbreviation	Function	
		Branch Trace Mode	RAM Monitor Mode
AUD data	AUDATA3 to AUDATA0	Branch destination address output	Monitor address/data input/output
AUD reset	AUDRST	AUD reset input	AUD reset input
AUD mode	AUDMD	Mode select input (L)	Mode select input (H)
AUD clock	AUDCK	Serial clock ( $\phi/2$ ) output	Serial clock input
AUD sync signal	AUDDSYNC	Data start position identification signal output	Data start position identification signal input

## 17.2.1 Pin Descriptions

### Pins Used in Both Modes

Pin	Description
AUDMD	<p>The mode is selected by changing the input level at this pin.</p> <p>Low: Branch trace mode</p> <p>High: RAM monitor mode</p> <p>The input at this pin should be changed when <math>\overline{\text{AUDRST}}</math> is low. When no connection is made, this pin is pulled up internally.</p>
$\overline{\text{AUDRST}}$	<p>The AUD's internal buffers and logic are initialized by inputting a low level to this pin. When this signal goes low, the AUD enters the reset state and the AUD's internal buffers and logic are reset. When <math>\overline{\text{AUDRST}}</math> goes high again after the AUDMD level settles, the AUD starts operating in the selected mode. When no connection is made, this pin is pulled down internally.</p>

## Pin Functions in Branch Trace Mode

Pin	Description
AUDCK	This pin outputs 1/2 the operating frequency ( $\phi/2$ ). This is the clock for AUDATA synchronization.
AUDSYNC	This pin indicates whether output from AUDATA is valid. High: Valid data is not being output Low: An address is being output
AUDATA3 to AUDATA0	<ol style="list-style-type: none"> <li>When <math>\overline{\text{AUDSYNC}}</math> is low When a program branch or interrupt branch occurs, the AUD asserts <math>\overline{\text{AUDSYNC}}</math> and outputs the branch destination address. The output order is A3 to A0, A7 to A4, A11 to A8, A15 to A12, A19 to A16, A23 to A20, A27 to A24, A31 to A28.</li> <li>When <math>\overline{\text{AUDSYNC}}</math> is high When waiting for branch destination address output, these pins constantly output 0011. When an branch occurs, AUDATA3 to AUDATA2 output 10, and AUDATA1 to AUDATA0 indicate whether a 4-, 8-, 16-, or 32-bit address is to be output by comparing the previous fully output address with the address output this time (see table below).</li> </ol>

AUDATA1, AUDATA0	
00	Address bits A31 to A4 match; 4 address bits A3 to A0 are to be output (i.e. output is performed once).
01	Address bits A31 to A8 match; 8 address bits A3 to A0 and A7 to A4 are to be output (i.e. output is performed twice).
10	Address bits A31 to A16 match; 16 address bits A3 to A0, A7 to A4, A11 to A8, and A15 to A12 are to be output (i.e. output is performed four times).
11	None of the above cases applies; 31 address bits A3 to A0, A7 to A4, A11 to A8, and A15 to A12, A19 to A16, A23 to A20, A27 to A24, and A31 to A28 are to be output (i.e. output is performed eight times).

## Pin Functions in RAM Monitor Mode

Pin	Description
AUDCK	The external clock input pin. Input the clock to be used for debugging to this pin. The input frequency must not exceed 1/4 the operating frequency. When no connection is made, this pin is pulled up internally.
$\overline{\text{AUDSYNC}}$	Do not assert this pin until a command is input to AUDATA from off-chip and the necessary data can be prepared. See the protocol description for details. When no connection is made, this pin is pulled up internally.
AUDATA3 to AUDATA0	When a command is input from off-chip, data is output after Ready reception. Output starts when $\overline{\text{AUDSYNC}}$ is negated. See the protocol description for details. When no connections are made, these pins are pulled up internally.

## 17.3 Branch Trace Mode

### 17.3.1 Overview

In this mode, the branch destination address is output when a branch occurs in the user program. Branches may be caused by branch instruction execution or interrupt/exception processing, but no distinction is made between the two in this mode.

### 17.3.2 Operation

Operation starts in branch trace mode when  $\overline{\text{AUDRST}}$  is asserted, AUDMD is driven low, then  $\overline{\text{AUDRST}}$  is negated.

Figure 17.2 shows an example of data output.

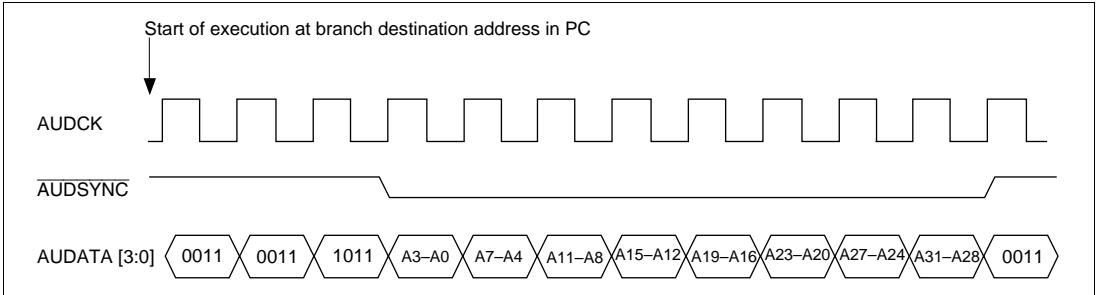
While the user program is being executed without branches, the AUDATA pins constantly output 0011 in synchronization with AUDCK.

When a branch occurs, after execution starts at the branch destination address in the PC, the previous fully output address (i.e. for which output was not interrupted by the occurrence of another branch) is compared with the current branch address, and depending on the result,  $\overline{\text{AUDSYNC}}$  is asserted and the branch destination address output after 1-clock output of 1000 (in the case of 4-bit output), 1001 (8-bit output), 1010 (16-bit output), or 1011 (32-bit output). The initial value of the compared address is H'00000000.

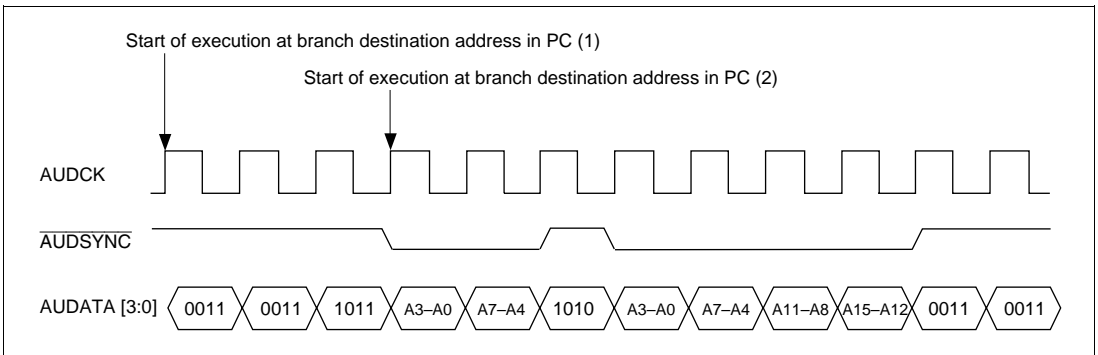
On completion of the cycle in which the address is output,  $\overline{\text{AUDSYNC}}$  is negated and 0011 is output from the AUDATA pins.

If another branch occurs during branch destination address output, the later branch has priority for output. In this case,  $\overline{\text{AUDSYNC}}$  is negated and the AUDATA pins output the address after outputting 10xx again (figure 17.3 shows an example of the output when consecutive branches occur). Note that the compared address is the previous fully output address, and not an interrupted address (since the upper address of an interrupted address will be unknown).

The interval from the start of execution at the branch destination address in the PC until the AUDATA pins output 10xx is 1.5 or 2 AUDCK cycles.



**Figure 17.2 Example of Data Output (32-Bit Output)**



**Figure 17.3 Example of Output in Case of Successive Branches**

## 17.4 RAM Monitor Mode

### 17.4.1 Overview

In this mode, all the modules connected to the SH7052F/SH7053F/SH7054F's internal or external bus can be read and written to, allowing RAM monitoring and tuning to be carried out.

### 17.4.2 Communication Protocol

The AUD latches the AUDATA input when  $\overline{\text{AUDSYNC}}$  is asserted. The following AUDATA input format should be used.

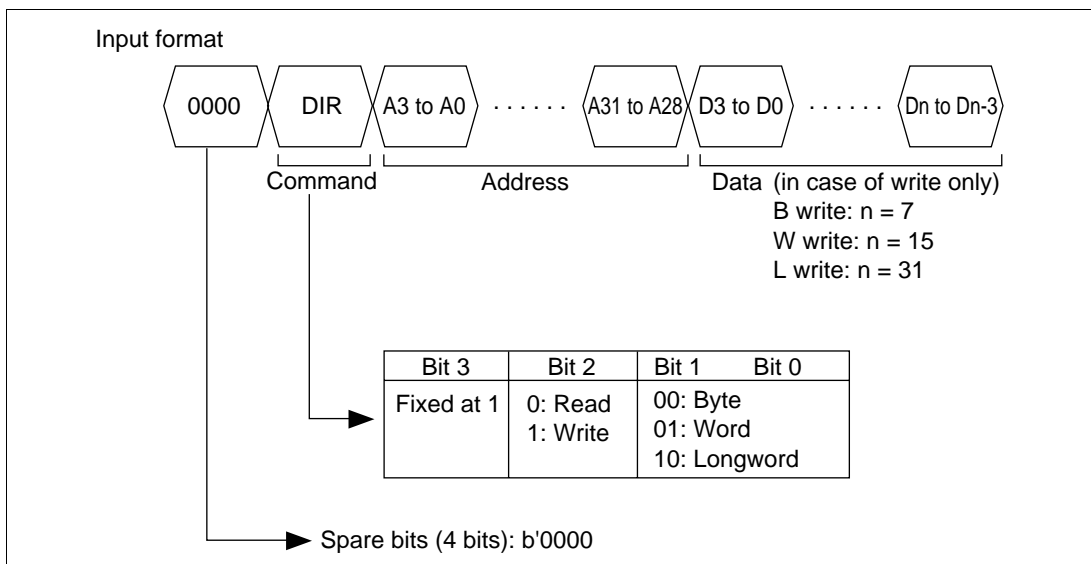


Figure 17.4 AUDATA Input Format

### 17.4.3 Operation

Operation starts in RAM monitor mode AUDMD is driven high after  $\overline{\text{AUDRST}}$  has been asserted, then  $\overline{\text{AUDRST}}$  is negated.

Figure 17.5 shows an example of a read operation, and figure 17.6 an example of a write operation.

When  $\overline{\text{AUDSYNC}}$  is asserted, input from the AUDATA pins begins. When a command, address, or data (writing only) is input in the format shown in figure 17.4 AUDATA Input Format, execution of read/write access to the specified address is started. During internal execution, the AUD returns Not Ready (0000). When execution is completed, the Ready flag (0001) is returned (figures 17.5 and 17.6).

In a read, data of the specified size is output when  $\overline{\text{AUDSYNC}}$  is negated following detection of this flag (figure 17.5).

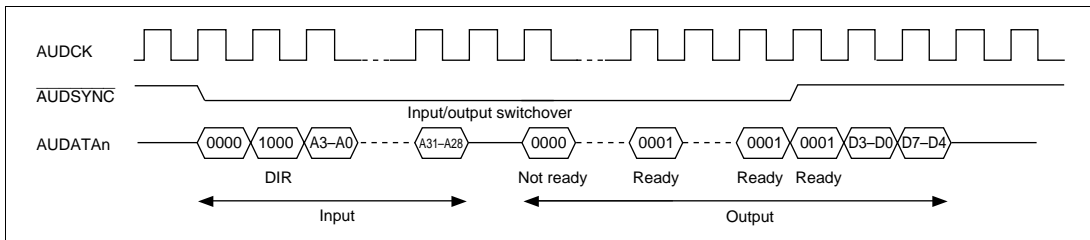
If a command other than the above is input in DIR, the AUD treats this as a command error, disables processing, and sets bit 1 in the Ready flag to 1. If a read/write operation initiated by the command specified in DIR causes a bus error, the AUD disables processing and sets bit 2 in the Ready flag to 1 (figure 17.7).

**Table 17.2 Ready Flag Format**

Bit 3	Bit 2	Bit 1	Bit 0
Fixed at 0	0: Normal status 1: Bus error	0: Normal status 1: Bus error	0: Not ready 1: Ready

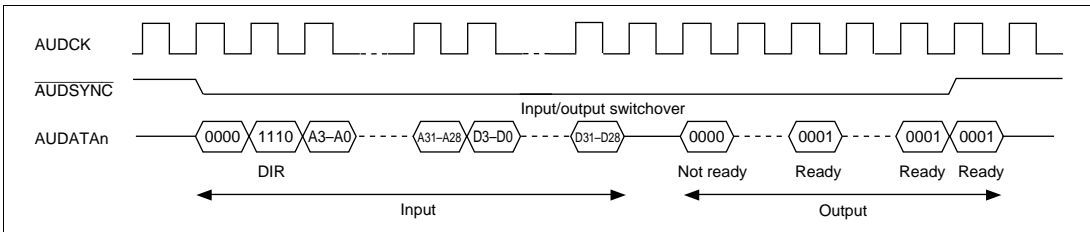
#### Bus error conditions

1. Word access to address  $4n+1$  or  $4n+3$
2. Longword access to address  $4n+1$ ,  $4n+2$ , or  $4n+3$
3. Longword access to on-chip I/O 8-bit space
4. Access to external space in single-chip mode

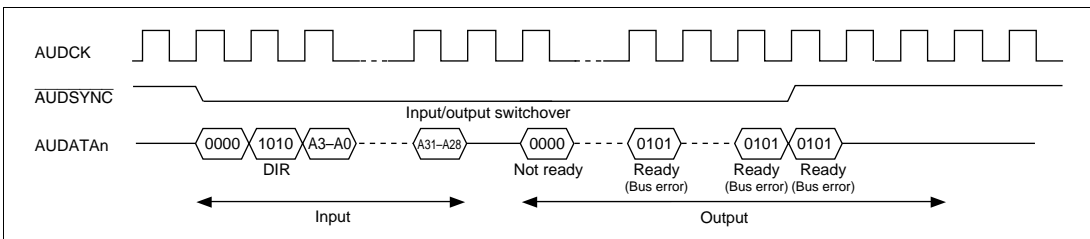


**Figure 17.5 Example of Read Operation (Byte Read)**





**Figure 17.6 Example of Write Operation (Longword Read)**



**Figure 17.7 Example of Error Occurrence (Longword Read)**

## 17.5 Usage Notes

### 17.5.1 Initialization

The debugger's internal buffers and processing states are initialized in the following cases:

1. In a power-on reset
2. In hardware standby mode
3. When  $\overline{\text{AUDRST}}$  is driven low
4. When the  $\overline{\text{AUDSRST}}$  bit is set to 1 in the SYSCR register (see section 23.2.2)
5. When the MSTOP3 bit is set to 1 in the MSTCR register (see section 23.2.3)

### 17.5.2 Operation in Software Standby Mode

The debugger is not initialized in software standby mode. However, since the SH7052F/SH7053F/SH7054F's internal operation halts in software standby mode:

1. When AUDMD is high (RAM monitor mode): Ready is not returned (Not Ready continues to be returned)  
However, when operating on an external clock, the protocol continues.
2. When AUDMD is low (PC trace): Operation stops. However, operation continues when STBY is released.

### 17.5.3 ROM Area Writes

Do not perform an AUD write to a ROM address immediately after an ATU register write cycle. For details, see “Writing to ROM Area Immediately after ATU Register Write” in section 10.7, Usage Notes.

# Section 18 Pin Function Controller (PFC)

## 18.1 Overview

The pin function controller (PFC) consists of registers for selecting multiplex pin functions and their input/output direction. Table 18.1 shows the SH7052F/SH7053F/SH7054F's multiplex pins.

**Table 18.1 SH7052F/SH7053F/SH7054F Multiplex Pins**

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)
A	PA0 input/output (port)	TIOA input (ATU)		
A	PA1 input/output (port)	TIOB input (ATU)		
A	PA2 input/output (port)	TIOC input (ATU)		
A	PA3 input/output (port)	TIOD input (ATU)		
A	PA4 input/output (port)	TIO3A input/output (ATU)		
A	PA5 input/output (port)	TIO3B input/output (ATU)		
A	PA6 input/output (port)	TIO3C input/output (ATU)		
A	PA7 input/output (port)	TIO3D input/output (ATU)		
A	PA8 input/output (port)	TIO4A input/output (ATU)		
A	PA9 input/output (port)	TIO4B input/output (ATU)		
A	PA10 input/output (port)	TIO4C input/output (ATU)		
A	PA11 input/output (port)	TIO4D input/output (ATU)		
A	PA12 input/output (port)	TIO5A input/output (ATU)		
A	PA13 input/output (port)	TIO5B input/output (ATU)		
A	PA14 input/output (port)	TxD0 output (SCI)		
A	PA15 input/output (port)	RxD0 input (SCI)		
B	PB0 input/output (port)	TO6A output (ATU)		
B	PB1 input/output (port)	TO6B output (ATU)		
B	PB2 input/output (port)	TO6C output (ATU)		
B	PB3 input/output (port)	TO6D output (ATU)		
B	PB4 input/output (port)	TO7A output (ATU)	TO8A output (ATU)	
B	PB5 input/output (port)	TO7B output (ATU)	TO8B output (ATU)	
B	PB6 input/output (port)	TO7C output (ATU)	TO8C output (ATU)	
B	PB7 input/output (port)	TO7D output (ATU)	TO8D output (ATU)	
B	PB8 input/output (port)	TxD3 output (SCI)	TO8E output (ATU)	
B	PB9 input/output (port)	RxD3 input (SCI)	TO8F output (ATU)	

**Table 18.1 SH7052F/SH7053F/SH7054F Multiplex Pins (cont)**

<b>Port</b>	<b>Function 1 (Related Module)</b>	<b>Function 2 (Related Module)</b>	<b>Function 3 (Related Module)</b>	<b>Function 4 (Related Module)</b>
B	PB10 input/output (port)	TxD4 output (SCI)	HTxD output (HCAN)	TO8G output (ATU)
B	PB11 input/output (port)	RxD4 input (SCI)	HRxD input (HCAN)	TO8H output (ATU)
B	PB12 input/output (port)	TCLKA input (ATU)	$\overline{\text{UBCTR}}\overline{\text{G}}$ output (UBC)	
B	PB13 input/output (port)	SCK0 input/output (SCI)		
B	PB14 input/output (port)	SCK1 input/output (SCI)	TCLKB input (ATU)	T110 input (ATU)
B	PB15 input/output (port)	PULS5 output (APC)	SCK2 input/output (SCI)	
C	PC0 input/output (port)	TxD1 output (SCI)		
C	PC1 input/output (port)	RxD1 input (SCI)		
C	PC2 input/output (port)	TxD2 output (SCI)		
C	PC3 input/output (port)	RxD2 input (SCI)		
C	PC4 input/output (port)	$\overline{\text{IRQ0}}$ input (INTC)		
D	PD0 input/output (port)	TIO1A input/output (ATU)		
D	PD1 input/output (port)	TIO1B input/output (ATU)		
D	PD2 input/output (port)	TIO1C input/output (ATU)		
D	PD3 input/output (port)	TIO1D input/output (ATU)		
D	PD4 input/output (port)	TIO1E input/output (ATU)		
D	PD5 input/output (port)	TIO1F input/output (ATU)		
D	PD6 input/output (port)	TIO1G input/output (ATU)		
D	PD7 input/output (port)	TIO1H input/output (ATU)		
D	PD8 input/output (port)	PULS0 output (APC)		
D	PD9 input/output (port)	PULS1 output (APC)		
D	PD10 input/output (port)	PULS2 output (APC)		
D	PD11 input/output (port)	PULS3 output (APC)		
D	PD12 input/output (port)	PULS4 output (APC)		
D	PD13 input/output (port)	PULS6 output (APC)	HTxD output (HCAN)	
E	PE0 input/output (port)	A0 output (BSC)		
E	PE1 input/output (port)	A1 output (BSC)		
E	PE2 input/output (port)	A2 output (BSC)		
E	PE3 input/output (port)	A3 output (BSC)		
E	PE4 input/output (port)	A4 output (BSC)		
E	PE5 input/output (port)	A5 output (BSC)		
E	PE6 input/output (port)	A6 output (BSC)		
E	PE7 input/output (port)	A7 output (BSC)		

**Table 18.1 SH7052F/SH7053F/SH7054F Multiplex Pins (cont)**

<b>Port</b>	<b>Function 1 (Related Module)</b>	<b>Function 2 (Related Module)</b>	<b>Function 3 (Related Module)</b>	<b>Function 4 (Related Module)</b>
E	PE8 input/output (port)	A8 output (BSC)		
E	PE9 input/output (port)	A9 output (BSC)		
E	PE10 input/output (port)	A10 output (BSC)		
E	PE11 input/output (port)	A11 output (BSC)		
E	PE12 input/output (port)	A12 output (BSC)		
E	PE13 input/output (port)	A13 output (BSC)		
E	PE14 input/output (port)	A14 output (BSC)		
E	PE15 input/output (port)	A15 output (BSC)		
F	PF0 input/output (port)	A16 output (BSC)		
F	PF1 input/output (port)	A17 output (BSC)		
F	PF2 input/output (port)	A18 output (BSC)		
F	PF3 input/output (port)	A19 output (BSC)		
F	PF4 input/output (port)	A20 output (BSC)		
F	PF5 input/output (port)	A21 output (BSC)	POD input (port)	
F	PF6 input/output (port)	$\overline{\text{WRL}}$ output (BSC)		
F	PF7 input/output (port)	$\overline{\text{WRH}}$ output (BSC)		
F	PF8 input/output (port)	$\overline{\text{WAIT}}$ input (BSC)		
F	PF9 input/output (port)	$\overline{\text{RD}}$ output (BSC)		
F	PF10 input/output (port)	$\overline{\text{CS0}}$ output (BSC)		
F	PF11 input/output (port)	$\overline{\text{CS1}}$ output (BSC)		
F	PF12 input/output (port)	$\overline{\text{CS2}}$ output (BSC)		
F	PF13 input/output (port)	$\overline{\text{CS3}}$ output (BSC)		
F	PF14 input/output (port)	$\overline{\text{BACK}}$ output (BSC)		
F	PF15 input/output (port)	$\overline{\text{BREQ}}$ input (BSC)		
G	PG0 input/output (port)	PULS7 output (APC)	HRxD input (HCAN)	
G	PG1 input/output (port)	$\overline{\text{IRQ1}}$ input (INTC)		
G	PG2 input/output (port)	$\overline{\text{IRQ2}}$ input (INTC)		
G	PG3 input/output (port)	$\overline{\text{IRQ3}}$ input (INTC)	ADTRG0 input (A/D)	
H	PH0 input/output (port)	D0 input/output (BSC)		
H	PH1 input/output (port)	D1 input/output (BSC)		
H	PH2 input/output (port)	D2 input/output (BSC)		
H	PH3 input/output (port)	D3 input/output (BSC)		
H	PH4 input/output (port)	D4 input/output (BSC)		

**Table 18.1 SH7052F/SH7053F/SH7054F Multiplex Pins (cont)**

<b>Port</b>	<b>Function 1 (Related Module)</b>	<b>Function 2 (Related Module)</b>	<b>Function 3 (Related Module)</b>	<b>Function 4 (Related Module)</b>
H	PH5 input/output (port)	D5 input/output (BSC)		
H	PH6 input/output (port)	D6 input/output (BSC)		
H	PH7 input/output (port)	D7 input/output (BSC)		
H	PH8 input/output (port)	D8 input/output (BSC)		
H	PH9 input/output (port)	D9 input/output (BSC)		
H	PH10 input/output (port)	D10 input/output (BSC)		
H	PH11 input/output (port)	D11 input/output (BSC)		
H	PH12 input/output (port)	D12 input/output (BSC)		
H	PH13 input/output (port)	D13 input/output (BSC)		
H	PH14 input/output (port)	D14 input/output (BSC)		
H	PH15 input/output (port)	D15 input/output (BSC)		
J	PJ0 input/output (port)	TIO2A input/output (ATU)		
J	PJ1 input/output (port)	TIO2B input/output (ATU)		
J	PJ2 input/output (port)	TIO2C input/output (ATU)		
J	PJ3 input/output (port)	TIO2D input/output (ATU)		
J	PJ4 input/output (port)	TIO2E input/output (ATU)		
J	PJ5 input/output (port)	TIO2F input/output (ATU)		
J	PJ6 input/output (port)	TIO2G input/output (ATU)		
J	PJ7 input/output (port)	TIO2H input/output (ATU)		
J	PJ8 input/output (port)	TIO5C input/output (ATU)		
J	PJ9 input/output (port)	TIO5D input/output (ATU)		
J	PJ10 input/output (port)	TI9A input (ATU)		
J	PJ11 input/output (port)	TI9B input (ATU)		
J	PJ12 input/output (port)	TI9C input (ATU)		
J	PJ13 input/output (port)	TI9D input (ATU)		
J	PJ14 input/output (port)	TI9E input (ATU)		
J	PJ15 input/output (port)	TI9F input (ATU)		
K	PK0 input/output (port)	TO8A output (ATU)		
K	PK1 input/output (port)	TO8B output (ATU)		
K	PK2 input/output (port)	TO8C output (ATU)		
K	PK3 input/output (port)	TO8D output (ATU)		
K	PK4 input/output (port)	TO8E output (ATU)		
K	PK5 input/output (port)	TO8F output (ATU)		

**Table 18.1 SH7052F/SH7053F/SH7054F Multiplex Pins (cont)**

<b>Port</b>	<b>Function 1 (Related Module)</b>	<b>Function 2 (Related Module)</b>	<b>Function 3 (Related Module)</b>	<b>Function 4 (Related Module)</b>
K	PK6 input/output (port)	TO8G output (ATU)		
K	PK7 input/output (port)	TO8H output (ATU)		
K	PK8 input/output (port)	TO8I output (ATU)		
K	PK9 input/output (port)	TO8J output (ATU)		
K	PK10 input/output (port)	TO8K output (ATU)		
K	PK11 input/output (port)	TO8L output (ATU)		
K	PK12 input/output (port)	TO8M output (ATU)		
K	PK13 input/output (port)	TO8N output (ATU)		
K	PK14 input/output (port)	TO8O output (ATU)		
K	PK15 input/output (port)	TO8P output (ATU)		

## 18.2 Register Configuration

PFC registers are listed in table 18.2.

**Table 18.2 PFC Registers**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port A IO register	PAIOR	R/W	H'0000	H'FFFFFF720	8, 16
Port A control register H	PACRH	R/W	H'0000	H'FFFFFF722	8, 16
Port A control register L	PACRL	R/W	H'0000	H'FFFFFF724	8, 16
Port B IO register	PBIOR	R/W	H'0000	H'FFFFFF730	8, 16
Port B control register H	PBCRH	R/W	H'0000	H'FFFFFF732	8, 16
Port B control register L	PBCRL	R/W	H'0000	H'FFFFFF734	8, 16
Port B invert register	PBIR	R/W	H'0000	H'FFFFFF736	8, 16
Port C IO register	PCIOR	R/W	H'0000	H'FFFFFF73A	8, 16
Port C control register	PCCR	R/W	H'0000	H'FFFFFF73C	8, 16
Port D IO register	PDIOR	R/W	H'0000	H'FFFFFF740	8, 16
Port D control register H	PDCRH	R/W	H'0000	H'FFFFFF742	8, 16
Port D control register L	PDCRL	R/W	H'0000	H'FFFFFF744	8, 16
Port E IO register	PEIOR	R/W	H'0000	H'FFFFFF750	8, 16
Port E control register	PECR	R/W	H'0000	H'FFFFFF752	8, 16
Port F IO register	PFIOR	R/W	H'0000	H'FFFFFF748	8, 16
Port F control register H	PFCRH	R/W	H'0015	H'FFFFFF74A	8, 16
Port F control register L	PFCRL	R/W	H'5000	H'FFFFFF74C	8, 16
Port G IO register	PGIOR	R/W	H'0000	H'FFFFFF760	8, 16
Port G control register	PGCR	R/W	H'0000	H'FFFFFF762	8, 16
Port H IO register	PHIOR	R/W	H'0000	H'FFFFFF728	8, 16
Port H control register	PHCR	R/W	H'0000	H'FFFFFF72A	8, 16
Port J IO register	PJIOR	R/W	H'0000	H'FFFFFF766	8, 16
Port J control register H	PJCRH	R/W	H'0000	H'FFFFFF768	8, 16
Port J control register L	PJCRL	R/W	H'0000	H'FFFFFF76A	8, 16
Port K IO register	PKIOR	R/W	H'0000	H'FFFFFF770	8, 16
Port K control register H	PKCRH	R/W	H'0000	H'FFFFFF772	8, 16
Port K control register L	PKCRL	R/W	H'0000	H'FFFFFF774	8, 16
Port K invert register	PKIR	R/W	H'0000	H'FFFFFF776	8, 16



## 18.3 Register Descriptions

### 18.3.1 Port A IO Register (PAIOR)

Bit:	15	14	13	12	11	10	9	8
	PA15 IOR	PA14 IOR	PA13 IOR	PA12 IOR	PA11 IOR	PA10 IOR	PA9 IOR	PA8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PA7 IOR	PA6 IOR	PA5 IOR	PA4 IOR	PA3 IOR	PA2 IOR	PA1 IOR	PA0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port A IO register (PAIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port A. Bits PA15IOR to PA0IOR correspond to pins PA15/RxD0 to PA0/TI0A. PAIOR is enabled when port A pins function as general input/output pins (PA15 to PA0) or ATU input/output pins, and disabled otherwise. For bits 3 to 0, when ATU input capture input is selected, the PAIOR bits should be cleared to 0.

When port A pins function as PA15 to PA0 or ATU input/output pins, a pin becomes an output when the corresponding bit in PAIOR is set to 1, and an input when the bit is cleared to 0.

PAIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.2 Port A Control Registers H and L (PACRH, PACRL)

Port A control registers H and L (PACRH, PACRL) are 16-bit readable/writable registers that select the functions of the 16 multiplex pins in port A. PACRH selects the functions of the pins for the upper 8 bits of port A, and PACRL selects the functions of the pins for the lower 8 bits.

PACRH and PACRL are initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. They are not initialized in software standby mode or sleep mode.

## Port A Control Register H (PACRH)

Bit:	15	14	13	12	11	10	9	8
	—	PA15MD	—	PA14MD	—	PA13MD	—	PA12MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

Bit:	7	6	5	4	3	2	1	0
	—	PA11MD	—	PA10MD	—	PA9MD	—	PA8MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PA15 Mode Bit (PA15MD): Selects the function of pin PA15/RxD0.

Bit 14: PA15MD	Description	
0	General input/output (PA15)	(Initial value)
1	Receive data input (RxD0)	

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PA14 Mode Bit (PA14MD): Selects the function of pin PA14/TxD0.

Bit 12: PA14MD	Description	
0	General input/output (PA14)	(Initial value)
1	Transmit data output (TxD0)	

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 10—PA13 Mode Bit (PA13MD): Selects the function of pin PA13/TIO5B.

Bit 10: PA13MD	Description	
0	General input/output (PA13)	(Initial value)
1	ATU input capture input/output compare output (TIO5B)	

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 8—PA12 Mode Bit (PA12MD): Selects the function of pin PA12/TIO5A.

Bit 8: PA12MD	Description
0	General input/output (PA12) (Initial value)
1	ATU input capture input/output compare output (TIO5A)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PA11 Mode Bit (PA11MD): Selects the function of pin PA11/TIO4D.

Bit 6: PA11MD	Description
0	General input/output (PA11) (Initial value)
1	ATU input capture input/output compare output (TIO4D)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PA10 Mode Bit (PA10MD): Selects the function of pin PA10/TIO4C.

Bit 4: PA10MD	Description
0	General input/output (PA10) (Initial value)
1	ATU input capture input/output compare output (TIO4C)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PA9 Mode Bit (PA9MD): Selects the function of pin PA9/TIO4B.

Bit 2: PA9MD	Description
0	General input/output (PA9) (Initial value)
1	ATU input capture input/output compare output (TIO4B)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PA8 Mode Bit (PA8MD): Selects the function of pin PA8/TIO4A.

Bit 0: PA8MD	Description
0	General input/output (PA8) (Initial value)
1	ATU input capture input/output compare output (TIO4A)

## Port A Control Register L (PACRL)

Bit:	15	14	13	12	11	10	9	8
	—	PA7MD	—	PA6MD	—	PA5MD	—	PA4MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	—	R/W	—	R/W	—	R/W	—	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PA3MD	—	PA2MD	—	PA1MD	—	PA0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	—	R/W	—	R/W	—	R/W	—	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PA7 Mode Bit (PA7MD): Selects the function of pin PA7/TIO3D.

Bit 14: PA7MD	Description
0	General input/output (PA7) (Initial value)
1	ATU input capture input/output compare output (TIO3D)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PA6 Mode Bit (PA6MD): Selects the function of pin PA6/TIO3C.

Bit 12: PA6MD	Description
0	General input/output (PA6) (Initial value)
1	ATU input capture input/output compare output (TIO3C)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 10—PA5 Mode Bit (PA5MD): Selects the function of pin PA5/TIO3B.

Bit 10: PA5MD	Description
0	General input/output (PA5) (Initial value)
1	ATU input capture input/output compare output (TIO3B)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 8—PA4 Mode Bit (PA4MD): Selects the function of pin PA4/TIO3A.

Bit 8: PA4MD	Description
0	General input/output (PA4) (Initial value)
1	ATU input capture input/output compare output (TIO3A)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PA3 Mode Bit (PA3MD): Selects the function of pin PA3/TIOD.

Bit 6: PA3MD	Description
0	General input/output (PA3) (Initial value)
1	ATU input capture input (TIOD)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PA2 Mode Bit (PA2MD): Selects the function of pin PA2/TIOC.

Bit 4: PA2MD	Description
0	General input/output (PA2) (Initial value)
1	ATU input capture input (TIOC)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PA1 Mode Bit (PA1MD): Selects the function of pin PA1/TIOB.

Bit 2: PA1MD	Description
0	General input/output (PA1) (Initial value)
1	ATU input capture input (TIOB)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PA0 Mode Bit (PA0MD): Selects the function of pin PA0/TIOA.

Bit 0: PA0MD	Description
0	General input/output (PA0) (Initial value)
1	ATU input capture input (TIOA)

### 18.3.3 Port B IO Register (PBIOR)

Bit:	15	14	13	12	11	10	9	8
	PB15 IOR	PB14 IOR	PB13 IOR	PB12 IOR	PB11 IOR	PB10 IOR	PB9 IOR	PB8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PB7 IOR	PB6 IOR	PB5 IOR	PB4 IOR	PB3 IOR	PB2 IOR	PB1 IOR	PB0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port B IO register (PBIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port B. Bits PB15IOR to PB0IOR correspond to pins PB15/PULS5/SCK2 to PB0/TO6A. PBIOR is enabled when port B pins function as general input/output pins (PB15 to PB0) or serial clock pins (SCK0, SCK1, SCK2), and disabled otherwise.

When port B pins function as PB15 to PB0 or SCK0, SCK1, and SCK2, a pin becomes an output when the corresponding bit in PBIOR is set to 1, and an input when the bit is cleared to 0.

PBIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.4 Port B Control Registers H and L (PBCRH, PBCRL)

Port B control registers H and L (PBCRH, PBCRL) are 16-bit readable/writable registers that select the functions of the 16 multiplex pins in port B. PBCRH selects the functions of the pins for the upper 8 bits of port B, and PBCRL selects the functions of the pins for the lower 8 bits.

PBCRH and PBCRL are initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. They are not initialized in software standby mode or sleep mode.

## Port B Control Register H (PBCRH)

Bit:	15	14	13	12	11	10	9	8
	PB15 MD1	PB15 MD0	PB14 MD1	PB14 MD0	—	PB13 MD	PB12 MD1	PB12 MD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PB11 MD1	PB11 MD0	PB10 MD1	PB10 MD0	PB9 MD1	PB9 MD0	PB8 MD1	PB8 MD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bits 15 and 14—PB15 Mode Bits 1 and 0 (PB15MD1, PB15MD0): These bits select the function of pin PB15/PULS5/SCK2.

Bit 15: PB15MD1	Bit 14: PB15MD0	Description
0	0	General input/output (PB15) (Initial value)
	1	APC pulse output (PULS5)
1	0	Serial clock input/output (SCK2)
	1	Reserved (Do not set)

- Bits 13 and 12—PB14 Mode Bits 1 and 0 (PB14MD1, PB14MD0): These bits select the function of pin PB14/SCK1/TCLKB/T110.

Bit 13: PB14MD1	Bit 12: PB14MD0	Description
0	0	General input/output (PB14) (Initial value)
	1	Serial clock input/output (SCK1)
1	0	ATU clock input (TCLKB)
	1	ATU edge input (T110)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 10—PB13 Mode Bit (PB13MD): Selects the function of pin PB13/SCK0.

Bit 10: PB13MD	Description
0	General input/output (PB13) (Initial value)
1	Serial clock input/output (SCK0)

- Bits 9 and 8—PB12 Mode Bits 1 and 0 (PB12MD1, PB12MD0): These bits select the function of pin PB12/TCLKA/ $\overline{\text{UBCTRG}}$ .

Bit 9: PB12MD1	Bit 8: PB12MD0	Description
0	0	General input/output (PB12) (Initial value)
	1	ATU clock input (TCLKA)
1	0	Trigger pulse output ( $\overline{\text{UBCTRG}}$ )
	1	Reserved (Do not set)

- Bits 7 and 6—PB11 Mode Bits 1 and 0 (PB11MD1, PB11MD0): These bits select the function of pin PB11/RxD4/HRxD0/TO8H.

Bit 7: PB11MD1	Bit 6: PB11MD0	Description
0	0	General input/output (PB11) (Initial value)
	1	Receive data input (RxD4)
1	0	HCAN receive data input (HRxD)
	1	ATU one-shot pulse output (TO8H)

- Bits 5 and 4—PB10 Mode Bits 1 and 0 (PB10MD1, PB10MD0): These bits select the function of pin PB10/TxD4/HTxD0/TO8G.

Bit 5: PB10MD1	Bit 4: PB10MD0	Description
0	0	General input/output (PB10) (Initial value)
	1	Transmit data output (TxD4)
1	0	HCAN transmit data output (HTxD)
	1	ATU one-shot pulse output (TO8G)



- Bits 3 and 2—PB9 Mode Bits 1 and 0 (PB9MD1, PB9MD0): These bits select the function of pin PB9/RxD3/TO8F.

Bit 3: PB9MD1	Bit 2: PB9MD0	Description
0	0	General input/output (PB9) (Initial value)
	1	Receive data input (RxD3)
1	0	ATU one-shot pulse output (TO8F)
	1	Reserved (Do not set)

- Bits 1 and 0—PB8 Mode Bits 1 and 0 (PB8MD1, PB8MD0): These bits select the function of pin PB8/TxD3/TO8E.

Bit 1: PB8MD1	Bit 0: PB8MD0	Description
0	0	General input/output (PB8) (Initial value)
	1	Transmit data output (TxD3)
1	0	ATU one-shot pulse output (TO8E)
	1	Reserved (Do not set)

### Port B Control Register L (PBCRL)

Bit:	15	14	13	12	11	10	9	8
	PB7MD1	PB7MD0	PB6MD1	PB6MD0	PB5MD1	PB5MD0	PB4MD1	PB4MD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	—	PB3MD	—	PB2MD	—	PB1MD	—	PB0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bits 15 and 14—PB7 Mode Bits 1 and 0 (PB7MD1, PB7MD0): These bits select the function of pin PB7/TO7D/TO8D.

Bit 15: PB7MD1	Bit 14: PB7MD0	Description
0	0	General input/output (PB7) (Initial value)
	1	ATU PWM output (TO7D)
1	0	ATU one-shot pulse output (TO8D)
	1	Reserved (Do not set)

- Bits 13 and 12—PB6 Mode Bits 1 and 0 (PB6MD1, PB6MD0): These bits select the function of pin PB6/TO7C/TO8C.

Bit 13: PB6MD1	Bit 12: PB6MD0	Description
0	0	General input/output (PB6) (Initial value)
	1	ATU PWM output (TO7C)
1	0	ATU one-shot pulse output (TO8C)
	1	Reserved (Do not set)

- Bits 11 and 10—PB5 Mode Bits 1 and 0 (PB5MD1, PB5MD0): These bits select the function of pin PB5/TO7B/TO8B.

Bit 11: PB5MD1	Bit 10: PB5MD0	Description
0	0	General input/output (PB5) (Initial value)
	1	ATU PWM output (TO7B)
1	0	ATU one-shot pulse output (TO8B)
	1	Reserved (Do not set)

- Bits 9 and 8—PB4 Mode Bits 1 and 0 (PB4MD1, PB4MD0): These bits select the function of pin PB4/TO7A/TO8A.

Bit 9: PB4MD1	Bit 8: PB4MD0	Description
0	0	General input/output (PB4) (Initial value)
	1	ATU PWM output (TO7A)
1	0	ATU one-shot pulse output (TO8A)
	1	Reserved (Do not set)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 6—PB3 Mode Bit (PB3MD): Selects the function of pin PB3/TO6D.

Bit 6: PB3MD	Description
0	General input/output (PB3) (Initial value)
1	ATU PWM output (TO6D)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 4—PB2 Mode Bit (PB2MD): Selects the function of pin PB2/TO6C.

Bit 4: PB2MD	Description
0	General input/output (PB2) (Initial value)
1	ATU PWM output (TO6C)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 2—PB1 Mode Bit (PB1MD): Selects the function of pin PB1/TO6B.

Bit 2: PB1MD	Description
0	General input/output (PB1) (Initial value)
1	ATU PWM output (TO6B)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 0—PB0 Mode Bit (PB0MD): Selects the function of pin PB0/TO6A.

Bit 0: PB0MD	Description
0	General input/output (PB0) (Initial value)
1	ATU PWM output (TO6A)

### 18.3.5 Port B Invert Register (PBIR)

Bit:	15	14	13	12	11	10	9	8
	PB15IR	PB14IR	PB13IR	—	PB11IR	PB10IR	PB9IR	PB8IR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PB7IR	PB6IR	PB5IR	PB4IR	PB3IR	PB2IR	PB1IR	PB0IR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port B invert register (PBIR) is a 16-bit readable/writable register that sets the port B inversion function. Bits PB15IR to PB13IR and PB11IR to PB0IR correspond to pins PB15/PULS5/SCK2 to PB13/SCK0 and PB11/RxD4/HRxD0/TO8H to PB0/TO6A. PBIR is enabled when port B pins function as ATU outputs or serial clock pins, and disabled otherwise.

When port B pins function as ATU outputs or serial clock pins, the value of a pin is inverted when the corresponding bit in PBIR is set to 1.

PBIR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

PBnIR	Description
0	Value is not inverted (Initial value)
1	Value is inverted

n = 15 to 0

### 18.3.6 Port C IO Register (PCIOR)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	PC4IOR	PC3IOR	PC2IOR	PC1IOR	PC0IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

The port C IO register (PCIOR) is a 16-bit readable/writable register that selects the input/output direction of the 5 pins in port C. Bits PC4IOR to PC0IOR correspond to pins PC4/ $\overline{\text{IRQ0}}$  to PC0/TxD1. PCIOR is enabled when port C pins function as general input/output pins (PC4 to PC0), and disabled otherwise.

When port C pins function as PC4 to PC0, a pin becomes an output when the corresponding bit in PCIOR is set to 1, and an input when the bit is cleared to 0.

PCIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.7 Port C Control Register (PCCR)

The port C control register (PCCR) is a 16-bit readable/writable register that selects the functions of the 5 multiplex pins in port C.

PCCR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	PC4MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PC3MD	—	PC2MD	—	PC1MD	—	PC0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bits 15 to 9—Reserved: These bits always read 0. The write value should always be 0.
- Bit 8—PC4 Mode Bit (PC4MD): Selects the function of pin PC4/ $\overline{\text{IRQ0}}$ .

Bit 8: PC4MD	Description	
0	General input/output (PC4)	(Initial value)
1	Interrupt request input ( $\overline{\text{IRQ0}}$ )	

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PC3 Mode Bit (PC3MD): Selects the function of pin PC3/RxD2.

Bit 6: PC3MD	Description	
0	General input/output (PC3)	(Initial value)
1	Receive data input (RxD2)	

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PC2 Mode Bit (PC2MD): Selects the function of pin PC2/TxD2.

Bit 4: PC2MD	Description	
0	General input/output (PC2)	(Initial value)
1	Transmit data output (TxD2)	

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PC1 Mode Bit (PC1MD): Selects the function of pin PC1/RxD1.

Bit 2: PC1MD	Description	
0	General input/output (PC1)	(Initial value)
1	Receive data input (RxD1)	

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PC0 Mode Bit (PC0MD): Selects the function of pin PC0/TxD1.

Bit 0: PC0MD	Description	
0	General input/output (PC0)	(Initial value)
1	Transmit data output (TxD1)	

### 18.3.8 Port D IO Register (PDIOR)

Bit:	15	14	13	12	11	10	9	8
	—	—	PD13 IOR	PD12 IOR	PD11 IOR	PD10 IOR	PD9 IOR	PC8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PD7 IOR	PD6 IOR	PD5 IOR	PD4 IOR	PD3 IOR	PD2 IOR	PD1 IOR	PD0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port D IO register (PDIOR) is a 16-bit readable/writable register that selects the input/output direction of the 14 pins in port D. Bits PD13IOR to PD0IOR correspond to pins PD13/PULS6/HTxD0/HTxD1 to PD0/TIO1A. PDIOR is enabled when port D pins function as general input/output pins (PD13 to PD0) or timer input/output pins, and disabled otherwise.

When port D pins function as PD13 to PD0 or timer input/output pins, a pin becomes an output when the corresponding bit in PDIOR is set to 1, and an input when the bit is cleared to 0.

PDIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.



### 18.3.9 Port D Control Registers H and L (PDCRH, PDCRL)

Port D control registers H and L (PDCRH, PDCRL) are 16-bit readable/writable registers that select the functions of the 14 multiplex pins in port D. PDCRH selects the functions of the pins for the upper 6 bits of port D, and PDCRL selects the functions of the pins for the lower 8 bits.

PDCRH and PDCRL are initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. They are not initialized in software standby mode or sleep mode.

#### Port D Control Register H (PDCRH)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	PD13 MD1	PD13 MD0	—	PD12 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PD11 MD	—	PD10 MD	—	PD9 MD	—	PD8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bits 15 to 12—Reserved: These bits always read 0. The write value should always be 0.
- Bits 11 and 10—PD13 Mode Bits 1 and 0 (PD13MD1, PD13MD0): These bits select the function of pin PD13/PULS6/HTxD.

Bit 11: PD13MD1	Bit 10: PD13MD0	Description
0	0	General input/output (PD13) (Initial value)
	1	APC pulse output (PULS6)
1	0	HCAN transmit data output (HTxD)
	1	Reserved (Do not set)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 8—PD12 Mode Bit (PD12MD): Selects the function of pin PD12/PULS4.

Bit 8: PD12MD	Description	
0	General input/output (PD12)	(Initial value)
1	APC pulse output (PULS4)	

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 6—PD11 Mode Bit (PD11MD): Selects the function of pin PD11/PULS3.

Bit 6: PD11MD	Description	
0	General input/output (PD11)	(Initial value)
1	APC pulse output (PULS3)	

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 4—PD10 Mode Bit (PD10MD): Selects the function of pin PD10/PULS2.

Bit 4: PD10MD	Description	
0	General input/output (PD10)	(Initial value)
1	APC pulse output (PULS2)	

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 2—PD9 Mode Bit (PD9MD): Selects the function of pin PD9/PULS1.

Bit 2: PD9MD	Description	
0	General input/output (PD9)	(Initial value)
1	APC pulse output (PULS1)	

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 0—PD8 Mode Bit (PD8MD): Selects the function of pin PD8/PULS0.

Bit 0: PD8MD	Description	
0	General input/output (PD8)	(Initial value)
1	APC pulse output (PULS0)	

## Port D Control Register L (PDCRL)

Bit:	15	14	13	12	11	10	9	8
	—	PD7MD	—	PD6MD	—	PD5MD	—	PD4MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PD3MD	—	PD2MD	—	PD1MD	—	PD0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PD7 Mode Bit (PD7MD): Selects the function of pin PD7/TIO1H.

Bit 14: PD7MD	Description
0	General input/output (PD7) <span style="float: right;">(Initial value)</span>
1	ATU input capture input/output compare output (TIO1H)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PD6 Mode Bit (PD6MD): Selects the function of pin PD6/TIO1G.

Bit 12: PD6MD	Description
0	General input/output (PD6) <span style="float: right;">(Initial value)</span>
1	ATU input capture input/output compare output (TIO1G)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 10—PD5 Mode Bit (PD5MD): Selects the function of pin PD5/TIO1F.

Bit 10: PD5MD	Description
0	General input/output (PD5) <span style="float: right;">(Initial value)</span>
1	ATU input capture input/output compare output (TIO1F)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 8—PD4 Mode Bit (PD4MD): Selects the function of pin PD4/TIO1E.

Bit 8: PD4MD	Description
0	General input/output (PD4) (Initial value)
1	ATU input capture input/output compare output (TIO1E)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 6—PD3 Mode Bit (PD3MD): Selects the function of pin PD3/TIO1D.

Bit 6: PD3MD	Description
0	General input/output (PD3) (Initial value)
1	ATU input capture input/output compare output (TIO1D)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 4—PD2 Mode Bit (PD2MD): Selects the function of pin PD2/TIO1C.

Bit 4: PD2MD	Description
0	General input/output (PD2) (Initial value)
1	ATU input capture input/output compare output (TIO1C)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 2—PD1 Mode Bit (PD1MD): Selects the function of pin PD1/TIO1B.

Bit 2: PD1MD	Description
0	General input/output (PD1) (Initial value)
1	ATU input capture input/output compare output (TIO1B)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 0—PD0 Mode Bit (PD0MD): Selects the function of pin PD0/TIO1A.

Bit 0: PD0MD	Description
0	General input/output (PD0) (Initial value)
1	ATU input capture input/output compare output (TIO1A)

### 18.3.10 Port E IO Register (PEIOR)

Bit:	15	14	13	12	11	10	9	8
	PE15 IOR	PE14 IOR	PE13 IOR	PE12 IOR	PE11 IOR	PE10 IOR	PE9 IOR	PE8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PE7 IOR	PE6 IOR	PE5 IOR	PE4 IOR	PE3 IOR	PE2 IOR	PE1 IOR	PE0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port E IO register (PEIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port E. Bits PE15IOR to PE0IOR correspond to pins PE15/A15 to PE0/A0. PEIOR is enabled when port E pins function as general input/output pins (PE15 to PE0), and disabled otherwise.

When port E pins function as PE15 to PE0, a pin becomes an output when the corresponding bit in PEIOR is set to 1, and an input when the bit is cleared to 0.

PEIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.11 Port E Control Register (PECR)

Bit:	15	14	13	12	11	10	9	8
	PE15 MD	PE14 MD	PE13 MD	PE12 MD	PE11 MD	PE10 MD	PE9 MD	PE8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PE7 MD	PE6 MD	PE5 MD	PE4 MD	PE3 MD	PE2 MD	PE1 MD	PE0 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port E control register (PECR) is a 16-bit readable/writable register that selects the functions of the 16 multiplex pins in port E. PECR settings are not valid in all operating modes.

- Expanded mode with on-chip ROM disabled  
Port E pins function as address output pins, and PECR settings are invalid.
- Expanded mode with on-chip ROM enabled  
Port E pins are multiplexed as address output pins and general input/output pins. PECR settings are valid.
- Single-chip mode  
Port E pins function as general input/output pins, and PECR settings are invalid.

PECR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

- Bit 15—PE15 Mode Bit (PE15MD): Selects the function of pin PE15/A15.

#### Description

Bit 15: PE15MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A15) (Initial value)	General input/output (PE15) (Initial value)	General input/output (PE15) (Initial value)
1	Address output (A15)	Address output (A15)	General input/output (PE15)

- Bit 14—PE14 Mode Bit (PE14MD): Selects the function of pin PE14/A14.

Description			
Bit 14: PE14MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A14) (Initial value)	General input/output (PE14) (Initial value)	General input/output (PE14) (Initial value)
1	Address output (A14)	Address output (A14)	General input/output (PE14)

- Bit 13—PE13 Mode Bit (PE13MD): Selects the function of pin PE13/A13.

Description			
Bit 13: PE13MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A13) (Initial value)	General input/output (PE13) (Initial value)	General input/output (PE13) (Initial value)
1	Address output (A13)	Address output (A13)	General input/output (PE13)

- Bit 12—PE12 Mode Bit (PE12MD): Selects the function of pin PE12/A12.

Description			
Bit 12: PE12MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A12) (Initial value)	General input/output (PE12) (Initial value)	General input/output (PE12) (Initial value)
1	Address output (A12)	Address output (A12)	General input/output (PE12)

- Bit 11—PE11 Mode Bit (PE11MD): Selects the function of pin PE11/A11.

Description			
Bit 11: PE11MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A11) (Initial value)	General input/output (PE11) (Initial value)	General input/output (PE11) (Initial value)
1	Address output (A11)	Address output (A11)	General input/output (PE11)

- Bit 10—PE10 Mode Bit (PE10MD): Selects the function of pin PE10/A10.

#### Description

Bit 10: PE10MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A10) (Initial value)	General input/output (PE10) (Initial value)	General input/output (PE10) (Initial value)
1	Address output (A10)	Address output (A10)	General input/output (PE10)

- Bit 9—PE9 Mode Bit (PE9MD): Selects the function of pin PE9/A9.

#### Description

Bit 9: PE9MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A9) (Initial value)	General input/output (PE9) (Initial value)	General input/output (PE9) (Initial value)
1	Address output (A9)	Address output (A9)	General input/output (PE9)

- Bit 8—PE8 Mode Bit (PE8MD): Selects the function of pin PE8/A8.

#### Description

Bit 8: PE8MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A8) (Initial value)	General input/output (PE8) (Initial value)	General input/output (PE8) (Initial value)
1	Address output (A8)	Address output (A8)	General input/output (PE8)

- Bit 7—PE7 Mode Bit (PE7MD): Selects the function of pin PE7/A7.

#### Description

Bit 7: PE7MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A7) (Initial value)	General input/output (PE7) (Initial value)	General input/output (PE7) (Initial value)
1	Address output (A7)	Address output (A7)	General input/output (PE7)



- Bit 6—PE6 Mode Bit (PE6MD): Selects the function of pin PE6/A6.

Description			
Bit 6: PE6MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A6) (Initial value)	General input/output (PE6) (Initial value)	General input/output (PE6) (Initial value)
1	Address output (A6)	Address output (A6)	General input/output (PE6)

- Bit 5—PE5 Mode Bit (PE5MD): Selects the function of pin PE5/A5.

Description			
Bit 5: PE5MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A5) (Initial value)	General input/output (PE5) (Initial value)	General input/output (PE5) (Initial value)
1	Address output (A5)	Address output (A5)	General input/output (PE5)

- Bit 4—PE4 Mode Bit (PE4MD): Selects the function of pin PE4/A4.

Description			
Bit 4: PE4MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A4) (Initial value)	General input/output (PE4) (Initial value)	General input/output (PE4) (Initial value)
1	Address output (A4)	Address output (A4)	General input/output (PE4)

- Bit 3—PE3 Mode Bit (PE3MD): Selects the function of pin PE3/A3.

Description			
Bit 3: PE3MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A3) (Initial value)	General input/output (PE3) (Initial value)	General input/output (PE3) (Initial value)
1	Address output (A3)	Address output (A3)	General input/output (PE3)

- Bit 2—PE2 Mode Bit (PE2MD): Selects the function of pin PE2/A2.

#### Description

Bit 2: PE2MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A2) (Initial value)	General input/output (PE2) (Initial value)	General input/output (PE2) (Initial value)
1	Address output (A2)	Address output (A2)	General input/output (PE2)

- Bit 1—PE1 Mode Bit (PE1MD): Selects the function of pin PE1/A1.

#### Description

Bit 1: PE1MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A1) (Initial value)	General input/output (PE1) (Initial value)	General input/output (PE1) (Initial value)
1	Address output (A1)	Address output (A1)	General input/output (PE1)

- Bit 0—PE0 Mode Bit (PE0MD): Selects the function of pin PE0/A0.

#### Description

Bit 0: PE0MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A0) (Initial value)	General input/output (PE0) (Initial value)	General input/output (PE0) (Initial value)
1	Address output (A0)	Address output (A0)	General input/output (PE0)

### 18.3.12 Port F IO Register (PFIOR)

Bit:	15	14	13	12	11	10	9	8
	PF15 IOR	PF14 IOR	PF13 IOR	PF12 IOR	PF11 IOR	PF10 IOR	PF9 IOR	PF8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PF7 IOR	PF6 IOR	PF5 IOR	PF4 IOR	PF3 IOR	PF2 IOR	PF1 IOR	PF0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port F IO register (PFIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port F. Bits PF15IOR to PF0IOR correspond to pins PF15/ $\overline{\text{BREQ}}$  to PF0/A16. PFIOR is enabled when port F pins function as general input/output pins (PF15 to PF0), and disabled otherwise.

When port F pins function as PF15 to PF0, a pin becomes an output when the corresponding bit in PFIOR is set to 1, and an input when the bit is cleared to 0.

PFIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.13 Port F Control Registers H and L (PFCRH, PFCRL)

Port F control registers H and L (PFCRH, PFCRL) are 16-bit readable/writable registers that select the functions of the 16 multiplex pins in port F and the function of the CK pin. PFCRH selects the functions of the pins for the upper 8 bits of port F, and PFCRL selects the functions of the pins for the lower 8 bits.

PFCRH and PFCRL are initialized to H'0015 and H'5000, respectively, by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. They are not initialized in software standby mode or sleep mode.

#### Port F Control Register H (PFCRH)

Bit:	15	14	13	12	11	10	9	8
	CKHIZ	PF15MD	—	PF14MD	—	PF13MD	—	PF12MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R	R/W	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PF11MD	—	PF10MD	—	PF9MD	—	PF8MD
Initial value:	0	0	0	1	0	1	0	1
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—CKHIZ Bit: Selects the function of pin CK.

Bit: CKHIZ	Description
0	CK pin output (Initial value)
1	CK pin Hi-Z

- Bit 14—PF15 Mode Bit (PF15MD): Selects the function of pin PF15/ $\overline{\text{BREQ}}$ .

Bit 14: PF15MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF15) (Initial value)	General input/output (PF15) (Initial value)
1	Bus request input ( $\overline{\text{BREQ}}$ )	General input/output (PF15)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PF14 Mode Bit (PF14MD): Selects the function of pin PF14/ $\overline{\text{BACK}}$ .

Bit 12: PF14MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF14) (Initial value)	General input/output (PF14) (Initial value)
1	Bus acknowledge output ( $\overline{\text{BACK}}$ )	General input/output (PF14)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 10—PF13 Mode Bit (PF13MD): Selects the function of pin PF13/ $\overline{\text{CS3}}$ .

Bit 10: PF13MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF13) (Initial value)	General input/output (PF13) (Initial value)
1	Chip select output ( $\overline{\text{CS3}}$ )	General input/output (PF13)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 8—PF12 Mode Bit (PF12MD): Selects the function of pin PF12/ $\overline{\text{CS2}}$ .

Bit 8: PF12MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF12) (Initial value)	General input/output (PF12) (Initial value)
1	Chip select output ( $\overline{\text{CS2}}$ )	General input/output (PF12)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PF11 Mode Bit (PF11MD): Selects the function of pin PF11/ $\overline{\text{CS1}}$ .

Bit 6: PF11MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF11) (Initial value)	General input/output (PF11) (Initial value)
1	Chip select output ( $\overline{\text{CS1}}$ )	General input/output (PF11)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PF10 Mode Bit (PF10MD): Selects the function of pin PF10/ $\overline{CS0}$ .

Bit 4: PF10MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF10)	General input/output (PF10)
1	Chip select output ( $\overline{CS0}$ ) (Initial value)	General input/output (PF10) (Initial value)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PF9 Mode Bit (PF9MD): Selects the function of pin PF9/ $\overline{RD}$ .

Bit 2: PF9MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF9)	General input/output (PF9)
1	Read output ( $\overline{RD}$ ) (Initial value)	General input/output (PF9) (Initial value)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PF8 Mode Bit (PF8MD): Selects the function of pin PF8/ $\overline{WAIT}$ .

Bit 0: PF8MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF8)	General input/output (PF8)
1	Wait state input ( $\overline{WAIT}$ ) (Initial value)	General input/output (PF8) (Initial value)

## Port F Control Register L (PFCRL)

Bit:	15	14	13	12	11	10	9	8
	—	PF7MD	—	PF6MD	PF5MD1	PF5MD0	—	PF4MD
Initial value:	0	1	0	1	0	0	0	0
R/W:	R	R/W	R	R/W	R/W	R/W	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PF3MD	—	PF2MD	—	PF1MD	—	PF0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PF7 Mode Bit (PF7MD): Selects the function of pin PF7/ $\overline{\text{WRH}}$ .

Bit 14: PF7MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF7)	General input/output (PF7)
1	Upper write output ( $\overline{\text{WRH}}$ ) (Initial value)	General input/output (PF7) (Initial value)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PF6 Mode Bit (PF6MD): Selects the function of pin PF6/ $\overline{\text{WRL}}$ .

Bit 12: PF6MD	Description	
	Expanded Mode	Single-Chip Mode
0	General input/output (PF6)	General input/output (PF6)
1	Lower write output ( $\overline{\text{WRL}}$ ) (Initial value)	General input/output (PF6) (Initial value)

- Bits 11 and 10—PF5 Mode Bits 1 and 0 (PF5MD1, PF5MD0): These bits select the function of pin PF5/A21/POD.

		Description		
Bit 11: PF5MD1	Bit 10: PF5MD0	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	0	Address output (A21) (Initial value)	General input/output (PF5) (Initial value)	General input/output (PF5) (Initial value)
	1	Address output (A21)	Address output (A21)	General input/output (PF5)
1	0	Address output (A21)	Port output disable input (POD)	Port output disable input ( $\overline{\text{POD}}$ )
	1	Reserved (Do not set)	Reserved (Do not set)	Reserved (Do not set)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 8—PF4 Mode Bit (PF4MD): Selects the function of pin PF4/A20.

		Description		
Bit 8: PF4MD		Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0		Address output (A20) (Initial value)	General input/output (PF4) (Initial value)	General input/output (PF4) (Initial value)
1		Address output (A20)	Address output (A20)	General input/output (PF4)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PF3 Mode Bit (PF3MD): Selects the function of pin PF3/A19.

		Description		
Bit 6: PF3MD		Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0		Address output (A19) (Initial value)	General input/output (PF3) (Initial value)	General input/output (PF3) (Initial value)
1		Address output (A19)	Address output (A19)	General input/output (PF3)



- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PF2 Mode Bit (PF2MD): Selects the function of pin PF2/A18.

Description			
Bit 4: PF2MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A18) (Initial value)	General input/output (PF2) (Initial value)	General input/output (PF2) (Initial value)
1	Address output (A18)	Address output (A18)	General input/output (PF2)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PF1 Mode Bit (PF1MD): Selects the function of pin PF1/A17.

Description			
Bit 2: PF1MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A17) (Initial value)	General input/output (PF1) (Initial value)	General input/output (PF1) (Initial value)
1	Address output (A17)	Address output (A17)	General input/output (PF1)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PF0 Mode Bit (PF0MD): Selects the function of pin PF0/A16.

Description			
Bit 0: PF0MD	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Address output (A16) (Initial value)	General input/output (PF0) (Initial value)	General input/output (PF0) (Initial value)
1	Address output (A16)	Address output (A16)	General input/output (PF0)

### 18.3.14 Port G IO Register (PGIOR)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	PG3IOR	PG2IOR	PG1IOR	PG0IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

The port G IO register (PGIOR) is a 16-bit readable/writable register that selects the input/output direction of the 4 pins in port G. Bits PG3IOR to PG0IOR correspond to pins PG3/IRQ3/ADTRG0 to PG0/PULS7/HRxD0/HRxD1.

When port G pins function as PG3 to PG0, a pin becomes an output when the corresponding bit in PGIOR is set to 1, and an input when the bit is cleared to 0.

PGIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.15 Port G Control Register (PGCR)

The port G control register (PGCR) is a 16-bit readable/writable register that selects the functions of the 4 multiplex pins in port G.

PGCR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	PG3MD1	PG3MD0	PG2MD1	PG2MD0	—	PG1MD	PG0MD1	PG0MD0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

- Bits 15 to 8—Reserved: These bits always read 0. The write value should always be 0.
- Bits 7 and 6—PG3 Mode Bits 1 and 0 (PG3MD1, PG3MD0): These bits select the function of pin PG3/ $\overline{\text{IRQ3}}$ / $\overline{\text{ADTRG0}}$ .

Bit 7: PG3MD1	Bit 6: PG3MD0	Description
0	0	General input/output (PG3) (Initial value)
	1	Interrupt request input ( $\overline{\text{IRQ3}}$ )
1	0	A/D conversion trigger input ( $\overline{\text{ADTRG0}}$ )
	1	Reserved (Do not set)

- Bits 5 and 4—PG2 Mode Bits 1 and 0 (PG2MD1, PG2MD0): These bits select the function of pin PG2/ $\overline{\text{IRQ2}}$ .

Bit 5: PG2MD1	Bit 4: PG2MD0	Description
0	0	General input/output (PG2) (Initial value)
	1	Interrupt request input ( $\overline{\text{IRQ2}}$ )
1	0	Reserved (Do not set)
	1	Reserved (Do not set)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PG1 Mode Bit (PG1MD): Selects the function of pin PG1/ $\overline{\text{IRQ1}}$ .

Bit 2: PG1MD	Description
0	General input/output (PG1) (Initial value)
1	Interrupt request input ( $\overline{\text{IRQ1}}$ )

- Bits 1 and 0—PG0 Mode Bits 1 and 0 (PG0MD1, PG2MD0): These bits select the function of pin PG0/PULS7/HRxD0.

Bit 1: PG0MD1	Bit 0: PG0MD0	Description
0	0	General input/output (PG0) (Initial value)
	1	APC pulse output (PULS7)
1	0	HCAN receive data input (HRxD)
	1	Reserved (Do not set)

### 18.3.16 Port H IO Register (PHIOR)

Bit:	15	14	13	12	11	10	9	8
	PH15 IOR	PH14 IOR	PH13 IOR	PH12 IOR	PH11 IOR	PH10 IOR	PH9 IOR	PH8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PH7 IOR	PH6 IOR	PH5 IOR	PH4 IOR	PH3 IOR	PH2 IOR	PH1 IOR	PH0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port H IO register (PHIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port H. Bits PH15IOR to PH0IOR correspond to pins PH15/D15 to PH0/D0. PHIOR is enabled when port H pins function as general input/output pins (PH15 to PH0), and disabled otherwise.

When port H pins function as PH15 to PH0, a pin becomes an output when the corresponding bit in PHIOR is set to 1, and an input when the bit is cleared to 0.

PHIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.17 Port H Control Register (PHCR)

Bit:	15	14	13	12	11	10	9	8
	PH15 MD	PH14 MD	PH13 MD	PH12 MD	PH11 MD	PH10 MD	PH9 MD	PH8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PH7 MD	PH6 MD	PH5 MD	PH4 MD	PH3 MD	PH2 MD	PH1 MD	PH0 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port H control register (PHCR) is a 16-bit readable/writable register that selects the functions of the 16 multiplex pins in port H. PHCR settings are not valid in all operating modes.

1. Expanded mode with on-chip ROM disabled (area 0: 8-bit bus)  
Port H pins D0 to D7 function as data input/output pins, and PHCR settings are invalid.
2. Expanded mode with on-chip ROM disabled (area 0: 16-bit bus)  
Port H pins function as data input/output pins, and PHCR settings are invalid.
3. Expanded mode with on-chip ROM enabled  
Port H pins are multiplexed as data input/output pins and general input/output pins. PHCR settings are valid.
4. Single-chip mode  
Port H pins function as general input/output pins, and PHCR settings are invalid.

PHCR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

- Bit 15—PH15 Mode Bit (PH15MD): Selects the function of pin PH15/D15.

Description				
Bit 15: PH15MD	Expanded Mode	Expanded Mode	Expanded Mode	Single-Chip Mode
	with ROM Disabled Area 0: 8 Bits	with ROM Disabled Area 0: 16 Bits	with ROM Enabled	
0	General input/output (PH15) (Initial value)	Data input/output (D15) (Initial value)	General input/output (PH15) (Initial value)	General input/output (PH15) (Initial value)
1	Data input/output (D15)	Data input/output (D15)	Data input/output (D15)	General input/output (PH15)

- Bit 14—PH14 Mode Bit (PH14MD): Selects the function of pin PH14/D14.

Description				
Bit 14: PH14MD	Expanded Mode	Expanded Mode	Expanded Mode	Single-Chip Mode
	with ROM Disabled Area 0: 8 Bits	with ROM Disabled Area 0: 16 Bits	with ROM Enabled	
0	General input/output (PH14) (Initial value)	Data input/output (D14) (Initial value)	General input/output (PH14) (Initial value)	General input/output (PH14) (Initial value)
1	Data input/output (D14)	Data input/output (D14)	Data input/output (D14)	General input/output (PH14)

- Bit 13—PH13 Mode Bit (PH13MD): Selects the function of pin PH13/D13.

Description				
Bit 13: PH13MD	Expanded Mode	Expanded Mode	Expanded Mode	Single-Chip Mode
	with ROM Disabled Area 0: 8 Bits	with ROM Disabled Area 0: 16 Bits	with ROM Enabled	
0	General input/output (PH13) (Initial value)	Data input/output (D13) (Initial value)	General input/output (PH13) (Initial value)	General input/output (PH13) (Initial value)
1	Data input/output (D13)	Data input/output (D13)	Data input/output (D13)	General input/output (PH13)

- Bit 12—PH12 Mode Bit (PH12MD): Selects the function of pin PH12/D12.

#### Description

Bit 12: PH12MD	Description			
	Expanded Mode with ROM Disabled Area 0: 8 Bits	Expanded Mode with ROM Disabled Area 0: 16 Bits	Expanded Mode with ROM Enabled	Single-Chip Mode
0	General input/output (PH12) (Initial value)	Data input/output (D12) (Initial value)	General input/output (PH12) (Initial value)	General input/output (PH12) (Initial value)
1	Data input/output (D12)	Data input/output (D12)	Data input/output (D12)	General input/output (PH12)

- Bit 11—PH11 Mode Bit (PH11MD): Selects the function of pin PH11/D11.

#### Description

Bit 11: PH11MD	Description			
	Expanded Mode with ROM Disabled Area 0: 8 Bits	Expanded Mode with ROM Disabled Area 0: 16 Bits	Expanded Mode with ROM Enabled	Single-Chip Mode
0	General input/output (PH11) (Initial value)	Data input/output (D11) (Initial value)	General input/output (PH11) (Initial value)	General input/output (PH11) (Initial value)
1	Data input/output (D11)	Data input/output (D11)	Data input/output (D11)	General input/output (PH11)

- Bit 10—PH10 Mode Bit (PH10MD): Selects the function of pin PH10/D10.

#### Description

Bit 10: PH10MD	Description			
	Expanded Mode with ROM Disabled Area 0: 8 Bits	Expanded Mode with ROM Disabled Area 0: 16 Bits	Expanded Mode with ROM Enabled	Single-Chip Mode
0	General input/output (PH10) (Initial value)	Data input/output (D10) (Initial value)	General input/output (PH10) (Initial value)	General input/output (PH10) (Initial value)
1	Data input/output (D10)	Data input/output (D10)	Data input/output (D10)	General input/output (PH10)



- Bit 9—PH9 Mode Bit (PH9MD): Selects the function of pin PH9/D9.

Description				
Bit 9: PH9MD	Expanded Mode	Expanded Mode	Expanded Mode	Single-Chip Mode
	with ROM Disabled Area 0: 8 Bits	with ROM Disabled Area 0: 16 Bits	with ROM Enabled	
0	General input/output (PH9) (Initial value)	Data input/output (D9) (Initial value)	General input/output (PH9) (Initial value)	General input/output (PH9) (Initial value)
1	Data input/output (D9)	Data input/output (D9)	Data input/output (D9)	General input/output (PH9)

- Bit 8—PH8 Mode Bit (PH8MD): Selects the function of pin PH8/D8.

Description				
Bit 8: PH8MD	Expanded Mode	Expanded Mode	Expanded Mode	Single-Chip Mode
	with ROM Disabled Area 0: 8 Bits	with ROM Disabled Area 0: 16 Bits	with ROM Enabled	
0	General input/output (PH8) (Initial value)	Data input/output (D8) (Initial value)	General input/output (PH8) (Initial value)	General input/output (PH8) (Initial value)
1	Data input/output (D8)	Data input/output (D8)	Data input/output (D8)	General input/output (PH8)

- Bit 7—PH7 Mode Bit (PH7MD): Selects the function of pin PH7/D7.

Description			
Bit 7: PH7MD	Expanded Mode	Expanded Mode	Single-Chip Mode
	with ROM Disabled	with ROM Enabled	
0	Data input/output (D7) (Initial value)	General input/output (PH7) (Initial value)	General input/output (PH7) (Initial value)
1	Data input/output (D7)	Data input/output (D7)	General input/output (PH7)

- Bit 6—PH6 Mode Bit (PH6MD): Selects the function of pin PH6/D6.

#### Description

Bit 6: PH6MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D6) (Initial value)	General input/output (PH6) (Initial value)	General input/output (PH6) (Initial value)
1	Data input/output (D6)	Data input/output (D6)	General input/output (PH6)

- Bit 5—PH5 Mode Bit (PH5MD): Selects the function of pin PH5/D5.

#### Description

Bit 5: PH5MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D5) (Initial value)	General input/output (PH5) (Initial value)	General input/output (PH5) (Initial value)
1	Data input/output (D5)	Data input/output (D5)	General input/output (PH5)

- Bit 4—PH4 Mode Bit (PH4MD): Selects the function of pin PH4/D4.

#### Description

Bit 4: PH4MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D4) (Initial value)	General input/output (PH4) (Initial value)	General input/output (PH4) (Initial value)
1	Data input/output (D4)	Data input/output (D4)	General input/output (PH4)

- Bit 3—PH3 Mode Bit (PH3MD): Selects the function of pin PH3/D3.

#### Description

Bit 3: PH3MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D3) (Initial value)	General input/output (PH3) (Initial value)	General input/output (PH3) (Initial value)
1	Data input/output (D3)	Data input/output (D3)	General input/output (PH3)

- Bit 2—PH2 Mode Bit (PH2MD): Selects the function of pin PH2/D2.

Bit 2: PH2MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D2) (Initial value)	General input/output (PH2) (Initial value)	General input/output (PH2) (Initial value)
1	Data input/output (D2)	Data input/output (D2)	General input/output (PH2)

- Bit 1—PH1 Mode Bit (PH1MD): Selects the function of pin PH1/D1.

Bit 1: PH1MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D1) (Initial value)	General input/output (PH1) (Initial value)	General input/output (PH1) (Initial value)
1	Data input/output (D1)	Data input/output (D1)	General input/output (PH1)

- Bit 0—PH0 Mode Bit (PH0MD): Selects the function of pin PH0/D0.

Bit 0: PH0MD	Description		
	Expanded Mode with ROM Disabled	Expanded Mode with ROM Enabled	Single-Chip Mode
0	Data input/output (D0) (Initial value)	General input/output (PH0) (Initial value)	General input/output (PH0) (Initial value)
1	Data input/output (D0)	Data input/output (D0)	General input/output (PH0)

### 18.3.18 Port J IO Register (PJIOR)

Bit:	15	14	13	12	11	10	9	8
	PJ15 IOR	PJ14 IOR	PJ13 IOR	PJ12 IOR	PJ11 IOR	PJ10 IOR	PJ9 IOR	PJ8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PJ7 IOR	PJ6 IOR	PJ5 IOR	PJ4 IOR	PJ3 IOR	PJ2 IOR	PJ1 IOR	PJ0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port J IO register (PJIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port J. Bits PJ15IOR to PJ0IOR correspond to pins PJ15/TI9F to PJ0/TIO2A. PJIOR is enabled when port J pins function as general input/output pins (PJ15 to PJ0) or ATU input/output pins, and disabled otherwise.

When port J pins function as PJ15 to PJ0 or ATU input/output pins, a pin becomes an output when the corresponding bit in PJIOR is set to 1, and an input when the bit is cleared to 0.

PJIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.19 Port J Control Registers H and L (PJCRH, PJCRL)

Port J control registers H and L (PJCRH, PJCRL) are 16-bit readable/writable registers that select the functions of the 16 multiplex pins in port J. PJCRH selects the functions of the pins for the upper 8 bits of port J, and PJCRL selects the functions of the pins for the lower 8 bits.

PJCRH and PJCRL are initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. They are not initialized in software standby mode or sleep mode.

#### Port J Control Register H (PJCRH)

Bit:	15	14	13	12	11	10	9	8
	—	PJ15MD	—	PJ14MD	—	PJ13MD	—	PJ12MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PJ11MD	—	PJ10MD	—	PJ9MD	—	PJ8MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PJ15 Mode Bit (PJ15MD): Selects the function of pin PJ15/TI9F.

Bit 14: PJ15MD	Description
0	General input/output (PJ15) <span style="float: right;">(Initial value)</span>
1	ATU event counter input (TI9F)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PJ14 Mode Bit (PJ14MD): Selects the function of pin PJ14/TI9E.

Bit 12: PJ14MD	Description
0	General input/output (PJ14) <span style="float: right;">(Initial value)</span>
1	ATU event counter input (TI9E)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 10—PJ13 Mode Bit (PJ13MD): Selects the function of pin PJ13/TI9D.

Bit 10: PJ13MD	Description	
0	General input/output (PJ13)	(Initial value)
1	ATU event counter input (TI9D)	

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 8—PJ12 Mode Bit (PJ12MD): Selects the function of pin PJ12/TI9C.

Bit 8: PJ12MD	Description	
0	General input/output (PJ12)	(Initial value)
1	ATU event counter input (TI9C)	

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PJ11 Mode Bit (PJ11MD): Selects the function of pin PJ11/TI9B.

Bit 6: PJ11MD	Description	
0	General input/output (PJ11)	(Initial value)
1	ATU event counter input (TI9B)	

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PJ10 Mode Bit (PJ10MD): Selects the function of pin PJ10/TI9A.

Bit 4: PJ10MD	Description	
0	General input/output (PJ10)	(Initial value)
1	ATU event counter input (TI9A)	

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PJ9 Mode Bit (PJ9MD): Selects the function of pin PJ9/TIO5D.

Bit 2: PJ9MD	Description	
0	General input/output (PJ9)	(Initial value)
1	ATU input capture input/output compare output (TIO5D)	

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PJ8 Mode Bit (PJ8MD): Selects the function of pin PJ8/TIO5C.

Bit 0: PJ8MD	Description
0	General input/output (PJ8) (Initial value)
1	ATU input capture input/output compare output (TIO5C)

### Port J Control Register L (PJCRL)

Bit:	15	14	13	12	11	10	9	8
	—	PJ7MD	—	PJ6MD	—	PJ5MD	—	PJ4MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

Bit:	7	6	5	4	3	2	1	0
	—	PJ3MD	—	PJ2MD	—	PJ1MD	—	PJ0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PJ7 Mode Bit (PJ7MD): Selects the function of pin PJ7/TIO2H.

Bit 14: PJ7MD	Description
0	General input/output (PJ7) (Initial value)
1	ATU input capture input/output compare output (TIO2H)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PJ6 Mode Bit (PJ6MD): Selects the function of pin PJ6/TIO2G.

Bit 12: PJ6MD	Description
0	General input/output (PJ6) (Initial value)
1	ATU input capture input/output compare output (TIO2G)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 10—PJ5 Mode Bit (PJ5MD): Selects the function of pin PJ5/TIO2F.

Bit 10: PJ5MD	Description	
0	General input/output (PJ5)	(Initial value)
1	ATU input capture input/output compare output (TIO2F)	

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 8—PJ4 Mode Bit (PJ4MD): Selects the function of pin PJ4/TIO2E.

Bit 8: PJ4MD	Description	
0	General input/output (PJ4)	(Initial value)
1	ATU input capture input/output compare output (TIO2E)	

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PJ3 Mode Bit (PJ3MD): Selects the function of pin PJ3/TIO2D.

Bit 6: PJ3MD	Description	
0	General input/output (PJ3)	(Initial value)
1	ATU input capture input/output compare output (TIO2D)	

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PJ2 Mode Bit (PJ2MD): Selects the function of pin PJ2/TIO2C.

Bit 4: PJ2MD	Description	
0	General input/output (PJ2)	(Initial value)
1	ATU input capture input/output compare output (TIO2C)	

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PJ1 Mode Bit (PJ1MD): Selects the function of pin PJ1/TIO2B.

Bit 2: PJ1MD	Description	
0	General input/output (PJ1)	(Initial value)
1	ATU input capture input/output compare output (TIO2B)	



- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 0—PJ0 Mode Bit (PJ0MD): Selects the function of pin PJ0/TIO2A.

Bit 0: PJ0MD	Description
0	General input/output (PJ0) <span style="float: right;">(Initial value)</span>
1	ATU input capture input/output compare output (TIO2A)

### 18.3.20 Port K IO Register (PKIOR)

Bit:	15	14	13	12	11	10	9	8
	PK15 IOR	PK14 IOR	PK13 IOR	PK12 IOR	PK11 IOR	PK10 IOR	PK9 IOR	PK8 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PK7 IOR	PK6 IOR	PK5 IOR	PK4 IOR	PK3 IOR	PK2 IOR	PK1 IOR	PK0 IOR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port K IO register (PKIOR) is a 16-bit readable/writable register that selects the input/output direction of the 16 pins in port K. Bits PK15IOR to PK0IOR correspond to pins PK15/TO8P to PK0/TO8A. PKIOR is enabled when port K pins function as general input/output pins (PK15 to PK0), and disabled otherwise.

When port K pins function as PK15 to PK0, a pin becomes an output when the corresponding bit in PKIOR is set to 1, and an input when the bit is cleared to 0.

PKIOR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

### 18.3.21 Port K Control Registers H and L (PKCRH, PKCRL)

Port K control registers H and L (PKCRH, PKCRL) are 16-bit readable/writable registers that select the functions of the 16 multiplex pins in port K. PKCRH selects the functions of the pins for the upper 8 bits of port K, and PKCRL selects the functions of the pins for the lower 8 bits.

PKCRH and PKCRL are initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. They are not initialized in software standby mode or sleep mode.

#### Port K Control Register H (PKCRH)

Bit:	15	14	13	12	11	10	9	8
	—	PK15 MD	—	PK14 MD	—	PK13 MD	—	PK12 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W
Bit:	7	6	5	4	3	2	1	0
	—	PK11 MD	—	PK10 MD	—	PK9 MD	—	PK8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PK15 Mode Bit (PK15MD): Selects the function of pin PK15/TO8P.

#### Bit 14: PK15MD Description

Bit 14: PK15MD	Description
0	General input/output (PK15) (Initial value)
1	ATU one-shot pulse output (TO8P)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PK14 Mode Bit (PK14MD): Selects the function of pin PK14/TO8O.

#### Bit 12: PK14MD Description

Bit 12: PK14MD	Description
0	General input/output (PK14) (Initial value)
1	ATU one-shot pulse output (TO8O)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 10—PK13 Mode Bit (PK13MD): Selects the function of pin PK13/TO8N.

Bit 10: PK13MD	Description
0	General input/output (PK13) (Initial value)
1	ATU one-shot pulse output (TO8N)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 8—PK12 Mode Bit (PK12MD): Selects the function of pin PK12/TO8M.

Bit 8: PK12MD	Description
0	General input/output (PK12) (Initial value)
1	ATU one-shot pulse output (TO8M)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 6—PK11 Mode Bit (PK11MD): Selects the function of pin PK11/TO8L.

Bit 6: PK11MD	Description
0	General input/output (PK11) (Initial value)
1	ATU one-shot pulse output (TO8L)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 4—PK10 Mode Bit (PK10MD): Selects the function of pin PK10/TO8K.

Bit 4: PK10MD	Description
0	General input/output (PK10) (Initial value)
1	ATU one-shot pulse output (TO8K)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 2—PK9 Mode Bit (PK9MD): Selects the function of pin PK9/TO8J.

Bit 2: PK9MD	Description
0	General input/output (PK9) (Initial value)
1	ATU one-shot pulse output (TO8J)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 0—PK8 Mode Bit (PK8MD): Selects the function of pin PK8/TO8I.

Bit 0: PK8MD	Description
0	General input/output (PK8) (Initial value)
1	ATU one-shot pulse output (TO8I)

### Port K Control Register L (PKCRL)

Bit:	15	14	13	12	11	10	9	8
	—	PK7MD	—	PK6MD	—	PK5MD	—	PK4MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

Bit:	7	6	5	4	3	2	1	0
	—	PK3MD	—	PK2MD	—	PK1MD	—	PK0MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R	R/W

- Bit 15—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 14—PK7 Mode Bit (PK7MD): Selects the function of pin PK7/TO8H.

Bit 14: PK7MD	Description
0	General input/output (PK7) (Initial value)
1	ATU one-shot pulse output (TO8H)

- Bit 13—Reserved: This bit always reads 0. The write value should always be 0.
- Bit 12—PK6 Mode Bit (PK6MD): Selects the function of pin PK6/TO8G.

Bit 12: PK6MD	Description
0	General input/output (PK6) (Initial value)
1	ATU one-shot pulse output (TO8G)

- Bit 11—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 10—PK5 Mode Bit (PK5MD): Selects the function of pin PK5/TO8F.

Bit 10: PK5MD	Description
0	General input/output (PK5) (Initial value)
1	ATU one-shot pulse output (TO8F)

- Bit 9—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 8—PK4 Mode Bit (PK4MD): Selects the function of pin PK4/TO8E.

Bit 8: PK4MD	Description
0	General input/output (PK4) (Initial value)
1	ATU one-shot pulse output (TO8E)

- Bit 7—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 6—PK3 Mode Bit (PK3MD): Selects the function of pin PK3/TO8D.

Bit 6: PK3MD	Description
0	General input/output (PK3) (Initial value)
1	ATU one-shot pulse output (TO8D)

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 4—PK2 Mode Bit (PK2MD): Selects the function of pin PK2/TO8C.

Bit 4: PK2MD	Description
0	General input/output (PK2) (Initial value)
1	ATU one-shot pulse output (TO8C)

- Bit 3—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 2—PK1 Mode Bit (PK1MD): Selects the function of pin PK1/TO8B.

Bit 2: PK1MD	Description
0	General input/output (PK1) (Initial value)
1	ATU one-shot pulse output (TO8B)

- Bit 1—Reserved: This bit always reads 0. The write value should always be 0.

- Bit 0—PK0 Mode Bit (PK0MD): Selects the function of pin PK0/TO8A.

Bit 0: PK0MD	Description
0	General input/output (PK0) <span style="float: right;">(Initial value)</span>
1	ATU one-shot pulse output (TO8A)

### 18.3.22 Port K Invert Register (PKIR)

Bit:	15	14	13	12	11	10	9	8
	PK15IR	PK14IR	PK13IR	PK12IR	PK11IR	PK10IR	PK9IR	PK8IR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PK7IR	PK6IR	PK5IR	PK4IR	PK3IR	PK2IR	PK1IR	PK0IR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port K invert register (PKIR) is a 16-bit readable/writable register that sets the port K inversion function. Bits PK15IR to PK0IR correspond to pins PK15/TO8P to PK0/TO8A. PKIR is enabled when port K pins function as ATU outputs, and disabled otherwise.

When port K pins function as ATU outputs, the value of a pin is inverted when the corresponding bit in PKIR is set to 1.

PKIR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

PKnIR	Description
0	Value is not inverted <span style="float: right;">(Initial value)</span>
1	Value is inverted

n = 15 to 0

# Section 19 I/O Ports (I/O)

## 19.1 Overview

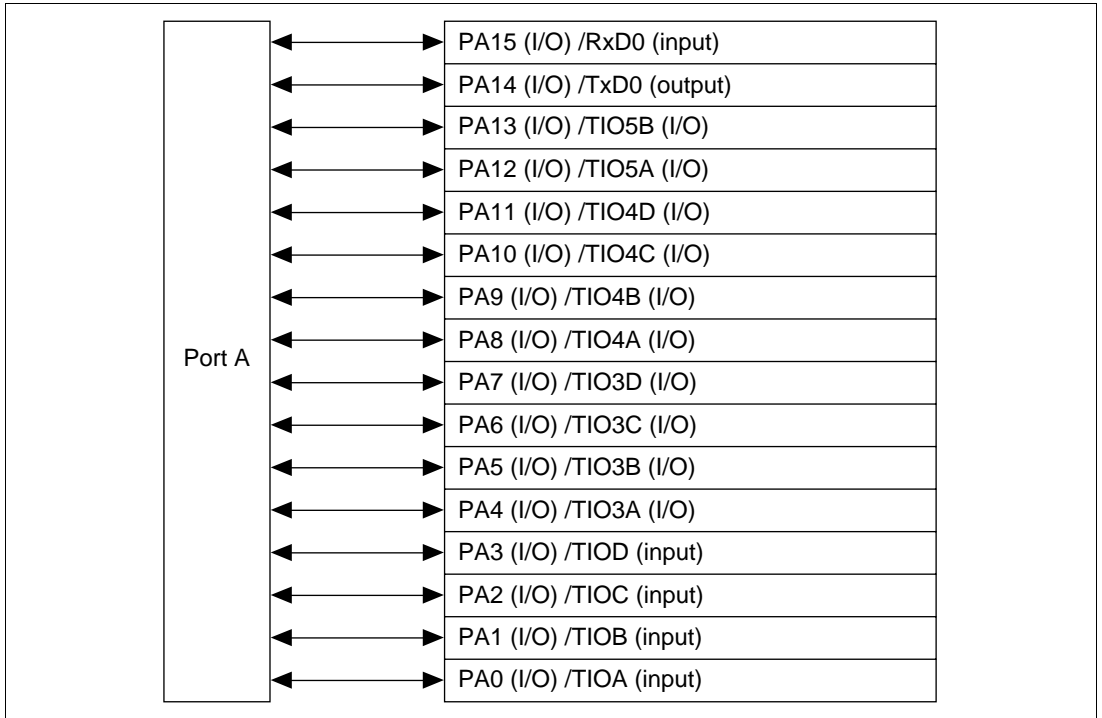
The SH7052F/SH7053F/SH7054F has 10 ports: A, B, C, D, E, F, G, H, J and K, all supporting both input and output.

Ports A, B, E, F, H, J and K are 16-bit ports, port C is a 5-bit port, port D is a 14-bit port, and port G is a 4-bit port.

All the port pins are multiplexed as general input/output pins and special function pins. The functions of the multiplex pins are selected by means of the pin function controller (PFC). Each port is provided with a data register for storing the pin data.

## 19.2 Port A

Port A is an input/output port with the 16 pins shown in figure 19.1.



**Figure 19.1 Port A**

### 19.2.1 Register Configuration

The port A register configuration is shown in table 19.1.

**Table 19.1 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port A data register	PADR	R/W	H'0000	H'FFFFFF726	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.



## 19.2.2 Port A Data Register (PADR)

Bit:	15	14	13	12	11	10	9	8
	PA15 DR	PA14 DR	PA13 DR	PA12 DR	PA11 DR	PA10 DR	PA9 DR	PA8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PA7 DR	PA6 DR	PA5 DR	PA4 DR	PA3 DR	PA2 DR	PA1 DR	PA0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port A data register (PADR) is a 16-bit readable/writable register that stores port A data. Bits PA15DR to PA0DR correspond to pins PA15/RxD0 to PA0/TIOA.

When a pin functions as a general output, if a value is written to PADR, that value is output directly from the pin, and if PADR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PADR is read the pin state, not the register value, is returned directly. If a value is written to PADR, although that value is written into PADR it does not affect the pin state. Table 19.2 summarizes port A data register read/write operations.

PADR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

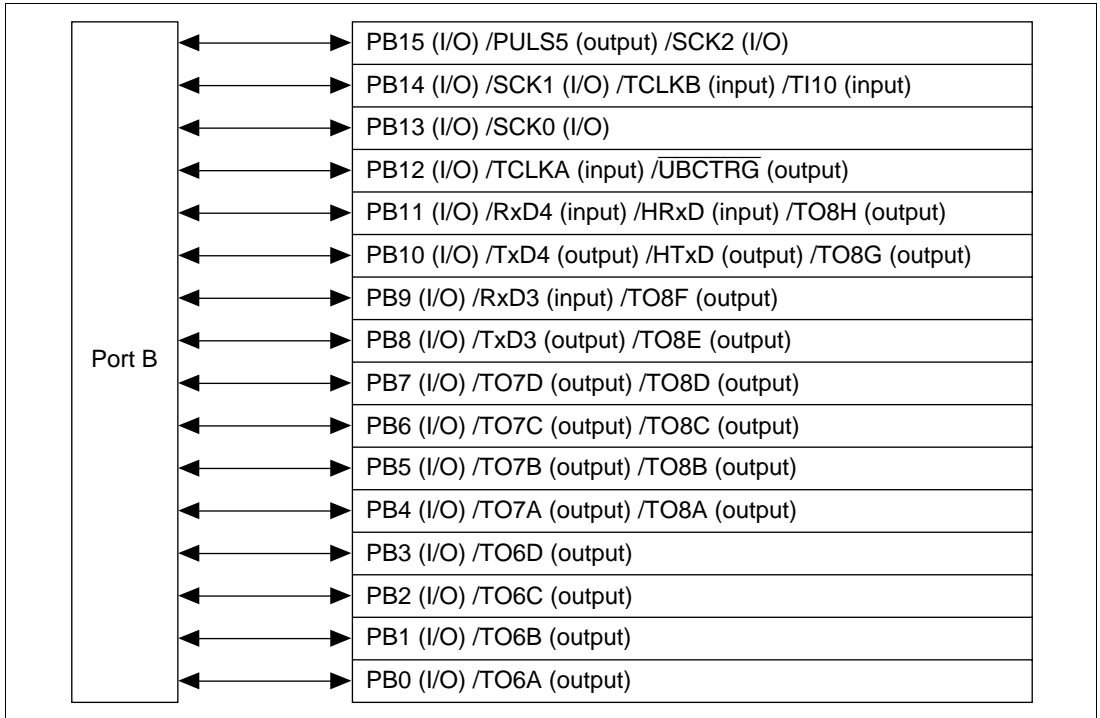
**Table 19.2 Port A Data Register (PADR) Read/Write Operations**

**Bits 15 to 0:**

PAIOR	Pin Function	Read	Write
0	General input	Pin state	Value is written to PADR, but does not affect pin state
	Other than general input	Pin state	Value is written to PADR, but does not affect pin state
1	General output	PADR value	Write value is output from pin
	Other than general output	PADR value	Value is written to PADR, but does not affect pin state

## 19.3 Port B

Port B is an input/output port with the 16 pins shown in figure 19.2.



**Figure 19.2 Port B**

### 19.3.1 Register Configuration

The port B register configuration is shown in table 19.3.

**Table 19.3 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port B data register	PBDR	R/W	H'0000	H'FFFFFF738	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

### 19.3.2 Port B Data Register (PBDR)

Bit:	15	14	13	12	11	10	9	8
	PB15 DR	PB14 DR	PB13 DR	PB12 DR	PB11 DR	PB10 DR	PB9 DR	PB8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PB7 DR	PB6 DR	PB5 DR	PB4 DR	PB3 DR	PB2 DR	PB1 DR	PB0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port B data register (PBDR) is a 16-bit readable/writable register that stores port B data. Bits PB15DR to PB0DR correspond to pins PB15/PULS5/SCK2 to PB0/TO6A.

When a pin functions as a general output, if a value is written to PBDR, that value is output directly from the pin, and if PBDR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PBDR is read the pin state, not the register value, is returned directly. If a value is written to PBDR, although that value is written into PBDR it does not affect the pin state. Table 19.4 summarizes port B data register read/write operations.

PBDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

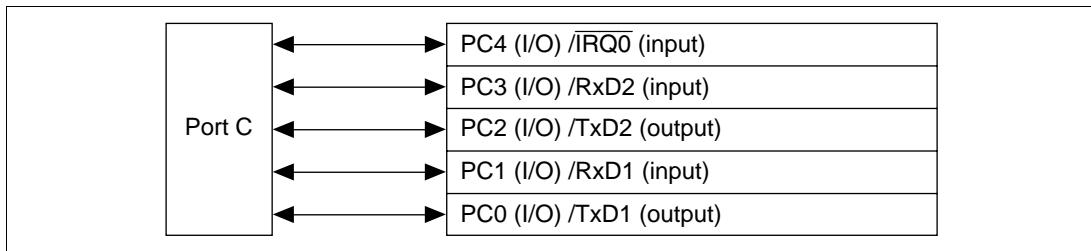
**Table 19.4 Port B Data Register (PBDR) Read/Write Operations**

**Bits 15 to 0:**

PBIOR	Pin Function	Read	Write
0	General input	Pin state	Value is written to PBDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PBDR, but does not affect pin state
1	General output	PBDR value	Write value is output from pin
	Other than general output	PBDR value	Value is written to PBDR, but does not affect pin state

## 19.4 Port C

Port C is an input/output port with the 5 pins shown in figure 19.3.



**Figure 19.3 Port C**

### 19.4.1 Register Configuration

The port C register configuration is shown in table 19.5.

**Table 19.5 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port C data register	PCDR	R/W	H'0000	H'FFFFFF73E	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

### 19.4.2 Port C Data Register (PCDR)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	PC4 DR	PC3 DR	PC2 DR	PC1 DR	PC0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W

The port C data register (PCDR) is a 16-bit readable/writable register that stores port C data. Bits PC4DR to PC0DR correspond to pins PC4/IRQ0 to PC0/TxD1.

When a pin functions as a general output, if a value is written to PCDR, that value is output directly from the pin, and if PCDR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PCDR is read the pin state, not the register value, is returned directly. If a value is written to PCDR, although that value is written into PCDR it does not affect the pin state. Table 19.6 summarizes port C data register read/write operations.

PCDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

- Bits 15 to 5—Reserved: These bits always read 0. The write value should always be 0.

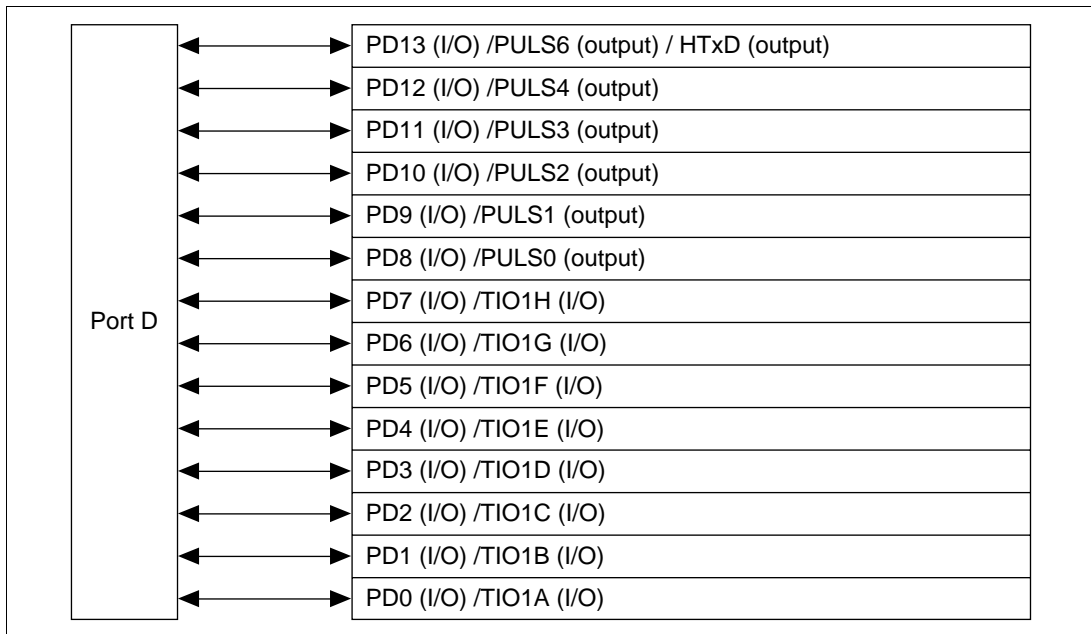
**Table 19.6 Port C Data Register (PCDR) Read/Write Operations**

**Bits 4 to 0:**

<b>PCIOR</b>	<b>Pin Function</b>	<b>Read</b>	<b>Write</b>
0	General input	Pin state	Value is written to PCDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PCDR, but does not affect pin state
1	General output	PCDR value	Write value is output from pin
	Other than general output	PCDR value	Value is written to PCDR, but does not affect pin state

## 19.5 Port D

Port D is an input/output port with the 14 pins shown in figure 19.4.



**Figure 19.4 Port D**

### 19.5.1 Register Configuration

The port D register configuration is shown in table 19.7.

**Table 19.7 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port D data register	PDDR	R/W	H'0000	H'FFFFFF746	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

## 19.5.2 Port D Data Register (PDDR)

Bit:	15	14	13	12	11	10	9	8
	—	—	PD13 DR	PD12 DR	PD11 DR	PD10 DR	PD9 DR	PD8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PD7 DR	PD6 DR	PD5 DR	PD4 DR	PD3 DR	PD2 DR	PD1 DR	PD0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port D data register (PDDR) is a 16-bit readable/writable register that stores port D data. Bits PD13DR to PD0DR correspond to pins PD13/PULS6/HTxD0/HTxD1 to PD0/TIO1A.

When a pin functions as a general output, if a value is written to PDDR, that value is output directly from the pin, and if PDDR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PDDR is read the pin state, not the register value, is returned directly. If a value is written to PDDR, although that value is written into PDDR it does not affect the pin state. Table 19.8 summarizes port D data register read/write operations.

PDDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

- Bits 15 and 14— Reserved: These bits always read 0. The write value should always be 0.

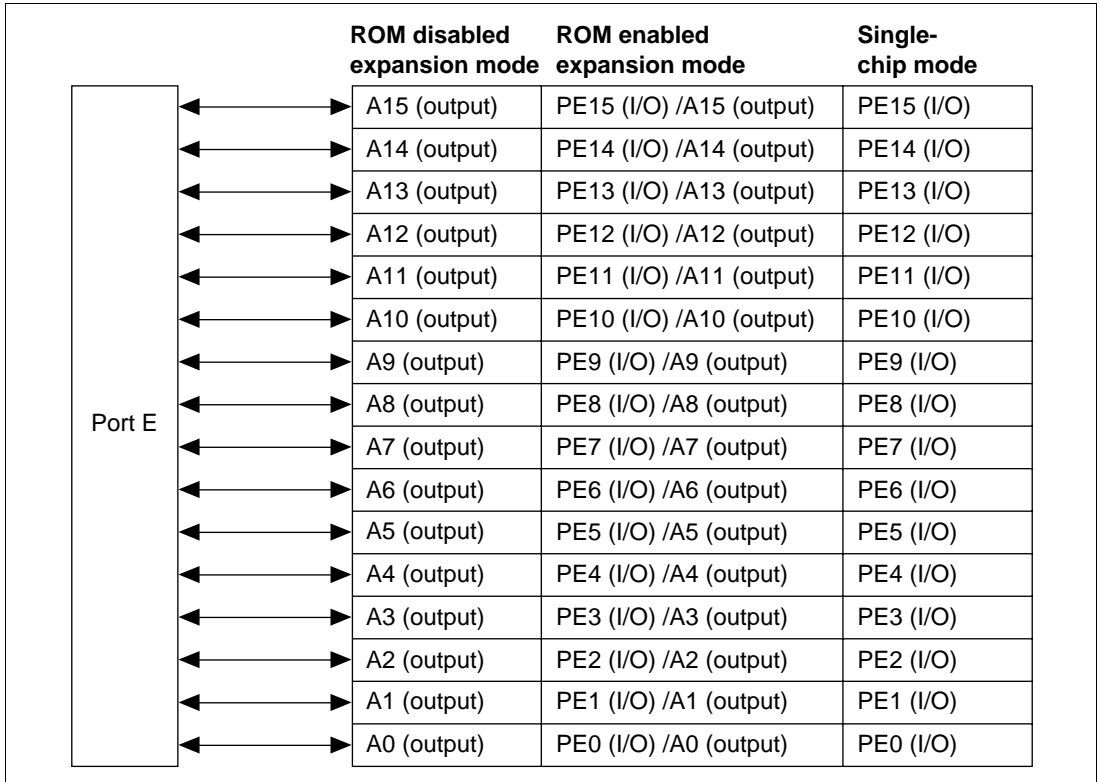
**Table 19.8 Port D Data Register (PDDR) Read/Write Operations**

**Bits 13 to 0:**

PDIOR	Pin Function	Read	Write
0	General input	Pin state	Value is written to PDDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PDDR, but does not affect pin state
1	General output	PDDR value	Write value is output from pin
	Other than general output	PDDR value	Value is written to PDDR, but does not affect pin state

## 19.6 Port E

Port E is an input/output port with the 16 pins shown in figure 19.5.



**Figure 19.5 Port E**

### 19.6.1 Register Configuration

The port E register configuration is shown in table 19.9.

**Table 19.9 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port E data register	PEDR	R/W	H'0000	H'FFFFFF754	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.



## 19.6.2 Port E Data Register (PEDR)

Bit:	15	14	13	12	11	10	9	8
	PE15 DR	PE14 DR	PE13 DR	PE12 DR	PE11 DR	PE10 DR	PE9 DR	PE8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PE7 DR	PE6 DR	PE5 DR	PE4 DR	PE3 DR	PE2 DR	PE1 DR	PE0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port E data register (PEDR) is a 16-bit readable/writable register that stores port E data. Bits PE15DR to PE0DR correspond to pins PE15/A15 to PE0/A0.

When a pin functions as a general output, if a value is written to PEDR, that value is output directly from the pin, and if PEDR is read, the register value is returned directly regardless of the pin state. When the  $\overline{\text{POD}}$  pin is driven low, general outputs go to the high-impedance state regardless of the PEDR value. When the  $\overline{\text{POD}}$  pin is driven high, the written value is output from the pin.

When a pin functions as a general input, if PEDR is read the pin state, not the register value, is returned directly. If a value is written to PEDR, although that value is written into PEDR it does not affect the pin state. Table 19.10 summarizes port E data register read/write operations.

PEDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

**Table 19.10 Port E Data Register (PEDR) Read/Write Operations****Bits 15 to 0:**

<b>PEIOR</b>	<b>Pin Function</b>	<b>Read</b>	<b>Write</b>
0	General input	Pin state	Value is written to PEDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PEDR, but does not affect pin state
1	General output	PEDR value	Write value is output from pin ( $\overline{POD}$ pin = high) High impedance regardless of PEDR value ( $\overline{POD}$ pin = low)
	Other than general output	PEDR value	Value is written to PEDR, but does not affect pin state

## 19.7 Port F

Port F is an input/output port with the 16 pins shown in figure 19.6.

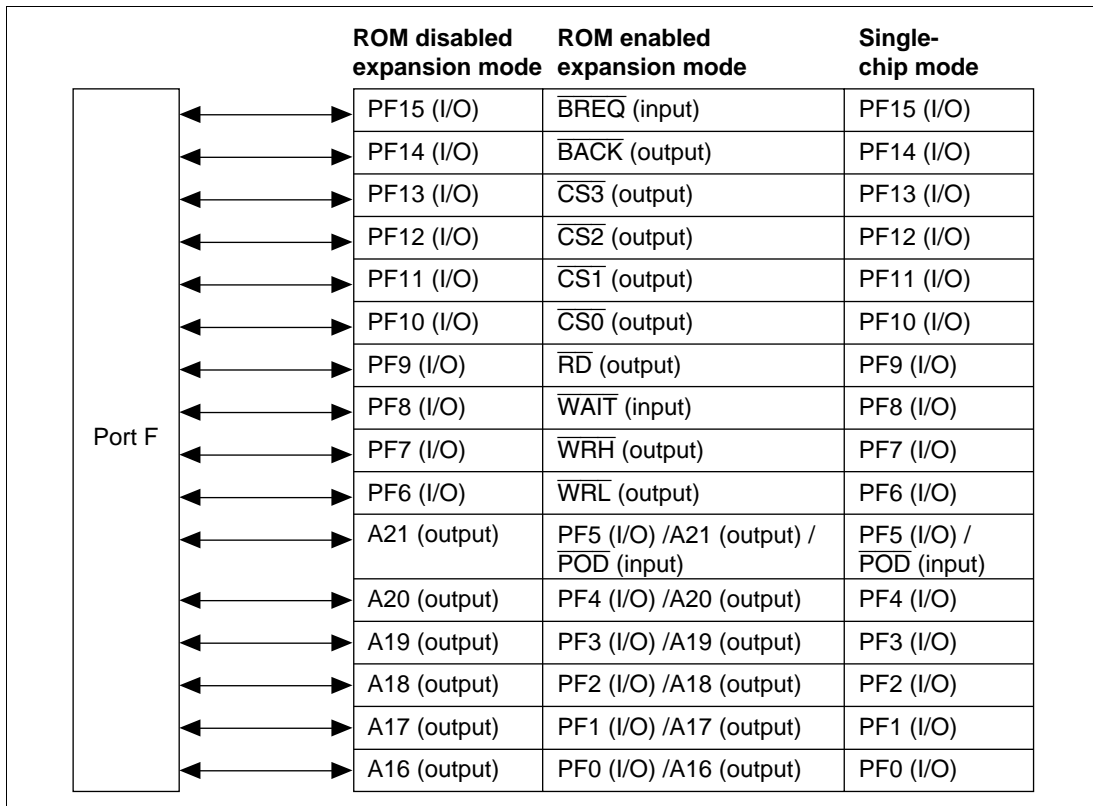


Figure 19.6 Port F

### 19.7.1 Register Configuration

The port F register configuration is shown in table 19.11.

Table 19.11 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port F data register	PFDR	R/W	H'0000	H'FFFFFF74E	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

### 19.7.2 Port F Data Register (PFDR)

Bit:	15	14	13	12	11	10	9	8
	PF15 DR	PF14 DR	PF13 DR	PF12 DR	PF11 DR	PF10 DR	PF9 DR	PF8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PF7 DR	PF6 DR	PF5 DR	PF4 DR	PF3 DR	PF2 DR	PF1 DR	PF0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port F data register (PFDR) is a 16-bit readable/writable register that stores port F data. Bits PF15DR to PF0DR correspond to pins PF15/ $\overline{\text{BREQ}}$  to PF0/A16.

When a pin functions as a general output, if a value is written to PFDR, that value is output directly from the pin, and if PFDR is read, the register value is returned directly regardless of the pin state. For pins PF0 to PF4, when the  $\overline{\text{POD}}$  pin is driven low, general outputs go to the high-impedance state regardless of the PFDR value. When the  $\overline{\text{POD}}$  pin is driven high, the written value is output from the pin.

When a pin functions as a general input, if PFDR is read the pin state, not the register value, is returned directly. If a value is written to PFDR, although that value is written into PFDR it does not affect the pin state. Table 19.12 summarizes port F data register read/write operations.

PFDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

**Table 19.12 Port F Data Register (PFDR) Read/Write Operations****Bits 15 to 5:**

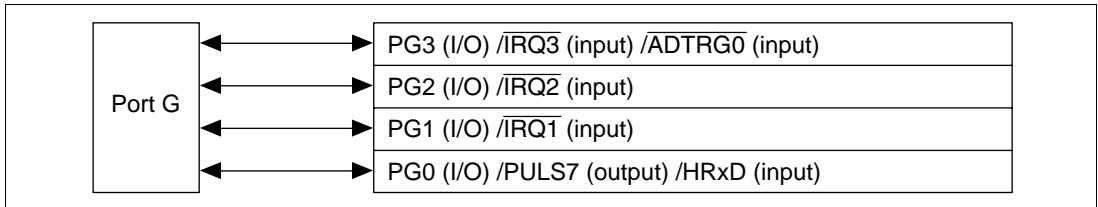
<b>PFIOR</b>	<b>Pin Function</b>	<b>Read</b>	<b>Write</b>
0	General input	Pin state	Value is written to PFDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PFDR, but does not affect pin state
1	General output	PFDR value	Write value is output from pin
	Other than general output	PFDR value	Value is written to PFDR, but does not affect pin state

**Bits 4 to 0:**

<b>PFIOR</b>	<b>Pin Function</b>	<b>Read</b>	<b>Write</b>
0	General input	Pin state	Value is written to PFDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PFDR, but does not affect pin state
1	General output	PFDR value	Write value is output from pin ( $\overline{P\!O\!D}$ pin = high) High impedance regardless of PFDR value ( $\overline{P\!O\!D}$ pin = low)
	Other than general output	PFDR value	Value is written to PFDR, but does not affect pin state

## 19.8 Port G

Port G is an input/output port with the 4 pins shown in figure 19.7.



**Figure 19.7 Port G**

### 19.8.1 Register Configuration

The port G register configuration is shown in table 19.13.

**Table 19.13 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port G data register	PGDR	R/W	H'0000	H'FFFFFF764	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

### 19.8.2 Port G Data Register (PGDR)

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	PG3 DR	PG2 DR	PG1 DR	PG0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

The port G data register (PGDR) is a 16-bit readable/writable register that stores port G data. Bits PG3DR to PG0DR correspond to pins PG3/ $\overline{\text{IRQ3}}$ / $\overline{\text{ADTRG0}}$  to PG0/PULS7/HRxD0.

When a pin functions as a general output, if a value is written to PGDR, that value is output directly from the pin, and if PGDR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PGDR is read the pin state, not the register value, is returned directly. If a value is written to PGDR, although that value is written into PGDR it does not affect the pin state. Table 19.14 summarizes port G data register read/write operations.

PGDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

- Bits 15 to 4—Reserved: These bits always read 0. The write value should always be 0.

**Table 19.14 Port G Data Register (PGDR) Read/Write Operations**

**Bits 3 to 0:**

<b>PGIOR</b>	<b>Pin Function</b>	<b>Read</b>	<b>Write</b>
0	General input	Pin state	Value is written to PGDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PGDR, but does not affect pin state
1	General output	PGDR value	Write value is output from pin
	Other than general output	PGDR value	Value is written to PGDR, but does not affect pin state

## 19.9 Port H

Port H is an input/output port with the 16 pins shown in figure 19.8.

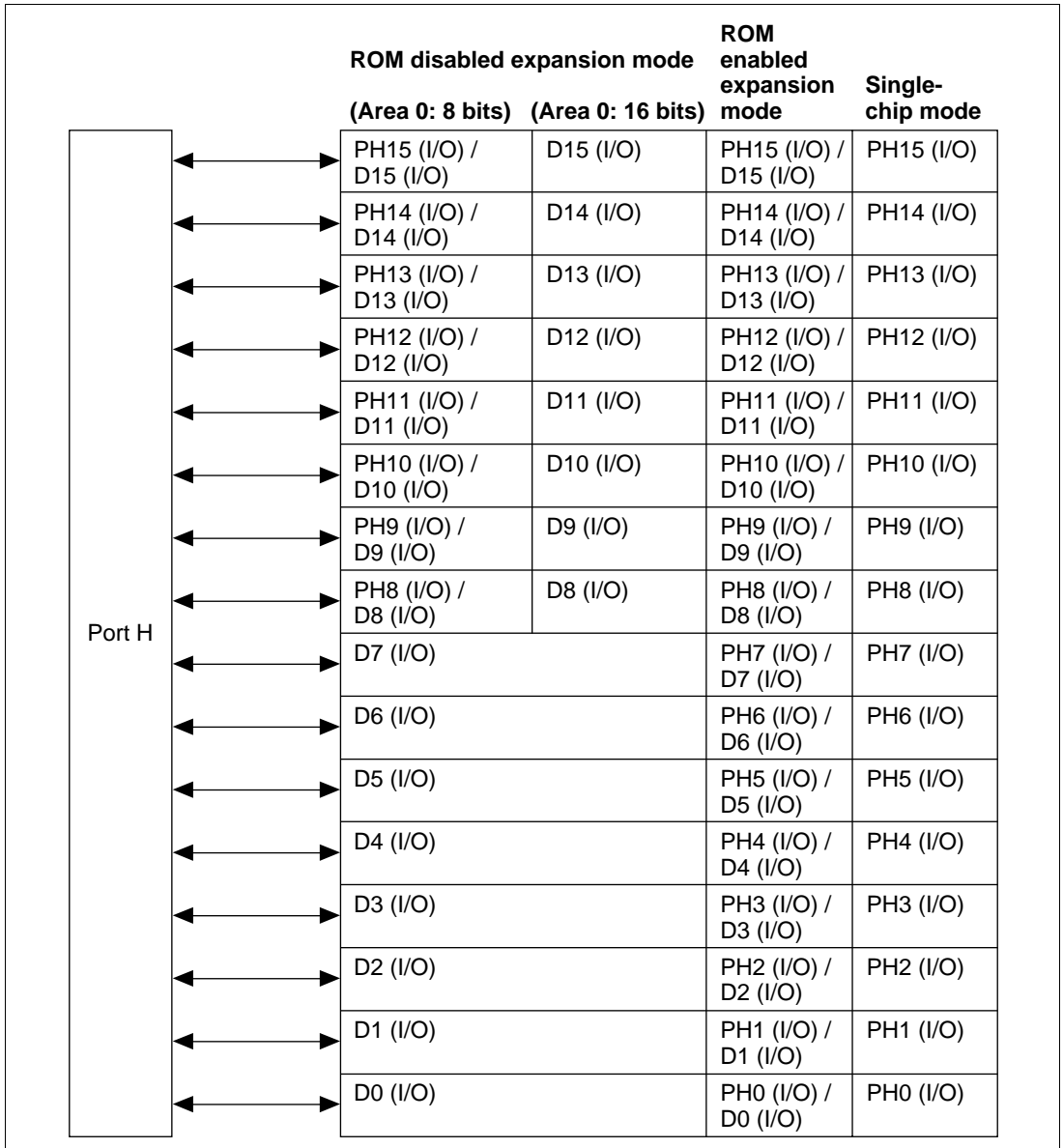


Figure 19.8 Port H



## 19.9.1 Register Configuration

The port H register configuration is shown in table 19.15.

**Table 19.15 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port H data register	PHDR	R/W	H'0000	H'FFFFFF72C	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

## 19.9.2 Port H Data Register (PHDR)

Bit:	15	14	13	12	11	10	9	8
	PH15 DR	PH14 DR	PH13 DR	PH12 DR	PH11 DR	PH10 DR	PH9 DR	PH8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PH7 DR	PH6 DR	PH5 DR	PH4 DR	PH3 DR	PH2 DR	PH1 DR	PH0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port H data register (PHDR) is a 16-bit readable/writable register that stores port H data. Bits PH15DR to PH0DR correspond to pins PH15/D15 to PH0/D0.

When a pin functions as a general output, if a value is written to PHDR, that value is output directly from the pin, and if PHDR is read, the register value is returned directly regardless of the pin state. When the  $\overline{\text{POD}}$  pin is driven low, general outputs go to the high-impedance state regardless of the PHDR value. When the  $\overline{\text{POD}}$  pin is driven high, the written value is output from the pin.

When a pin functions as a general input, if PHDR is read the pin state, not the register value, is returned directly. If a value is written to PHDR, although that value is written into PHDR it does not affect the pin state. Table 19.16 summarizes port H data register read/write operations.

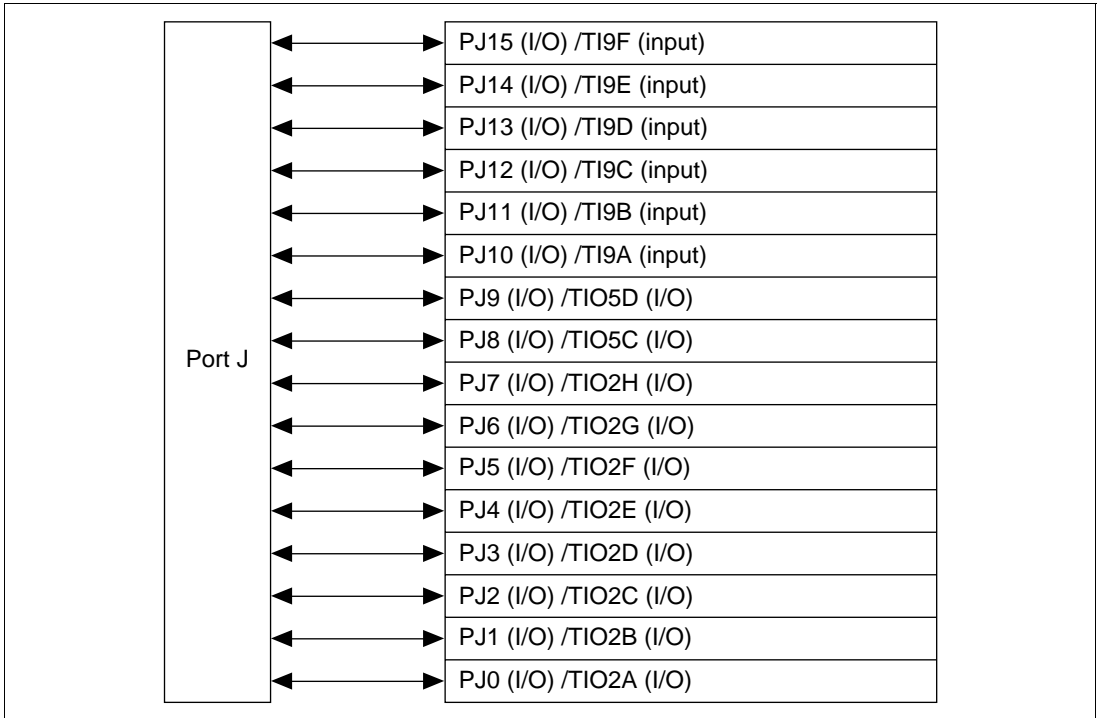
PHDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

**Table 19.16 Port H Data Register (PHDR) Read/Write Operations****Bits 15 to 0:**

<b>PHIOR</b>	<b>Pin Function</b>	<b>Read</b>	<b>Write</b>
0	General input	Pin state	Value is written to PHDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PHDR, but does not affect pin state
1	General output	PHDR value	Write value is output from pin ( $\overline{P\!O\!D}$ pin = high) High impedance regardless of PHDR value ( $\overline{P\!O\!D}$ pin = low)
	Other than general output	PHDR value	Value is written to PHDR, but does not affect pin state

## 19.10 Port J

Port J is an input/output port with the 16 pins shown in figure 19.9.



**Figure 19.9 Port J**

### 19.10.1 Register Configuration

The port J register configuration is shown in table 19.17.

**Table 19.17 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port J data register	PJDR	R/W	H'0000	H'FFFFFF76C	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

## 19.10.2 Port J Data Register (PJDR)

Bit:	15	14	13	12	11	10	9	8
	PJ15 DR	PJ14 DR	PJ13 DR	PJ12 DR	PJ11 DR	PJ10 DR	PJ9 DR	PJ8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PJ7 DR	PJ6 DR	PJ5 DR	PJ4 DR	PJ3 DR	PJ2 DR	PJ1 DR	PJ0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port J data register (PJDR) is a 16-bit readable/writable register that stores port J data. Bits PJ15DR to PJ0DR correspond to pins PJ15/TI9F to PJ0/TIO2A.

When a pin functions as a general output, if a value is written to PJDR, that value is output directly from the pin, and if PJDR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PJDR is read the pin state, not the register value, is returned directly. If a value is written to PJDR, although that value is written into PJDR it does not affect the pin state. Table 19.18 summarizes port J data register read/write operations.

PJDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

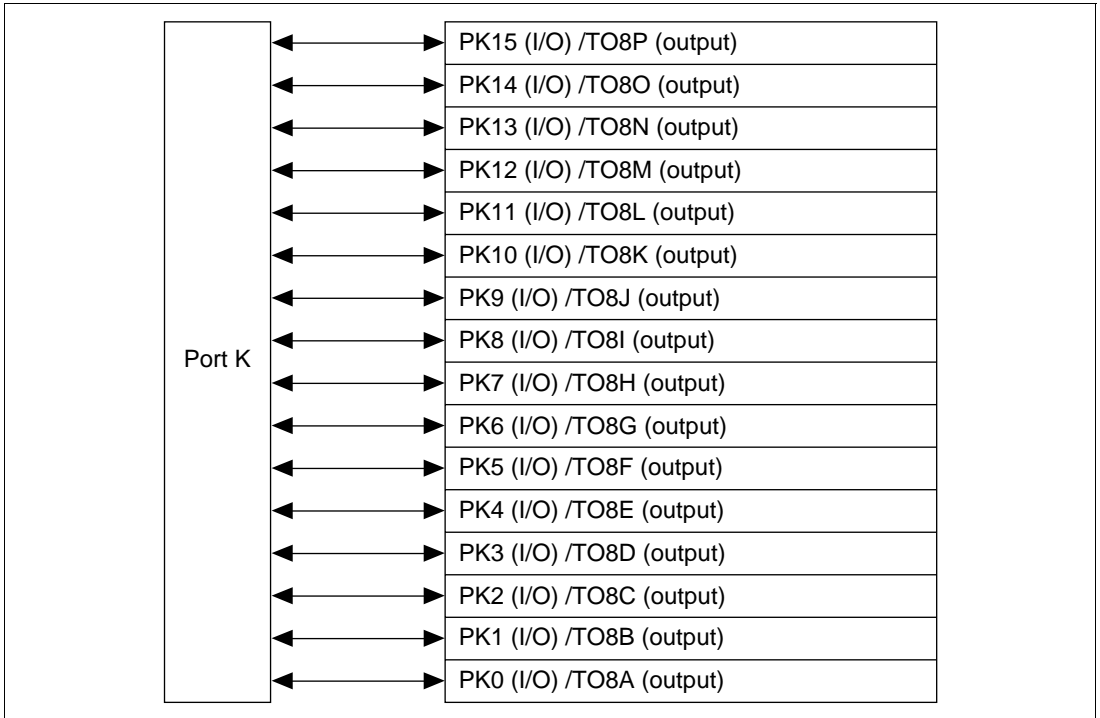
**Table 19.18 Port J Data Register (PJDR) Read/Write Operations**

**Bits 15 to 0:**

PJIOR	Pin Function	Read	Write
0	General input	Pin state	Value is written to PJDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PJDR, but does not affect pin state
1	General output	PJDR value	Write value is output from pin
	Other than general output	PJDR value	Value is written to PJDR, but does not affect pin state

## 19.11 Port K

Port K is an input/output port with the 16 pins shown in figure 19.10.



**Figure 19.10 Port K**

### 19.11.1 Register Configuration

The port K register configuration is shown in table 19.19.

**Table 19.19 Register Configuration**

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port K data register	PKDR	R/W	H'0000	H'FFFFFF778	8, 16

Note: A register access is performed in four or five cycles regardless of the access size.

## 19.11.2 Port K Data Register (PKDR)

Bit:	15	14	13	12	11	10	9	8
	PK15 DR	PK14 DR	PK13 DR	PK12 DR	PK11 DR	PK10 DR	PK9 DR	PK8 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	7	6	5	4	3	2	1	0
	PK7 DR	PK6 DR	PK5 DR	PK4 DR	PK3 DR	PK2 DR	PK1 DR	PK0 DR
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The port K data register (PKDR) is a 16-bit readable/writable register that stores port K data. Bits PK15DR to PK0DR correspond to pins PK15/TO8P to PK0/TO8A.

When a pin functions as a general output, if a value is written to PKDR, that value is output directly from the pin, and if PKDR is read, the register value is returned directly regardless of the pin state.

When a pin functions as a general input, if PKDR is read the pin state, not the register value, is returned directly. If a value is written to PKDR, although that value is written into PKDR it does not affect the pin state. Table 19.20 summarizes port K data register read/write operations.

PKDR is initialized to H'0000 by a power-on reset (excluding a WDT power-on reset), and in hardware standby mode. It is not initialized in software standby mode or sleep mode.

**Table 19.20 Port K Data Register (PKDR) Read/Write Operations**

**Bits 15 to 0:**

PKIOR	Pin Function	Read	Write
0	General input	Pin state	Value is written to PKDR, but does not affect pin state
	Other than general input	Pin state	Value is written to PKDR, but does not affect pin state
1	General output	PKDR value	Write value is output from pin
	Other than general output	PKDR value	Value is written to PKDR, but does not affect pin state

## 19.12 POD (Port Output Disable) Control

The output port drive buffers for the address bus pins (A20 to A0) and data bus pins (D15 to D0) can be controlled by the  $\overline{\text{POD}}$  (port output disable) pin input level. However, this function is enabled only when the address bus pins (A20 to A0) and data bus pins (D15 to D0) are designated as general output ports.

Output buffer control by means of  $\overline{\text{POD}}$  is performed asynchronously from bus cycles.

$\overline{\text{POD}}$	Address Bus Pins (A20 to A0) and Data Bus Pins (D15 to D0) (when designated as output ports)
0	Enabled (high-impedance)
1	Disabled (general output)





# Section 20 ROM (SH7052F/SH7053F)

## 20.1 Features

The SH7052F/SH7053F has 256 kbytes of on-chip flash memory. The features of the flash memory are summarized below.

- Four flash memory operating modes
  - Program mode
  - Erase mode
  - Program-verify mode
  - Erase-verify mode
- Programming/erase methods

The flash memory is programmed 128 bytes at a time. Block erase (in single-block units) can be performed. To erase the entire flash memory, individual blocks must be erased in turn. Block erasing can be performed as required on 4 kB, 32 kB, and 64 kB blocks.
- Programming/erase times

The flash memory programming time is 7 ms (typ.) for simultaneous 128-byte programming, equivalent to 55  $\mu$ s (typ.) per byte, and the erase time is 100 ms (typ.) per block.
- Reprogramming capability

The flash memory can be reprogrammed up to 100 times.
- On-board programming modes

There are two modes in which flash memory can be programmed/erased/verified on-board:

  - Boot mode
  - User program mode
- Automatic bit rate adjustment

With data transfer in boot mode, the SH7052F/SH7053F's bit rate can be automatically adjusted to match the transfer bit rate of the host.
- Flash memory emulation in RAM

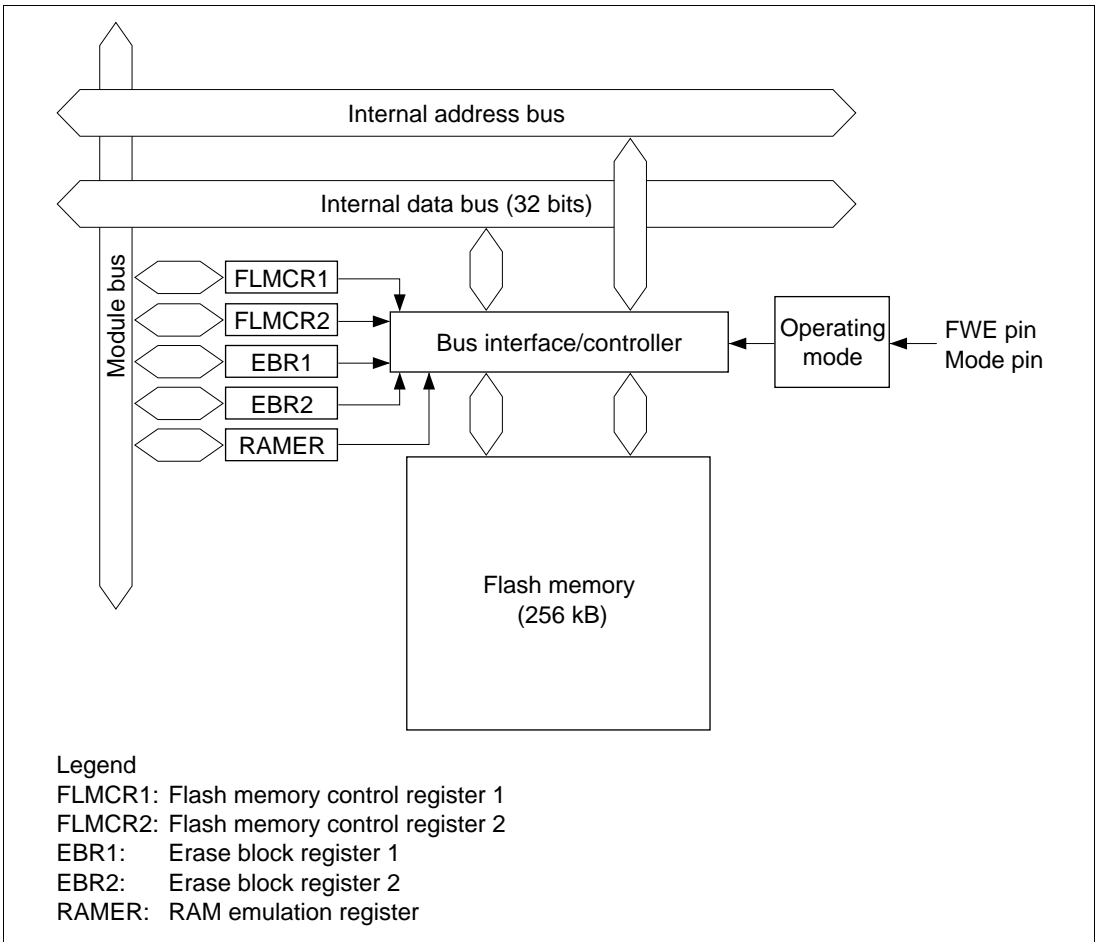
Flash memory programming can be emulated in real time by overlapping a part of RAM onto flash memory.
- Protect modes

There are two protect modes, hardware and software, which allow protected status to be designated for flash memory program/erase/verify operations.
- Programmer mode

Flash memory can be programmed/erased in programmer mode, using a PROM programmer, as well as in on-board programming mode.

## 20.2 Overview

### 20.2.1 Block Diagram



**Figure 20.1 Block Diagram of Flash Memory**

## 20.2.2 Mode Transitions

When the mode pins and the FWE pin are set in the reset state and a reset-start is executed, the microcomputer enters an operating mode as shown in figure 20.2. In user mode, flash memory can be read but not programmed or erased.

The boot, user program and programmer modes are provided as modes to write and erase the flash memory.

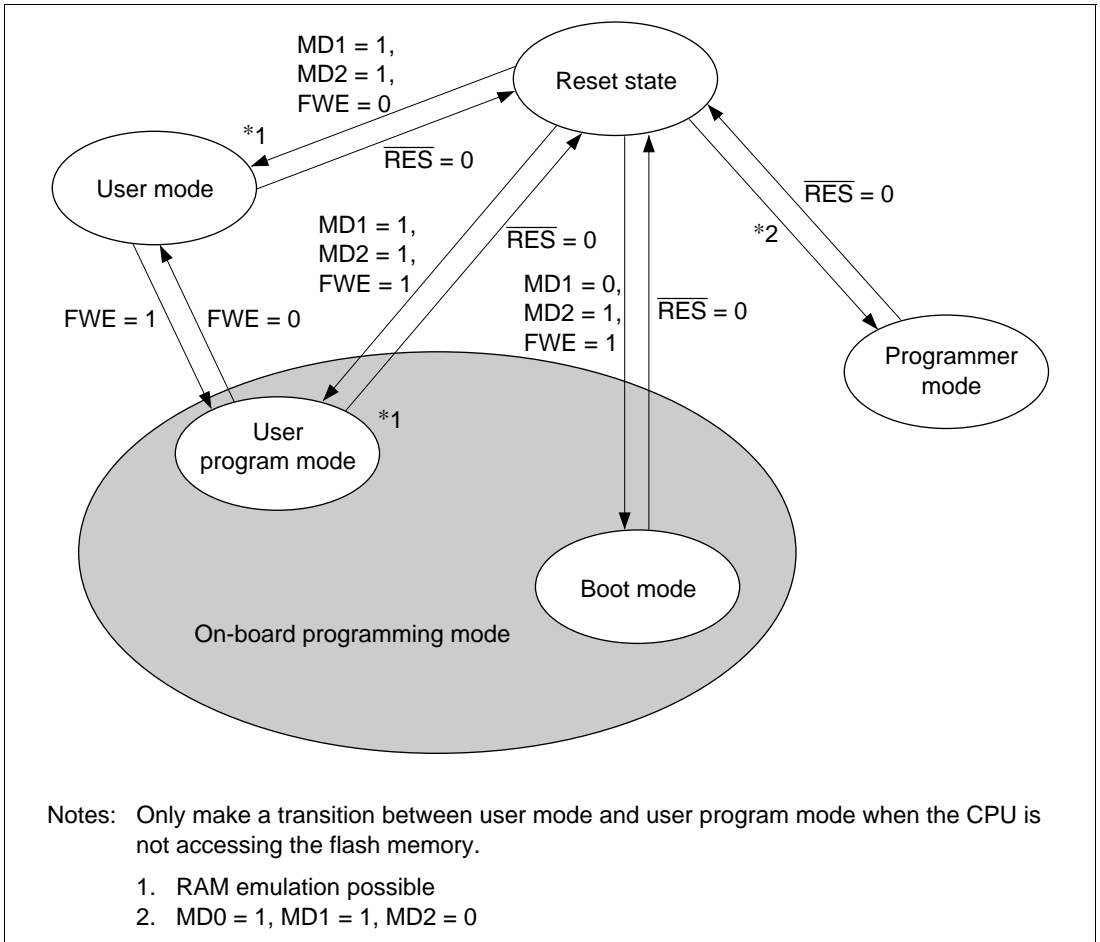
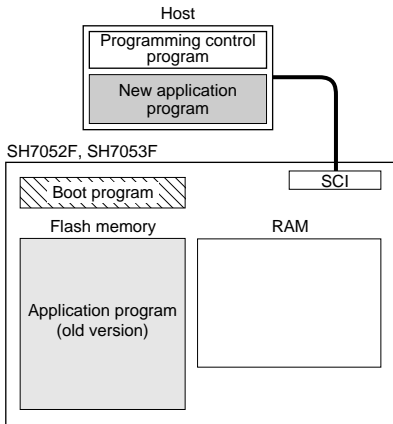


Figure 20.2 Flash Memory State Transitions

### Boot Mode

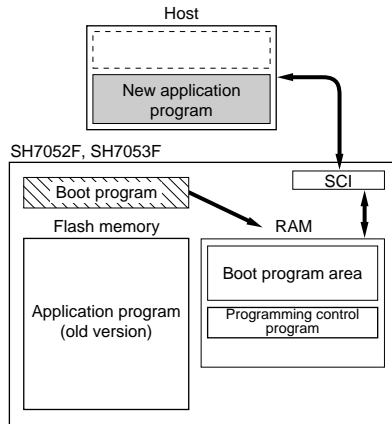
#### 1. Initial state

The old program version or data remains written in the flash memory. The user should prepare the programming control program and new application program beforehand in the host.



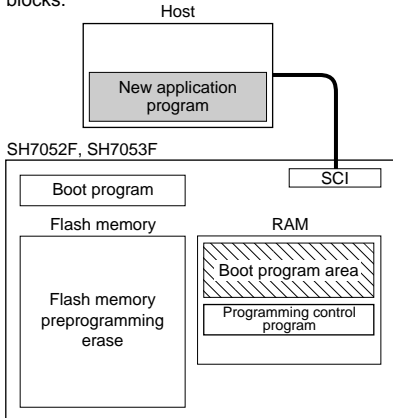
#### 2. Programming control program transfer

When boot mode is entered, the boot program in the SH7052F, SH7053F (originally incorporated in the chip) is started and the programming control program in the host is transferred to RAM via SCI communication. The boot program required for flash memory erasing is automatically transferred to the RAM boot program area.



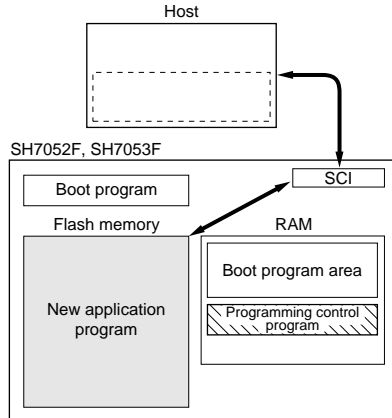
#### 3. Flash memory initialization

The erase program in the boot program area (in RAM) is executed, and the flash memory is initialized (to H'FF). In boot mode, total flash memory erasure is performed, without regard to blocks.



#### 4. Writing new application program

The programming control program transferred from the host to RAM is executed, and the new application program in the host is written into the flash memory.




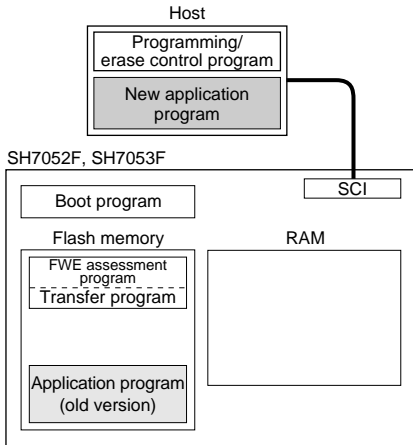
 Program execution state

Figure 20.3 Boot Mode

# User Program Mode

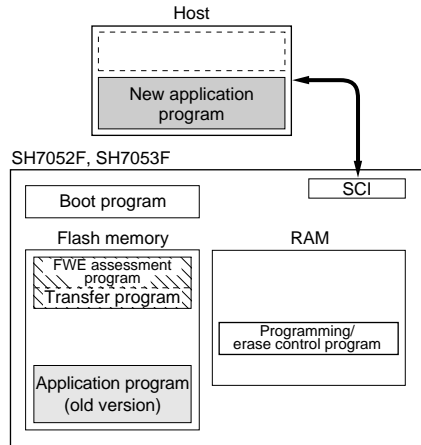
## 1. Initial state

The FWE assessment program that confirms that user program mode has been entered, and the program that will transfer the programming/erase control program from flash memory to on-chip RAM should be written into the flash memory by the user beforehand. The programming/erase control program should be prepared in the host or in the flash memory.



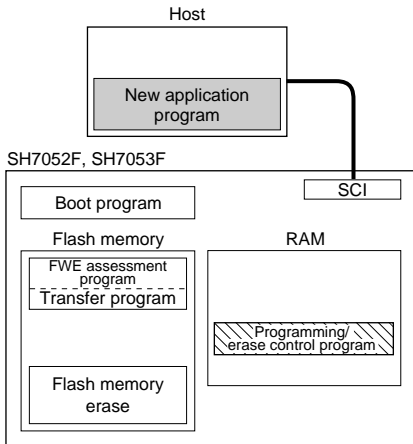
## 2. Programming/erase control program transfer

When user program mode is entered, user software confirms this fact, executes transfer program in the flash memory, and transfers the programming/erase control program to RAM.



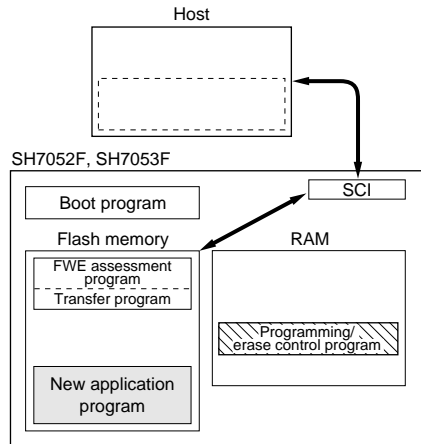
## 3. Flash memory initialization

The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.



## 4. Writing new application program

Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.




 Program execution state

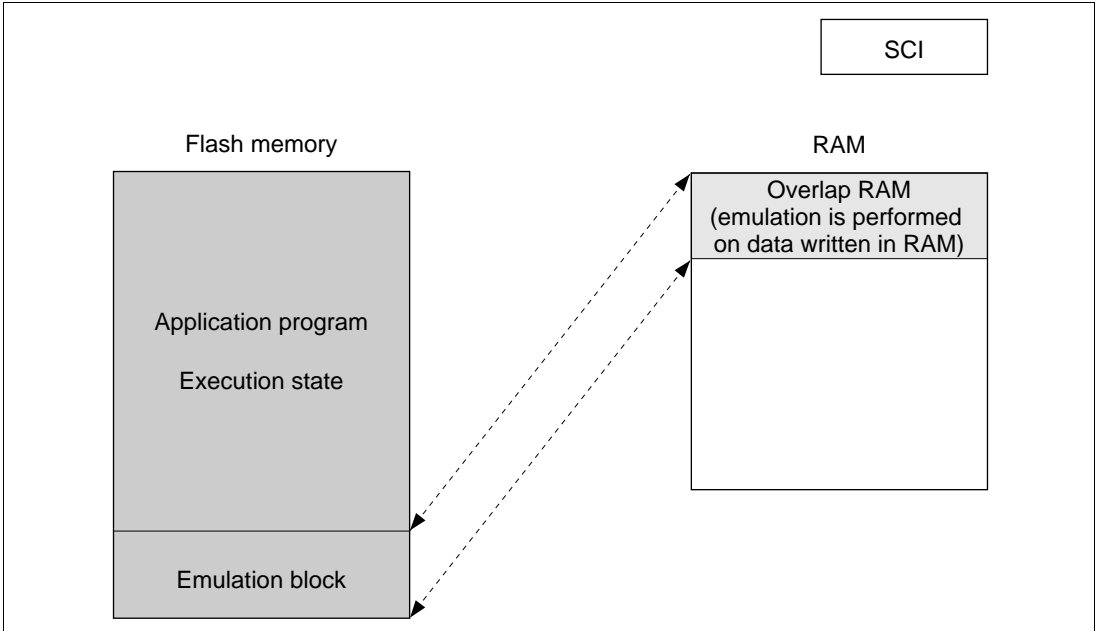
Figure 20.4 User Program Mode

## 20.2.4 Flash Memory Emulation in RAM

Emulation should be performed in user mode or user program mode. When the emulation block set in RAMER is accessed while the emulation function is being executed, data written in the overlap RAM is read.

### User Mode

- User Program Mode

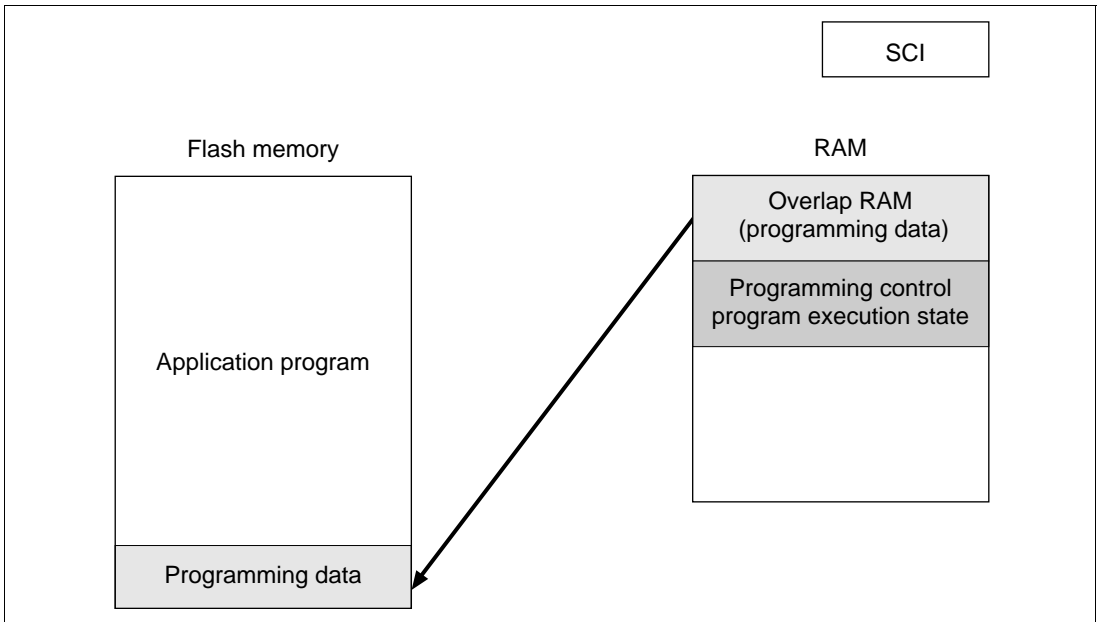


**Figure 20.5 Emulation**

When overlap RAM data is confirmed, the RAMS bit is cleared, RAM overlap is released, and writes should actually be performed to the flash memory.

When the programming control program is transferred to RAM, ensure that the transfer destination and the overlap RAM do not overlap, as this will cause data in the overlap RAM to be rewritten.

- User Program Mode



**Figure 20.6 Programming Flash Memory**

### 20.2.5 Differences between Boot Mode and User Program Mode

**Table 20.1 Differences between Boot Mode and User Mode**

	<b>Boot Mode</b>	<b>User Program Mode</b>
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	(2)	(1) (2) (3)

(1) Erase/erase-verify

(2) Program/program-verify

(3) Emulation

Note: \* To be provided by the user, in accordance with the recommended algorithm.

## 20.2.6 Block Configuration

The flash memory is divided into three 64 kB blocks, one 32 kB block, and eight 4 kB blocks.



**Figure 20.7 Block Configuration**

## 20.3 Pin Configuration

The flash memory is controlled by means of the pins shown in table 20.2.

**Table 20.2 Pin Configuration**

Pin Name	Abbreviation	I/O	Function
Reset	$\overline{\text{RES}}$	Input	Reset
Flash write enable	FWE	Input	Flash program/erase protection by hardware
Mode 2	MD2	Input	Sets SH7052F/SH7053F operating mode
Mode 1	MD1	Input	Sets SH7052F/SH7053F operating mode
Mode 0	MD0	Input	Sets SH7052F/SH7053F operating mode
Transmit data	TxD1	Output	Serial transmit data output
Receive data	RxD1	Input	Serial receive data input



## 20.4 Register Configuration

The registers used to control the on-chip flash memory when enabled are shown in table 20.3.

**Table 20.3 Register Configuration**

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Flash memory control register 1	FLMCR1	R/W* <sup>1</sup>	H'00* <sup>2</sup>	H'FFFFE800	8
Flash memory control register 2	FLMCR2	R/W* <sup>1</sup>	H'00	H'FFFFE801	8
Erase block register 1	EBR1	R/W* <sup>1</sup>	H'00* <sup>3</sup>	H'FFFFE802	8
Erase block register 2	EBR2	R/W* <sup>1</sup>	H'00* <sup>4</sup>	H'FFFFE803	8
RAM emulation register	RAMER	R/W	H'0000	H'FFFEC26	8, 16, 32

- Notes:
1. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit is set to 1 in FLMCR1.
  2. When a high level is input to the FWE pin, the initial value is H'80.
  3. When a low level is input to the FWE pin, or if a high level is input and the SWE1 bit in FLMCR1 is not set, these registers are initialized to H'00.
  4. Will be initialized to H'00 if a low level is input to pin FWE or if bit SWE2 of FLMCR2 is not set even though a high level is input.
  5. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers, and RAMER is a 16-bit register.
  6. Only byte accesses are valid for FLMCR1, FLMCR2, EBR1, and EBR2, the access requiring 3 cycles. Three cycles are required for a byte or word access to RAMER, and 6 cycles for a longword access.

## 20.5 Register Descriptions

### 20.5.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is an 8-bit register used for flash memory operating mode control. Program-verify mode or erase-verify mode is entered by setting SWE1 bit to 1 when FWE = 1, then setting the EV1 or PV1 bit. Program mode is entered by setting SWE1 bit to 1 when FWE = 1, then setting the PSU1 bit, and finally setting the P1 bit. Erase mode for addresses H'00000 to H'3FFFF is entered by setting SWE1 bit to 1 when FWE = 1, then setting the ESU1 bit, and finally setting the E1 bit. FLMCR1 is initialized by a power-on reset, and in hardware standby mode and software standby mode. Its initial value is H'80 when a high level is input to the FWE pin, and H'00 when a low level is input. When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

Writes are enabled only in the following cases: Writes to bit SWE1 of FLMCR1 enabled when FWE = 1, to bits ESU1, PSU1, EV1, and PV1 when FWE = 1 and SWE1 = 1, to bit E1 when FWE = 1, SWE1 = 1 and ESU1 = 1, and to bit P1 when FWE = 1, SWE1 = 1, and PSU1 = 1.

Bit:	7	6	5	4	3	2	1	0
	FWE	SWE1	ESU1	PSU1	EV1	PV1	E1	P1
Initial value:	1/0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 7—Flash Write Enable Bit (FWE): Sets hardware protection against flash memory programming/erasing.

#### Bit 7: FWE Description

0	When a low level is input to the FWE pin (hardware-protected state)
1	When a high level is input to the FWE pin

- Bit 6—Software Write Enable Bit 1 (SWE1): Enables or disables flash memory programming and erasing. Set this bit when setting bits 5 to 0, bits 7 to 0 of EBR1, and bits 3 to 0 of EBR2.

#### Bit 6: SWE1 Description

0	Writes disabled	(Initial value)
1	Writes enabled [Setting condition] When FWE = 1	

- Bit 5—Erase Setup Bit 1 (ESU1): Prepares for a transition to erase mode. Do not set the SWE1, PSU1, EV1, PV1, E1, or P1 bit at the same time.

---

**Bit 5: ESU1 Description**


---

0	Erase setup cleared	(Initial value)
1	Erase setup [Setting condition] When FWE = 1 and SWE1 = 1	

---

- Bit 4—Program Setup Bit 1 (PSU1): Prepares for a transition to program mode. Do not set the SWE1, ESU1, EV1, PV1, E1, or P1 bit at the same time.

---

**Bit 4: PSU1 Description**


---

0	Program setup cleared	(Initial value)
1	Program setup [Setting condition] When FWE = 1 and SWE1 = 1	

---

- Bit 3—Erase-Verify 1 (EV1): Selects erase-verify mode transition or clearing. Do not set the SWE1, ESU1, PSU1, PV1, E1, or P1 bit at the same time.

---

**Bit 3: EV1 Description**


---

0	Erase-verify mode cleared	(Initial value)
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE1 = 1	

---

- Bit 2—Program-Verify 1 (PV1): Selects program-verify mode transition or clearing. Do not set the SWE1, ESU1, PSU1, EV1, E1, or P1 bit at the same time.

---

**Bit 2: PV1 Description**


---

0	Program-verify mode cleared	(Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE1 = 1	

---

- Bit 1—Erase 1 (E1): Selects erase mode transition or clearing. Do not set the SWE1, ESU1, PSU1, EV1, PV1, or P1 bit at the same time.

**Bit 1: E1 Description**

0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE1 = 1, and ESU1 = 1	

- Bit 0—Program 1 (P1): Selects program mode transition or clearing. Do not set the SWE1, PSU1, ESU1, EV1, PV1, or E1 bit at the same time.

**Bit 0: P1 Description**

0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE1 = 1, and PSU1 = 1	

**20.5.2 Flash Memory Control Register 2 (FLMCR2)**

FLMCR2 is a status register that indicates the occurrence of an error during flash memory programming or erasing. FLMCR2 is initialized to H'00 by a power-on reset and in hardware standby mode. When on-chip flash memory is disabled, a read will return H'00 and writes are invalid.

Bit:	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

- Bit 7—Flash Memory Error (FLER): Indicates that an error has occurred during an operation on flash memory (programming or erasing). When FLER is set to 1, flash memory goes to the error-protection state.

Bit 7: FLER	Description
0	Flash memory is operating normally (Initial value) Flash memory program/erase protection (error protection) is disabled [Clearing condition] Power-on reset or hardware standby mode
1	An error has occurred during flash memory programming/erasing Flash memory program/erase protection (error protection) is enabled [Setting condition] See 20.8.3 Error Protection

- Bits 6 to 0—Reserved: These bits always read 0. The write value should always be 0.

### 20.5.3 Erase Block Register 1 (EBR1)

EBR1 is an 8-bit register that specifies the flash memory erase area block by block. EBR1 is initialized to H'00 by a power-on reset, in hardware standby mode and software standby mode, when a low level is input to the FWE pin, and when a high level is input to the FWE pin and the SWE1 bit in FLMCR1 is not set. When a bit in EBR1 is set to 1, the corresponding block can be erased. Other blocks are erase-protected. Only one of the bits of EBR1 and EBR2 combined can be set. Do not set more than one bit. (Do not set more than one bit, as this will automatically clear both EBR1 and EBR2 to 0.) When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 20.4.

Bit:	7	6	5	4	3	2	1	0
	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### 20.5.4 Erase Block Register 2 (EBR2)

EBR2 is an 8-bit register that specifies the flash memory erase area block by block. EBR2 is initialized to H'00 by a power-on reset, in hardware standby mode and software standby mode, when a low level is input to the FWE pin. Bits 3 to 0 will be initialized to 0 if bit SWE1 is not set, even though a high level is input to pin FWE. When a bit in EBR2 is set to 1, the corresponding

block can be erased. Other blocks are erase-protected. Only one of the bits of EBR1 and EBR2 combined can be set. Do not set more than one bit. (Do not set more than one bit, as this will automatically clear both EBR1 and EBR2 to 0.) When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 20.5.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	EB11	EB10	EB9	EB8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

**Table 20.4 Flash Memory Erase Blocks**

<b>Block (Size)</b>	<b>Addresses</b>
EB0 (4 kB)	H'000000 to H'000FFF
EB1 (4 kB)	H'001000 to H'001FFF
EB2 (4 kB)	H'002000 to H'002FFF
EB3 (4 kB)	H'003000 to H'003FFF
EB4 (4 kB)	H'004000 to H'004FFF
EB5 (4 kB)	H'005000 to H'005FFF
EB6 (4 kB)	H'006000 to H'006FFF
EB7 (4 kB)	H'007000 to H'007FFF
EB8 (32 kB)	H'008000 to H'00FFFF
EB9 (64 kB)	H'010000 to H'01FFFF
EB10 (64 kB)	H'020000 to H'02FFFF
EB11 (64 kB)	H'030000 to H'03FFFF

## 20.5.5 RAM Emulation Register (RAMER)

RAMER specifies the area of flash memory to be overlapped with part of RAM when emulating real-time flash memory programming. RAMER is initialized to H'0000 by a power-on reset and in hardware standby mode. It is not initialized in software standby mode. RAMER settings should be made in user mode or user program mode.

Flash memory area divisions are shown in table 20.5. To ensure correct operation of the emulation function, the ROM for which RAM emulation is performed should not be accessed immediately after this register has been modified. Normal execution of an access immediately after register modification is not guaranteed.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

- Bits 15 to 4—Reserved: These bits always read 0. The write value should always be 0.
- Bit 3—RAM Select (RAMS): Specifies selection or non-selection of flash memory emulation in RAM. When RAMS = 1, all flash memory block are program/erase-protected.

### Bit 3: RAMS Description

0	Emulation not selected Program/erase-protection of all flash memory blocks is disabled	(Initial value)
1	Emulation selected Program/erase-protection of all flash memory blocks is enabled	

- Bits 2 to 0—Flash Memory Area Selection (RAM2, RAM1, RAM0): These bits are used together with bit 3 to select the flash memory area to be overlapped with RAM. (See table 22.5.)

**Table 20.5 Flash Memory Area Divisions**

<b>Addresses</b>	<b>Block Name</b>	<b>RAMS</b>	<b>RAM1</b>	<b>RAM1</b>	<b>RAM0</b>
H'FFFF8000 to H'FFFF8FFF	RAM area 4 kB	0	*	*	*
H'00000000 to H'00000FFF	EB0 (4 kB)	1	0	0	0
H'00001000 to H'00001FFF	EB1 (4 kB)	1	0	0	1
H'00002000 to H'00002FFF	EB2 (4 kB)	1	0	1	0
H'00003000 to H'00003FFF	EB3 (4 kB)	1	0	1	1
H'00004000 to H'00004FFF	EB4 (4 kB)	1	1	0	0
H'00005000 to H'00005FFF	EB5 (4 kB)	1	1	0	1
H'00006000 to H'00006FFF	EB6 (4 kB)	1	1	1	0
H'00007000 to H'00007FFF	EB7 (4 kB)	1	1	1	1

\*: Don't care



## 20.6 On-Board Programming Modes

When pins are set to on-board programming mode and a reset-start is executed, a transition is made to the on-board programming state in which program/erase/verify operations can be performed on the on-chip flash memory. There are two on-board programming modes: boot mode and user program mode. The pin settings for transition to each of these modes are shown in table 20.6. For a diagram of the transitions to the various flash memory modes, see figure 20.2.

**Table 20.6 Setting On-Board Programming Modes**

Mode		PLL Multiple	FWE	MD2	MD1	MD0
Boot mode	Expanded mode	× 4	1	1	0	0
	Single-chip mode			1	0	1
User program mode	Expanded mode		1	1	1	0
	Single-chip mode			1	1	1

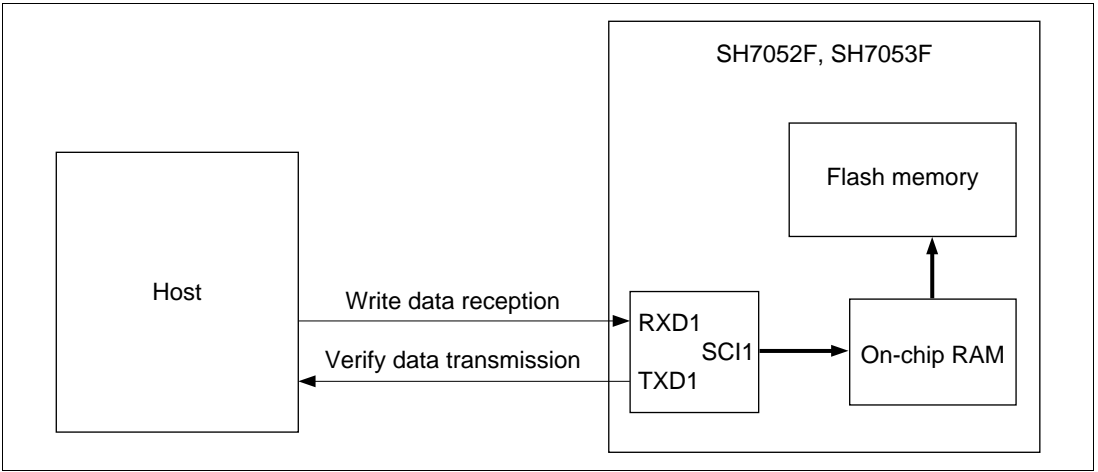
### 20.6.1 Boot Mode

When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. The SCI channel to be used is set to asynchronous mode.

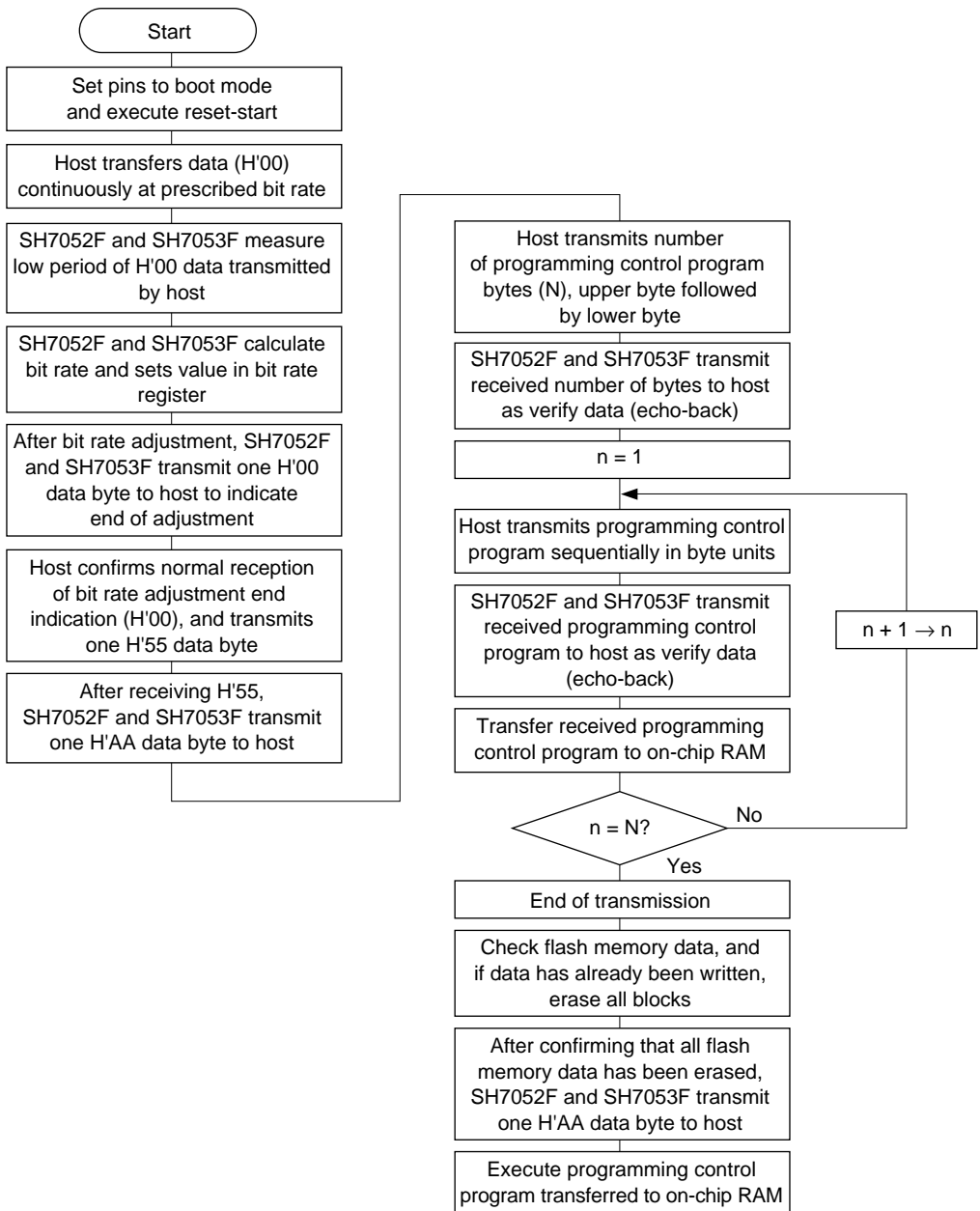
When a reset-start is executed after the SH7052F/SH7053F's pins have been set to boot mode, the boot program built into the SH7052F/SH7053F is started and the programming control program prepared in the host is serially transmitted to the SH7052F/SH7053F via the SCI. In the SH7052F/SH7053F, the programming control program received via the SCI is written into the programming control program area in on-chip RAM. After the transfer is completed, control branches to the start address of the programming control program area and the programming control program execution state is entered (flash memory programming is performed).

The transferred programming control program must therefore include coding that follows the programming algorithm given later.

The system configuration in boot mode is shown in figure 20.8, and the boot mode execution procedure in figure 20.9.



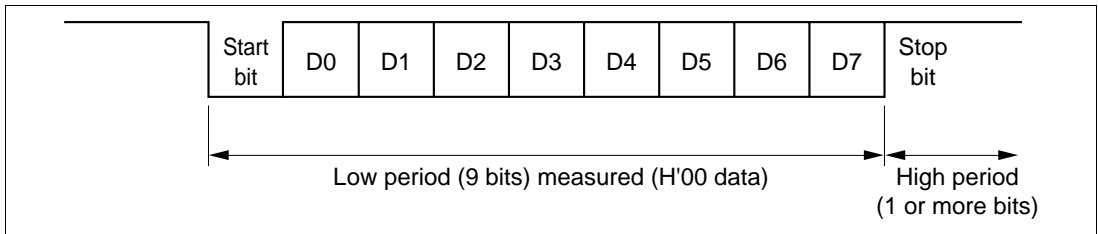
**Figure 20.8 System Configuration in Boot Mode**



Note: If a memory cell does not operate normally and cannot be erased, one H'FF byte is transmitted as an erase error, and the erase operation and subsequent operations are halted.

Figure 20.9 Boot Mode Execution Procedure

## Automatic SCI Bit Rate Adjustment



**Figure 20.10 Automatic SCI Bit Rate Adjustment**

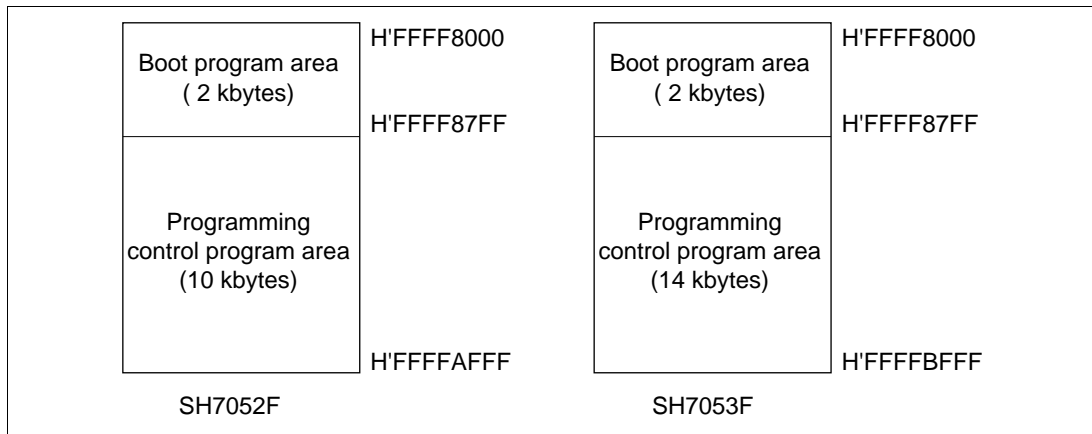
When boot mode is initiated, the SH7052F/SH7053F measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The SH7052F/SH7053F calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the SH7052F/SH7053F. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the SH7052F/SH7053F's system clock frequency, there will be a discrepancy between the bit rates of the host and the SH7052F/SH7053F. Set the host transfer bit rate at 9,600 or 19,200 bps to operate the SCI properly.

Table 20.7 shows host transfer bit rates and system clock frequencies for which automatic adjustment of the SH7052F/SH7053F bit rate is possible. The boot program should be executed within this system clock range.

**Table 20.7 System Clock Frequencies for which Automatic Adjustment of SH7052F/SH7053F Bit Rate is Possible**

Host Bit Rate	System Clock Frequency for Which Automatic Adjustment of SH7052F/SH7053F Bit Rate is Possible
9,600 bps	20 to 40 MHz (input frequency: 5 to 10 MHz)
19,200 bps	20 to 40 MHz (input frequency: 5 to 10 MHz)

**On-Chip RAM Area Divisions in Boot Mode:** In boot mode, the RAM area is divided into an area used by the boot program and an area to which the programming control program is transferred via the SCI, as shown in figure 20.11. The boot program area cannot be used until the execution state in boot mode switches to the programming control program transferred from the host.



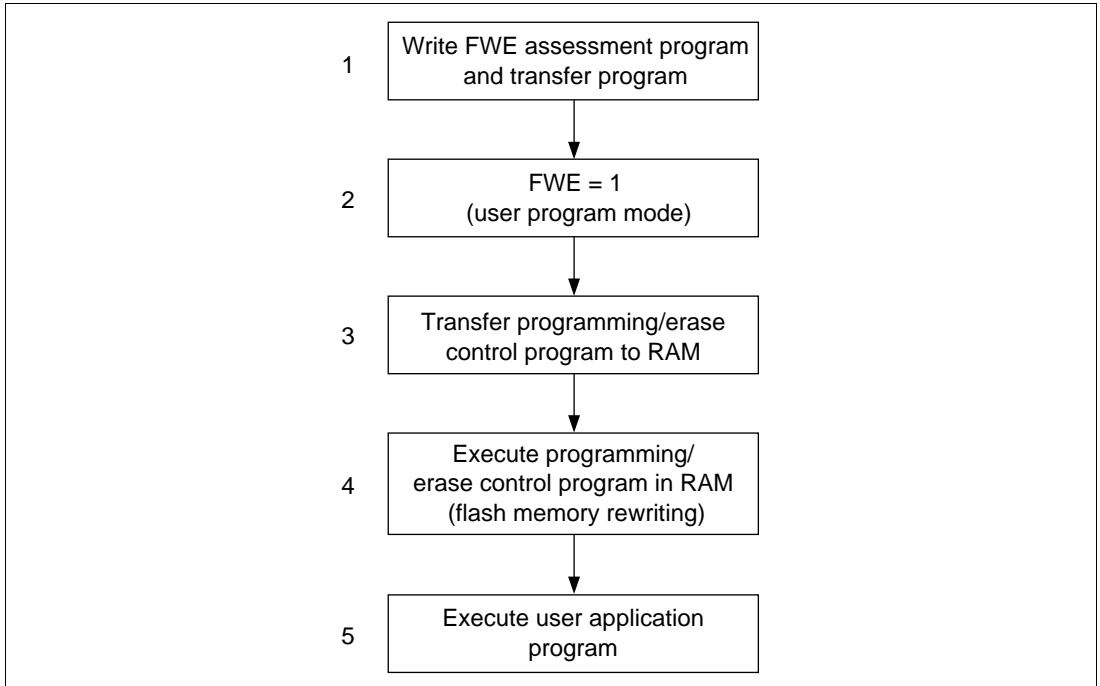
**Figure 20.11 RAM Areas in Boot Mode**

Note: The boot program area cannot be used until a transition is made to the execution state for the programming control program transferred to RAM. Note also that the boot program remains in this area of the on-chip RAM even after control branches to the programming control program.

## 20.6.2 User Program Mode

After setting FWE, the user should branch to, and execute, the previously prepared programming/erase control program.

Use the following procedure (figure 20.12) to execute the programming control program that writes to flash memory (when transferred to RAM).



**Figure 20.12 User Program Mode Execution Procedure**

Note: When programming and erasing, start the watchdog timer so that measures can be taken to prevent program runaway, etc. Memory cells may not operate normally if overprogrammed or overerased due to program runaway.

## 20.7 Programming/Erasing Flash Memory

A software method, using the CPU, is employed to program and erase flash memory in the on-board programming modes. There are four flash memory operating modes: program mode, erase mode, program-verify mode, and erase-verify mode. Transitions to these modes are made by setting the PSU1, ESU1, P1, E1, PV1, and EV1 bits in FLMCR1.

The flash memory cannot be read while it is being written or erased. Install the program to control flash memory programming and erasing (programming control program) in the on-chip RAM, in

external memory, or in flash memory outside the address area, and execute the program from there.

- Notes:
1. Operation is not guaranteed if bits SWE1, ESU1, PSU1, EV1, PV1, E1, and P1 of FLMCR1 are set/reset by a program in flash memory in the corresponding address areas.
  2. When programming or erasing, set FWE to 1 (programming/erasing will not be executed if FWE = 0).
  3. Programming should be performed in the erased state. Do not perform additional programming on previously programmed addresses.

### 20.7.1 Program Mode

When writing data or programs to flash memory, the program/program-verify flowchart shown in figures 20.13 and 20.14 should be followed. Performing program operations according to this flowchart will enable data or programs to be written to flash memory without subjecting the device to voltage stress or sacrificing program data reliability. Programming should be carried out 128 bytes at a time.

Following the elapse of 10  $\mu$ s or more after the SWE1 bit is set to 1 in flash memory control register 1 (FLMCR1), 128-byte program data is stored in the program data area and reprogram data area, and the 128-byte data in the program data area in RAM is written consecutively to the program address (the lower 8 bits of the first address written to must be H'00 or H'80). 128 consecutive byte data transfers are performed. The program address and program data are latched in the flash memory. A 128-byte data transfer must be performed even if writing fewer than 128 bytes; in this case, H'FF data must be written to the extra addresses.

Next, the watchdog timer is set to prevent overprogramming in the event of program runaway, etc. Set 6.6 ms as the WDT overflow period. After this, preparation for program mode (program setup) is carried out by setting the PSU1 bit in FLMCR1, and after the elapse of  $t_{\text{SPSU}}$ , the operating mode is switched to program mode by setting the P1 bit in FLMCR1. The time during which the Pn bit is set is the flash memory programming time. Follow the table in the programming flowchart for the write time.

After the elapse of a given programming time, programming mode is exited. In exiting programming mode, the P1 bit in FLMCR1 is cleared, then after an interval of  $t_{\text{CP}}$  or longer the PSU1 bit is cleared, and after an interval of  $t_{\text{CPSU}}$  or longer the watchdog timer is halted.

## 20.7.2 Program-Verify Mode

In program-verify mode, the data written in program mode is read to check whether it has been correctly written in the flash memory.

A transition to program-verify mode is made by setting the PV1 bit in FLMCR1 and waiting for an interval of  $t_{SPV}$ . Before reading in program-verify mode, perform a dummy write of H'FF data to the read addresses, and then wait for an interval of  $t_{SPVR}$  or longer. When the flash memory is read in this state (verify data is read in longword units), the data at the latched address is read. Next, the written data is compared with the verify data, and reprogram data is computed (see figures 20.13 and 20.14) and transferred to the reprogram data area. After 128 bytes of data have been verified, exit program-verify mode. Program-verify mode is exited by clearing the PV1 bit in FLMCR1, then clearing the SWEn bit after an interval of  $t_{CPV}$  or longer, and waiting for an interval of  $t_{CSWE}$  or longer. If reprogramming is necessary, set program mode again, and repeat the program/program-verify sequence as before. However, ensure that the program/program-verify sequence is not repeated more than 1,000 times on the same bits.



Data writes must be performed in the memory-erased state. Do not write additional data to an address to which data is already written.

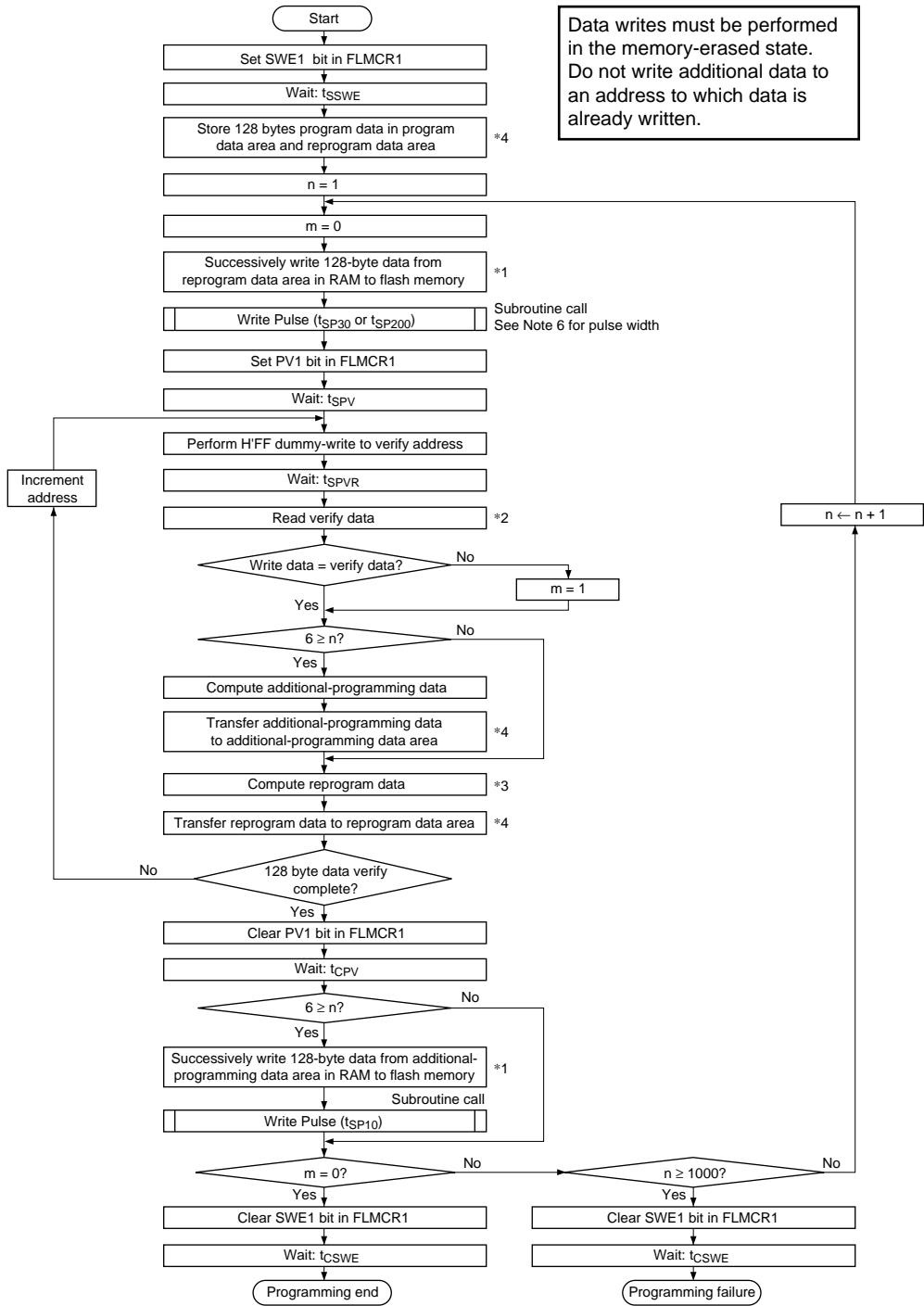
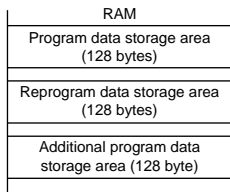
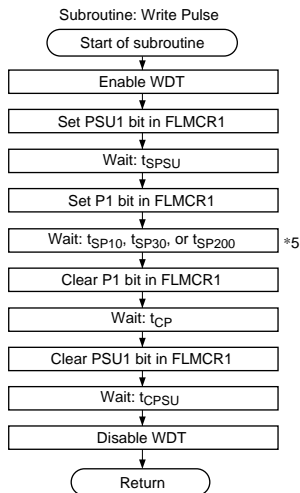


Figure 20.13 Program/Program-Verify Flowchart (1)



- Notes:
1. Transfer data in byte units. The lower eight bits of the start address to which data has already been written must be H'00 or H'80. Transfer 128-byte data even when writing fewer than 128 bytes. In this case, Set H'FF in unused addresses.
  2. Read verify data in longword form (32 bits).
  3. Even for bits to which data has already been written in the 128-byte programming loop, an additional write should be performed if the next verify write data is not the same as the verify data.
  4. A 128-byte area for storing program data, a 128-byte area for storing reprogram data, and a 128-byte area for storing additional program data must be provided in RAM. The reprogram and additional program data contents are modified as programming proceeds.
  5. A write pulse of  $t_{SP30}$  or  $t_{SP200}$  is applied according to the progress of the programming operation. See Note 6 for the pulse widths. When writing of the additional program data is executed, a  $t_{SP10}$  write pulse should be applied. Reprogram data 'X' means reprogram data when the pulse is applied.
  6. Write Pulse Width

Number of Writes n	Write Time (z) $\mu$ sec
1	$t_{SP30}$
2	$t_{SP30}$
3	$t_{SP30}$
4	$t_{SP30}$
5	$t_{SP30}$
6	$t_{SP30}$
7	$t_{SP200}$
8	$t_{SP200}$
9	$t_{SP200}$
10	$t_{SP200}$
11	$t_{SP200}$
12	$t_{SP200}$
13	$t_{SP200}$
.	.
.	.
998	$t_{SP200}$
999	$t_{SP200}$
1000	$t_{SP200}$

Note: Use a  $t_{SP10}$  write pulse for additional programming.

Reprogram Data Computation Table

Original Data (D)	Verify Data (V)	Reprogram Data (X)	Comments
0	0	1	Programming complete.
0	1	0	Programming is incomplete; reprogramming should be performed.
1	0	1	—
1	1	1	Left in the erased state.

Additional-Programming Data Computation Table

Reprogram Data (X)	Verify Data (V)	Additional-Programming Data (Y)	Comments
0	0	0	Additional programming executed
0	1	1	Additional programming not executed
1	0	1	Additional programming not executed
1	1	1	Additional programming not executed

Figure 20.14 Program/Program-Verify Flowchart (2)

**Table 20.8 Program/Program-Verify Parameter**

Flow Section	Item	Symbol	Min	Typ	Max	Unit	Notes
Program/ program-verify	Wait time after PSU1 bit setting	$t_{SPSU}$	50	50	—	$\mu\text{s}$	
	Wait time after P1 bit setting (10 $\mu\text{s}$ )	$t_{SP10}$	8	10	12	$\mu\text{s}$	Additional-programming time wait
	Wait time after P1 bit setting (30 $\mu\text{s}$ )	$t_{SP30}$	28	30	32	$\mu\text{s}$	Programming time wait
	Wait time after P1 bit setting (200 $\mu\text{s}$ )	$t_{SP200}$	198	200	202	$\mu\text{s}$	Programming time wait
	Wait time after P1 bit clearing	$t_{CP}$	5	5	—	$\mu\text{s}$	
	Wait time after PSU1 bit clearing	$t_{CPSU}$	5	5	—	$\mu\text{s}$	
	Wait time after PV1 bit setting	$t_{SPV}$	4	4	—	$\mu\text{s}$	
	Wait time after dummy write	$t_{SPVR}$	2	2	—	$\mu\text{s}$	
	Wait time after PV1 bit clearing	$t_{CPV}$	2	2	—	$\mu\text{s}$	
All	Wait time after SWE1 bit setting	$t_{SSWE}$	1	1	—	$\mu\text{s}$	
	Wait time after SWE1 bit clearing	$t_{CSWE}$	100	100	—	$\mu\text{s}$	

### 20.7.3 Erase Mode

When erasing flash memory, the erase/erase-verify flowchart (single-block erase) shown in figure 20.15 should be followed for each block.

To perform data or program erasure, set the SWE1 bit to 1 in flash memory control register n (FLMCR1), then, after an interval of  $t_{SSWE}$  or longer, make a 1-bit setting for the flash memory area to be erased in erase block register 1 or 2 (EBR1, EBR2). Next, the watchdog timer is set to prevent overerasing in the event of program runaway, etc. Set 19.8 ms as the WDT overflow period. After this, preparation for erase mode (erase setup) is carried out by setting the ESU1 bit in FLMCR1, and after an interval of  $t_{SESU}$  or longer, the operating mode is switched to erase mode by setting the E1 bit in FLMCR1. The time during which the E1 bit is set is the flash memory erase time. Ensure that the erase time does not exceed  $t_{SE}$ .

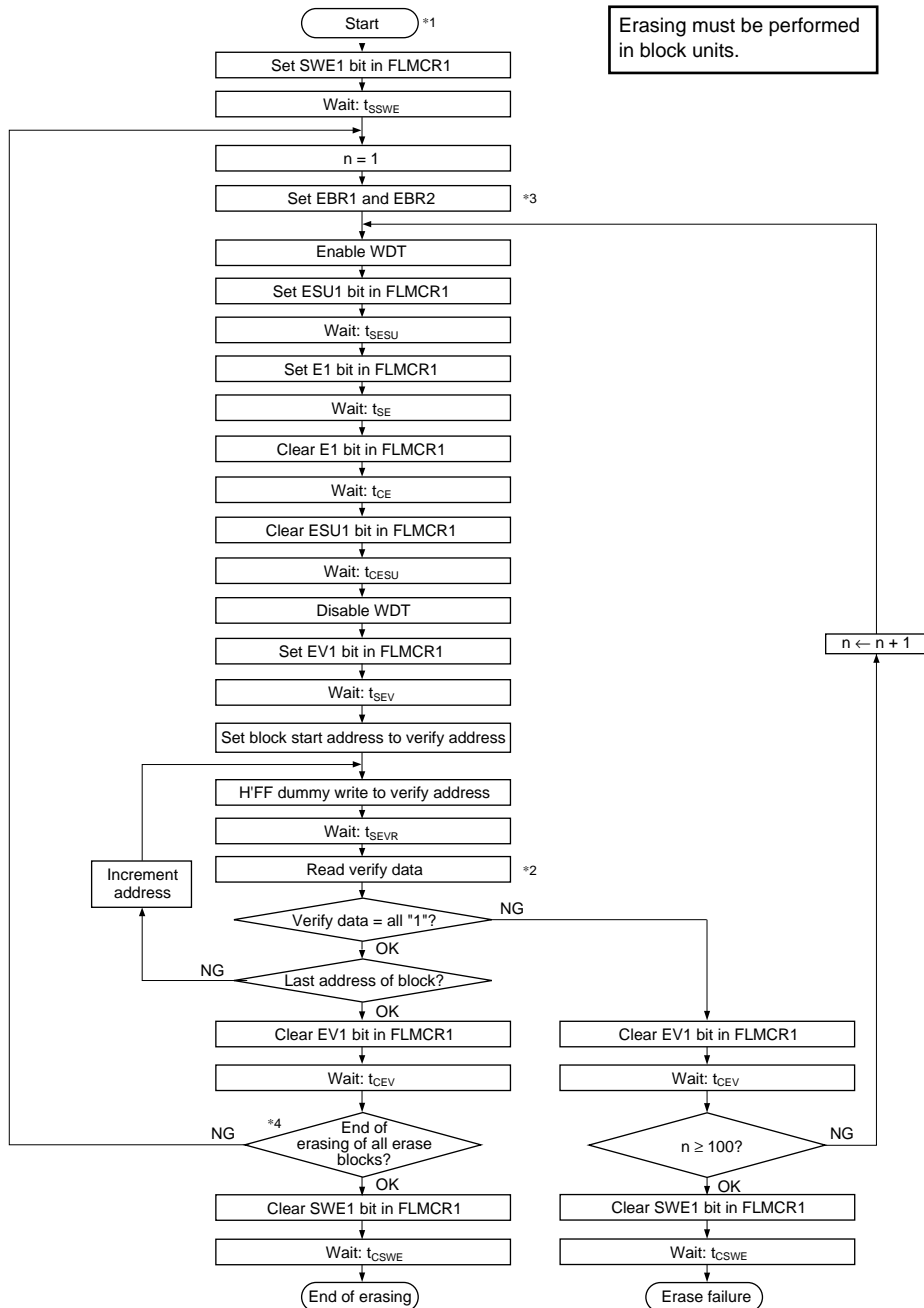
After the elapse of the erase time, erase mode is exited. In exiting erase mode, the E1 bit in FLMCR1 is cleared, then after an interval of  $t_{CE}$  or longer the ESU1 bit is cleared, and after a further interval of  $t_{CESU}$  or longer the watchdog timer is halted.

Note: With flash memory erasing, preprogramming (setting all memory data in the memory to be erased to all “0”) is not necessary before starting the erase procedure.

#### 20.7.4 Erase-Verify Mode

In erase-verify mode, data is read after memory has been erased to check whether it has been correctly erased.

A transition to erase-verify mode is made by setting the E1 bit in FLMCR1 and waiting for an interval of  $t_{SEV}$ . Before reading in erase-verify mode, perform a dummy write of H'FF data to the read addresses, and then wait for an interval of  $t_{SEVR}$  or longer. When the flash memory is read in this state (verify data is read in longword units), the data at the latched address is read. If the read data has been erased (all “1”), a dummy write is performed to the next address, and erase-verify is performed. If there are any unerased blocks, make a 1-bit setting for the flash memory area to be erased, and repeat the erase/erase-verify sequence as before. Ensure that the operation is not repeated more than 100 times. When verification is completed, exit erase-verify mode. Erase-verify mode is exited by clearing the EV1 bit in FLMCR1, then waiting for an interval of  $t_{CEV}$  or longer. If erasure has been completed on all the erase blocks, clear the SWE1 bit in FLMCR1. If there are any unerased blocks, make a 1-bit setting for the flash memory area to be erased, and repeat the erase/erase-verify sequence as before.



- Notes:
1. Preprogramming (setting erase block data to all "0") is not necessary.
  2. Verify data is read in 32-bit (longword) units.
  3. Set only one bit in EBR1 and EBR2. More than one bit cannot be set.
  4. Erasing is performed in block units. To erase a number of blocks, each block must be erased in turn.

**Figure 20.15 Erase/Erase-Verify Flowchart**

**Table 20.9 Erase/Erase-Verify Parameter**

Flow Section	Item	Symbol	Min	Typ	Max	Unit	Notes
Erase/ erase-verify	Wait time after ESU1 bit setting	$t_{\text{SESU}}$	100	100	—	$\mu\text{s}$	
	Wait time after E1 bit setting	$t_{\text{SE}}$	10	10	100	ms	Erase time wait
	Wait time after E1 bit clearing	$t_{\text{CE}}$	10	10	—	$\mu\text{s}$	
	Wait time after ESU1 bit clearing	$t_{\text{CESU}}$	10	10	—	$\mu\text{s}$	
	Wait time after EV1 bit setting	$t_{\text{SEV}}$	20	20	—	$\mu\text{s}$	
	Wait time after dummy write	$t_{\text{SEVR}}$	2	2	—	$\mu\text{s}$	
	Wait time after EV1 bit clearing	$t_{\text{CEV}}$	4	4	—	$\mu\text{s}$	
All	Wait time after SWE1 bit setting	$t_{\text{SSWE}}$	1	1	—	$\mu\text{s}$	
	Wait time after SWE1 bit clearing	$t_{\text{CSWE}}$	100	100	—	$\mu\text{s}$	

## 20.8 Protection

There are two kinds of flash memory program/erase protection, hardware protection and software protection.

### 20.8.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted. Hardware protection is reset by settings in flash memory control register 1 (FLMCR1), erase block register 1 (EBR1), and erase block register 2 (EBR2). The FLMCR1, EBR1, and EBR2 settings are retained in the error-protected state. (See table 20.10.)

**Table 20.10 Hardware Protection**

Item	Description	Functions	
		Program	Erase
FWE pin protection	<ul style="list-style-type: none"><li>When a low level is input to the FWE pin, FLMCR1, FLMCR2, EBR1, and EBR2 are initialized, and the program/erase-protected state is entered.</li></ul>	Yes	Yes
Reset/standby protection	<ul style="list-style-type: none"><li>In a power-on reset (including a WDT power-on reset) and in standby mode, FLMCR1, FLMCR2, EBR1, and EBR2 are initialized, and the program/erase-protected state is entered.</li><li>In a reset via the <math>\overline{\text{RES}}</math> pin, the reset state is not entered unless the <math>\overline{\text{RES}}</math> pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the <math>\overline{\text{RES}}</math> pin low for the <math>\overline{\text{RES}}</math> pulse width specified in the AC Characteristics section. Do not execute a reset during programming or erasing, as the values in the flash memory are not guaranteed if this is done. In this case, execute an erase, then execute programming once again.</li></ul>	Yes	Yes

## 20.8.2 Software Protection

Software protection can be implemented by setting the SWE1 bit in FLMCR1, erase block register 1 (EBR1), erase block register 2 (EBR2), and the RAMS bit in the RAM emulation register (RAMER). When software protection is in effect, setting the P1 or E1 bit in flash memory control register 1 (FLMCR1), does not cause a transition to program mode or erase mode. (See table 20.11.)

**Table 20.11 Software Protection**

Item	Description	Functions	
		Program	Erase
SWE bit protection	<ul style="list-style-type: none"><li>Setting bit SWE1 in FLMCR1 to 0 sets the program/erase-protected state. (Execute the program in the on-chip RAM, external memory.)</li></ul>	Yes	Yes
Block specification protection	<ul style="list-style-type: none"><li>Erase protection can be set for individual blocks by settings in erase block register 1 (EBR1) and erase block register 2 (EBR2).</li><li>Setting EBR1 and EBR2 to H'00 places all blocks in the erase-protected state.</li></ul>	—	Yes
Emulation protection	<ul style="list-style-type: none"><li>Setting the RAMS bit to 1 in the RAM emulation register (RAMER) places all blocks in the program/erase-protected state.</li></ul>	Yes	Yes

## 20.8.3 Error Protection

In error protection, an error is detected when SH7052F/SH7053F runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

If the SH7052F/SH7053F malfunctions during flash memory programming/erasing, the FLER bit is set to 1 in FLMCR2 and the error protection state is entered. The FLMCR1, FLMCR2, EBR1, and EBR2 settings are retained, but program mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be re-entered by re-setting the P1 or E1 bit. However, PV1 and EV1 bit setting is enabled, and a transition can be made to verify mode.

FLER bit setting conditions are as follows:

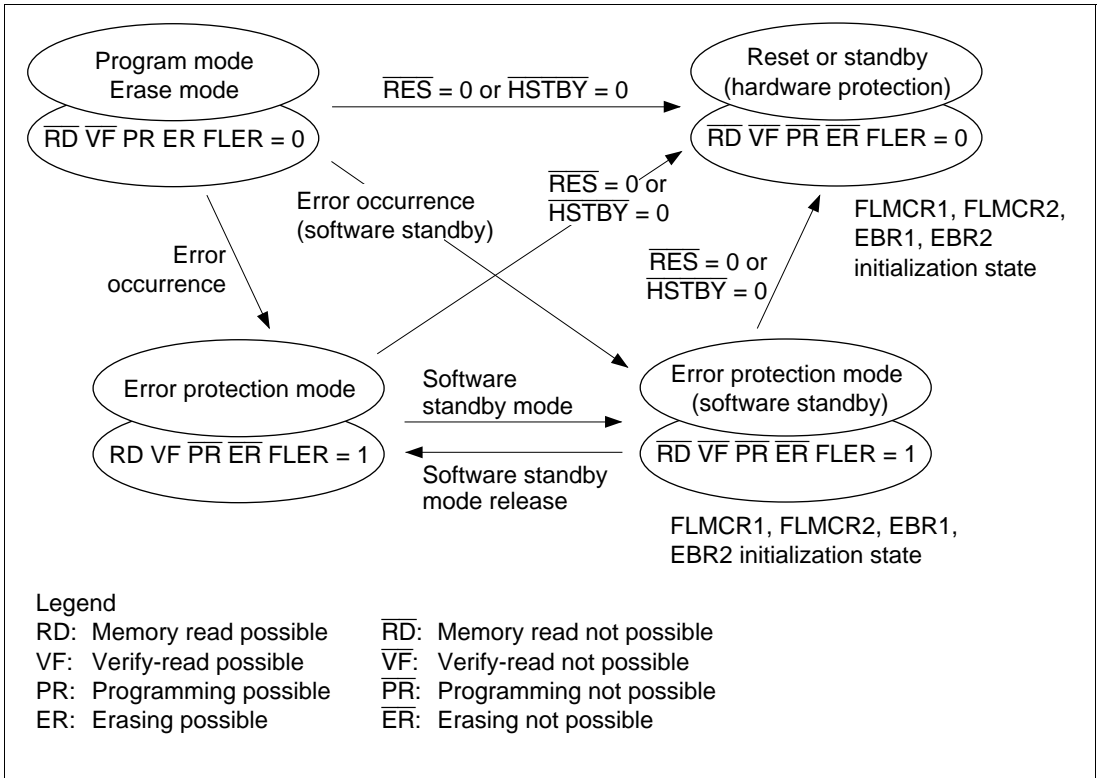
1. When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)



2. When a SLEEP instruction (including software standby) is executed during programming/erasing

Error protection is released only by a power-on reset and in hardware standby mode.

Figure 20.16 shows the flash memory state transition diagram.



**Figure 20.16 Flash Memory State Transitions**

## 20.9 Flash Memory Emulation in RAM

Making a setting in the RAM emulation register (RAMER) enables part of RAM to be overlapped onto the flash memory area so that data to be written to flash memory can be emulated in RAM in real time. After the RAMER setting has been made, accesses cannot be made from the flash memory area or the RAM area overlapping flash memory. Emulation can be performed in user mode and user program mode. Figure 20.17 shows an example of emulation of real-time flash memory programming.

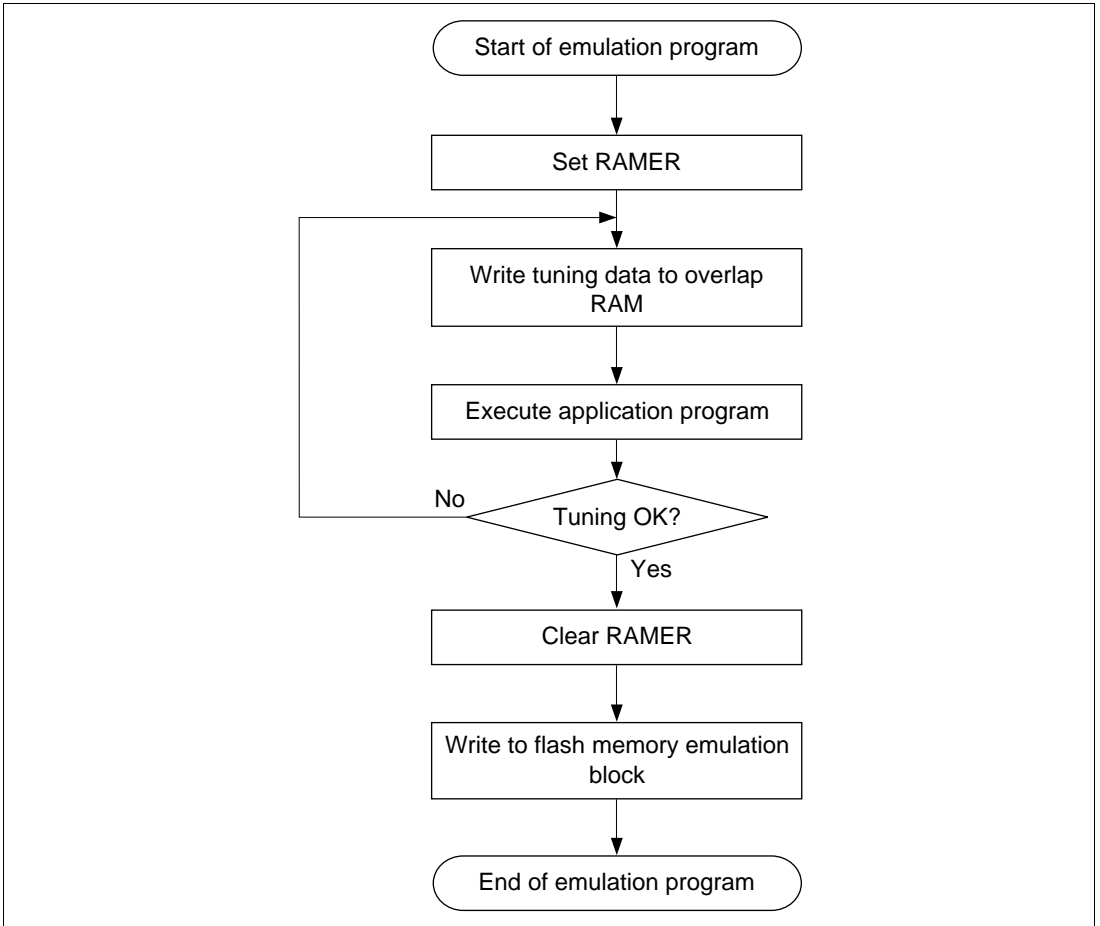
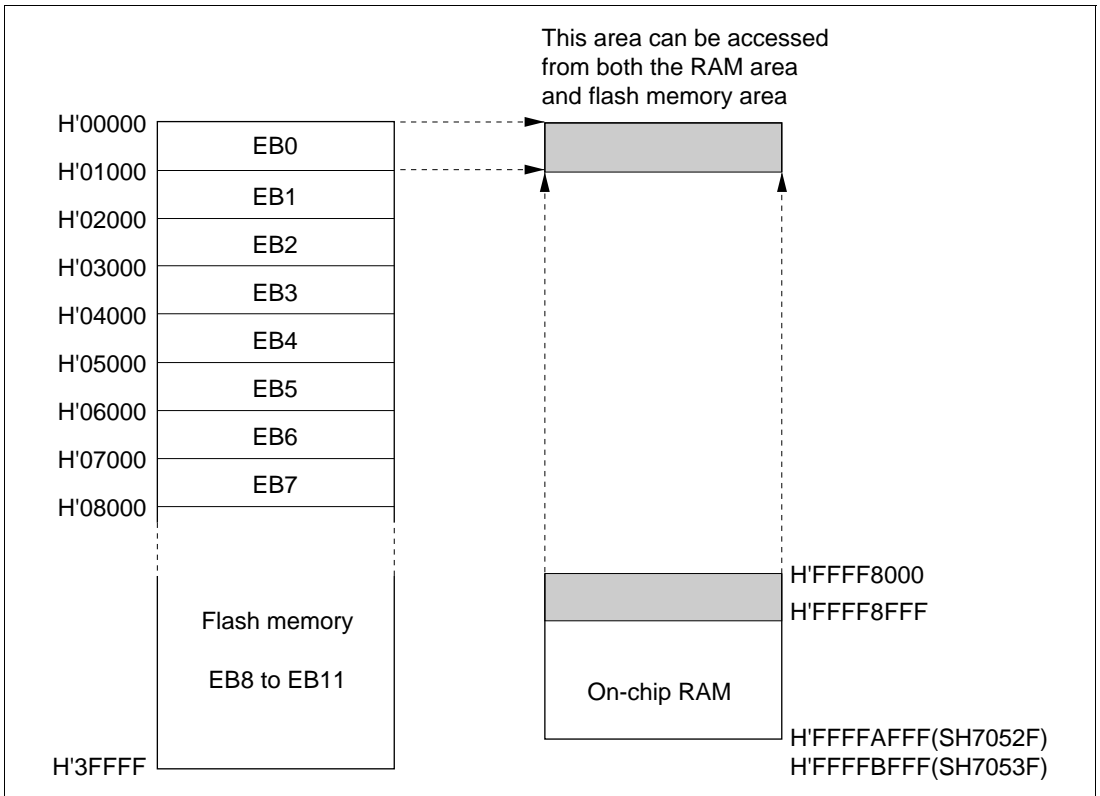


Figure 20.17 Flowchart for Flash Memory Emulation in RAM



**Figure 20.18 Example of RAM Overlap Operation**

### Example in which Flash Memory Block Area EB0 is Overlapped

1. Set bits RAMS and RAM2 to RAM0 in RAMER to 1, 0, 0, 0, to overlap part of RAM onto the area (EB0) for which real-time programming is required.
2. Real-time programming is performed using the overlapping RAM.
3. After the program data has been confirmed, the RAMS bit is cleared, releasing RAM overlap.
4. The data written in the overlapping RAM is written into the flash memory space (EB0).

- Notes:
1. When the RAMS bit is set to 1, program/erase protection is enabled for all blocks regardless of the value of RAM2 to RAM0 (emulation protection). In this state, setting the P1 or E1 bit in flash memory control register 1 (FLMCR1) will not cause a transition to program mode or erase mode. When actually programming or erasing a flash memory area, the RAMS bit should be cleared to 0.
  2. A RAM area cannot be erased by execution of software in accordance with the erase algorithm while flash memory emulation in RAM is being used.

## 20.10 Note on Flash Memory Programming/Erasing

In the on-board programming modes (user mode and user program mode), NMI input should be disabled to give top priority to the program/erase operations (including RAM emulation).

Do not perform a write to a ROM area immediately after an ATU register write cycle. For details, see “Writing to ROM Area Immediately after ATU Register Write” in section 10.7, Usage Notes.

When reading flash memory after changing the SWE1 bit from 1 to 0 on completion of a program/erase operation, wait for at least  $t_{CSWE}$  after clearing SWE1 to 0 before executing the flash memory read. Regarding the timing of  $\overline{RES}$  input after changing the SWE1 bit from 1 to 0 on completion of a program/erase operation, wait for at least  $t_{CSWE}$  after clearing SWE1 to 0 before executing the reset operation.

## 20.11 Flash Memory Programmer Mode

Programs and data can be written and erased in programmer mode as well as in the on-board programming modes. In programmer mode, flash memory read mode, auto-program mode, auto-erase mode, and status read mode are supported. In auto-program mode, auto-erase mode, and status read mode, a status polling procedure is used, and in status read mode, detailed internal signals are output after execution of an auto-program or auto-erase operation.

In programmer mode, set the mode pins to programmer mode (see table 20.12) and input a 6 MHz input clock, so that the SH7052F/SH7053F runs at 24 MHz.

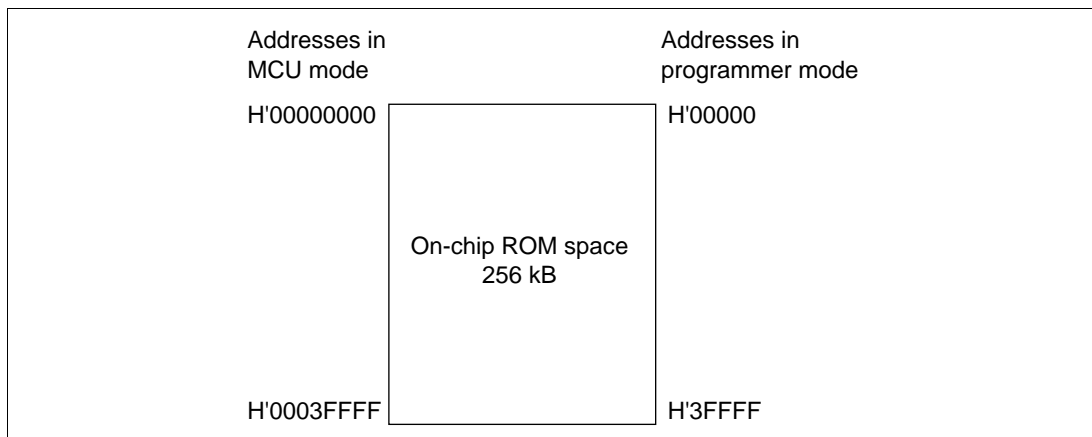
Table 20.12 shows the pin settings for programmer mode. For the pin names in programmer mode, see section 1.3.2, Pin Functions.

**Table 20.12 PROM Mode Pin Settings**

Pin Names	Settings
Mode pins: MD2, MD1, MD0	0, 1, 1
FWE pin	High level input (in auto-program and auto-erase modes)
$\overline{RES}$ pin	Power-on reset circuit
XTAL, EXTAL, PLLV <sub>CC</sub> , PLLCAP, PLLV <sub>SS</sub> pins	Oscillator circuit

### 20.11.1 Socket Adapter Pin Correspondence Diagram

Connect the socket adapter to the chip as shown in figure 20.20. This will enable conversion to a 40-pin arrangement. The on-chip ROM memory map is shown in figure 20.19, and the socket adapter pin correspondence diagram in figure 20.20.



**Figure 20.19 On-Chip ROM Memory Map**

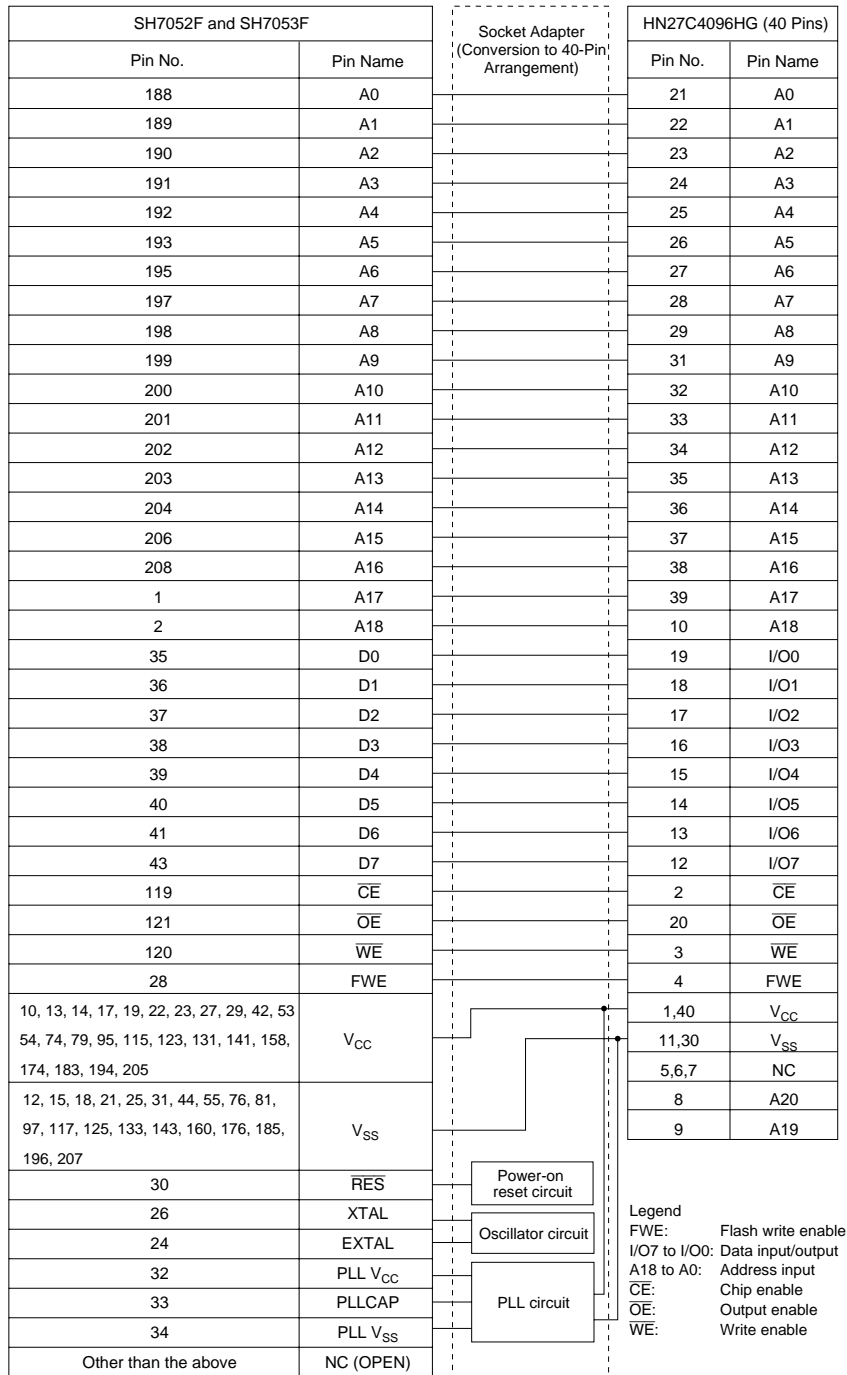


Figure 20.20 Socket Adapter Pin Correspondence Diagram

## 20.11.2 Programmer Mode Operation

Table 20.13 shows how the different operating modes are set when using programmer mode, and table 20.14 lists the commands used in programmer mode. Details of each mode are given below.

- **Memory Read Mode**  
Memory read mode supports byte reads.
- **Auto-Program Mode**  
Auto-program mode supports programming of 128 bytes at a time. Status polling is used to confirm the end of auto-programming.
- **Auto-Erase Mode**  
Auto-erase mode supports automatic erasing of the entire flash memory. Status polling is used to confirm the end of auto-programming.
- **Status Read Mode**  
Status polling is used for auto-programming and auto-erasing, and normal termination can be confirmed by reading the I/O6 signal. In status read mode, error information is output if an error occurs.

**Table 20.13 Settings for Various Operating Modes In Programmer Mode**

Mode	Pin Names					
	FWE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O7 to I/O0	A18 to A0
Read	H or L	L	L	H	Data output	Ain
Output disable	H or L	L	H	H	Hi-z	X
Command write	H or L	L	H	L	Data input	*Ain
Chip disable	H or L	H	X	X	Hi-z	X

- Notes:
1. Chip disable is not a standby state; internally, it is an operation state.
  2. \*Ain indicates that there is also address input in auto-program mode.
  3. For command writes in auto-program and auto-erase modes, input a high level to the FWE pin.

**Table 20.14 Programmer Mode Commands**

Command Name	Number of Cycles	1st Cycle			2nd Cycle		
		Mode	Address	Data	Mode	Address	Data
Memory read mode	1 + n	Write	X	H'00	Read	RA	Dout
Auto-program mode	129	Write	X	H'40	Write	WA	Din
Auto-erase mode	2	Write	X	H'20	Write	X	H'20
Status read mode	2	Write	X	H'71	Write	X	H'71

Notes: 1. In auto-program mode, 129 cycles are required for command writing by a simultaneous 128-byte write.

2. In memory read mode, the number of cycles depends on the number of address write cycles (n).

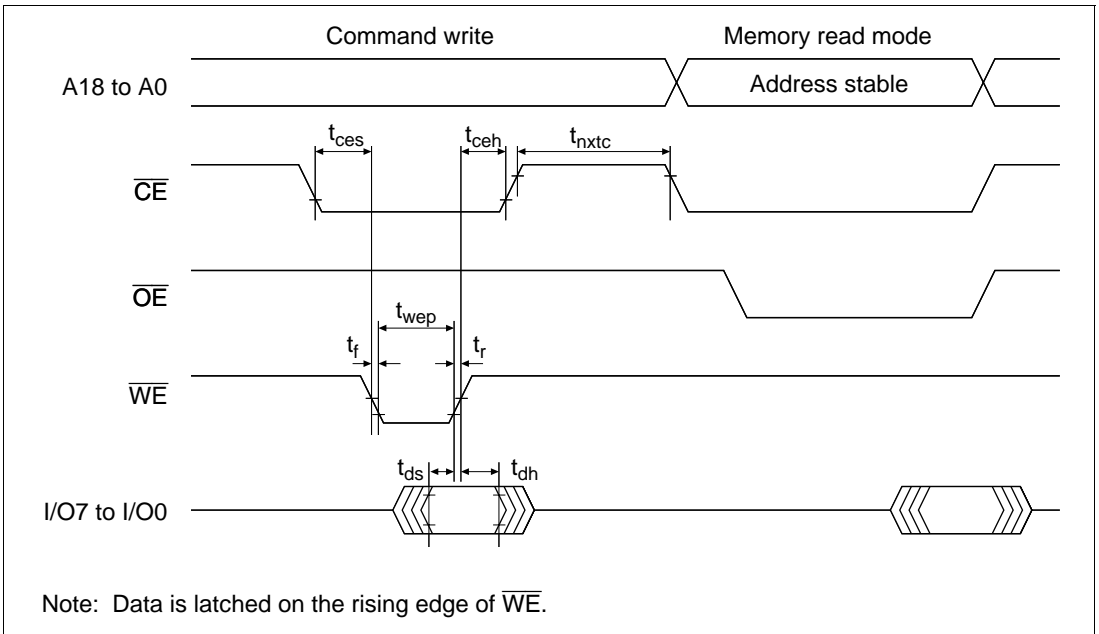
### 20.11.3 Memory Read Mode

1. After completion of auto-program/auto-erase/status read operations, a transition is made to the command wait state. When reading memory contents, a transition to memory read mode must first be made with a command write, after which the memory contents are read.
2. In memory read mode, command writes can be performed in the same way as in the command wait state.
3. Once memory read mode has been entered, consecutive reads can be performed.
4. After powering on, memory read mode is entered.

**Table 20.15 AC Characteristics in Transition to Memory Read Mode**  
(Conditions:  $V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{ceh}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
$\overline{\text{WE}}$ rise time	$t_r$		30	ns	
$\overline{\text{WE}}$ fall time	$t_f$		30	ns	

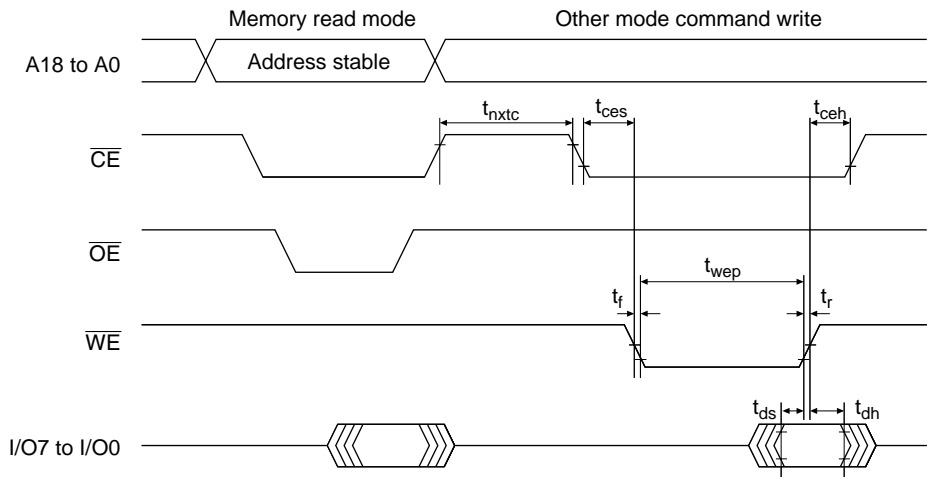




**Figure 20.21 Timing Waveforms for Memory Read after Memory Write**

**Table 20.16 AC Characteristics in Transition from Memory Read Mode to Another Mode**  
 (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{CE}$ hold time	$t_{ceh}$	0		ns	
$\overline{CE}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
$\overline{WE}$ rise time	$t_r$		30	ns	
$\overline{WE}$ fall time	$t_f$		30	ns	

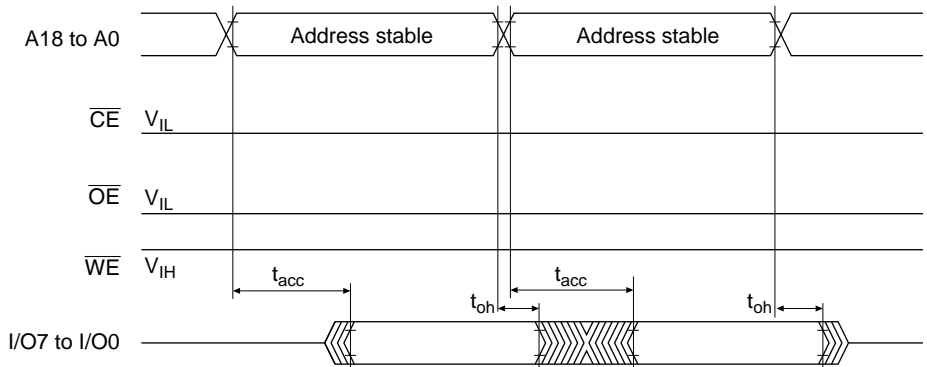


Note: Do not enable  $\overline{WE}$  and  $\overline{OE}$  at the same time.

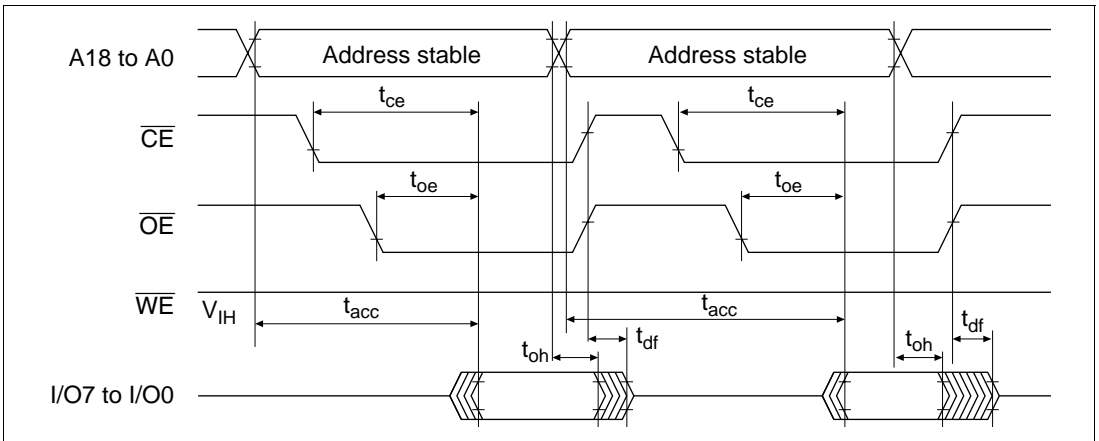
**Figure 20.22 Timing Waveforms in Transition from Memory Read Mode to Another Mode**

**Table 20.17 AC Characteristics in Memory Read Mode (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Access time	$t_{acc}$		20	$\mu\text{s}$	
$\overline{CE}$ output delay time	$t_{ce}$		150	ns	
$\overline{OE}$ output delay time	$t_{oe}$		150	ns	
Output disable delay time	$t_{df}$		100	ns	
Data output hold time	$t_{oh}$	5		ns	



**Figure 20.23  $\overline{CE}$  and  $\overline{OE}$  Enable State Read Timing Waveforms**



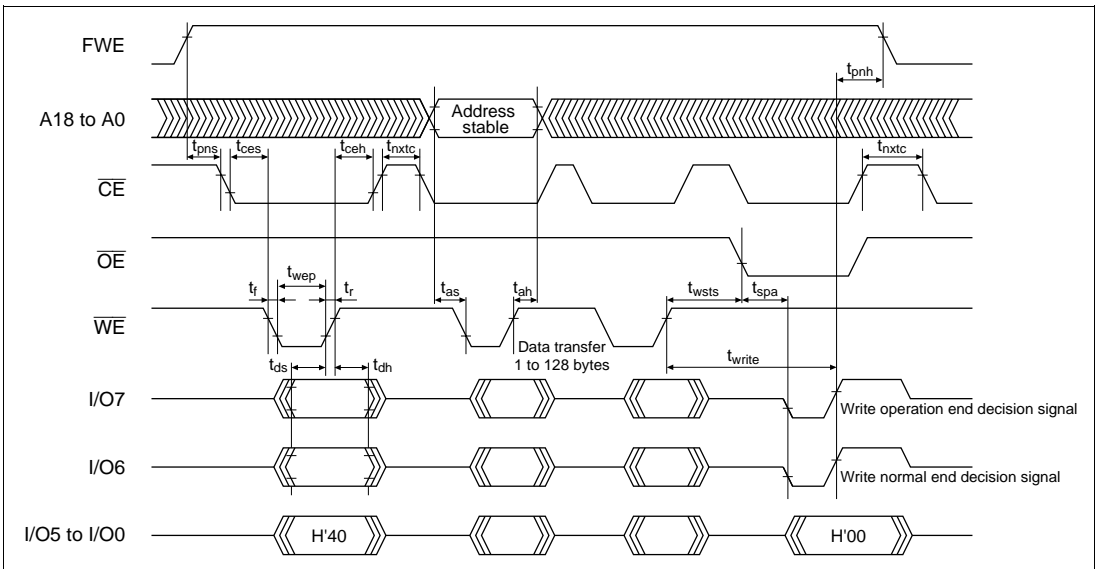
**Figure 20.24**  $\overline{CE}$  and  $\overline{OE}$  Clock System Read Timing Waveforms

### 20.11.4 Auto-Program Mode

1. In auto-program mode, 128 bytes are programmed simultaneously. This should be carried out by executing 128 consecutive byte transfers.
2. A 128-byte data transfer is necessary even when programming fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. The lower 7 bits of the transfer address must be low. If a value other than an effective address is input, processing will switch to a memory write operation but a write error will be flagged.
4. Memory address transfer is performed in the second cycle (figure 20.25). Do not perform transfer after the second cycle.
5. Do not perform a command write during a programming operation.
6. Perform one auto-program operation for a 128-byte block for each address. Two or more additional programming operations cannot be performed on a previously programmed address block.
7. Confirm normal end of auto-programming by checking I/O6. Alternatively, status read mode can also be used for this purpose (I/O7 status polling uses the auto-program operation end decision pin).
8. Status polling I/O6 and I/O7 pin information is retained until the next command write. As long as the next command write has not been performed, reading is possible by enabling  $\overline{CE}$  and  $\overline{OE}$ .

**Table 20.18 AC Characteristics in Auto-Program Mode (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{ceh}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
Status polling start time	$t_{wsts}$	1		ms	
Status polling access time	$t_{spa}$		150	ns	
Address setup time	$t_{as}$	0		ns	
Address hold time	$t_{ah}$	60		ns	
Memory write time	$t_{write}$	1	3000	ms	
Write setup time	$t_{pns}$	100		ns	
Write end setup time	$t_{pnh}$	100		ns	
$\overline{\text{WE}}$ rise time	$t_r$		30	ns	
$\overline{\text{WE}}$ fall time	$t_f$		30	ns	



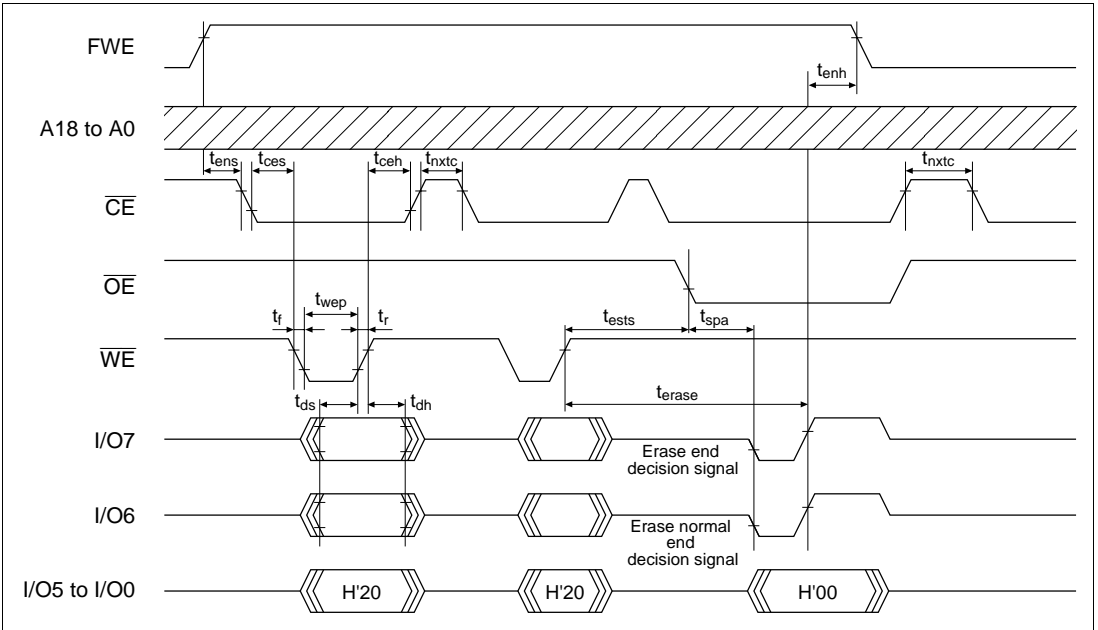
**Figure 20.25 Auto-Program Mode Timing Waveforms**

## 20.11.5 Auto-Erase Mode

1. Auto-erase mode supports only entire memory erasing.
2. Do not perform a command write during auto-erasing.
3. Confirm normal end of auto-erasing by checking I/O6. Alternatively, status read mode can also be used for this purpose (I/O7 status polling uses the auto-erase operation end decision pin).
4. Status polling I/O6 and I/O7 pin information is retained until the next command write. As long as the next command write has not been performed, reading is possible by enabling  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$ .

**Table 20.19 AC Characteristics in Auto-Erase Mode (Conditions:  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{\text{nxtc}}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{\text{ceh}}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{\text{ces}}$	0		ns	
Data hold time	$t_{\text{dh}}$	50		ns	
Data setup time	$t_{\text{ds}}$	50		ns	
Write pulse width	$t_{\text{wep}}$	70		ns	
Status polling start time	$t_{\text{ests}}$	1		ms	
Status polling access time	$t_{\text{s pa}}$		150	ns	
Memory erase time	$t_{\text{erase}}$	100	40000	ms	
Erase setup time	$t_{\text{ens}}$	100		ns	
Erase end setup time	$t_{\text{enh}}$	100		ns	
$\overline{\text{WE}}$ rise time	$t_{\text{r}}$		30	ns	
$\overline{\text{WE}}$ fall time	$t_{\text{f}}$		30	ns	



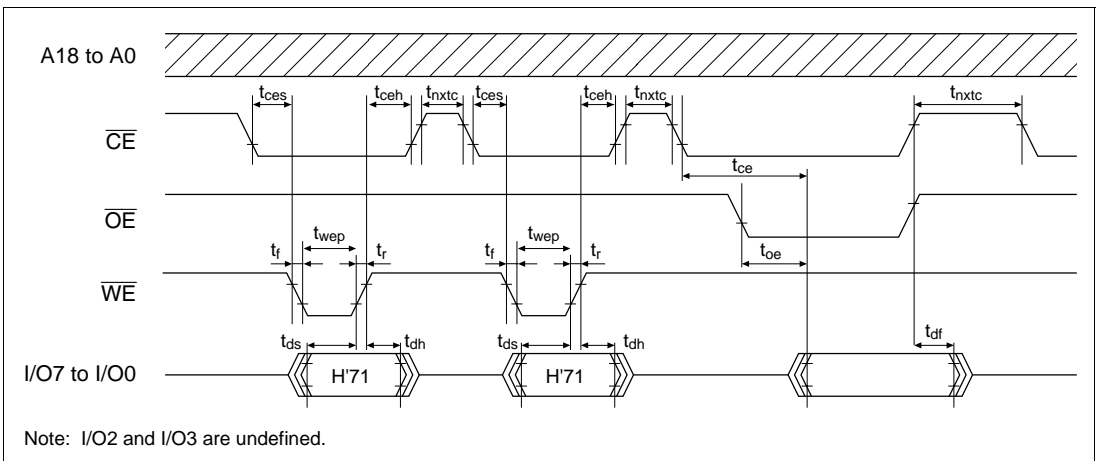
**Figure 20.26 Auto-Erase Mode Timing Waveforms**

## 20.11.6 Status Read Mode

1. Status read mode is provided to identify the kind of abnormal end. Use this mode when an abnormal end occurs in auto-program mode or auto-erase mode.
2. The return code is retained until a command write other than a status read mode command write is executed.

**Table 20.20 AC Characteristics in Status Read Mode (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Read time after command write	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{ceh}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
$\overline{\text{OE}}$ output delay time	$t_{oe}$		150	ns	
Disable delay time	$t_{df}$		100	ns	
$\overline{\text{CE}}$ output delay time	$t_{ce}$		150	ns	
$\overline{\text{WE}}$ rise time	$t_r$		30	ns	
$\overline{\text{WE}}$ fall time	$t_f$		30	ns	



**Figure 20.27 Status Read Mode Timing Waveforms**

**Table 20.21 Status Read Mode Return Commands**

Pin Name	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Attribute	Normal end decision	Command error	Programming error	Erase error	—	—	Programming or erase count exceeded	Effective address error
Initial value	0	0	0	0	0	0	0	0
Indications	Normal end: 0 Abnormal end: 1	Command error: 1 Otherwise: 0	Programming error: 1 Otherwise: 0	Erasing error: 1 Otherwise: 0	—	—	Count exceeded: 1 Otherwise: 0	Effective address error: 1 Otherwise: 0

Note: I/O2 and I/O3 are undefined.

### 20.11.7 Status Polling

1. The I/O7 status polling flag indicates the operating status in auto-program/auto-erase mode.
2. The I/O6 status polling flag indicates a normal or abnormal end in auto-program/auto-erase mode.

**Table 20.22 Status Polling Output Truth Table**

Pin Name	During Internal Operation		—	Normal End
	Abnormal End	—		
I/O7	0	1	0	1
I/O6	0	0	1	1
I/O0 to I/O5	0	0	0	0

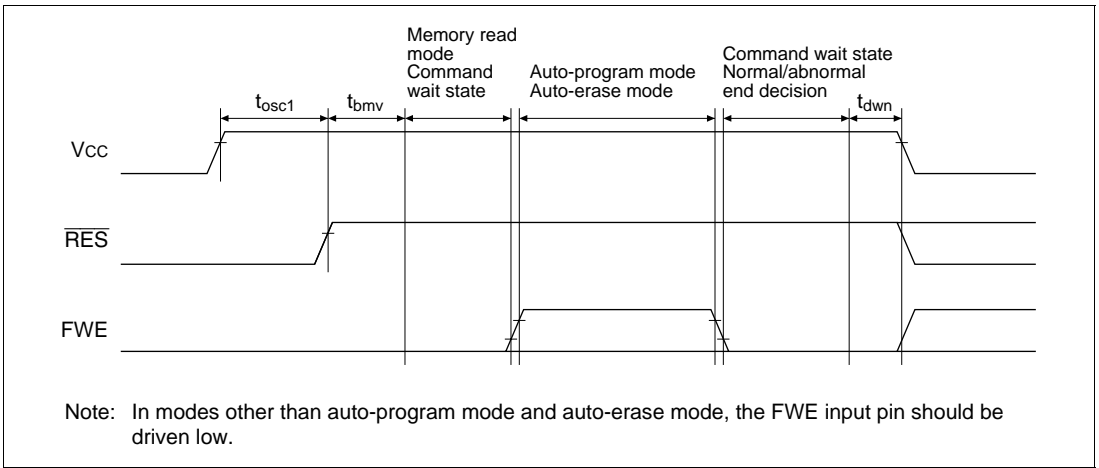
### 20.11.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

**Table 20.23 Stipulated Transition Times to Command Wait State**

Item	Symbol	Min	Max	Unit	Notes
Standby release (oscillation stabilization time)	$t_{osc1}$	30		ms	
Programmer mode setup time	$t_{bmv}$	10		ms	
$V_{CC}$ hold time	$t_{dwn}$	0		ms	





**Figure 20.28 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence**

### 20.11.9 Notes on Memory Programming

1. When programming addresses which have previously been programmed, carry out auto-erasing before auto-programming.
2. When performing programming using programmer mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.

- Notes:
1. The flash memory is initially in the erased state when the device is shipped by Hitachi. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.
  2. Auto-programming should be performed once only on the same address block. Additional programming cannot be performed on previously programmed address blocks.



## 21.1 Features

The SH7054F has 384 kbytes of on-chip flash memory. The features of the flash memory are summarized below.

- Four flash memory operating modes
  - Program mode
  - Erase mode
  - Program-verify mode
  - Erase-verify mode
- Programming/erase methods

The flash memory is programmed 128 bytes at a time. Block erase (in single-block units) can be performed. To erase the entire flash memory, individual blocks must be erased in turn. Block erasing can be performed as required on 4 kB, 32 kB, and 64 kB blocks.
- Programming/erase times

The flash memory programming time is 7 ms (typ.) for simultaneous 128-byte programming, equivalent to 55  $\mu$ s (typ.) per byte, and the erase time is 100 ms (typ.) per block.
- Reprogramming capability

The flash memory can be reprogrammed up to 100 times.
- On-board programming modes

There are two modes in which flash memory can be programmed/erased/verified on-board:

  - Boot mode
  - User program mode
- Automatic bit rate adjustment

With data transfer in boot mode, the SH7054F's bit rate can be automatically adjusted to match the transfer bit rate of the host.
- Flash memory emulation in RAM

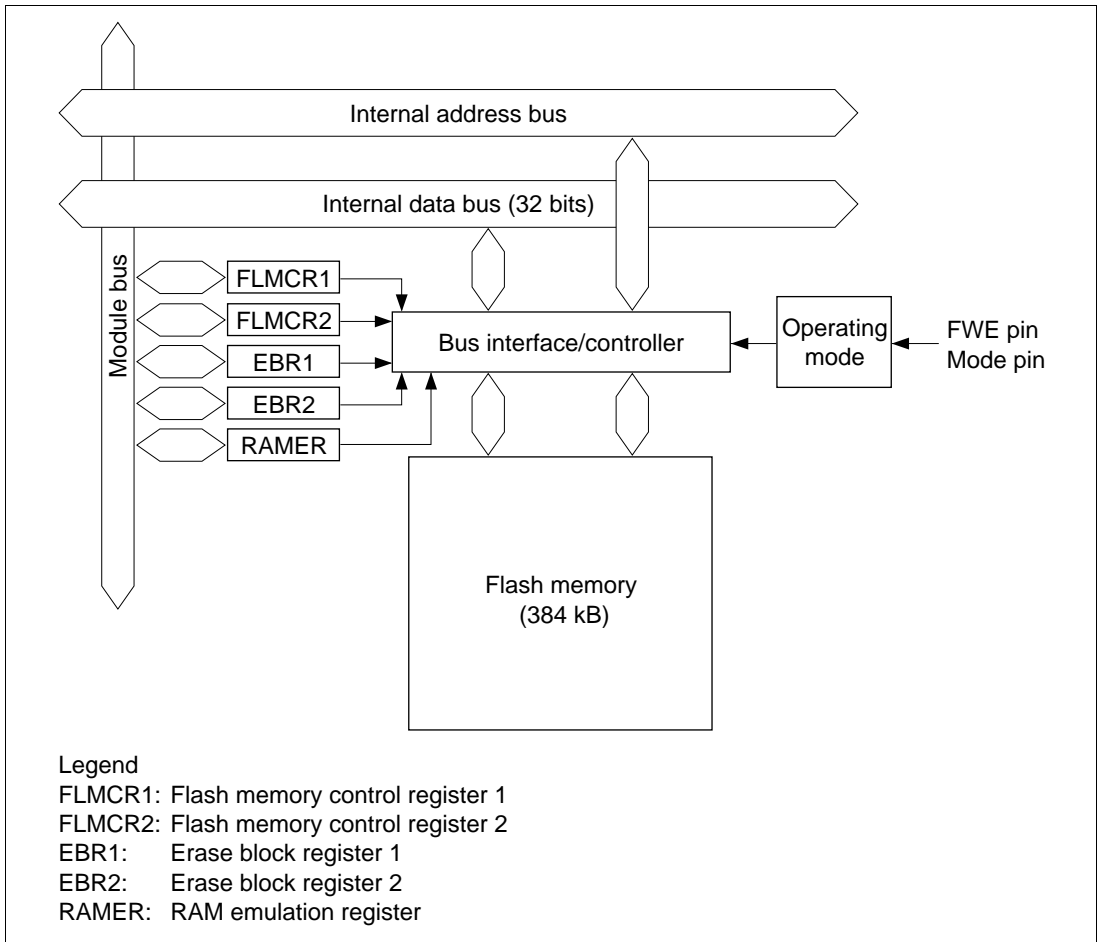
Flash memory programming can be emulated in real time by overlapping a part of RAM onto flash memory.
- Protect modes

There are two protect modes, hardware and software, which allow protected status to be designated for flash memory program/erase/verify operations.
- Programmer mode

Flash memory can be programmed/erased in programmer mode, using a PROM programmer, as well as in on-board programming mode.

## 21.2 Overview

### 21.2.1 Block Diagram



**Figure 21.1 Block Diagram of Flash Memory**

## 21.2.2 Mode Transitions

When the mode pins and the FWE pin are set in the reset state and a reset-start is executed, the microcomputer enters an operating mode as shown in figure 21.2. In user mode, flash memory can be read but not programmed or erased.

The boot, user program and programmer modes are provided as modes to write and erase the flash memory.

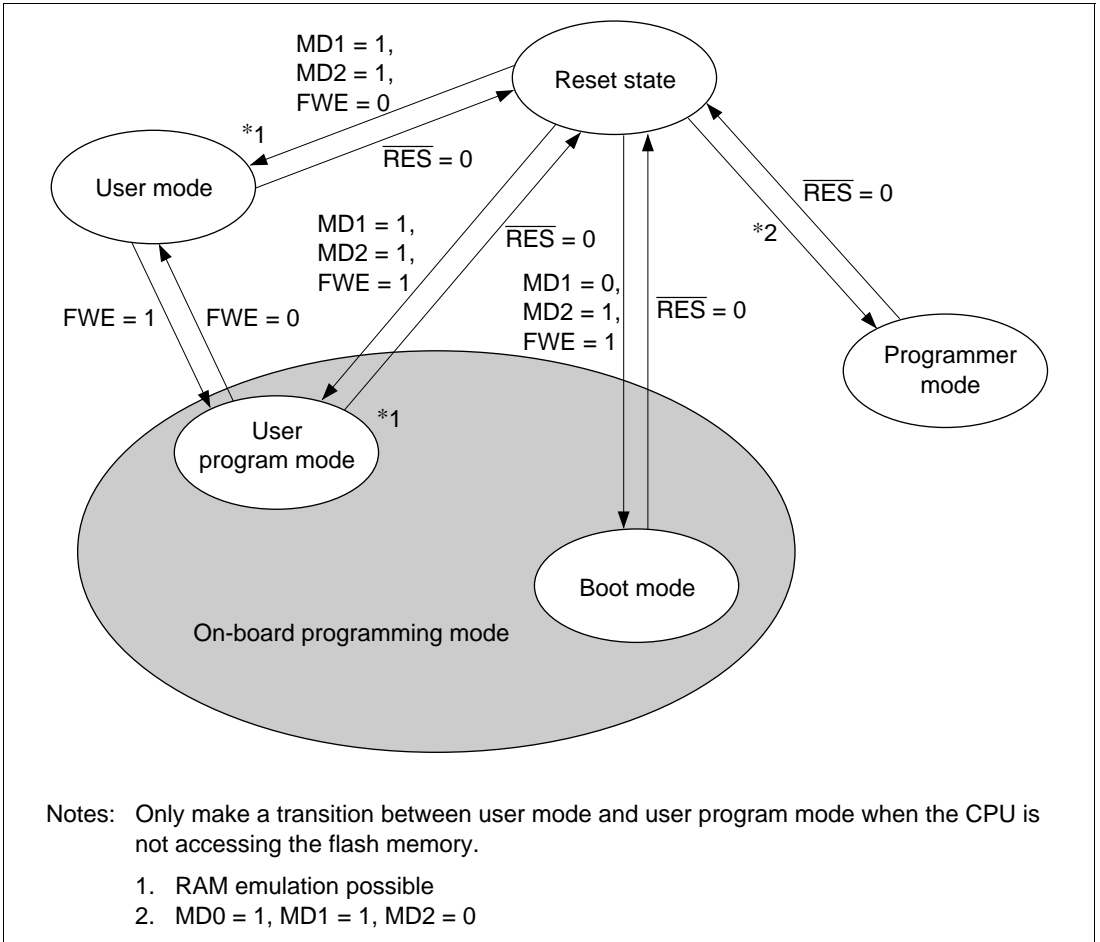


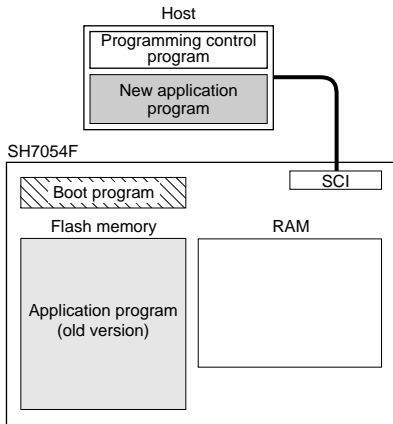
Figure 21.2 Flash Memory State Transitions

## 21.2.3 On-Board Programming Modes

### Boot Mode

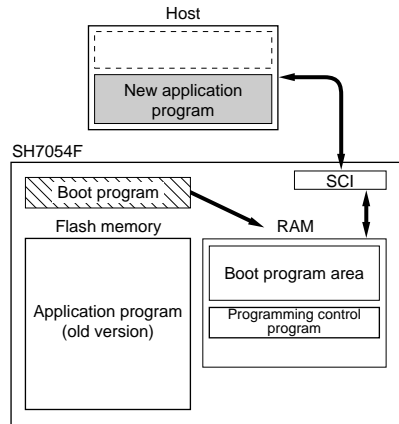
#### 1. Initial state

The old program version or data remains written in the flash memory. The user should prepare the programming control program and new application program beforehand in the host.



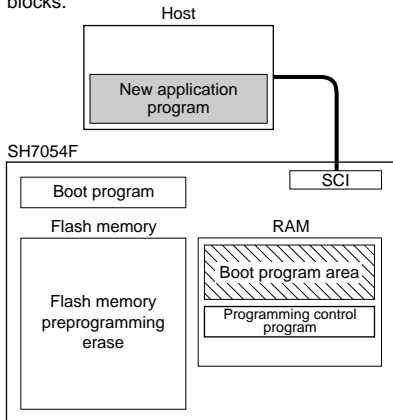
#### 2. Programming control program transfer

When boot mode is entered, the boot program in the SH7054F (originally incorporated in the chip) is started and the programming control program in the host is transferred to RAM via SCI communication. The boot program required for flash memory erasing is automatically transferred to the RAM boot program area.



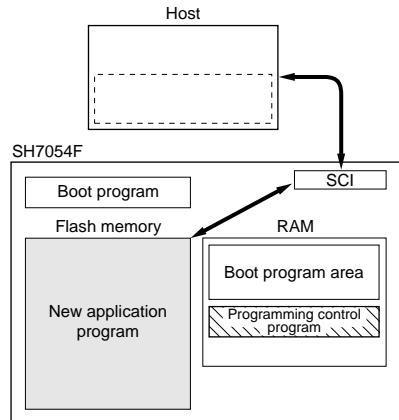
#### 3. Flash memory initialization

The erase program in the boot program area (in RAM) is executed, and the flash memory is initialized (to H'FF). In boot mode, total flash memory erasure is performed, without regard to blocks.



#### 4. Writing new application program

The programming control program transferred from the host to RAM is executed, and the new application program in the host is written into the flash memory.




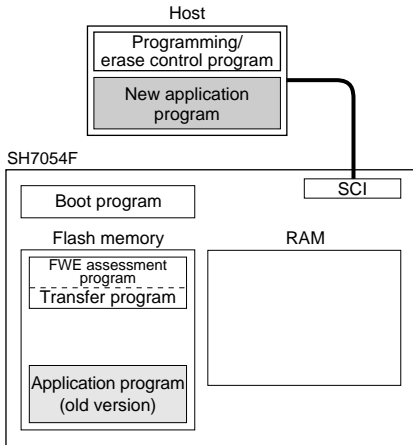
 Program execution state

Figure 21.3 Boot Mode

# User Program Mode

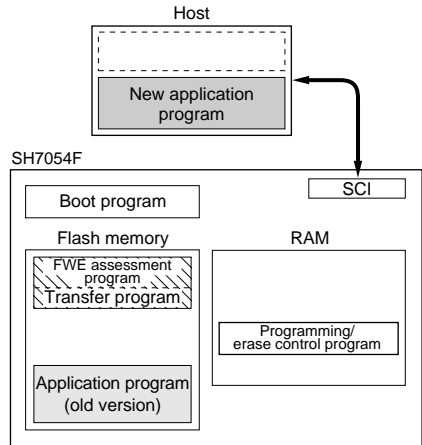
## 1. Initial state

The FWE assessment program that confirms that user program mode has been entered, and the program that will transfer the programming/erase control program from flash memory to on-chip RAM should be written into the flash memory by the user beforehand. The programming/erase control program should be prepared in the host or in the flash memory.



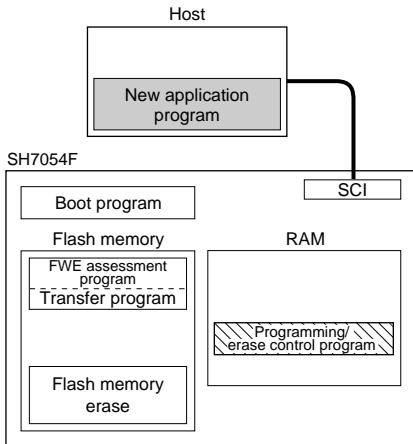
## 2. Programming/erase control program transfer

When user program mode is entered, user software confirms this fact, executes transfer program in the flash memory, and transfers the programming/erase control program to RAM.



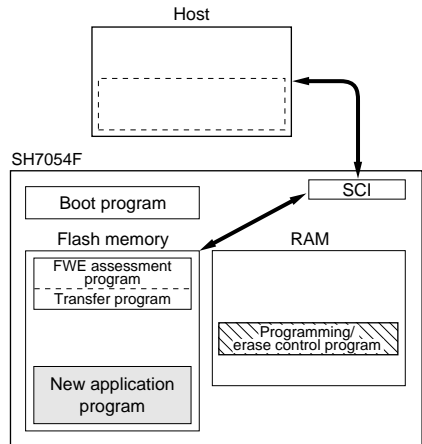
## 3. Flash memory initialization

The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.



## 4. Writing new application program

Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.




 Program execution state

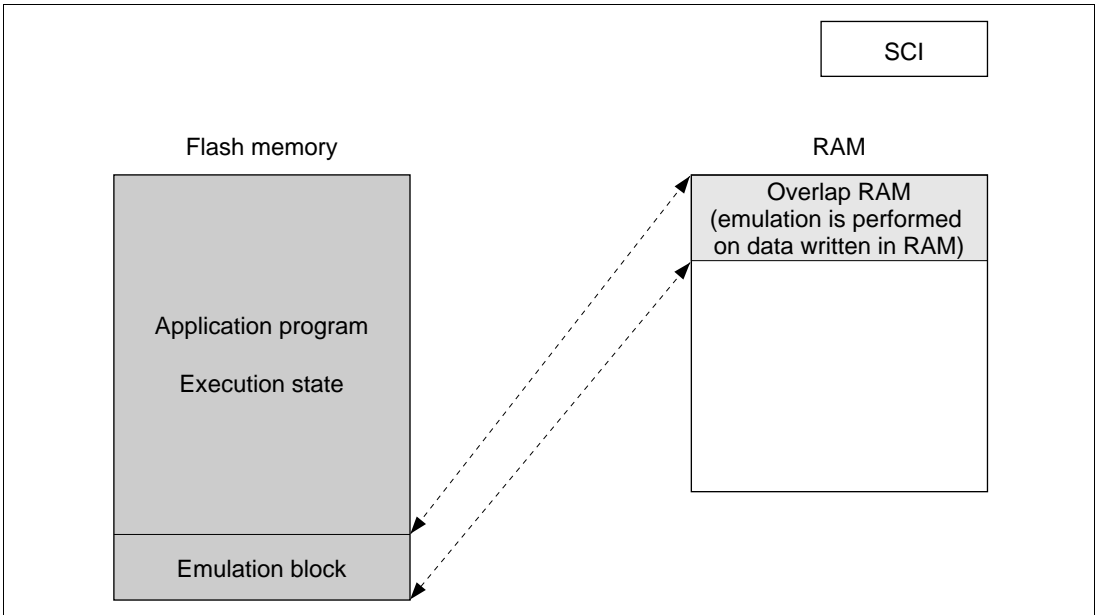
Figure 21.4 User Program Mode

## 21.2.4 Flash Memory Emulation in RAM

Emulation should be performed in user mode or user program mode. When the emulation block set in RAMER is accessed while the emulation function is being executed, data written in the overlap RAM is read.

### User Mode

- User Program Mode



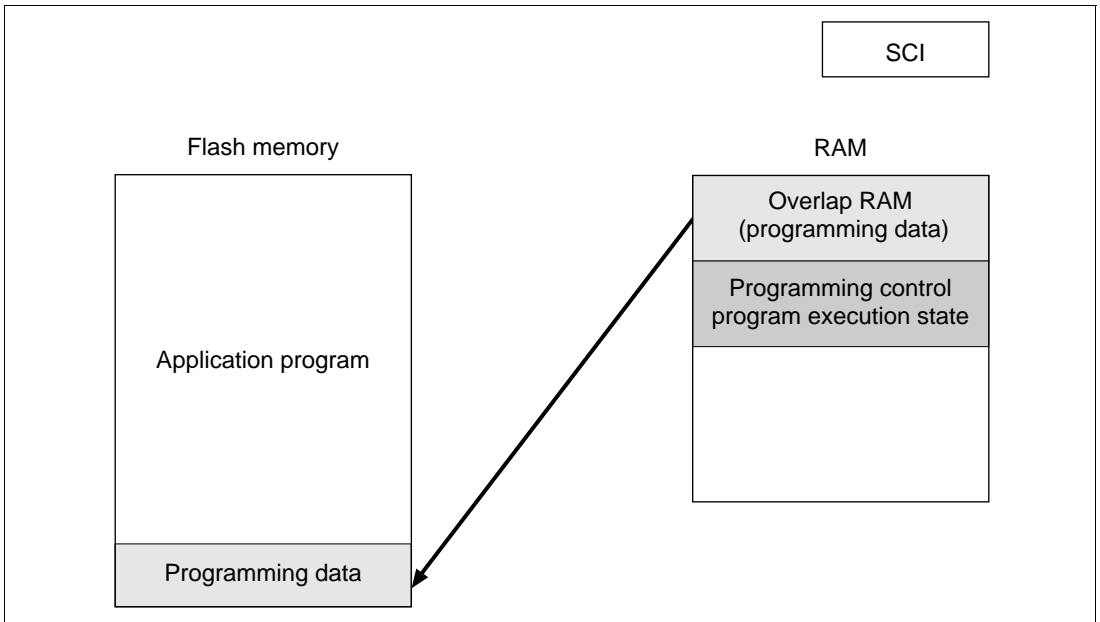
**Figure 21.5 Emulation**

When overlap RAM data is confirmed, the RAMS bit is cleared, RAM overlap is released, and writes should actually be performed to the flash memory.

When the programming control program is transferred to RAM, ensure that the transfer destination and the overlap RAM do not overlap, as this will cause data in the overlap RAM to be rewritten.



- User Program Mode



**Figure 21.6 Programming Flash Memory**

### 21.2.5 Differences between Boot Mode and User Program Mode

**Table 21.1 Differences between Boot Mode and User Mode**

	<b>Boot Mode</b>	<b>User Program Mode</b>
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	(2)	(1) (2) (3)

(1) Erase/erase-verify

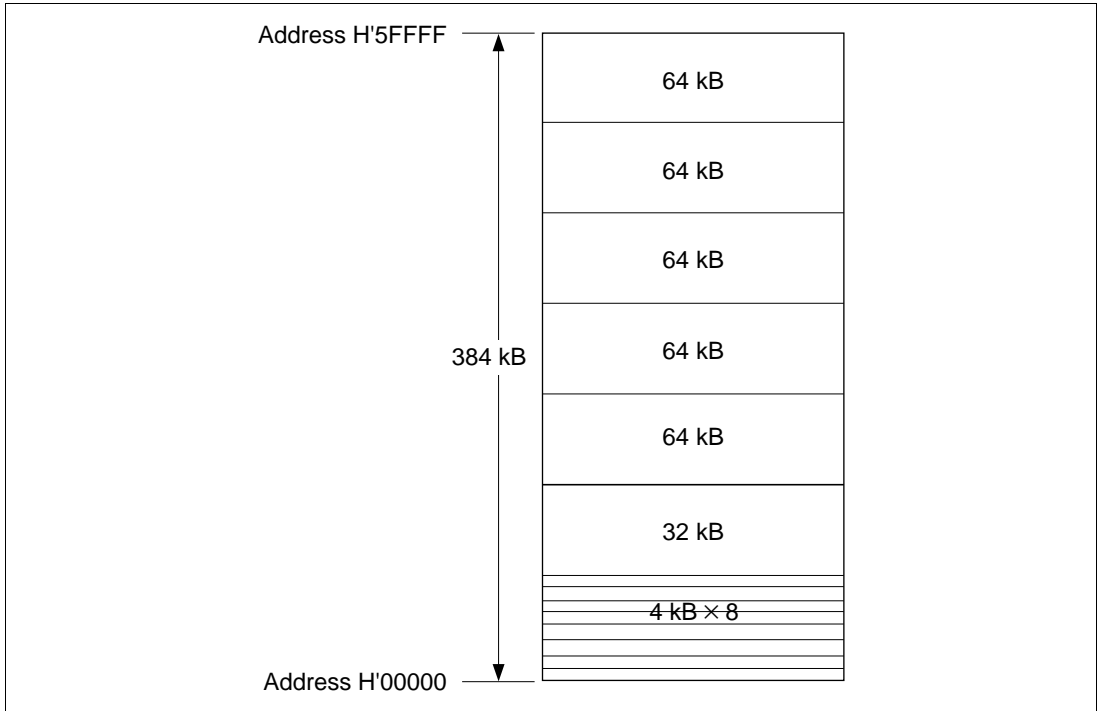
(2) Program/program-verify

(3) Emulation

Note: \* To be provided by the user, in accordance with the recommended algorithm.

## 21.2.6 Block Configuration

The flash memory is divided into five 64 kB blocks, one 32 kB block, and eight 4 kB blocks.



**Figure 21.7 Block Configuration**

## 21.3 Pin Configuration

The flash memory is controlled by means of the pins shown in table 21.2.

**Table 21.2 Pin Configuration**

Pin Name	Abbreviation	I/O	Function
Reset	$\overline{\text{RES}}$	Input	Reset
Flash write enable	FWE	Input	Flash program/erase protection by hardware
Mode 2	MD2	Input	Sets SH7054F operating mode
Mode 1	MD1	Input	Sets SH7054F operating mode
Mode 0	MD0	Input	Sets SH7054F operating mode
Transmit data	TxD1	Output	Serial transmit data output
Receive data	RxD1	Input	Serial receive data input

## 21.4 Register Configuration

The registers used to control the on-chip flash memory when enabled are shown in table 21.3.

**Table 21.3 Register Configuration**

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Flash memory control register 1	FLMCR1	R/W* <sup>1</sup>	H'00* <sup>2</sup>	H'FFFFE800	8
Flash memory control register 2	FLMCR2	R/W* <sup>1</sup>	H'00	H'FFFFE801	8
Erase block register 1	EBR1	R/W* <sup>1</sup>	H'00* <sup>3</sup>	H'FFFFE802	8
Erase block register 2	EBR2	R/W* <sup>1</sup>	H'00* <sup>4</sup>	H'FFFFE803	8
RAM emulation register	RAMER	R/W	H'0000	H'FFFEC26	8, 16, 32

- Notes:
1. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit is set to 1 in FLMCR1.
  2. When a high level is input to the FWE pin, the initial value is H'80.
  3. When a low level is input to the FWE pin, or if a high level is input and the SWE1 bit in FLMCR1 is not set, these registers are initialized to H'00.
  4. Will be initialized to H'00 if a low level is input to pin FWE or if bit SWE2 of FLMCR2 is not set even though a high level is input.
  5. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers, and RAMER is a 16-bit register.
  6. Only byte accesses are valid for FLMCR1, FLMCR2, EBR1, and EBR2, the access requiring 3 cycles. Three cycles are required for a byte or word access to RAMER, and 6 cycles for a longword access.

## 21.5 Register Descriptions

### 21.5.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is an 8-bit register used for flash memory operating mode control. Program-verify mode or erase-verify mode is entered by setting SWE1 bit to 1 when FWE = 1, then setting the EV1 or PV1 bit. Program mode is entered by setting SWE1 bit to 1 when FWE = 1, then setting the PSU1 bit, and finally setting the P1 bit. Erase mode is entered by setting SWE1 bit to 1 when FWE = 1, then setting the ESU1 bit, and finally setting the E1 bit. FLMCR1 is initialized by a power-on reset, and in hardware standby mode and software standby mode. Its initial value is H'80 when a high level is input to the FWE pin, and H'00 when a low level is input. When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

Writes are enabled only in the following cases: Writes to bit SWE1 of FLMCR1 enabled when FWE = 1, to bits ESU1, PSU1, EV1, and PV1 when FWE = 1 and SWE1 = 1, to bit E1 when FWE = 1, SWE1 = 1 and ESU1 = 1, and to bit P1 when FWE = 1, SWE1 = 1, and PSU1 = 1.

Bit:	7	6	5	4	3	2	1	0
	FWE	SWE1	ESU1	PSU1	EV1	PV1	E1	P1
Initial value:	1/0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Bit 7—Flash Write Enable Bit (FWE): Sets hardware protection against flash memory programming/erasing.

#### Bit 7: FWE Description

0	When a low level is input to the FWE pin (hardware-protected state)
1	When a high level is input to the FWE pin

- Bit 6—Software Write Enable Bit 1 (SWE1): Enables or disables flash memory programming and erasing. Set this bit when setting bits 5 to 0, bits 7 to 0 of EBR1, and bits 3 to 0 of EBR2.

#### Bit 6: SWE1 Description

0	Writes disabled	(Initial value)
1	Writes enabled	
	[Setting condition]	
	When FWE = 1	

- Bit 5—Erase Setup Bit 1 (ESU1): Prepares for a transition to erase mode. Do not set the SWE1, PSU1, EV1, PV1, E1, or P1 bit at the same time.

**Bit 5: ESU1 Description**

0	Erase setup cleared	(Initial value)
1	Erase setup [Setting condition] When FWE = 1 and SWE1 = 1	

- Bit 4—Program Setup Bit 1 (PSU1): Prepares for a transition to program mode. Do not set the SWE1, ESU1, EV1, PV1, E1, or P1 bit at the same time.

**Bit 4: PSU1 Description**

0	Program setup cleared	(Initial value)
1	Program setup [Setting condition] When FWE = 1 and SWE1 = 1	

- Bit 3—Erase-Verify 1 (EV1): Selects erase-verify mode transition or clearing. Do not set the SWE1, ESU1, PSU1, PV1, E1, or P1 bit at the same time.

**Bit 3: EV1 Description**

0	Erase-verify mode cleared	(Initial value)
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE1 = 1	

- Bit 2—Program-Verify 1 (PV1): Selects program-verify mode transition or clearing. Do not set the SWE1, ESU1, PSU1, EV1, E1, or P1 bit at the same time.

**Bit 2: PV1 Description**

0	Program-verify mode cleared	(Initial value)
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE1 = 1	

- Bit 1—Erase 1 (E1): Selects erase mode transition or clearing. Do not set the SWE1, ESU1, PSU1, EV1, PV1, or P1 bit at the same time.

**Bit 1: E1 Description**

0	Erase mode cleared	(Initial value)
1	Transition to erase mode [Setting condition] When FWE = 1, SWE1 = 1, and ESU1 = 1	

- Bit 0—Program 1 (P1): Selects program mode transition or clearing. Do not set the SWE1, PSU1, ESU1, EV1, PV1, or E1 bit at the same time.

**Bit 0: P1 Description**

0	Program mode cleared	(Initial value)
1	Transition to program mode [Setting condition] When FWE = 1, SWE1 = 1, and PSU1 = 1	

**21.5.2 Flash Memory Control Register 2 (FLMCR2)**

FLMCR2 is a status register that indicates the occurrence of an error during flash memory programming or erasing. FLMCR2 is initialized to H'00 by a power-on reset and in hardware standby mode. When on-chip flash memory is disabled, a read will return H'00 and writes are invalid.

Bit:	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

- Bit 7—Flash Memory Error (FLER): Indicates that an error has occurred during an operation on flash memory (programming or erasing). When FLER is set to 1, flash memory goes to the error-protection state.

Bit 7: FLER	Description
0	Flash memory is operating normally (Initial value) Flash memory program/erase protection (error protection) is disabled [Clearing condition] Power-on reset or hardware standby mode
1	An error has occurred during flash memory programming/erasing Flash memory program/erase protection (error protection) is enabled [Setting condition] See 201.8.3 Error Protection

- Bits 6 to 0—Reserved: These bits always read 0. The write value should always be 0.

### 21.5.3 Erase Block Register 1 (EBR1)

EBR1 is an 8-bit register that specifies the flash memory erase area block by block. EBR1 is initialized to H'00 by a power-on reset, in hardware standby mode and software standby mode, when a low level is input to the FWE pin, and when a high level is input to the FWE pin and the SWE1 bit in FLMCR1 is not set. When a bit in EBR1 is set to 1, the corresponding block can be erased. Other blocks are erase-protected. Only one of the bits of EBR1 and EBR2 combined can be set. Do not set more than one bit. (Do not set more than one bit, as this will automatically clear both EBR1 and EBR2 to 0.) When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 21.4.

Bit:	7	6	5	4	3	2	1	0
	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### 21.5.4 Erase Block Register 2 (EBR2)

EBR2 is an 8-bit register that specifies the flash memory erase area block by block. EBR2 is initialized to H'00 by a power-on reset, in hardware standby mode and software standby mode, when a low level is input to the FWE pin. Bits 3 to 0 will be initialized even though a high level is input to pin FWE. When a bit in EBR2 is set to 1, the corresponding block can be erased. Other

blocks are erase-protected. Only one of the bits of EBR1 and EBR2 combined can be set. Do not set more than one bit. (Do not set more than one bit, as this will automatically clear both EBR1 and EBR2 to 0.) When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

The flash memory block configuration is shown in table 21.5.

Bit:	7	6	5	4	3	2	1	0
	—	—	EB13	EB12	EB11	EB10	EB9	EB8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

**Table 21.4 Flash Memory Erase Blocks**

<b>Block (Size)</b>	<b>Addresses</b>
EB0 (4 kB)	H'000000 to H'000FFF
EB1 (4 kB)	H'001000 to H'001FFF
EB2 (4 kB)	H'002000 to H'002FFF
EB3 (4 kB)	H'003000 to H'003FFF
EB4 (4 kB)	H'004000 to H'004FFF
EB5 (4 kB)	H'005000 to H'005FFF
EB6 (4 kB)	H'006000 to H'006FFF
EB7 (4 kB)	H'007000 to H'007FFF
EB8 (32 kB)	H'008000 to H'00FFFF
EB9 (64 kB)	H'010000 to H'01FFFF
EB10 (64 kB)	H'020000 to H'02FFFF
EB11 (64 kB)	H'030000 to H'03FFFF
EB12 (64 kB)	H'040000 to H'04FFFF
EB13 (64 kB)	H'050000 to H'05FFFF



## 21.5.5 RAM Emulation Register (RAMER)

RAMER specifies the area of flash memory to be overlapped with part of RAM when emulating real-time flash memory programming. RAMER is initialized to H'0000 by a power-on reset and in hardware standby mode. It is not initialized in software standby mode. RAMER settings should be made in user mode or user program mode.

Flash memory area divisions are shown in table 21.5. To ensure correct operation of the emulation function, the ROM for which RAM emulation is performed should not be accessed immediately after this register has been modified. Normal execution of an access immediately after register modification is not guaranteed.

Bit:	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W

- Bits 15 to 4—Reserved: These bits always read 0.
- Bit 3—RAM Select (RAMS): Specifies selection or non-selection of flash memory emulation in RAM. When RAMS = 1, all flash memory block are program/erase-protected.

### Bit 3: RAMS Description

0	Emulation not selected Program/erase-protection of all flash memory blocks is disabled	(Initial value)
1	Emulation selected Program/erase-protection of all flash memory blocks is enabled	

- Bits 2, 1 and 0—Flash Memory Area Selection (RAM2, RAM1, RAM0): These bits are used together with bit 3 to select the flash memory area to be overlapped with RAM. (See table 21.5.)

**Table 21.5 Flash Memory Area Divisions**

<b>Addresses</b>	<b>Block Name</b>	<b>RAMS</b>	<b>RAM1</b>	<b>RAM1</b>	<b>RAM0</b>
H'FFFF8000 to H'FFFF8FFF	RAM area 4 kB	0	*	*	*
H'00000000 to H'00000FFF	EB0 (4 kB)	1	0	0	0
H'00001000 to H'00001FFF	EB1 (4 kB)	1	0	0	1
H'00002000 to H'00002FFF	EB2 (4 kB)	1	0	1	0
H'00003000 to H'00003FFF	EB3 (4 kB)	1	0	1	1
H'00004000 to H'00004FFF	EB4 (4 kB)	1	1	0	0
H'00005000 to H'00005FFF	EB5 (4 kB)	1	1	0	1
H'00006000 to H'00006FFF	EB6 (4 kB)	1	1	1	0
H'00007000 to H'00007FFF	EB7 (4 kB)	1	1	1	1

\*: Don't care

## 21.6 On-Board Programming Modes

When pins are set to on-board programming mode and a reset-start is executed, a transition is made to the on-board programming state in which program/erase/verify operations can be performed on the on-chip flash memory. There are two on-board programming modes: boot mode and user program mode. The pin settings for transition to each of these modes are shown in table 21.6. For a diagram of the transitions to the various flash memory modes, see figure 21.2.

**Table 21.6 Setting On-Board Programming Modes**

Mode		PLL Multiple	FWE	MD2	MD1	MD0
Boot mode	Expanded mode	× 4	1	1	0	0
	Single-chip mode			1	0	1
User program mode	Expanded mode		1	1	1	0
	Single-chip mode			1	1	1

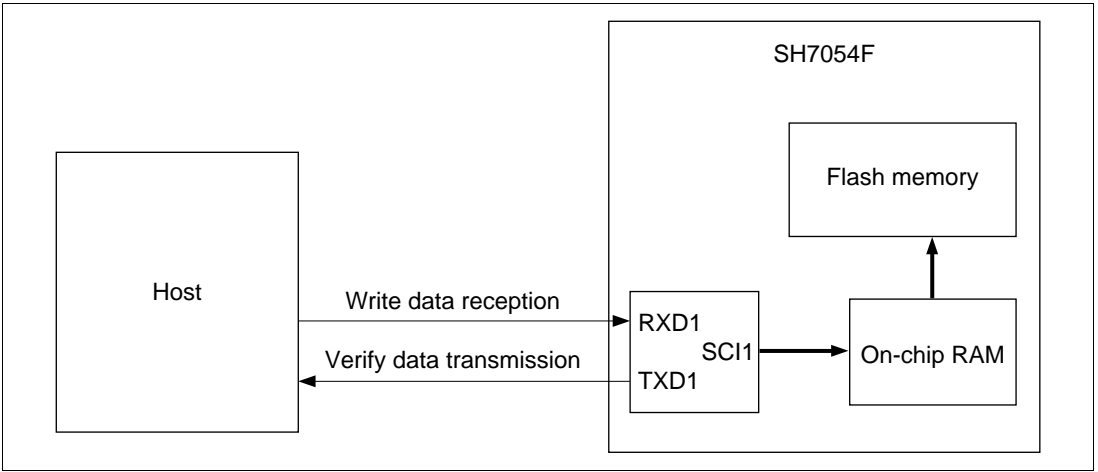
### 21.6.1 Boot Mode

When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. The SCI channel to be used is set to asynchronous mode.

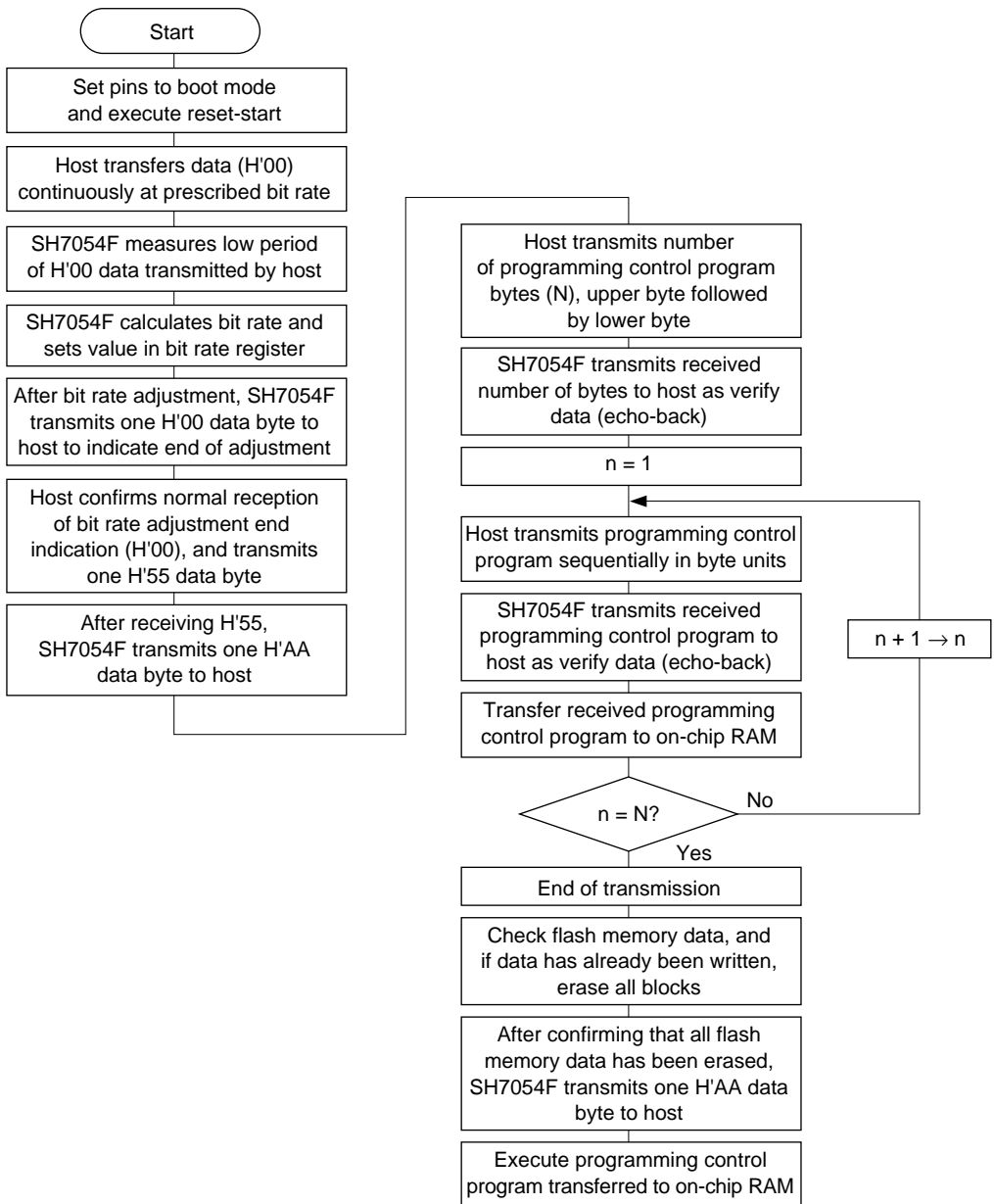
When a reset-start is executed after the SH7054F's pins have been set to boot mode, the boot program built into the SH7054F is started and the programming control program prepared in the host is serially transmitted to the SH7054F via the SCI. In the SH7054F, the programming control program received via the SCI is written into the programming control program area in on-chip RAM. After the transfer is completed, control branches to the start address of the programming control program area and the programming control program execution state is entered (flash memory programming is performed).

The transferred programming control program must therefore include coding that follows the programming algorithm given later.

The system configuration in boot mode is shown in figure 21.8, and the boot mode execution procedure in figure 21.9.

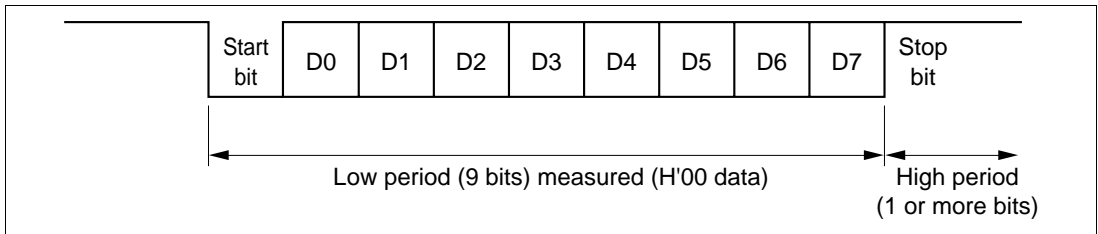


**Figure 21.8 System Configuration in Boot Mode**



Note: If a memory cell does not operate normally and cannot be erased, one H'FF byte is transmitted as an erase error, and the erase operation and subsequent operations are halted.

**Figure 21.9 Boot Mode Execution Procedure**



**Figure 21.10 Automatic SCI Bit Rate Adjustment**

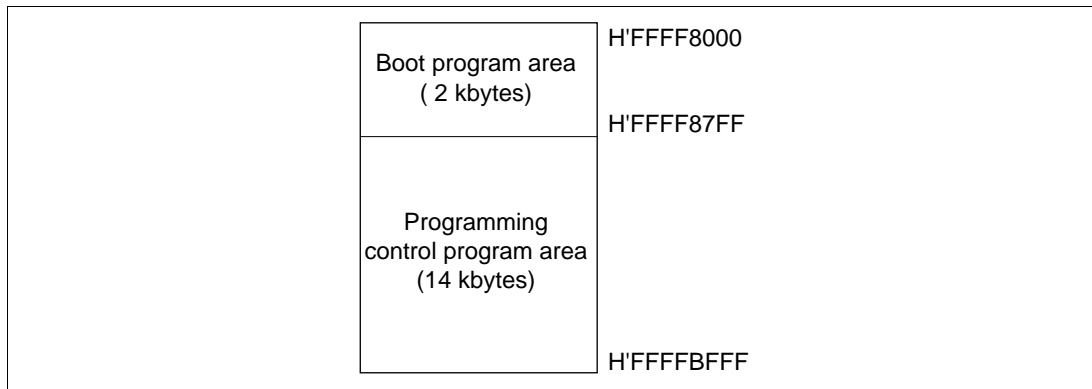
When boot mode is initiated, the SH7054F measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The SH7054F calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the SH7054F. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the SH7054F's system clock frequency, there will be a discrepancy between the bit rates of the host and the SH7054F. Set the host transfer bit rate at 9,600 or 19,200 bps to operate the SCI properly.

Table 21.7 shows host transfer bit rates and system clock frequencies for which automatic adjustment of the SH7054F bit rate is possible. The boot program should be executed within this system clock range.

**Table 21.7 System Clock Frequencies for which Automatic Adjustment of SH7054F Bit Rate is Possible**

Host Bit Rate	System Clock Frequency for Which Automatic Adjustment of SH7054F Bit Rate is Possible
9,600 bps	20 to 40 MHz (input frequency: 5 to 10 MHz)
19,200 bps	20 to 40 MHz (input frequency: 5 to 10 MHz)

**On-Chip RAM Area Divisions in Boot Mode:** In boot mode, the RAM area is divided into an area used by the boot program and an area to which the programming control program is transferred via the SCI, as shown in figure 21.11. The boot program area cannot be used until the execution state in boot mode switches to the programming control program transferred from the host.



**Figure 21.11 RAM Areas in Boot Mode**

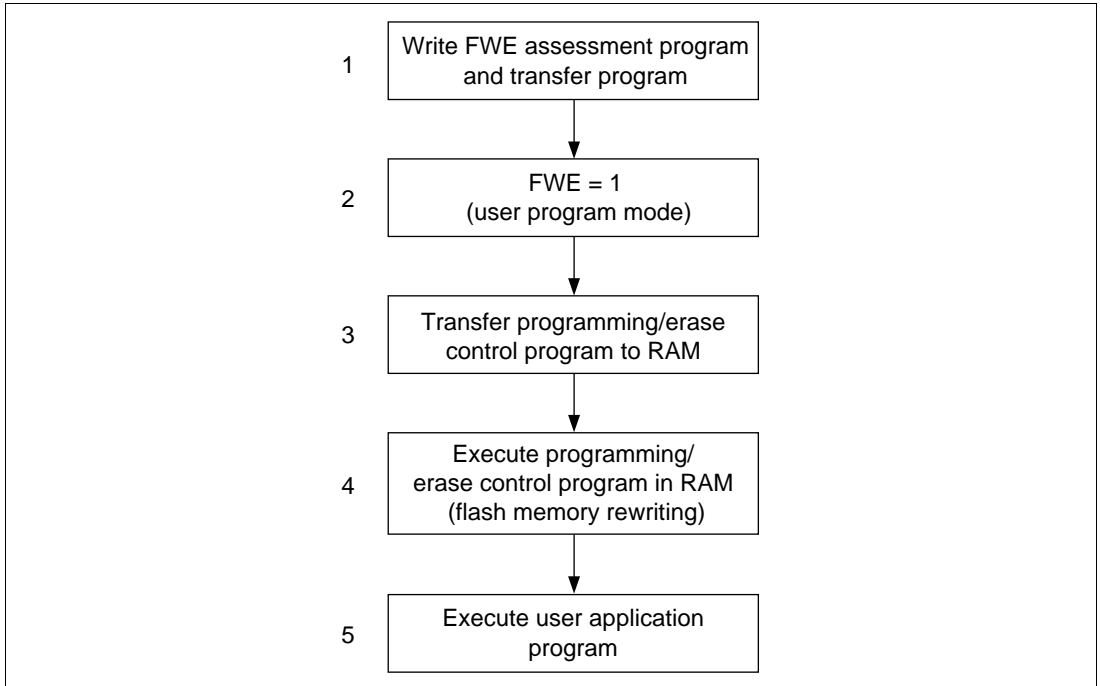
Note: The boot program area cannot be used until a transition is made to the execution state for the programming control program transferred to RAM. Note also that the boot program remains in this area of the on-chip RAM even after control branches to the programming control program.

## 21.6.2 User Program Mode

After setting FWE, the user should branch to, and execute, the previously prepared programming/erase control program.

The Flash memory cannot be read while the flash memory is being written/erased. Execute the control program for programming or erasing using the on-chip RAM, external memory, or flash memory outside the address areas.

Use the following procedure (figure 21.12) to execute the programming control program that writes to flash memory (when transferred to RAM).



**Figure 21.12 User Program Mode Execution Procedure**

Note: When programming and erasing, start the watchdog timer so that measures can be taken to prevent program runaway, etc. Memory cells may not operate normally if overprogrammed or overerased due to program runaway.



## 21.7 Programming/Erasing Flash Memory

A software method, using the CPU, is employed to program and erase flash memory in the on-board programming modes. There are four flash memory operating modes: program mode, erase mode, program-verify mode, and erase-verify mode. Transitions to these modes are made by setting the PSU1, ESU1, P1, E1, PV1, and EV1 bits in FLMCR1.

The flash memory cannot be read while it is being written or erased. Install the program to control flash memory programming and erasing (programming control program) in the on-chip RAM, in external memory, or in flash memory outside the address area, and execute the program from there.

- Notes:
1. Operation is not guaranteed if bits SWE1, ESU1, PSU1, EV1, PV1, E1, and P1 of FLMCR1 are set/reset by a program in flash memory in the corresponding address areas.
  2. When programming or erasing, set FWE to 1 (programming/erasing will not be executed if FWE = 0).
  3. Programming should be performed in the erased state. Do not perform additional programming on previously programmed addresses.

### 21.7.1 Program Mode

When writing data or programs to flash memory, the program/program-verify flowchart shown in figures 21.13 and 21.14 should be followed. Performing program operations according to this flowchart will enable data or programs to be written to flash memory without subjecting the device to voltage stress or sacrificing program data reliability. Programming should be carried out 128 bytes at a time.

Following the elapse of 10  $\mu$ s or more after the SWE1 bit is set to 1 in flash memory control register 1 (FLMCR1), 128-byte program data is stored in the program data area and reprogram data area, and the 128-byte data in the program data area in RAM is written consecutively to the program address (the lower 8 bits of the first address written to must be H'00 or H'80). 128 consecutive byte data transfers are performed. The program address and program data are latched in the flash memory. A 128-byte data transfer must be performed even if writing fewer than 128 bytes; in this case, H'FF data must be written to the extra addresses.

Next, the watchdog timer is set to prevent overprogramming in the event of program runaway, etc. Set 6.6 ms as the WDT overflow period. After this, preparation for program mode (program setup) is carried out by setting the PSU1 bit in FLMCR1, and after the elapse of  $t_{SPSU}$ , the operating mode is switched to program mode by setting the P1 bit in FLMCR1. The time during which the P1 bit is set is the flash memory programming time. Follow the table in the programming flowchart for the write time.

After the elapse of a given programming time, programming mode is exited. In exiting programming mode, the P1 bit in FLMCR1 is cleared, then after an interval of  $t_{CP}$  or longer the PSU1 bit is cleared, and after an interval of  $t_{CPSU}$  or longer the watchdog timer is halted.

### 21.7.2 Program-Verify Mode

In program-verify mode, the data written in program mode is read to check whether it has been correctly written in the flash memory.

A transition to program-verify mode is made by setting the PV1 bit in FLMCR1 and waiting for an interval of  $t_{SPV}$ . Before reading in program-verify mode, perform a dummy write of H'FF data to the read addresses, and then wait for an interval of  $t_{SPVR}$  or longer. When the flash memory is read in this state (verify data is read in longword units), the data at the latched address is read. Next, the written data is compared with the verify data, and reprogram data is computed (see figures 21.13 and 21.14) and transferred to the reprogram data area. After 128 bytes of data have been verified, exit program-verify mode. Program-verify mode is exited by clearing the PV1 bit in FLMCR1, then clearing the SWE1 bit after an interval of  $t_{CPV}$  or longer, and waiting for an interval of  $t_{CSWE}$  or longer. If reprogramming is necessary, set program mode again, and repeat the program/program-verify sequence as before. However, ensure that the program/program-verify sequence is not repeated more than 1,000 times on the same bits.

Data writes must be performed in the memory-erased state. Do not write additional data to an address to which data is already written.

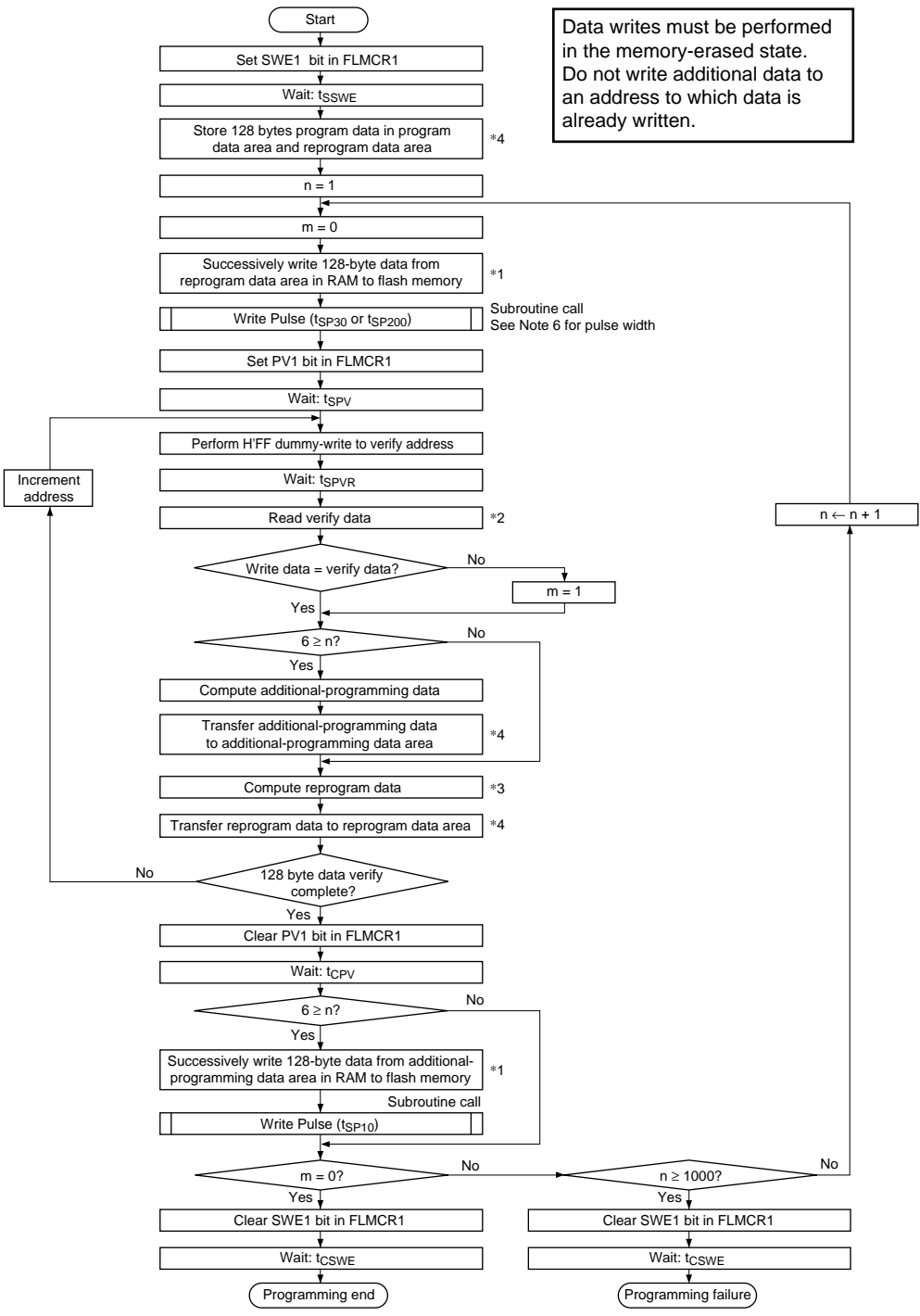
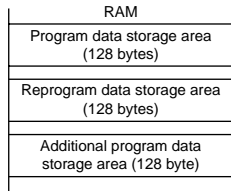
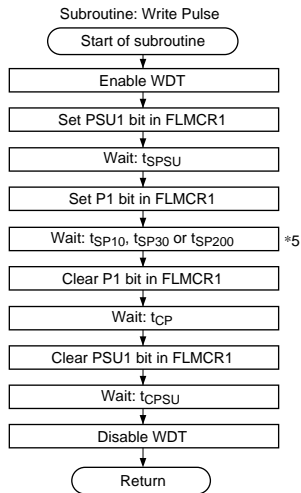


Figure 21.13 Program/Program-Verify Flowchart (1)



- Notes:
1. Transfer data in byte units. The lower eight bits of the start address to which data is written must be H'00 or H'80. Transfer 128-byte data even when writing fewer than 128 bytes. In this case, Set H'FF in unused addresses.
  2. Read verify data in longword form (32 bits).
  3. Even for bits to which data has already been written in the 128-byte programming loop, an additional write should be performed if the next verify write data is not the same as the verify data.
  4. A 128-byte area for storing program data, a 128-byte area for storing reprogram data, and a 128-byte area for storing additional program data must be provided in RAM. The reprogram and additional program data contents are modified as programming proceeds.
  5. A write pulse of  $t_{SP30}$  or  $t_{SP200}$  is applied according to the progress of the programming operation. See Note 6 for the pulse widths. When writing of the additional program data is executed, a  $t_{SP10}$  write pulse should be applied. Reprogram data 'X' means reprogram data when the pulse is applied.
  6. Write Pulse Width

Number of Writes n	Write Time (z) $\mu$ sec
1	$t_{SP30}$
2	$t_{SP30}$
3	$t_{SP30}$
4	$t_{SP30}$
5	$t_{SP30}$
6	$t_{SP30}$
7	$t_{SP200}$
8	$t_{SP200}$
9	$t_{SP200}$
10	$t_{SP200}$
11	$t_{SP200}$
12	$t_{SP200}$
13	$t_{SP200}$
.	.
.	.
998	$t_{SP200}$
999	$t_{SP200}$
1000	$t_{SP200}$

Note: Use a  $t_{SP10}$  write pulse for additional programming.

Reprogram Data Computation Table

Original Data (D)	Verify Data (V)	Reprogram Data (X)	Comments
0	0	1	Programming complete.
0	1	0	Programming is incomplete; reprogramming should be performed.
1	0	1	—
1	1	1	Left in the erased state.

Additional-Programming Data Computation Table

Reprogram Data (X')	Verify Data (V)	Additional-Programming Data (Y)	Comments
0	0	0	Additional programming executed
0	1	1	Additional programming not executed
1	0	1	Additional programming not executed
1	1	1	Additional programming not executed

Figure 21.14 Program/Program-Verify Flowchart (2)

**Table 21.8 Program/Program-Verify Parameter**

Flow Section	Item	Symbol	Min	Typ	Max	Unit	Notes
Program/ program-verify	Wait time after PSU1 bit setting	$t_{SPSU}$	50	50	—	$\mu\text{s}$	
	Wait time after P1 bit setting (10 $\mu\text{s}$ )	$t_{SP10}$	8	10	12	$\mu\text{s}$	Additional-programming time wait
	Wait time after P1 bit setting (30 $\mu\text{s}$ )	$t_{SP30}$	28	30	32	$\mu\text{s}$	Programming time wait
	Wait time after P1 bit setting (200 $\mu\text{s}$ )	$t_{SP200}$	198	200	202	$\mu\text{s}$	Programming time wait
	Wait time after P1 bit clearing	$t_{CP}$	5	5	—	$\mu\text{s}$	
	Wait time after PSU1 bit clearing	$t_{CPSU}$	5	5	—	$\mu\text{s}$	
	Wait time after PV1 bit setting	$t_{SPV}$	4	4	—	$\mu\text{s}$	
	Wait time after dummy write	$t_{SPVR}$	2	2	—	$\mu\text{s}$	
	Wait time after PV1 bit clearing	$t_{CPV}$	2	2	—	$\mu\text{s}$	
All	Wait time after SWE1 bit setting	$t_{SSWE}$	1	1	—	$\mu\text{s}$	
	Wait time after SWE1 bit clearing	$t_{CSWE}$	100	100	—	$\mu\text{s}$	

### 21.7.3 Erase Mode

When erasing flash memory, the erase/erase-verify flowchart (single-block erase) shown in figure 21.15 should be followed for each block.

To perform data or program erasure, set the SWE1 bit to 1 in flash memory control register n (FLMCR1), then, after an interval of  $t_{SSWE}$  or longer, make a 1-bit setting for the flash memory area to be erased in erase block register 1 or 2 (EBR1, EBR2). Next, the watchdog timer is set to prevent overerasing in the event of program runaway, etc. Set 19.8 ms as the WDT overflow period. After this, preparation for erase mode (erase setup) is carried out by setting the ESU1 bit in FLMCR1, and after an interval of  $t_{SESU}$  or longer, the operating mode is switched to erase mode by setting the E1 bit in FLMCR1. The time during which the E1 bit is set is the flash memory erase time. Ensure that the erase time does not exceed  $t_{SE}$ .

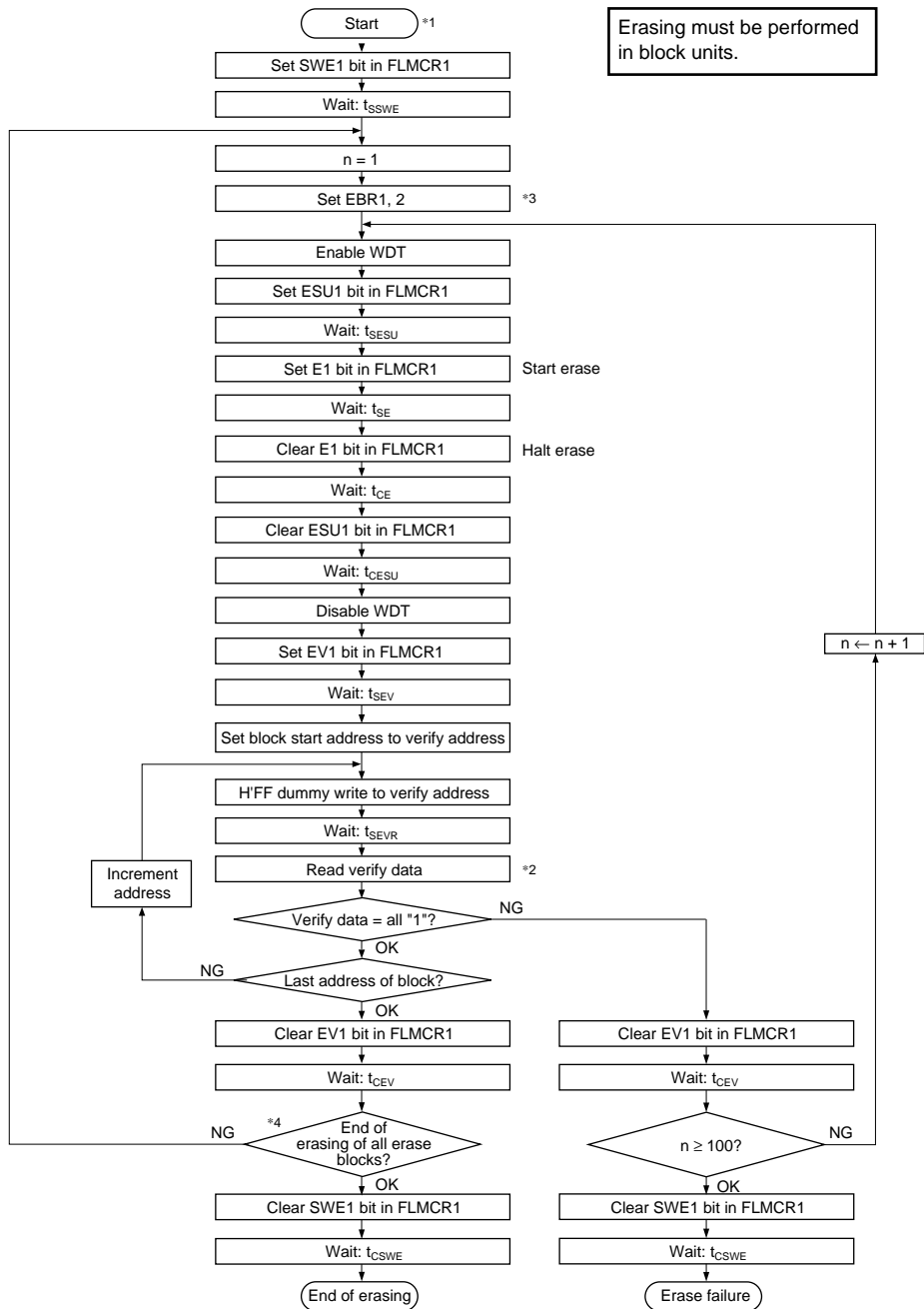
After the elapse of the erase time, erase mode is exited. In exiting erase mode, the E1 bit in FLMCR1 is cleared, then after an interval of  $t_{CE}$  or longer the ESU1 bit is cleared, and after a further interval of  $t_{CESU}$  or longer the watchdog timer is halted.

Note: With flash memory erasing, preprogramming (setting all memory data in the memory to be erased to all “0”) is not necessary before starting the erase procedure.

#### 21.7.4 Erase-Verify Mode

In erase-verify mode, data is read after memory has been erased to check whether it has been correctly erased.

A transition to erase-verify mode is made by setting the E1 bit in FLMCR1 and waiting for an interval of  $t_{SEV}$ . Before reading in erase-verify mode, perform a dummy write of H'FF data to the read addresses, and then wait for an interval of  $t_{SEVR}$  or longer. When the flash memory is read in this state (verify data is read in longword units), the data at the latched address is read. If the read data has been erased (all “1”), a dummy write is performed to the next address, and erase-verify is performed. The erase-verify operation is carried out on all the erase blocks; the erase block register bit for an erased block should be cleared to prevent excessive application of the erase voltage. Ensure that the operation is not repeated more than 100 times. When verification is completed, exit erase-verify mode. Erase-verify mode is exited by clearing the EV1 bit in FLMCR1, then waiting for an interval of  $t_{CEV}$  or longer. If erasure has been completed on all the erase blocks, clear the SWE1 bit in FLMCR1. If there are any unerased blocks, make a 1-bit setting for the flash memory area to be erased, and repeat the erase/erase-verify sequence as before.



- Notes:
1. Preprogramming (setting erase block data to all "0") is not necessary.
  2. Verify data is read in 32-bit (longword) units.
  3. Set only one bit in EBR1. More than one bit cannot be set.
  4. Erasing is performed in block units. To erase a number of blocks, each block must be erased in turn.

**Figure 21.15 Erase/Erase-Verify Flowchart**

**Table 21.9 Erase/Erase-Verify Parameter**

Flow Section	Item	Symbol	Min	Typ	Max	Unit	Notes
Erase/ erase-verify	Wait time after ESU1 bit setting	$t_{\text{SESU}}$	100	100	—	$\mu\text{s}$	
	Wait time after E1 bit setting	$t_{\text{SE}}$	10	10	100	ms	Erase time wait
	Wait time after E1 bit clearing	$t_{\text{CE}}$	10	10	—	$\mu\text{s}$	
	Wait time after ESU1 bit clearing	$t_{\text{CESU}}$	10	10	—	$\mu\text{s}$	
	Wait time after EV1 bit setting	$t_{\text{SEV}}$	20	20	—	$\mu\text{s}$	
	Wait time after dummy write	$t_{\text{SEVR}}$	2	2	—	$\mu\text{s}$	
	Wait time after EV1 bit clearing	$t_{\text{CEV}}$	4	4	—	$\mu\text{s}$	
All	Wait time after SWE1 bit setting	$t_{\text{SSWE}}$	1	1	—	$\mu\text{s}$	
	Wait time after SWE1 bit clearing	$t_{\text{CSWE}}$	100	100	—	$\mu\text{s}$	



## 21.8 Protection

There are two kinds of flash memory program/erase protection, hardware protection and software protection.

### 21.8.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted. Hardware protection is reset by settings in flash memory control register 1 (FLMCR1), erase block register 1 (EBR1) and erase block register 2 (EBR2). The FLMCR1, and EBR1 settings are retained in the error-protected state. (See table 21.10.)

**Table 21.10 Hardware Protection**

Item	Description	Functions	
		Program	Erase
FWE pin protection	<ul style="list-style-type: none"><li>When a low level is input to the FWE pin, FLMCR1, FLMCR2, EBR1, and EBR2 are initialized, and the program/erase-protected state is entered.</li></ul>	Yes	Yes
Reset/standby protection	<ul style="list-style-type: none"><li>In a power-on reset (including a WDT power-on reset) and in standby mode, FLMCR1, FLMCR2, EBR1, and EBR2 are initialized, and the program/erase-protected state is entered.</li><li>In a reset via the <math>\overline{\text{RES}}</math> pin, the reset state is not entered unless the <math>\overline{\text{RES}}</math> pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the <math>\overline{\text{RES}}</math> pin low for the <math>\overline{\text{RES}}</math> pulse width specified in the AC Characteristics section. Do not execute a reset during programming or erasing, as the values in the flash memory are not guaranteed if this is done. In this case, execute an erase, then execute programming once again.</li></ul>	Yes	Yes

## 21.8.2 Software Protection

Software protection can be implemented by setting the SWE1 bit in FLMCR1, erase block register 1 (EBR1), erase block register 2 (EBR2), and the RAMS bit in the RAM emulation register (RAMER). When software protection is in effect, setting the P1 or E1 bit in flash memory control register 1 (FLMCR1), does not cause a transition to program mode or erase mode. (See table 21.11.)

**Table 21.11 Software Protection**

Item	Description	Functions	
		Program	Erase
SWE bit protection	<ul style="list-style-type: none"><li>Setting bit SWE1 in FLMCR1 to 0 will place in the program/erase-protected state.</li></ul>	Yes	Yes
Block specification protection	<ul style="list-style-type: none"><li>Erase protection can be set for individual blocks by settings in erase block register 1 (EBR1) and erase block register 2 (EBR2).</li><li>Setting EBR1 and EBR2 to H'00 places all blocks in the erase-protected state.</li></ul>	—	Yes
Emulation protection	<ul style="list-style-type: none"><li>Setting the RAMS bit to 1 in the RAM emulation register (RAMER) places all blocks in the program/erase-protected state.</li></ul>	Yes	Yes

## 21.8.3 Error Protection

In error protection, an error is detected when SH7054F runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

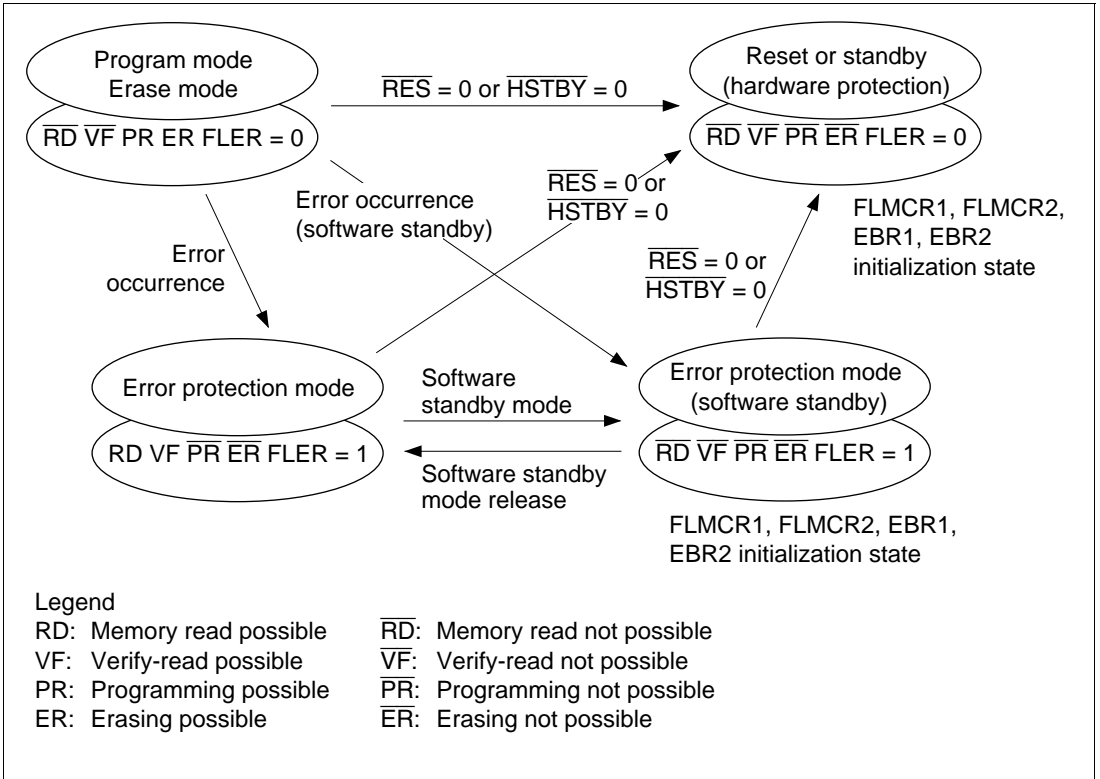
If the SH7054F malfunctions during flash memory programming/erasing, the FLER bit is set to 1 in FLMCR2 and the error protection state is entered. The FLMCR1, EBR1, and EBR2 settings are retained, but program mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be re-entered by re-setting the P1 or E1 bit. However, PV1 and EV1 bit setting is enabled, and a transition can be made to verify mode.

FLER bit setting conditions are as follows:

1. When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
2. When a SLEEP instruction (including software standby) is executed during programming/erasing

Error protection is released only by a power-on reset and in hardware standby mode.

Figure 21.16 shows the flash memory state transition diagram.



**Figure 21.16 Flash Memory State Transitions**

## 21.9 Flash Memory Emulation in RAM

Making a setting in the RAM emulation register (RAMER) enables part of RAM to be overlapped onto the flash memory area so that data to be written to flash memory can be emulated in RAM in real time. After the RAMER setting has been made, accesses cannot be made from the flash memory area or the RAM area overlapping flash memory. Emulation can be performed in user mode and user program mode. Figure 21.17 shows an example of emulation of real-time flash memory programming.

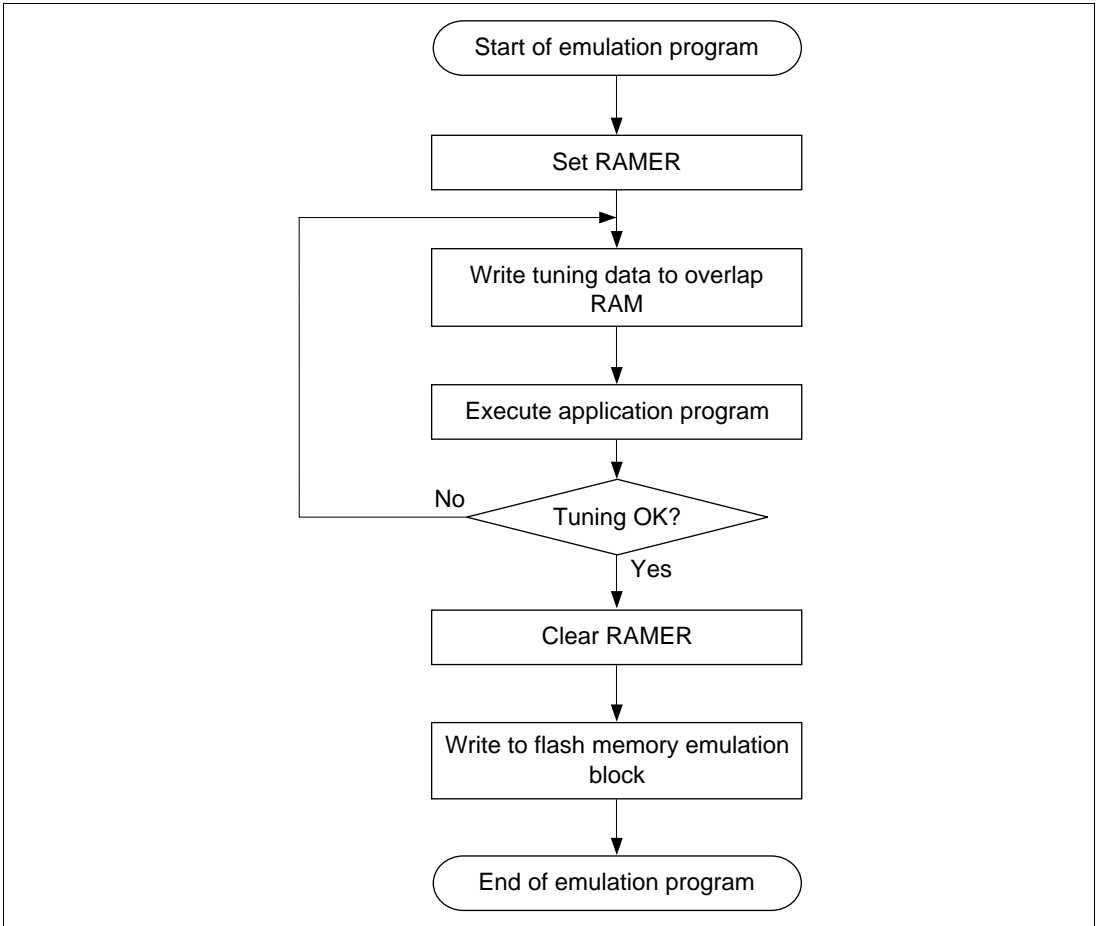
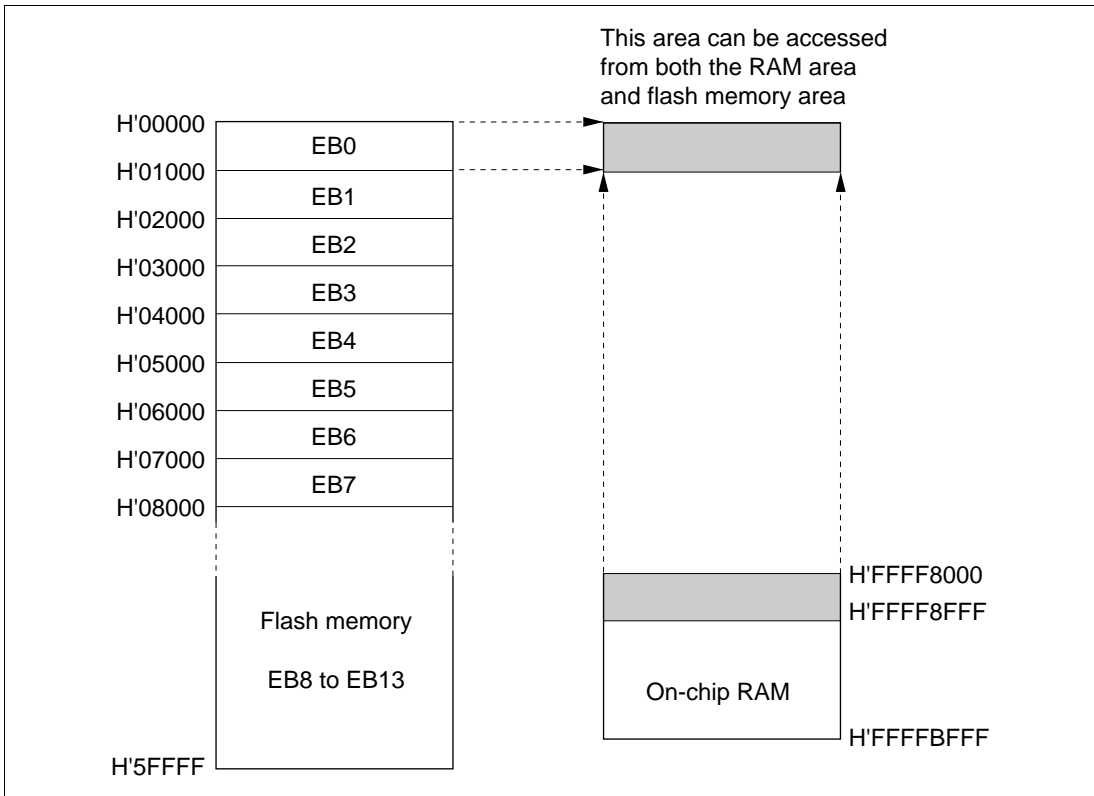


Figure 21.17 Flowchart for Flash Memory Emulation in RAM



**Figure 21.18 Example of RAM Overlap Operation**

### Example in which Flash Memory Block Area EB0 is Overlapped

1. Set bits RAMS and RAM2 to RAM0 in RAMER to 1, 0, 0, 0, to overlap part of RAM onto the area (EB0) for which real-time programming is required.
2. Real-time programming is performed using the overlapping RAM.
3. After the program data has been confirmed, the RAMS bit is cleared, releasing RAM overlap.
4. The data written in the overlapping RAM is written into the flash memory space (EB0).

- Notes:
1. When the RAMS bit is set to 1, program/erase protection is enabled for all blocks regardless of the value of RAM2 to RAM0 (emulation protection). In this state, setting the P1 or E1 bit in flash memory control register 1 (FLMCR1) will not cause a transition to program mode or erase mode. When actually programming or erasing a flash memory area, the RAMS bit should be cleared to 0.
  2. A RAM area cannot be erased by execution of software in accordance with the erase algorithm while flash memory emulation in RAM is being used.

## 21.10 Note on Flash Memory Programming/Erasing

In the on-board programming modes (user mode and user program mode), NMI input should be disabled to give top priority to the program/erase operations (including RAM emulation).

When reading flash memory after changing the SWE1 bit from 1 to 0 on completion of a program/erase operation, wait for at least  $t_{CSWE}$  after clearing SWE1 to 0 before executing the flash memory read. Regarding the timing of  $\overline{RES}$  input after changing the SWE1 bit from 1 to 0 on completion of a program/erase operation, wait for at least  $t_{CSWE}$  after clearing SWE1 to 0 before executing the reset operation.

## 21.11 Flash Memory Programmer Mode

Programs and data can be written and erased in programmer mode as well as in the on-board programming modes. In programmer mode, flash memory read mode, auto-program mode, auto-erase mode, and status read mode are supported. In auto-program mode, auto-erase mode, and status read mode, a status polling procedure is used, and in status read mode, detailed internal signals are output after execution of an auto-program or auto-erase operation.

In programmer mode, set the mode pins to programmer mode (see table 21.12) and input a 6 MHz input clock, so that the SH7054F runs at 24 MHz.

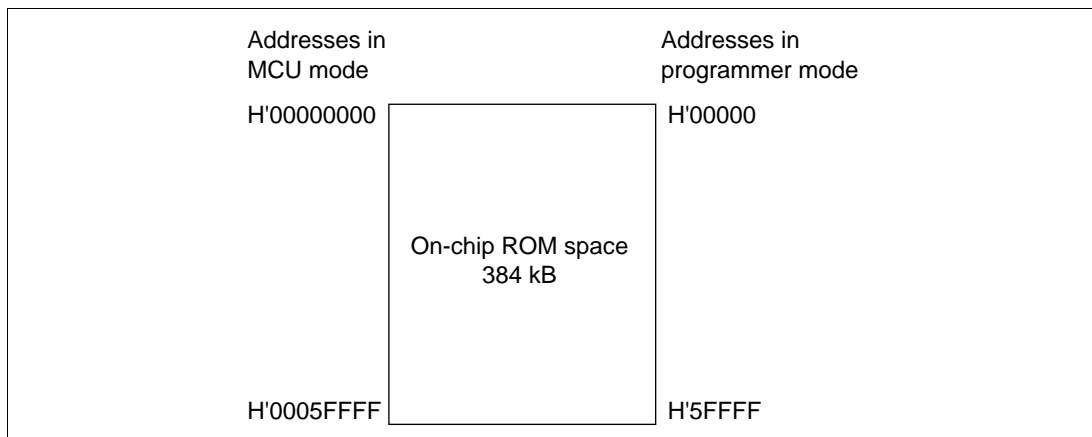
Table 21.12 shows the pin settings for programmer mode. For the pin names in programmer mode, see section 1.3.2, Pin Functions.

**Table 21.12 PROM Mode Pin Settings**

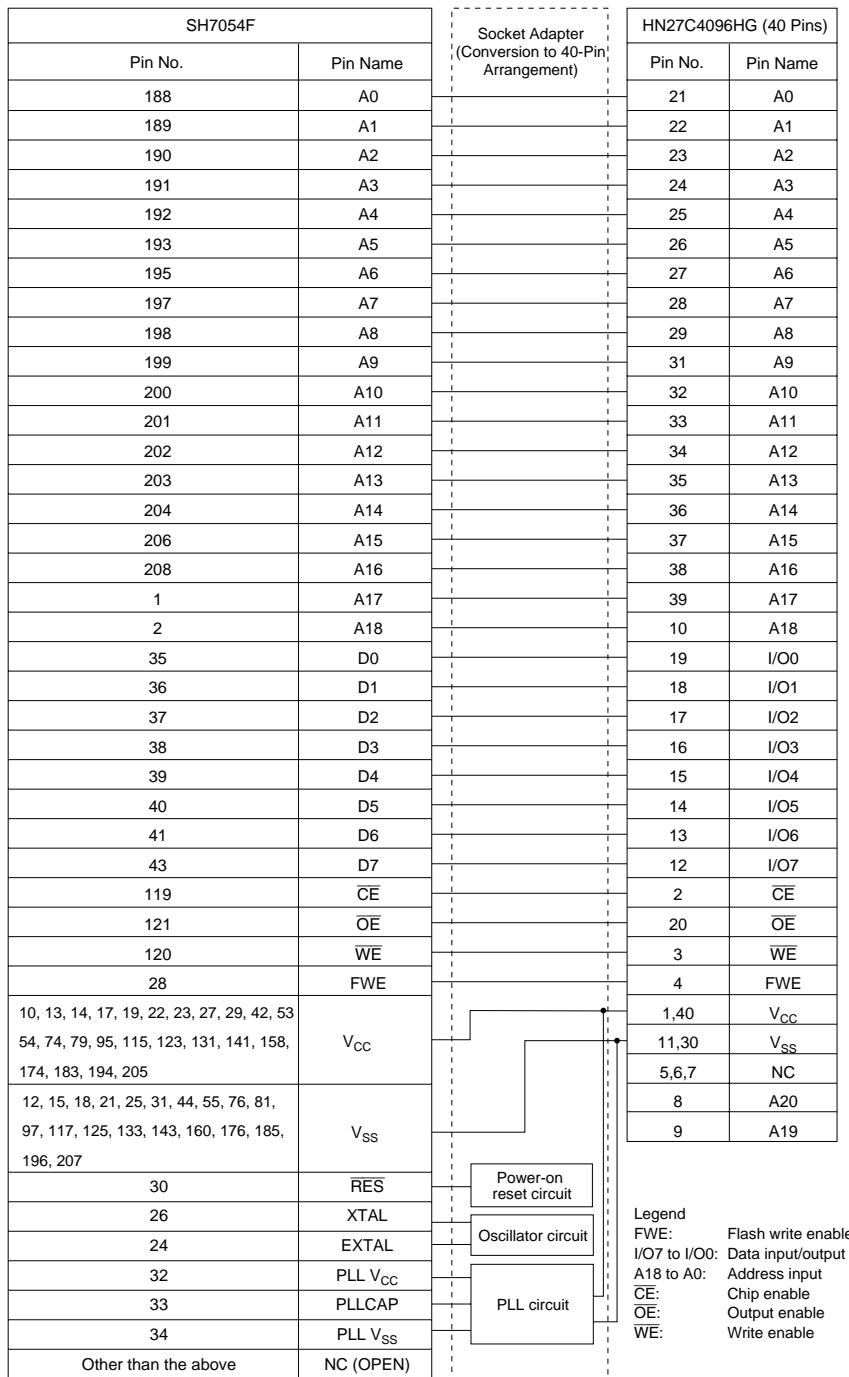
Pin Names	Settings
Mode pins: MD2, MD1, MD0	0, 1, 1
FWE pin	High level input (in auto-program and auto-erase modes)
$\overline{RES}$ pin	Power-on reset circuit
XTAL, EXTAL, PLLV <sub>CC</sub> , PLLCAP, PLLV <sub>SS</sub> pins	Oscillator circuit

### 21.11.1 Socket Adapter Pin Correspondence Diagram

Connect the socket adapter to the chip as shown in figure 21.20. This will enable conversion to a 40-pin arrangement. The on-chip ROM memory map is shown in figure 21.19, and the socket adapter pin correspondence diagram in figure 21.20.



**Figure 21.19 On-Chip ROM Memory Map**



Legend  
 FWE: Flash write enable  
 I/O7 to I/O0: Data input/output  
 A18 to A0: Address input  
 $\overline{CE}$ : Chip enable  
 $\overline{OE}$ : Output enable  
 $\overline{WE}$ : Write enable

Figure 21.20 Socket Adapter Pin Correspondence Diagram



## 21.11.2 Programmer Mode Operation

Table 21.13 shows how the different operating modes are set when using programmer mode, and table 21.14 lists the commands used in programmer mode. Details of each mode are given below.

- **Memory Read Mode**  
Memory read mode supports byte reads.
- **Auto-Program Mode**  
Auto-program mode supports programming of 128 bytes at a time. Status polling is used to confirm the end of auto-programming.
- **Auto-Erase Mode**  
Auto-erase mode supports automatic erasing of the entire flash memory. Status polling is used to confirm the end of auto-programming.
- **Status Read Mode**  
Status polling is used for auto-programming and auto-erasing, and normal termination can be confirmed by reading the I/O6 signal. In status read mode, error information is output if an error occurs.

**Table 21.13 Settings for Various Operating Modes In Programmer Mode**

Mode	Pin Names					
	FWE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O7 to I/O0	A18 to A0
Read	H or L	L	L	H	Data output	Ain
Output disable	H or L	L	H	H	Hi-z	X
Command write	H or L	L	H	L	Data input	*Ain
Chip disable	H or L	H	X	X	Hi-z	X

- Notes:
1. Chip disable is not a standby state; internally, it is an operation state.
  2. \*Ain indicates that there is also address input in auto-program mode.
  3. For command writes in auto-program and auto-erase modes, input a high level to the FWE pin.

**Table 21.14 Programmer Mode Commands**

Command Name	Number of Cycles	1st Cycle			2nd Cycle		
		Mode	Address	Data	Mode	Address	Data
Memory read mode	1 + n	Write	X	H'00	Read	RA	Dout
Auto-program mode	129	Write	X	H'40	Write	WA	Din
Auto-erase mode	2	Write	X	H'20	Write	X	H'20
Status read mode	2	Write	X	H'71	Write	X	H'71

Notes: 1. In auto-program mode, 129 cycles are required for command writing by a simultaneous 128-byte write.

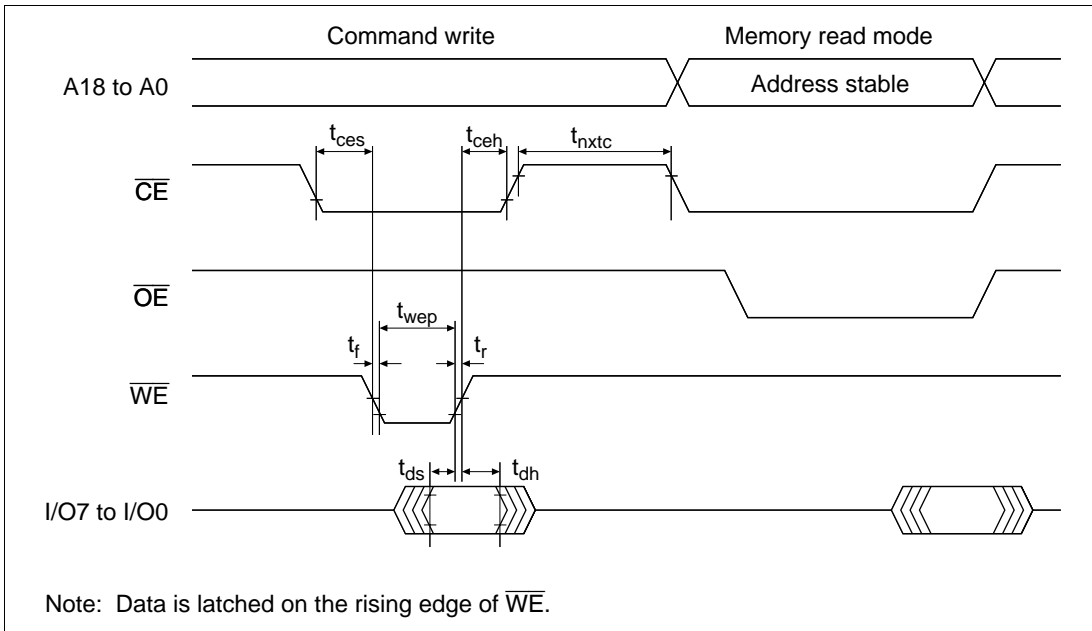
2. In memory read mode, the number of cycles depends on the number of address write cycles (n).

### 21.11.3 Memory Read Mode

1. After completion of auto-program/auto-erase/status read operations, a transition is made to the command wait state. When reading memory contents, a transition to memory read mode must first be made with a command write, after which the memory contents are read.
2. In memory read mode, command writes can be performed in the same way as in the command wait state.
3. Once memory read mode has been entered, consecutive reads can be performed.
4. After powering on, memory read mode is entered.

**Table 21.15 AC Characteristics in Transition to Memory Read Mode**  
 (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

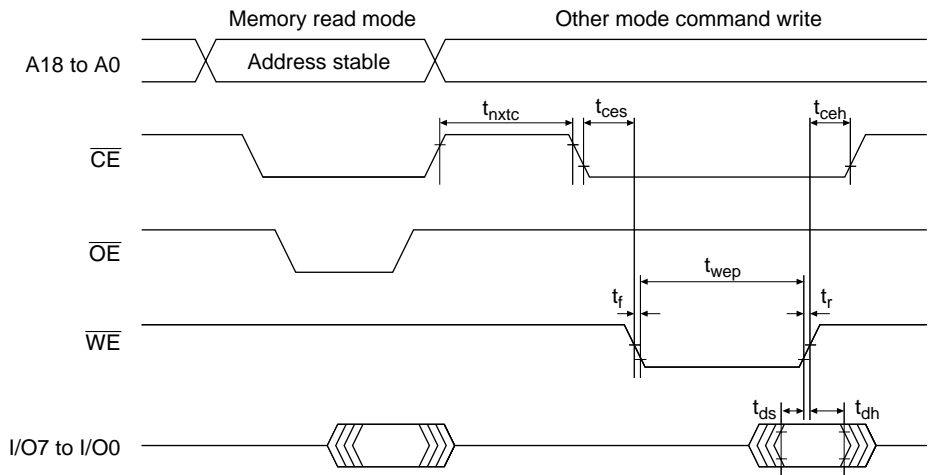
Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{ceh}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
$\overline{\text{WE}}$ rise time	$t_r$		30	ns	
$\overline{\text{WE}}$ fall time	$t_f$		30	ns	



**Figure 21.21 Timing Waveforms for Memory Read after Memory Write**

**Table 21.16 AC Characteristics in Transition from Memory Read Mode to Another Mode**  
 (Conditions:  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{CE}$ hold time	$t_{ceh}$	0		ns	
$\overline{CE}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
$\overline{WE}$ rise time	$t_r$		30	ns	
$\overline{WE}$ fall time	$t_f$		30	ns	

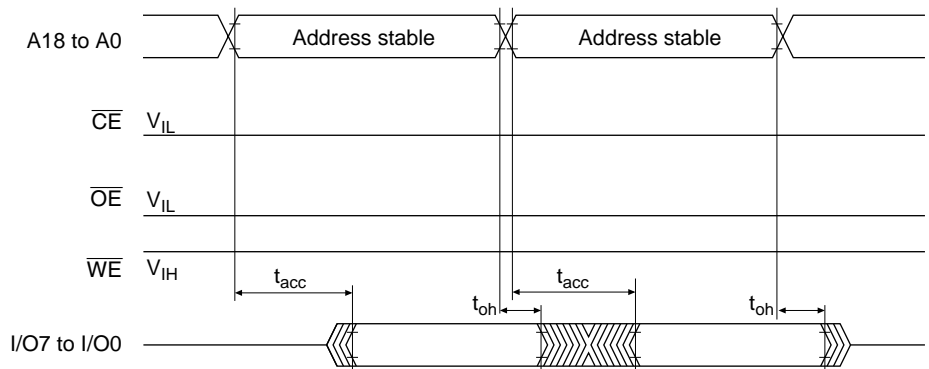


Note: Do not enable  $\overline{WE}$  and  $\overline{OE}$  at the same time.

**Figure 21.22 Timing Waveforms in Transition from Memory Read Mode to Another Mode**

**Table 21.17 AC Characteristics in Memory Read Mode (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Access time	$t_{acc}$		20	$\mu\text{s}$	
$\overline{CE}$ output delay time	$t_{ce}$		150	ns	
$\overline{OE}$ output delay time	$t_{oe}$		150	ns	
Output disable delay time	$t_{df}$		100	ns	
Data output hold time	$t_{oh}$	5		ns	



**Figure 21.23  $\overline{CE}$  and  $\overline{OE}$  Enable State Read Timing Waveforms**

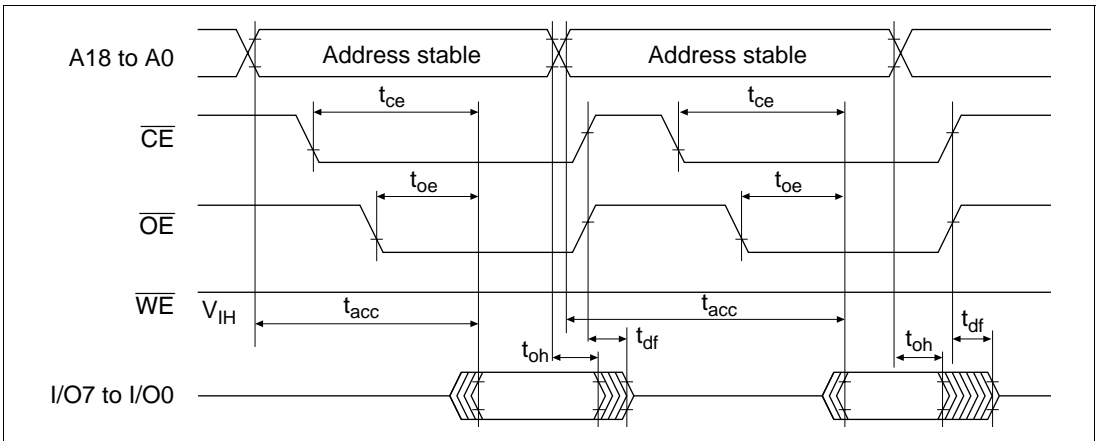


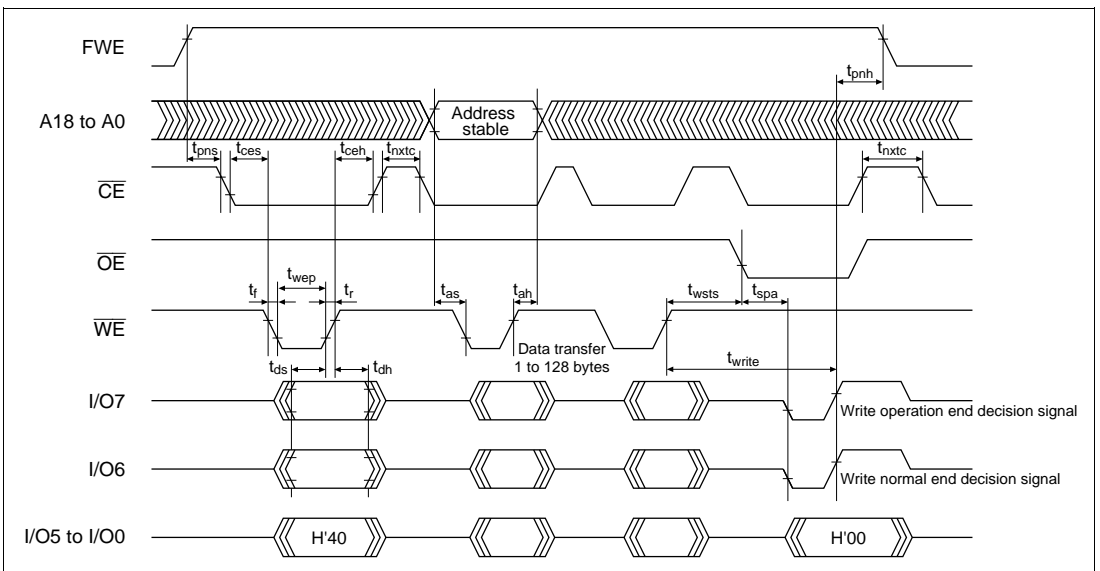
Figure 21.24  $\overline{CE}$  and  $\overline{OE}$  Clock System Read Timing Waveforms

#### 21.11.4 Auto-Program Mode

1. In auto-program mode, 128 bytes are programmed simultaneously. This should be carried out by executing 128 consecutive byte transfers.
2. A 128-byte data transfer is necessary even when programming fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. The lower 7 bits of the transfer address must be low. If a value other than an effective address is input, processing will switch to a memory write operation but a write error will be flagged.
4. Memory address transfer is performed in the second cycle (figure 21.25). Do not perform transfer after the second cycle.
5. Do not perform a command write during a programming operation.
6. Perform one auto-program operation for a 128-byte block for each address. Two or more additional programming operations cannot be performed on a previously programmed address block.
7. Confirm normal end of auto-programming by checking I/O6. Alternatively, status read mode can also be used for this purpose (I/O7 status polling uses the auto-program operation end decision pin).
8. Status polling I/O6 and I/O7 pin information is retained until the next command write. As long as the next command write has not been performed, reading is possible by enabling  $\overline{CE}$  and  $\overline{OE}$ .

**Table 21.18 AC Characteristics in Auto-Program Mode (Conditions:  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{ceh}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
Status polling start time	$t_{wsts}$	1		ms	
Status polling access time	$t_{spa}$		150	ns	
Address setup time	$t_{as}$	0		ns	
Address hold time	$t_{ah}$	60		ns	
Memory write time	$t_{write}$	1	3000	ms	
Write setup time	$t_{pns}$	100		ns	
Write end setup time	$t_{pnh}$	100		ns	
$\overline{\text{WE}}$ rise time	$t_r$		30	ns	
$\overline{\text{WE}}$ fall time	$t_f$		30	ns	



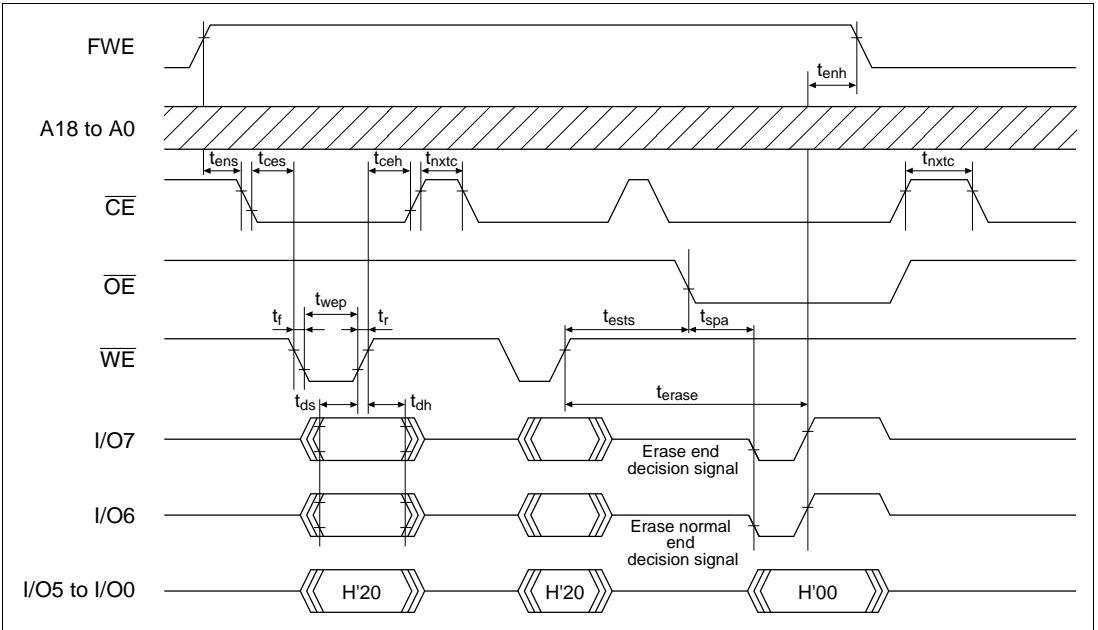
**Figure 21.25 Auto-Program Mode Timing Waveforms**

## 21.11.5 Auto-Erase Mode

1. Auto-erase mode supports only entire memory erasing.
2. Do not perform a command write during auto-erasing.
3. Confirm normal end of auto-erasing by checking I/O6. Alternatively, status read mode can also be used for this purpose (I/O7 status polling uses the auto-erase operation end decision pin).
4. Status polling I/O6 and I/O7 pin information is retained until the next command write. As long as the next command write has not been performed, reading is possible by enabling  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$ .

**Table 21.19 AC Characteristics in Auto-Erase Mode (Conditions:  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	$t_{\text{nxtc}}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{\text{ceh}}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{\text{ces}}$	0		ns	
Data hold time	$t_{\text{dh}}$	50		ns	
Data setup time	$t_{\text{ds}}$	50		ns	
Write pulse width	$t_{\text{wep}}$	70		ns	
Status polling start time	$t_{\text{ests}}$	1		ms	
Status polling access time	$t_{\text{s pa}}$		150	ns	
Memory erase time	$t_{\text{erase}}$	100	40000	ms	
Erase setup time	$t_{\text{ens}}$	100		ns	
Erase end setup time	$t_{\text{enh}}$	100		ns	
$\overline{\text{WE}}$ rise time	$t_{\text{r}}$		30	ns	
$\overline{\text{WE}}$ fall time	$t_{\text{f}}$		30	ns	



**Figure 21.26 Auto-Erase Mode Timing Waveforms**

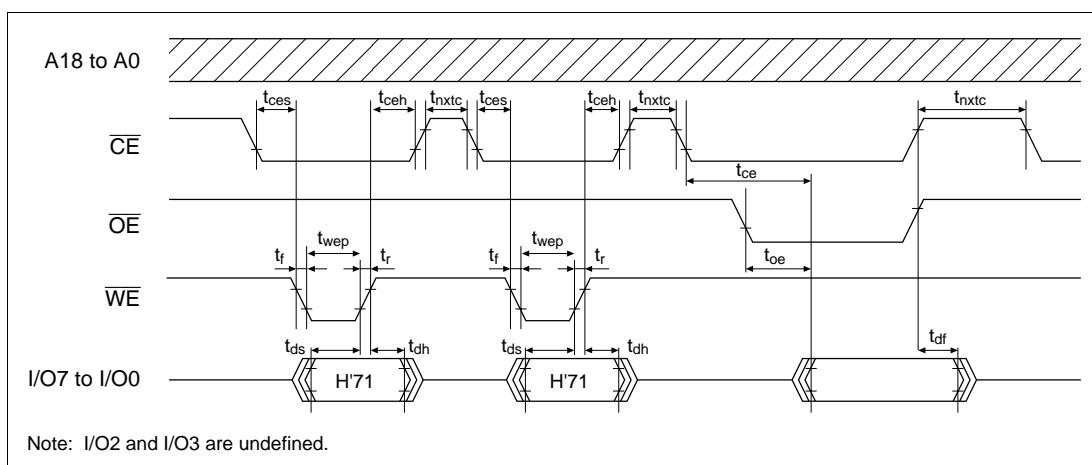


## 21.11.6 Status Read Mode

1. Status read mode is provided to identify the kind of abnormal end. Use this mode when an abnormal end occurs in auto-program mode or auto-erase mode.
2. The return code is retained until a command write other than a status read mode command write is executed.

**Table 21.20 AC Characteristics in Status Read Mode (Conditions:  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )**

Item	Symbol	Min	Max	Unit	Notes
Read time after command write	$t_{nxtc}$	20		$\mu\text{s}$	
$\overline{\text{CE}}$ hold time	$t_{ceh}$	0		ns	
$\overline{\text{CE}}$ setup time	$t_{ces}$	0		ns	
Data hold time	$t_{dh}$	50		ns	
Data setup time	$t_{ds}$	50		ns	
Write pulse width	$t_{wep}$	70		ns	
$\overline{\text{OE}}$ output delay time	$t_{oe}$		150	ns	
Disable delay time	$t_{df}$		100	ns	
$\overline{\text{CE}}$ output delay time	$t_{ce}$		150	ns	
$\overline{\text{WE}}$ rise time	$t_r$		30	ns	
$\overline{\text{WE}}$ fall time	$t_f$		30	ns	



**Figure 21.27 Status Read Mode Timing Waveforms**

**Table 21.21 Status Read Mode Return Commands**

Pin Name	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Attribute	Normal end decision	Command error	Programming error	Erase error	—	—	Programming or erase count exceeded	Effective address error
Initial value	0	0	0	0	0	0	0	0
Indications	Normal end: 0 Abnormal end: 1	Command error: 1 Otherwise: 0	Programming error: 1 Otherwise: 0	Erasing error: 1 Otherwise: 0	—	—	Count exceeded: 1 Otherwise: 0	Effective address error: 1 Otherwise: 0

Note: I/O2 and I/O3 are undefined.

### 21.11.7 Status Polling

1. The I/O7 status polling flag indicates the operating status in auto-program/auto-erase mode.
2. The I/O6 status polling flag indicates a normal or abnormal end in auto-program/auto-erase mode.

**Table 21.22 Status Polling Output Truth Table**

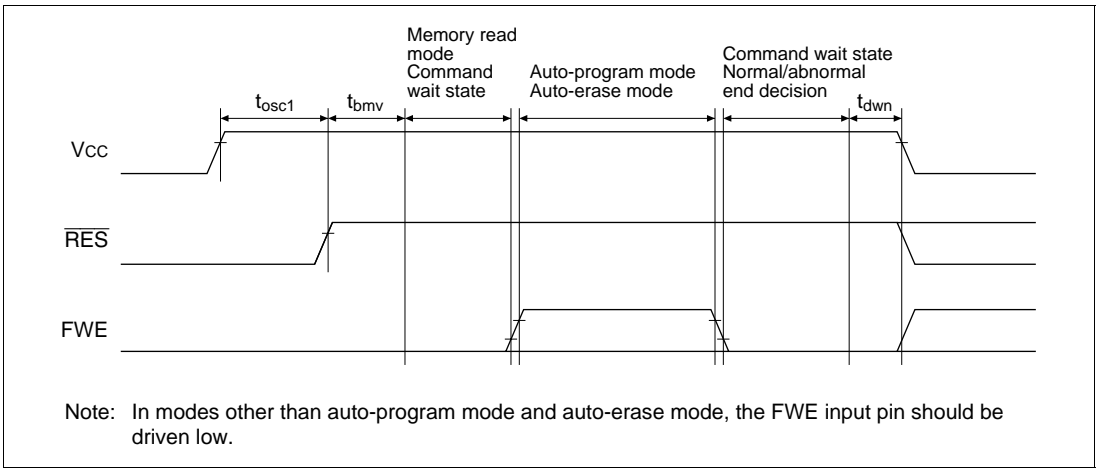
Pin Name	During Internal Operation			Normal End
	Abnormal End	—		
I/O7	0	1	0	1
I/O6	0	0	1	1
I/O0 to I/O5	0	0	0	0

### 21.11.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

**Table 21.23 Stipulated Transition Times to Command Wait State**

Item	Symbol	Min	Max	Unit	Notes
Standby release (oscillation stabilization time)	$t_{osc1}$	30		ms	
Programmer mode setup time	$t_{bmv}$	10		ms	
$V_{CC}$ hold time	$t_{dwn}$	0		ms	



**Figure 21.28 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence**

### 21.11.9 Notes on Memory Programming

1. When programming addresses which have previously been programmed, carry out auto-erasing before auto-programming.
2. When performing programming using programmer mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.

- Notes:
1. The flash memory is initially in the erased state when the device is shipped by Hitachi. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.
  2. Auto-programming should be performed once only on the same address block. Additional programming cannot be performed on previously programmed address blocks.



# Section 22 RAM

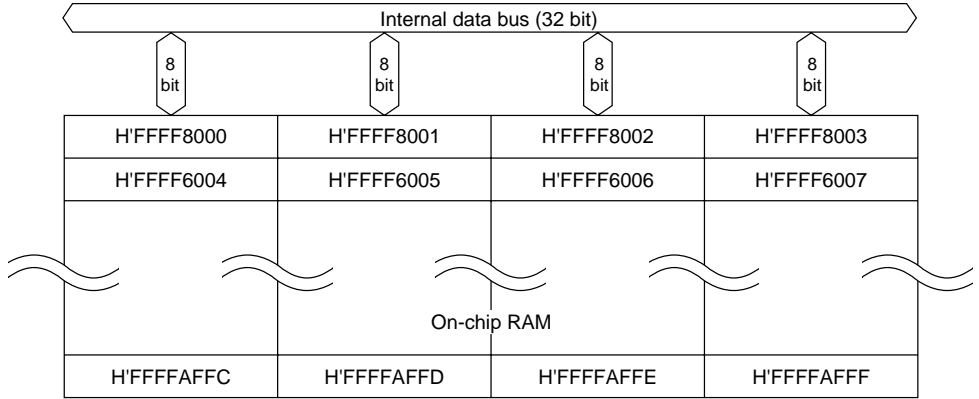
## 22.1 Overview

The SH7052F has 12 kbytes of on-chip RAM, SH7053F and SH7054F each have 16 kbytes, of on-chip RAM. The on-chip RAM is linked to the CPU, direct memory access controller (DMAC), and advanced user debugger (AUD) with a 32-bit data bus (figure 22.1).

The CPU, DMAC, and AUD can access data in the on-chip RAM in 8, 16, or 32 bit widths. On-chip RAM data can always be accessed in one state, making the RAM ideal for use as a program area, stack area, or data area, which require high-speed access. The contents of the on-chip RAM are held in both the sleep and software standby modes. When the RAME bit (see below) is cleared to 0, the on-chip RAM contents are also held in hardware standby mode.

The on-chip RAM of SH7052F is allocated to addresses H'FFFF8000 to H'FFFFAFFF. Each on-chip RAM of SH7053F and SH7054F is allocated to address H'FFFF8000 to H'FFFFBFFF

SH7052F



SH7053F/7054F

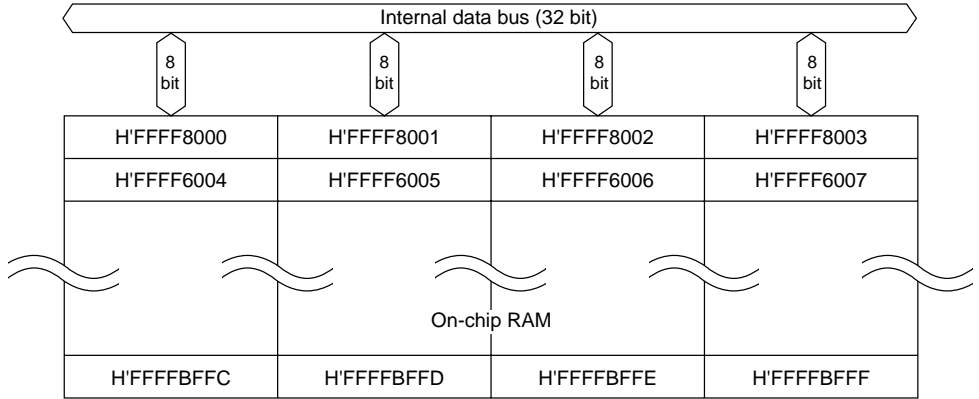


Figure 22.1 Block Diagram of RAM

## 22.2 Operation

The on-chip RAM is controlled by means of the system control register (SYSCR).

When the RAME bit in SYSCR is set to 1, the on-chip RAM is enabled. Accesses to addresses H'FFFF8000 to H'FFFFAFFF is SH7052F, or accesses to address H'FFFF8000 to H'FFFFBFFF in SH7053F and SH7054F are then directed to the on-chip RAM.

When the RAME bit in SYSCR is cleared to 0, the on-chip RAM is not accessed. A read will return an undefined value, and a write is invalid. If a transition is made to hardware standby mode after the RAME bit in SYSCR is cleared to 0, the contents of the on-chip RAM are held.

For details of SYSCR, see 23.2.2, System Control Register (SYSCR), in section 23, Power-Down State.





# Section 23 Power-Down State

## 23.1 Overview

Three modes are provided as power-save modes, namely, the hardware standby, software standby and sleep modes. Also, a module stop function is available to stop some modules. These standby modes can be selected depending on applications to reduce the power consumption of the SH7052F/SH7053F/SH7054F.

### 23.1.1 Power-Down States

The power-down state is effected by the following modes:

#### 1. Hardware standby mode

A transition to hardware standby mode is made according to the input level of the  $\overline{\text{RES}}$  and  $\overline{\text{HSTBY}}$  pins.

In hardware standby mode, all SH7052F/SH7053F/SH7054F functions are halted.

This state is exited by means of a power-on reset.

#### 2. Software standby mode

A transition to software standby mode is made by means of software (a CPU instruction).

In software standby mode, all SH7052F/SH7053F/SH7054F functions are halted.

This state is exited by means of a power-on reset or an NMI interrupt.

#### 3. Sleep mode

A transition to sleep mode is made by means of a CPU instruction.

In software standby mode, basically only the CPU is halted, and all on-chip peripheral modules operate.

This state is exited by means of a power-on reset, a manual reset, interrupt, or DMA address error.

#### 4. Module standby mode

Operation of the on-chip peripheral modules\* which can be placed in a standby mode can be stopped by stopping the clock supply. Clock supply to the individual modules can be controlled by setting bits in the module standby control register (MSTCR).

Note: \* AUD, H-UDI, and UBC

Table 23.1 shows the transition conditions for entering the modes from the program execution state, as well as the CPU and peripheral function status in each mode and the procedures for canceling each mode.

**Table 23.1 Power-Down State Conditions**

Mode	Entering Procedure	State						Canceling Procedure
		Clock	CPU	CPU Registers	On-Chip Peripheral Modules	RAM	Pins	
Hardware standby	Low-level input at HSTBY pin	Halted	Halted	Halted	Undefined	Held <sup>*2</sup>	Initialized	High-level input at HSTBY pin, executing power-on reset
Software standby	Execute SLEEP instruction with SSBY bit set to 1 in SBYCR	Halted	Halted	Held	Halted <sup>*1</sup>	Held	Held or high impedance <sup>*3</sup>	<ul style="list-style-type: none"> <li>NMI interrupt</li> <li>Power-on reset</li> </ul>
Sleep	Execute SLEEP instruction with SSBY bit cleared to 0 in SBYCR	Runs	Halted	Held	Run	Held	Held	<ul style="list-style-type: none"> <li>Interrupt</li> <li>DMA address error</li> <li>Power-on reset</li> <li>Manual reset</li> </ul>

Notes: SBYCR: Standby control register  
SSBY: Software standby bit

1. Some bits within on-chip peripheral module registers are initialized in software standby mode, and some are not. See table 23.4, Register States in Software Standby Mode. Also refer to the register descriptions for each peripheral module.
2. Clear the RAME bit of the SYSCR to 0 in advance when changing the state from the program execution state to the hardware standby state.
3. The state of the I/O ports in standby mode is set by the port high impedance bit (HIZ) in SBYCR. See section 23.2.1, Standby Control Register (SBYCR). For details of other pin states, refer to Appendix B Pin States.

## 23.1.2 Pin Configuration

Pins related to power-down modes are shown in table 23.2.

**Table 23.2 Pin Configuration**

Pin Name	Abbreviation	I/O	Function
Hardware standby input pin	$\overline{\text{HSTBY}}$	Input	Input level determines transition to hardware standby mode
Power-on reset input pin	$\overline{\text{RES}}$	Input	Power-on reset signal input pin

## 23.1.3 Related Registers

Table 23.3 shows the registers used for power-down state control.

**Table 23.3 Related Registers**

Name	Abbreviation	R/W	Initial Value	Address		Access Size
				Write	Read	
Standby control register	SBYCR <sup>*1</sup>	R/W	H'1F		H'FFFFFFE14	8
System control register	SYSCR <sup>*1</sup>	R/W	H'01		H'FFFFFF708	8
Module standby control register	MSTCR <sup>*1</sup>	R/W	H'01	H'FFFFFF70A <sup>*2</sup>	H'FFFFFF70B <sup>*3</sup>	8, 16

- Notes:
1. SBYCR is accessed in three cycles, SYSCR and MSTCR in four or five cycles.
  2. Write data in word units. Data cannot be written in byte or longword units.
  3. Read data in byte units. Values cannot be read correctly if data is read in word or longword units.

## 23.2 Register Descriptions

### 23.2.1 Standby Control Register (SBYCR)

The standby control register (SBYCR) is an 8-bit readable/writable register that sets the transition to standby mode, and the port state in standby mode. SBYCR is initialized to H'1F by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	SSBY	HIZ	—	—	—	—	—	—
Initial value:	0	0	0	1	1	1	1	1
R/W:	R/W	R/W	R	R	R	R	R	R

- Bit 7—Software Standby (SSBY): Specifies transition to software standby mode. The SSBY bit cannot be set to 1 while the watchdog timer is running (when the timer enable bit (TME) in the WDT timer control/status register (TCSR) is set to 1). To enter software standby mode, always halt the WDT by clearing the TME bit to 0, then set the SSBY bit.

Bit 7: SSBY	Description
-------------	-------------

0	Executing SLEEP instruction puts the SH7052F/SH7053F/SH7054F into sleep mode (Initial value)
1	Executing SLEEP instruction puts the SH7052F/SH7053F/SH7054F into standby mode

- Bit 6—Port High Impedance (HIZ): In software standby mode, this bit selects whether to set I/O port pins to high impedance or hold the pin state. The HIZ bit cannot be set to 1 when the TME bit of the WDT timer control/status register (TCSR) is set to 1. When making the I/O port pin state high impedance, always clear the TME bit to 0 before setting the HIZ bit.

Bit 6: HIZ	Description
------------	-------------

0	Pin states held in software standby mode (Initial value)
1	Pins go to high impedance in software standby mode

- Bit 5—Reserved: This bit always reads 0. The write value should always be 0.
- Bits 4 to 0—Reserved: These bits always read 1. The write value should always be 1.

## 23.2.2 System Control Register (SYSCR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	AUDSRST	RAME
Initial value:	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R/W	R/W

The system control register (SYSCR) is an 8-bit readable/writable register that performs AUD software reset control and enables or disables access to the on-chip RAM.

SYSCR is initialized to H'01 by a power-on reset.

- Bits 7 to 2—Reserved: These bits always read 0. The write value should always be 0.
- Bit1— AUD Software Reset (AUDSRST): This bit controls AUD reset using software. Setting the AUDSRST bit to 1 places, the AUD module in the power-on reset state.

### Bit 1: AUDSRST Description

0	AUD reset state cleared	
1	AUD reset state entered	(Initial value)

- Bit 0—RAME Enable (RAME): Selects enabling or disabling of the on-chip RAM. When RAME is set to 1, on-chip RAM is enabled. When RAME is cleared to 0, on-chip RAM cannot be accessed. In this case, a read or instruction fetch from on-chip RAM will return an undefined value, and a write to on-chip RAM will be ignored. The initial value of RAME is 1. When on-chip RAM is disabled by clearing RAME to 0, do not place an instruction that attempts to access on-chip RAM immediately after the SYSCR write instruction, as normal access cannot be guaranteed in this case. When on-chip RAM is enabled by setting RAME to 1, place an SYSCR read instruction immediately after the SYSCR write instruction. Normal access cannot be guaranteed if an on-chip RAM access instruction is placed immediately after the SYSCR write instruction.

### Bit 0: RAME Description

0	On-chip RAM disabled	
1	On-chip RAM enabled	(Initial value)

### 23.2.3 Module Standby Control Register (MSTCR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	MSTOP3	—	—	MSTOP0
Initial value:	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R/W	R	R	R/W

The module standby control register (MSTCR) is an 8-bit readable/writable register that controls the standby state of the AUD, and UBC on-chip modules.

MSTCR is initialized to H'01 by a power-on reset.

Note: The method of writing to MSTCR is different from that of ordinary registers to prevent inadvertent rewriting. See section 23.2.4, Notes on Register Access, for more information.

- Bits 7 to 4—Reserved: These bits always read 0. The write value should always be 0.
- Bit 3—Module Stop 3 (MSTOP3): Specifies halting of the clock supply to the AUD on-chip peripheral module. Setting the MSTOP3 bit to 1 stops the clock supply to the AUD. To cancel halting of the clock supply to the AUD, first set the AUD software reset bit (AUDSRST) in the system control register (SYSCR) to the AUD reset state value. Use of the AUD will then be enabled by clearing the AUD reset.

#### Bit 3: MSTOP3 Description

0	AUD operates	(Initial value)
1	Clock supply to AUD stopped	

- Bits 2 and 1—Reserved: These bits always read 0. The write value should always be 0.
- Bit 0—Module Stop 0 (MSTOP0): Specifies halting of the clock supply stop to the UBC on-chip peripheral module.  
Clearing the MSTOP0 bit to 0 starts the clock supply to the UBC.  
Stopping clock supply to the UBC will reset the internal state of the UBC including its registers.

#### Bit 0: MSTOP0 Description

0	UBC operates	
1	Clock supply to UBC stopped	(Initial value)

## 23.2.4 Notes on Register Access

The method of writing to the module standby control register (MSTCR) is different from that of ordinary registers to prevent inadvertent rewriting.

Be certain to use a word transfer instruction when writing data to MSTCR. Data cannot be written by a byte transfer instruction. As shown in figure 23.1, set the upper byte to H'3C and transfer data using the lower byte as write data.

Data can be read by the same method as for ordinary registers.

MSTCR is allocated to address H'FFFFFF70A. Always use a byte transfer instruction to read data.

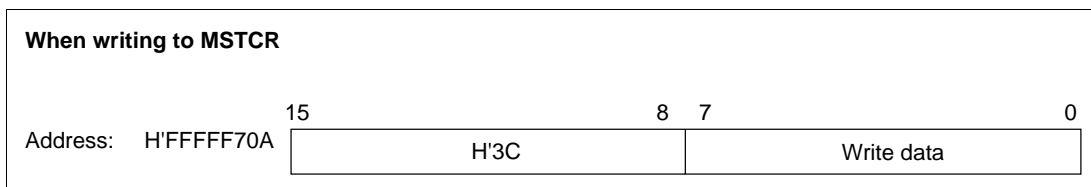


Figure 23.1 Writing to MSTCR

## 23.3 Hardware Standby Mode

### 23.3.1 Transition to Hardware Standby Mode

The chip enters hardware standby mode when the  $\overline{\text{HSTBY}}$  pin or  $\overline{\text{RES}}$  pin goes low. Hardware standby mode reduces power consumption drastically by halting all SH7052F/SH7053F/SH7054F functions. As the transition to hardware standby mode is made by means of external pin input, the transition is made asynchronously, regardless of the current state of the SH7052F/SH7053F/SH7054F, and therefore the chip state prior to the transition is not preserved. However, on-chip RAM data is retained as long as the specified voltage is supplied. To retain on-chip RAM data, clear the RAM enable bit (RAME) to 0 in the system control register (SYSCR) before driving the  $\overline{\text{HSTBY}}$  pin low. See Appendix B Pin States for the pin states in hardware standby mode.

### 23.3.2 Canceling Hardware Standby Mode

Hardware standby mode is canceled by means of the  $\overline{\text{HSTBY}}$  pin and  $\overline{\text{RES}}$  pin. When  $\overline{\text{HSTBY}}$  is driven high while  $\overline{\text{RES}}$  is low, the clock oscillator starts running. The  $\overline{\text{RES}}$  pin should be held low long enough for clock oscillation to stabilize. When  $\overline{\text{RES}}$  is driven high, power-on reset exception processing is started and a transition is made to the program execution state.

### 23.3.3 Hardware Standby Mode Timing

Figure 23.2 shows sample pin timings for hardware standby mode. A transition to hardware standby mode is made by driving the  $\overline{\text{HSTBY}}$  pin low after driving the  $\overline{\text{RES}}$  pin low. Hardware standby mode is canceled by driving  $\overline{\text{HSTBY}}$  high, waiting for clock oscillation to stabilize, then switching  $\overline{\text{RES}}$  from low to high.

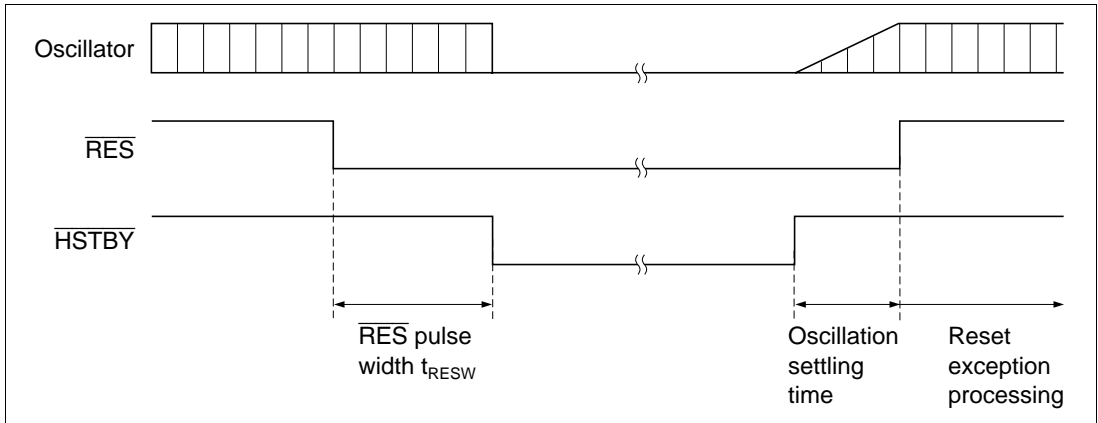


Figure 23.2 Hardware Standby Mode Timing

## 23.4 Software Standby Mode

### 23.4.1 Transition to Software Standby Mode

To enter software standby mode, set the software standby bit (SSBY) to 1 in SBYCR, then execute the SLEEP instruction. The SH7052F/SH7053F/SH7054F switches from the program execution state to software standby mode. In software standby mode, power consumption is greatly reduced by halting not only the CPU, but the clock and on-chip peripheral modules as well. CPU register contents and on-chip RAM data are held as long as the prescribed voltages are applied (when the RAME bit in SYSCR is 0). The register contents of some on-chip peripheral modules are initialized, but some are not (table 23.4). The I/O port state can be selected as held or high impedance by the port high impedance bit (HIZ) in SBYCR. For other pin states, refer to Appendix B Pin States.



**Table 23.4 Register States in Software Standby Mode**

<b>On-Chip Peripheral Module</b>	<b>Registers Initialized</b>	<b>Registers that Retain Data</b>
Interrupt controller (INTC)	—	All registers
User break controller (UBC)	—	All registers
Bus state controller (BSC)	—	All registers
Direct memory access controller (DMAC)	All registers	—
Advanced timer unit (ATU)	All registers	—
Advanced pulse controller (APC)	—	All registers
Watchdog timer (WDT)	<ul style="list-style-type: none"> <li>• Bits 7 to 5 (OVF, WT/<math>\overline{IT}</math>, TME) of the timer control status register (TCSR)</li> <li>• Reset control/status register (RSTCSR)</li> <li>• Timer counter (TCNT)</li> </ul>	<ul style="list-style-type: none"> <li>• Bits 2 to 0 (CKS2 to CKS0) of TCSR</li> </ul>
Compare match timer (CMT)	All registers	—
HCAN	Registers other than MC0[1:8] to MC15[1:8] MD0[1:8] to MD15[1:8]	MC0[1:8] to MC15[1:8] MD0[1:8] to MD15[1:8]
Serial communication interface (SCI)	All registers	—
A/D converter (A/D)	All registers	—
Pin function controller (PFC)	—	All registers
I/O ports (I/O)	—	All registers
Flash memory control registers	All registers (except RAMER)	—
Power-down state related	—	<ul style="list-style-type: none"> <li>• Standby control register (SBYCR)</li> <li>• System control register (SYSCR)</li> <li>• Module stop control register (MSTCR)</li> </ul>

## 23.4.2 Canceling Software Standby Mode

Software standby mode is canceled by an NMI interrupt or a power-on reset.

**Cancellation by NMI:** Clock oscillation starts when a rising edge or falling edge (selected by the NMI edge select bit (NMIE) in the interrupt control register (ICR) of the INTC) is detected in the NMI signal. This clock is supplied only to the watchdog timer (WDT). A WDT overflow occurs if the time established by the clock select bits (CKS2 to CKS0) in TCSR of the WDT elapses before transition to software standby mode. The occurrence of this overflow is used to indicate that the clock has stabilized, so the clock is supplied to the entire chip, software standby mode is canceled, and NMI exception processing begins.

When canceling standby mode with an NMI interrupt, set the CKS2 to CKS0 bits so that the WDT overflow period is longer than the oscillation stabilization time.

When canceling standby mode with an NMI pin set for falling edge, be sure that the NMI pin level upon entering software standby (when the clock is halted) is high, and that the NMI pin level upon returning from software standby (when the clock starts after oscillation stabilization) is low. When canceling software standby mode with an NMI pin set for rising edge, be sure that the NMI pin level upon entering software standby (when the clock is halted) is low, and that the NMI pin level upon returning from software standby (when the clock starts after oscillation stabilization) is high.

**Cancellation by Power-On Reset:** A power-on reset of the SH7052F/SH7053F/SH7054F caused by driving the  $\overline{\text{RES}}$  pin low cancels software standby mode.

### 23.4.3 Software Standby Mode Application Example

This example describes a transition to software standby mode on the falling edge of the NMI signal, and cancellation on the rising edge of the NMI signal. The timing is shown in figure 23.3.

When the NMI pin is changed from high to low level while the NMI edge select bit (NMIE) in ICR is set to 0 (falling edge detection), the NMI interrupt is accepted. When the NMIE bit is set to 1 (rising edge detection) by the NMI exception service routine, the software standby bit (SSBY) in SBYCR is set to 1, and a SLEEP instruction is executed, software standby mode is entered.

Thereafter, software standby mode is canceled when the NMI pin is changed from low to high level.

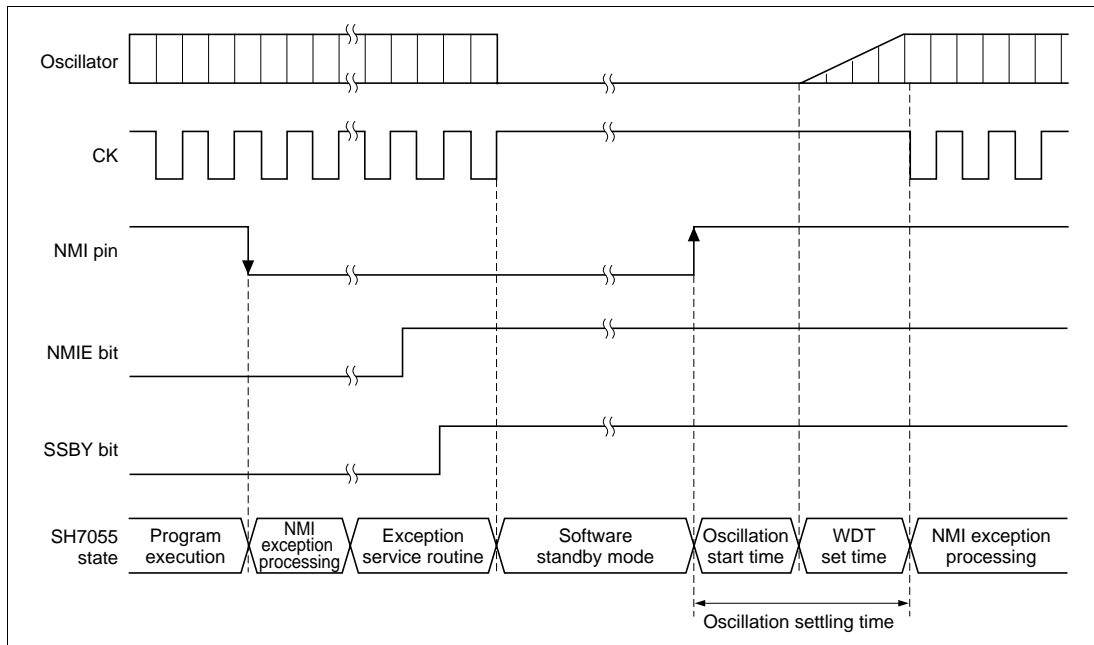


Figure 23.3 Software Standby Mode NMI Timing (Application Example)

## 23.5 Sleep Mode

### 23.5.1 Transition to Sleep Mode

Executing the SLEEP instruction after the software standby bit (SSBY) in SBYCR has been cleared to 0 causes a transition from the program execution state to sleep mode. Although the CPU halts immediately after executing the SLEEP instruction, the contents of its internal registers remain unchanged. The on-chip peripheral modules continue to run during sleep mode.

### 23.5.2 Canceling Sleep Mode

**Cancellation by Interrupt:** When an interrupt occurs, sleep mode is canceled and interrupt exception processing is executed. The sleep mode is not canceled if the interrupt cannot be accepted because its priority level is equal to or less than the mask level set in the CPU's status register (SR) or if an interrupt by an on-chip peripheral module is disabled at the peripheral module.

**Cancellation by DMA Address Error:** If a DMA address error occurs, sleep mode is canceled and DMA address error exception processing is executed.

**Cancellation by Manual Reset:** When an internal manual reset is triggered by the WDT and the CPU acquires the bus during the internal manual reset period, the state of the SH7052F/SH7053F/SH7054F changes to the manual reset state and sleep mode will be released.

**Cancellation by Power-On Reset:** A power-on reset of the SH7052F/SH7053F/SH7054F resulting from driving the  $\overline{\text{RES}}$  pin low, or caused by the WDT, cancels sleep mode.

## 24.1 Absolute Maximum Ratings

Table 24.1 shows the absolute maximum ratings.

**Table 24.1 Absolute Maximum Ratings**

Item	Symbol	Rating	Unit	Remarks	
Power supply voltage	$V_{CC}, PLLV_{CC}$	$V_{CC}$	-0.3 to +4.3	V	The PLLCAP, EXTAL, XTAL, and CK pins are concerned. (The same voltage must be used for $V_{CC}$ and $PLLV_{CC}$ )
	$PV_{CC1}, PV_{CC2}$	$PV_{CC}$	-0.3 to +7.0	V	Except for the PLLCAP, EXTAL, XTAL, and CK pins and the analog input pin
Input voltage	EXTAL	$V_{in}$	-0.3 to $V_{CC} + 0.3$	V	
	All pins other than the analog input pin and EXTAL pin	$V_{in}$	-0.3 to $PV_{CC} + 0.3$	V	Refer to table 24.2
Analog power supply voltage	$AV_{CC}$	-0.3 to +7.0	V		
Analog reference voltage	AVref	-0.3 to $AV_{CC} + 0.3$	V		
Analog input voltage	$V_{AN}$	-0.3 to $AV_{CC} + 0.3$	V		
Operating temperature (except when writing or erasing flash EEPROM)	Topr	-40 to +85	°C		
Operating temperature (When writing or erasing flash EEPROM)	TWEopr	-40 to +85	°C	Only when flash EEPROM is written or erased	
Storage temperature	Tstg	-55 to +125	°C		

### [Operating precautions]

Operating the LSI in excess of the absolute maximum ratings may result in permanent damage. The two power supply voltages of  $PV_{CC}$  of 5V and  $V_{CC}$  of 3V may be used simultaneously with the LSI. Be sure to use the LSI in compliance with the connection of power pins, combination conditions of applicable power supply voltages, voltage applicable to each pin, and conditions of output voltage, as specified in the manual. Connecting a non-specified power supply or using the LSI at an incorrect voltage may result in permanent damage of the LSI or the system that contains the LSI.

## 24.2 DC Characteristics

Table 24.2 shows the correspondence between power supply names and pins.

Table 24.4 shows DC characteristics.

**Table 24.2 Correspondence between Power Supply Names and Pins**

Pin No.	Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
1			PF1	A17			PVcc1	PVcc1+0.3	
2			PF2	A18			PVcc1	PVcc1+0.3	
3			PF3	A19			PVcc1	PVcc1+0.3	
4			PF4	A20			PVcc1	PVcc1+0.3	
5			PF5	A21	$\overline{\text{POD}}$		PVcc1	PVcc1+0.3	
6			PF6	$\overline{\text{WRL}}$			PVcc1	PVcc1+0.3	
7			PF7	$\overline{\text{WRH}}$			PVcc1	PVcc1+0.3	
8			PF8	$\overline{\text{WAIT}}$			PVcc1	PVcc1+0.3	
9			PF9	$\overline{\text{RD}}$			PVcc1	PVcc1+0.3	
10	PVcc1								
11			PF10	$\overline{\text{CS0}}$			PVcc1	PVcc1+0.3	
12	Vss								
13			PF11	$\overline{\text{CS1}}$			PVcc1	PVcc1+0.3	
14			PF12	$\overline{\text{CS2}}$			PVcc1	PVcc1+0.3	
15			PF13	$\overline{\text{CS3}}$			PVcc1	PVcc1+0.3	
16			PF14	$\overline{\text{BACK}}$			PVcc1	PVcc1+0.3	
17			PF15	$\overline{\text{BREQ}}$			PVcc1	PVcc1+0.3	
18		MD2						5.5+0.3	
19	Vcc								
20			CK				Vcc		
21	Vss								
22		MD1						5.5+0.3	
23		MD0						5.5+0.3	
24		EXTAL						Vcc+0.3	

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
25	Vss								
26		XTAL					Vcc		
27	Vcc								
28		FWE						5.5+0.3	
29		HSTBY						5.5+0.3	
30		RES						5.5+0.3	
31		NMI						5.5+0.3	
32	PLLVcc								
33	PLLCA P								
34	PLLVss								
35			PH0	D0			PVcc1	PVcc1+0.3	
36			PH1	D1			PVcc1	PVcc1+0.3	
37			PH2	D2			PVcc1	PVcc1+0.3	
38			PH3	D3			PVcc1	PVcc1+0.3	
39			PH4	D4			PVcc1	PVcc1+0.3	
40			PH5	D5			PVcc1	PVcc1+0.3	
41			PH6	D6			PVcc1	PVcc1+0.3	
42	PVcc1								
43			PH7	D7			PVcc1	PVcc1+0.3	
44	Vss								
45			PH8	D8			PVcc1	PVcc1+0.3	
46			PH9	D9			PVcc1	PVcc1+0.3	
47			PH10	D10			PVcc1	PVcc1+0.3	
48			PH11	D11			PVcc1	PVcc1+0.3	
49			PH12	D12			PVcc1	PVcc1+0.3	
50			PH13	D13			PVcc1	PVcc1+0.3	
51			PH14	D14			PVcc1	PVcc1+0.3	

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
52			PH15	D15			PVcc1	PVcc1+0.3	
53	AVcc								
54		AVref							
55	AVss								
56			AN0					AVcc+0.3	
57			AN1					AVcc+0.3	
58			AN2					AVcc+0.3	
59			AN3					AVcc+0.3	
60			AN4					AVcc+0.3	
61			AN5					AVcc+0.3	
62			AN6					AVcc+0.3	
63			AN7					AVcc+0.3	
64			AN8					AVcc+0.3	
65			AN9					AVcc+0.3	
66			AN10					AVcc+0.3	
67			AN11					AVcc+0.3	
68			AN12					AVcc+0.3	
69			AN13					AVcc+0.3	
70			AN14					AVcc+0.3	
71			AN15					AVcc+0.3	
72		WDTOVF					PVcc2		
73			PA0	TI0A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
74	PVcc2								
75			PA1	TI0B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
76	Vss								



**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
77			PA2	TIOC			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
78			PA3	TIOD			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
79	Vcc								
80			PA4	TIO3A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
81	Vss								
82			PA5	TIO3B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
83			PA6	TIO3C			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
84			PA7	TIO3D			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
85			PA8	TIO4A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
86			PA9	TIO4B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
87			PA10	TIO4C			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
88			PA11	TIO4D			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
89			PA12	TIO5A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
90			PA13	TIO5B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
91			PA14	TxD0			PVcc2	PVcc2+0.3	
92			PA15	RxD0			PVcc2	PVcc2+0.3	
93			PB0	TO6A			PVcc2	PVcc2+0.3	
94			PB1	TO6B			PVcc2	PVcc2+0.3	
95	PVcc2								
96			PB2	TO6C			PVcc2	PVcc2+0.3	
97	Vss								
98			PB3	TO6D			PVcc2	PVcc2+0.3	
99			PB4	TO7A	TO8A		PVcc2	PVcc2+0.3	
100			PB5	TO7B	TO8B		PVcc2	PVcc2+0.3	
101			PB6	TO7C	TO8C		PVcc2	PVcc2+0.3	
102			PB7	TO7D	TO8D		PVcc2	PVcc2+0.3	
103			PB8	TxD3	TO8E		PVcc2	PVcc2+0.3	
104			PB9	RxD3	TO8F		PVcc2	PVcc2+0.3	
105			PB10	TxD4	HTxD	TO8G	PVcc2	PVcc2+0.3	
106			PB11	RxD4	HRxD	TO8H	PVcc2	PVcc2+0.3	
107			PB12	TCLKA	$\overline{\text{UBCTR}}\overline{\text{G}}$		PVcc2	PVcc2+0.3	Schmitt-trigger input pin
108			PB13	SCK0			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
109			PB14	SCK1	TCLKB	TI10	PVcc2	PVcc2+0.3	Schmitt-trigger input pin
110			PB15	PULS5	SCK2		PVcc2	PVcc2+0.3	Schmitt-trigger input pin

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
111			PC0	TxD1			PVcc2	PVcc2+0.3	
112			PC1	RxD1			PVcc2	PVcc2+0.3	
113			PC2	TxD2			PVcc2	PVcc2+0.3	
114			PC3	RxD2			PVcc2	PVcc2+0.3	
115	PVcc2								
116			PC4	$\overline{\text{IRQ0}}$			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
117	Vss								
118			PG0	PULS7	HRxD		PVcc2	PVcc2+0.3	
119			PG1	$\overline{\text{IRQ1}}$			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
120			PG2	$\overline{\text{IRQ2}}$			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
121			PG3	$\overline{\text{IRQ3}}$	$\overline{\text{ADTRG0}}$		PVcc2	PVcc2+0.3	Schmitt-trigger input pin
122			PJ0	TIO2A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
123	Vcc								
124			PJ1	TIO2B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
125	Vss								
126			PJ2	TIO2C			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
127			PJ3	TIO2D			PVcc2	PVcc2+0.3	Schmitt-trigger input pin

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
128			PJ4	TIO2E			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
129			PJ5	TIO2F			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
130			PJ6	TIO2G			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
131	Vcc								
132			PJ7	TIO2H			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
133	Vss								
134			PJ8	TIO5C			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
135			PJ9	TIO5D			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
136			PJ10	TI9A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
137			PJ11	TI9B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
138			PJ12	TI9C			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
139			PJ13	TI9D			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
140			PJ14	TI9E			PVcc2	PVcc2+0.3	Schmitt-trigger input pin

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
141	PVcc2								
142			PJ15	TI9F			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
143	Vss								
144			PK0	TO8A			PVcc2	PVcc2+0.3	
145			PK1	TO8B			PVcc2	PVcc2+0.3	
146			PK2	TO8C			PVcc2	PVcc2+0.3	
147			PK3	TO8D			PVcc2	PVcc2+0.3	
148			PK4	TO8E			PVcc2	PVcc2+0.3	
149			PK5	TO8F			PVcc2	PVcc2+0.3	
150			PK6	TO8G			PVcc2	PVcc2+0.3	
151			PK7	TO8H			PVcc2	PVcc2+0.3	
152			PK8	TO8I			PVcc2	PVcc2+0.3	
153			PK9	TO8J			PVcc2	PVcc2+0.3	
154			PK10	TO8K			PVcc2	PVcc2+0.3	
155			PK11	TO8L			PVcc2	PVcc2+0.3	
156			PK12	TO8M			PVcc2	PVcc2+0.3	
157			PK13	TO8N			PVcc2	PVcc2+0.3	
158	PVcc2								
159			PK14	TO8O			PVcc2	PVcc2+0.3	
160	Vss								
161			PK15	TO8P			PVcc2	PVcc2+0.3	
162			AUDRST					PVcc2+0.3	
163			AUDMD					PVcc2+0.3	
164			AUDATA0				PVcc2	PVcc2+0.3	
165			AUDATA1				PVcc2	PVcc2+0.3	
166			AUDATA2				PVcc2	PVcc2+0.3	
167			AUDATA3				PVcc2	PVcc2+0.3	

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
168			AUDCK				PVcc2	PVcc2+0.3	
169			AUDSYNC				PVcc2	PVcc2+0.3	
170			PD0	TIO1A			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
171			PD1	TIO1B			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
172			PD2	TIO1C			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
173			PD3	TIO1D			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
174	PVcc2								
175			PD4	TIO1E			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
176	Vss								
177			PD5	TIO1F			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
178			PD6	TIO1G			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
179			PD7	TIO1H			PVcc2	PVcc2+0.3	Schmitt-trigger input pin
180			PD8	PULS0			PVcc2	PVcc2+0.3	
181			PD9	PULS1			PVcc2	PVcc2+0.3	
182			PD10	PULS2			PVcc2	PVcc2+0.3	
183	Vcc								
184			PD11	PULS3			PVcc2	PVcc2+0.3	

**Table 24.2 Correspondence between Power Supply Names and Pins (cont)**

Pin No.	Power Supply Pin Power Supply Name	Dedicated Pin	User Pin				Output Circuit Power Supply Name	Input Voltage Upper Limit (V)	Notes
			Function 1	Function 2	Function 3	Function 4			
185	Vss								
186			PD12	PULS4			PVcc2	PVcc2+0.3	
187			PD13	PULS6	HTxD		PVcc2	PVcc2+0.3	
188			PE0	A0			PVcc1	PVcc1+0.3	
189			PE1	A1			PVcc1	PVcc1+0.3	
190			PE2	A2			PVcc1	PVcc1+0.3	
191			PE3	A3			PVcc1	PVcc1+0.3	
192			PE4	A4			PVcc1	PVcc1+0.3	
193			PE5	A5			PVcc1	PVcc1+0.3	
194	PVcc1								
195			PE6	A6			PVcc1	PVcc1+0.3	
196	Vss								
197			PE7	A7			PVcc1	PVcc1+0.3	
198			PE8	A8			PVcc1	PVcc1+0.3	
199			PE9	A9			PVcc1	PVcc1+0.3	
200			PE10	A10			PVcc1	PVcc1+0.3	
201			PE11	A11			PVcc1	PVcc1+0.3	
202			PE12	A12			PVcc1	PVcc1+0.3	
203			PE13	A13			PVcc1	PVcc1+0.3	
204			PE14	A14			PVcc1	PVcc1+0.3	
205	PVcc1								
206			PE15	A15			PVcc1	PVcc1+0.3	
207	Vss								
208			PF0	A16			PVcc1	PVcc1+0.3	

## Usage Notes

Set power supply voltages during LSI operation as shown below.

$V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  
 $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$

When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$

The  $PV_{CC1}$  power supply voltage depends on the operating mode as shown below. Operation cannot be guaranteed with other  $PV_{CC1}$  power supply voltages.

**Table 24.3**  $PV_{CC1}$  Voltage in Each Operating Mode

Operating Mode No.	Mode Name	$PV_{CC1}$ Voltage
Modes 0, 1, 2	MCU expanded mode	$3.3 \text{ V} \pm 0.3 \text{ V}$
Mode 3	Single-chip mode	$5.0 \text{ V} \pm 0.5 \text{ V}$
Mode 4	Boot mode	$3.3 \text{ V} \pm 0.3 \text{ V}$
Mode 5	Boot mode	$5.0 \text{ V} \pm 0.5 \text{ V}$
Mode 6	User program mode	$3.3 \text{ V} \pm 0.3 \text{ V}$
Mode 7	User program mode	$5.0 \text{ V} \pm 0.5 \text{ V}$



**Table 24.4 DC Characteristics**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $PV_{CC1} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  
 $PV_{CC2} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{ref} = 4.5\text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

When  $PV_{CC1} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{CC} = PV_{CC1}$ .

When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions	
Input high-level voltage (except Schmitt trigger input voltage)	$\overline{RES}$ , $\overline{NMI}$ , $\overline{FWE}$ , MD2 to 0, $\overline{HSTBY}$	$V_{IH}$	$V_{CC}$ - 0.5	—	5.8	V	
	EXTAL		$V_{CC}$ $\times 0.7$	—	$V_{CC}$ + 0.3	V	
	D15 to D0, $\overline{WAIT}$ , $\overline{BREQ}$ (When in MCU expansion mode)		2.2	—	$PV_{CC1}$ + 0.3	V	$PV_{CC1} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
	$\overline{AUDRST}$ , $\overline{AUDMD}$		$V_{CC}$ - 0.5	—	$PV_{CC2}$ + 0.3	V	
	Other input pins		2.2	—	$PV_{CC}$ + 0.3	V	
Input low-level voltage (except Schmitt trigger input voltage)	$\overline{RES}$ , $\overline{NMI}$ , $\overline{FWE}$ , MD2 to 0, $\overline{HSTBY}$ , $\overline{AUDRST}$ , $\overline{AUDMD}$	$V_{IL}$	-0.3	—	0.5	V	
	Other input pins		-0.3	—	0.8	V	

**Table 24.4 DC Characteristics (cont)**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Schmitt trigger input voltage	TIOA to TIOD, TIO1A to TIO1H, TIO2A to TIO2H, TIO3A to TIO3D, TIO4A to TIO4D, TIO5A to TIO5D, TI9A to TI9F, TI10, TCLKA, TCLKB, ADTRG0, SCK0 to SCK2, IRQ0 to IRQ3 and when these pins are selected as I/O ports	$(V_{IH})$	4.0	—	$(PV_{CC2}$	V	Refer to table 24.2
		$V_T^+$			+ 0.3)		
		$(V_{IL})$	(-0.3)	—	1.0	V	
		$V_T^-$					
Input leak current	$\overline{RES}$ , NMI, FWE, MD2 to 0, HSTBY,	$ I_{in} $	—	—	1.0	$\mu\text{A}$	$V_{in} = 0.5 \text{ V}$ to $5.5 + 0.3 \text{ V}$
	EXTAL (Standby)		—	—	1.0	$\mu\text{A}$	$V_{in} = 0.5 \text{ V}$ to $V_{CC} - 0.5 \text{ V}$
	AUDMD, AUDCK, AUDSYNC, AUDATA3 to 0 (Standby)		—	—	1.0	$\mu\text{A}$	$V_{in} = 0.5 \text{ V}$ to $PV_{CC2} - 0.5 \text{ V}$
	AUDRST (Standby)		—	—	1.0	$\mu\text{A}$	$V_{in} = 0.5 \text{ V}$ to $PV_{CC2} - 0.5 \text{ V}$
	A/D port		—	—	0.2	$\mu\text{A}$	$V_{in} = 0.5 \text{ V}$ to $AV_{CC} - 0.5 \text{ V}$

**Table 24.4 DC Characteristics (cont)**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V}/3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions	
Input leak current	D15 to D0, $\overline{WAIT}$ , $\overline{BREQ}$ (MCU expansion mode)	lin	—	—	1.0	$\mu\text{A}$ $V_{in} = 0.5 \text{ V}$ to $PV_{CC1} - 0.5 \text{ V}$ $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$	
	Other input pins	—	—	1.0	$\mu\text{A}$	$V_{in} = 0.5 \text{ V}$ to $PV_{CC2} - 0.5 \text{ V}$	
Input pull-up MOS current	AUDMD, AUDCK, AUDSYNC, AUDA3 to 0 (pull-up characteristic)	- Ipu	—	—	500	$\mu\text{A}$ $V_{in} = 0 \text{ V}$	
Input pull-down MOS current	$\overline{AUDRST}$ (pull-down characteristic)	Ipd	—	—	700	$\mu\text{A}$ $V_{in} = PV_{CC2}$	
Three-state leak current	A21 to A0, D15 to D0, $\overline{CS3}$ to $\overline{CS0}$ , $\overline{WRH}$ , $\overline{WRL}$ , $\overline{RD}$ , $\overline{BACK}$ (When in MCU expansion mode)	Its	—	—	1.0	$\mu\text{A}$ $V_{in} = 0.5 \text{ V}$ to $PV_{CC1} - 0.5 \text{ V}$ $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$	
Output high-level voltage	A21 to A0, D15 to D0, $\overline{CS3}$ to $\overline{CS0}$ , $\overline{WRH}$ , $\overline{WRL}$ , $\overline{RD}$ , $\overline{BACK}$ (When in MCU expansion mode)	$V_{OH}$	$PV_{CC1} - 0.5$	—	—	$\text{V}$ $I_{OH} = 200 \mu\text{A}$ $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$	
	PE15 to PE0, PF15 to PF0, PH15 to PH0 (When in MCU expansion mode)		$PV_{CC1} - 0.5$	—	—	$\text{V}$ $I_{OH} = 200 \mu\text{A}$ $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$	
	CK		$V_{CC} - 0.5$	—	—	$\text{V}$ $I_{OH} = 200 \mu\text{A}$	
	Other output pins			$PV_{CC} - 0.5$	—	—	$\text{V}$ $I_{OH} = 200 \mu\text{A}$
				$PV_{CC} - 1.0$	—	—	$\text{V}$ $I_{OH} = 1 \text{ mA}$

**Table 24.4 DC Characteristics (cont)**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions	
Output low-level voltage	A21 to A0, D15 to D0, $\overline{CS3}$ to $\overline{CS0}$ , $\overline{WRH}$ , $\overline{WRL}$ , $\overline{RD}$ , $\overline{BACK}$ (When in MCU expansion mode)	$V_{OL}$	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$ $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$	
	PE15 to PE0, PF15 to PF0, PH15 to PH0 (When in MCU expansion mode)		—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$ $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$	
	CK		—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$	
	Other output pins (except XTAL)		—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$	
				—	—	1.2	V	$I_{OL} = 6 \text{ mA}$
Input capacitance	$\overline{RES}$	$C_{in}$	—	—	60	pF	$V_{in} = 0 \text{ V}$ $f = 1 \text{ MHz}$	
	NMI		—	—	30	pF	$T_a = 25^\circ\text{C}$	
	All other input pins		—	—	20	pF		
Current consumption	Normal operation	$I_{CC}$	—	120	170	mA	$f = 40 \text{ MHz}$	
	Sleep		—	100	150	mA		
	Standby			—	1	100	$\mu\text{A}$	$T_a \leq 50^\circ\text{C}$
				—	—	500	$\mu\text{A}$	$50^\circ\text{C} < T_a$
	Write operation		—	130	170	mA	$V_{CC} = 3.3 \text{ V}$ $f = 40 \text{ MHz}$	
Analog supply current	During A/D conversion	$AI_{CC}$	—	1.2	5	mA		
	Awaiting A/D conversion, standby		—	1.0	5	$\mu\text{A}$		

**Table 24.4 DC Characteristics (cont)**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Reference power supply current	During A/D conversions, awaiting A/D conversion	$I_{ref}$	—	1.1	5	mA	$AV_{ref} = 5 \text{ V}$
	Standby		—	1.1	5	$\mu\text{A}$	
RAM standby voltage		$V_{RAM}$	2.0	—	—	V	$V_{CC}$

**[Operating precautions]**

1. When the A/D converter is not used (including during standby), do not leave the  $AV_{CC}$ ,  $AV_{ref}$ , and  $AV_{SS}$  pins open.
2. The current consumption is measured when  $V_{IHmin} = V_{CC} - 0.5 \text{ V} / PV_{CC} - 0.5 \text{ V}$ ,  $V_{IL} = 0.5 \text{ V}$ , with all output pins unloaded.
3. The operation guaranteed voltage range of power supply  $PV_{CC1}$  in MCU expansion mode is  $3.3 \text{ V} \pm 0.3 \text{ V}$ . Do not use a voltage outside this range.
4. The operation guaranteed voltage range of power supply  $PV_{CC1}$  in MCU single-chip mode is  $5.0 \text{ V} \pm 0.5 \text{ V}$ . Do not use a voltage outside this range.

**Table 24.5 Permitted Output Current Values**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V}/3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Typ	Max	Unit
Output low-level permissible current (per pin)	$I_{OL}$	—	—	6.0	mA
Output low-level permissible current (total)	$\Sigma I_{OL}$	—	—	80	mA
Output high-level permissible current (per pin)	$I_{OH}$	—	—	2.0	mA
Output high-level permissible current (total)	$\Sigma I_{OL}$	—	—	25	mA

**[Operating precautions]**

To assure LSI reliability, do not exceed the output values listed in this table.

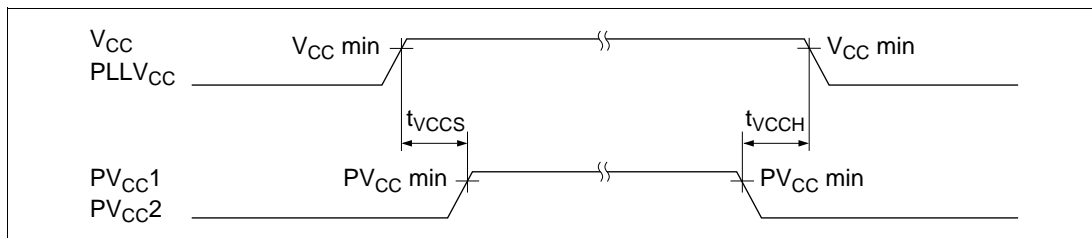
## 24.3 AC Characteristics

### 24.3.1 Power-On/Off Timing

**Table 24.6 Power-On/Off Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $PV_{CC1} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  
 $PV_{CC2} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{ref} = 4.5\text{ V to } AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40^\circ\text{C to } 85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C to } 85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figure
$V_{CC}$ lead power-on time	$t_{VCCS}$	0	—	ms	Figure 24.1
$V_{CC}$ hold time from $PV_{CC}$ cut-off	$t_{VCCH}$	0	—	ms	



**Figure 24.1 Power-On/Off Timing**

## 24.3.2 Clock Timing

Table 24.7 shows the clock timing.

**Table 24.7 Clock Timing**

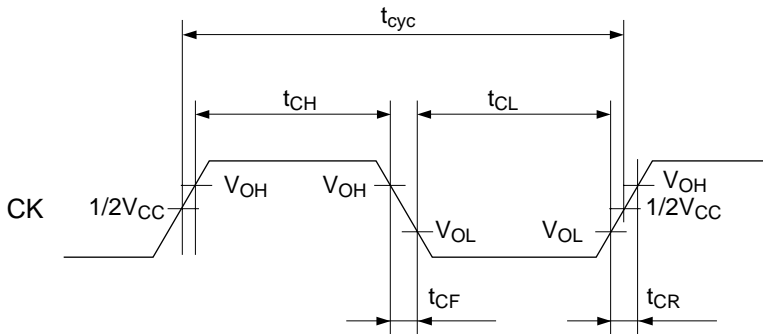
Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
Operating frequency	$f_{op}$	20	40	MHz	Figure 24.2
Clock cycle time	$t_{cyc}$	25	50	ns	
Clock low-level pulse width	$t_{CL}$	4	—	ns	
Clock high-level pulse width	$t_{CH}$	4	—	ns	
Clock rise time	$t_{CR}$	—	8	ns	
Clock fall time	$t_{CF}$	—	8	ns	
EXTAL clock input frequency	$f_{EX}$	5	10	MHz	Figure 24.3
EXTAL clock input cycle time	$t_{EXCyc}$	100	200	ns	
EXTAL clock input low-level pulse width	$t_{EXL}$	30	—	ns	
EXTAL clock input high-level pulse width	$t_{EXH}$	30	—	ns	
EXTAL clock input rise time	$t_{EXR}$	—	8	ns	
EXTAL clock input fall time	$t_{EXF}$	—	8	ns	
Reset oscillation settling time	$t_{osc1}$	30	—	ms	Figure 24.4
Standby return clock settling time	$t_{osc2}$	30	—	ms	

### [Operating precautions]

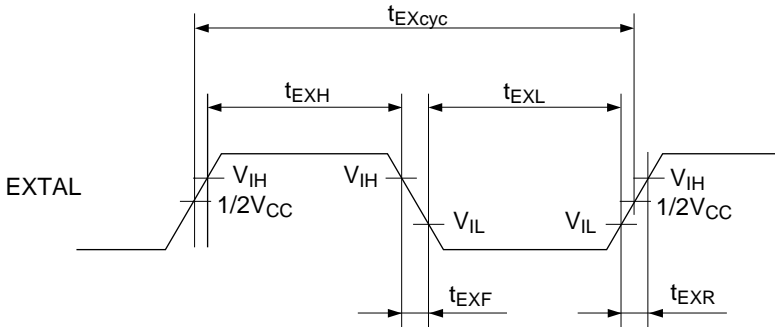
The EXTAL, XTAL, and CK pins constitute a circuit requiring a power supply voltage of  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ . Comply with the input and output voltages specified in the DC characteristics.





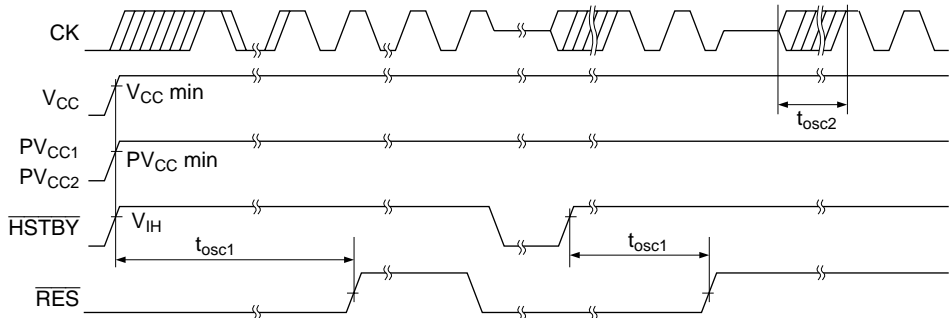
Note: CK pin is  $V_{CC} = 3.3V \pm 0.3V$  power supply circuit.

**Figure 24.2 System Clock Timing**



Note: EXTAL pin is  $V_{CC} = 3.3V \pm 0.3V$  power supply circuit.

**Figure 24.3 EXTAL Clock Input Timing**



**Figure 24.4 Oscillation Settling Time**

### 24.3.3 Control Signal Timing

Table 24.8 shows control signal timing.

**Table 24.8 Control Signal Timing**

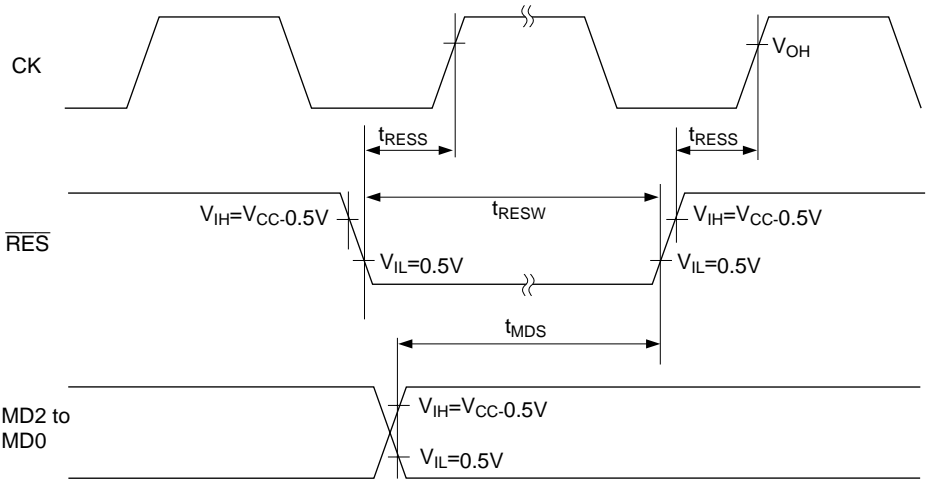
Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
$\overline{\text{RES}}$ pulse width	$t_{\text{RESW}}$	20	—	$t_{\text{cyc}}$	Figure 24.5
$\overline{\text{RES}}$ setup time	$t_{\text{RESS}}$	24	—	ns	
MD2 to MD0 setup time	$t_{\text{MDS}}$	20	—	$t_{\text{cyc}}$	Figure 24.6
NMI setup time	$t_{\text{NMIS}}$	24	—	ns	
$\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ setup time* <sup>1</sup> (edge detection)	$t_{\text{IRQES}}$	24	—	ns	
$\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ setup time* <sup>1</sup> (level detection)	$t_{\text{IRQLS}}$	24	—	ns	
NMI hold time	$t_{\text{NMIH}}$	24	—	ns	Figure 24.7
$\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$ hold time	$t_{\text{IRQEH}}$	24	—	ns	
Bus request setup time	$t_{\text{BRQS}}$	24	—	ns	
Bus acknowledge delay time 1	$t_{\text{BACKD1}}$	—	30	ns	
Bus acknowledge delay time 2	$t_{\text{BACKD2}}$	—	30	ns	
Bus three-state delay time	$t_{\text{BZD}}$	—	30	ns	

#### [Operating precautions]

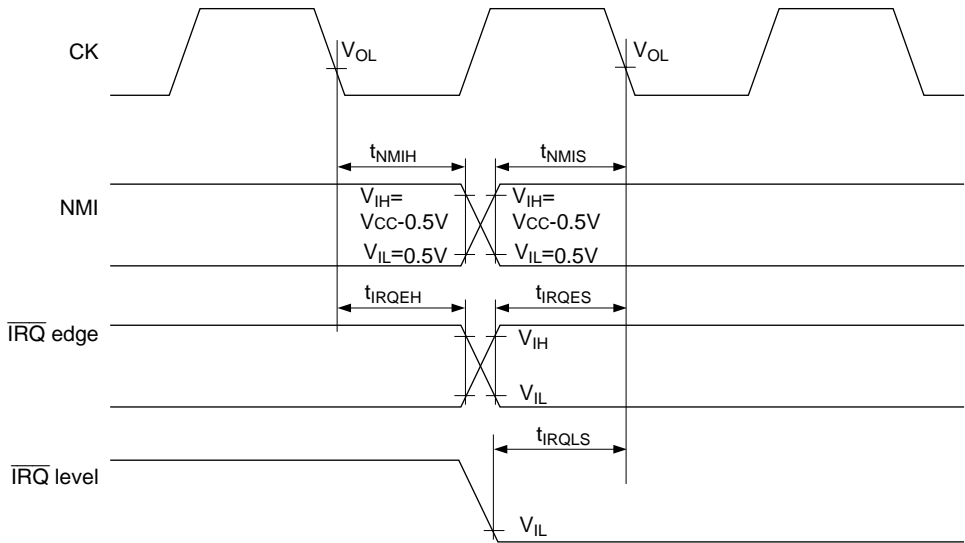
The operation guaranteed voltage range of power supply  $PV_{CC1}$  in MCU expansion mode is  $3.3 \text{ V} \pm 0.3 \text{ V}$ . Do not use a voltage outside this range.

\*1 The  $\overline{\text{RES}}$ , NMI and  $\overline{\text{IRQ3}}$  to  $\overline{\text{IRQ0}}$  signals are asynchronous inputs, but when the setup times shown here are provided, the signals are considered to have been changed at clock fall. If the setup times are not provided, recognition is delayed until the next clock rise or fall.



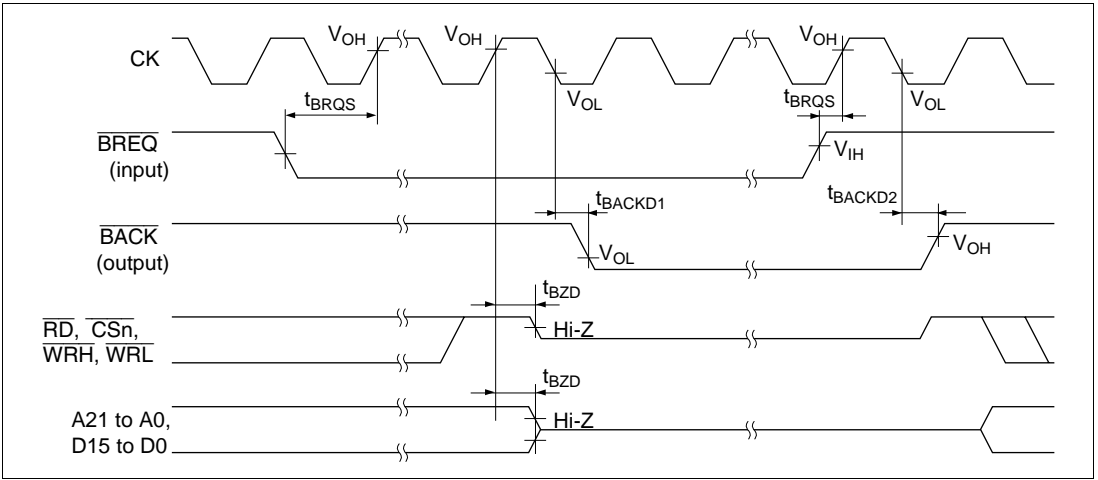
Note:  $\overline{RES}$  pin is controlled by  $V_{IL}$  and  $V_{IH}$  shown above.

**Figure 24.5 Reset Input Timing**



Note: NMI pin is controlled by  $V_{IL}$  and  $V_{IH}$  shown above.

**Figure 24.6 Interrupt Signal Input Timing**



**Figure 24.7 Bus Right Release Timing**

### 24.3.4 Bus Timing

Table 24.9 shows bus timing.

**Table 24.9 Bus Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  
 $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  
 $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .

When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
Address delay time	$t_{AD}$	—	35	ns	Figure 24.8, 24.9
CS delay time 1	$t_{CSD1}$	—	30	ns	
CS delay time 2	$t_{CSD2}$	—	30	ns	
Read strobe delay time 1	$t_{RSD1}$	—	30	ns	
Read strobe delay time 2	$t_{RSD2}$	—	30	ns	
Read data setup time	$t_{RDS}$	15	—	ns	
Read data hold time	$t_{RDH}$	0	—	ns	
Write strobe delay time 1	$t_{WSD1}$	—	30	ns	
Write strobe delay time 2	$t_{WSD2}$	—	30	ns	
Write data delay time	$t_{WDD}$	—	30	ns	
Write data hold time	$t_{WDH}$	$t_{cyc} \times m$	—	ns	
WAIT setup time	$t_{WTS}$	15	—	ns	
WAIT hold time	$t_{WTH}$	0	—	ns	Figure 24.10
Read data access time	$t_{ACC}$	$t_{cyc} \times (n+1.5) - 39$	—	ns	
Access time from read strobe	$t_{OE}$	$t_{cyc} \times (n+1.0) - 39$	—	ns	
Write address setup time	$t_{AS}$	0	—	ns	Figure 24.8, 24.9
Write address hold time	$t_{WR}$	5	—	ns	

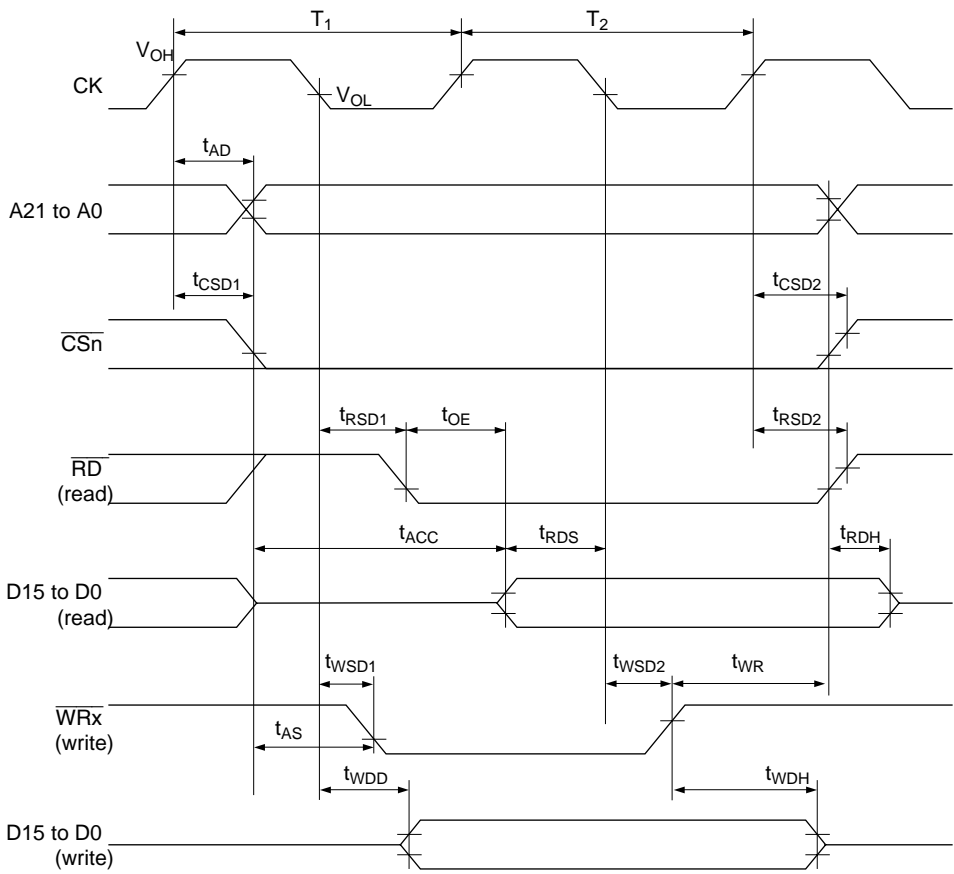
n: Number of waits

m = 1: CS assertion extension cycle

m = 0: Ordinary cycle (CS assertion non-extension cycle)

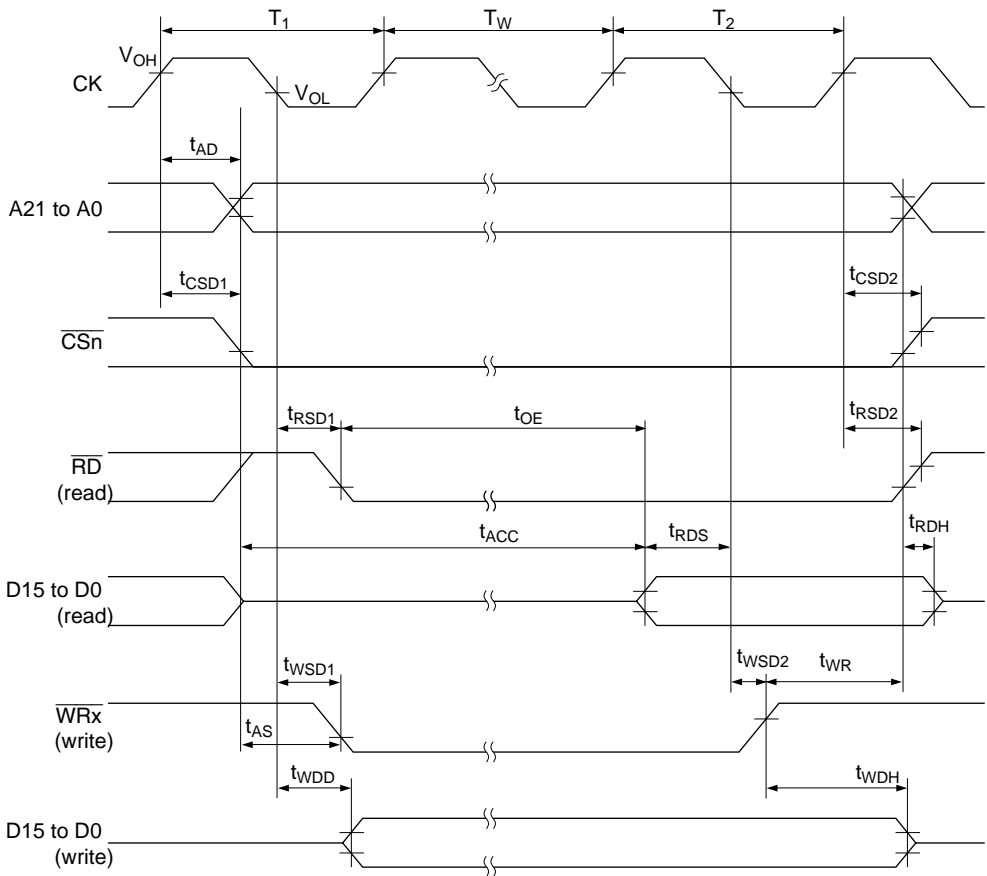
#### [Operating precautions]

The operation guaranteed voltage range of power supply  $PV_{CC1}$  in MCU expansion mode is  $3.3 \text{ V} \pm 0.3 \text{ V}$ . Do not use a voltage outside this range.



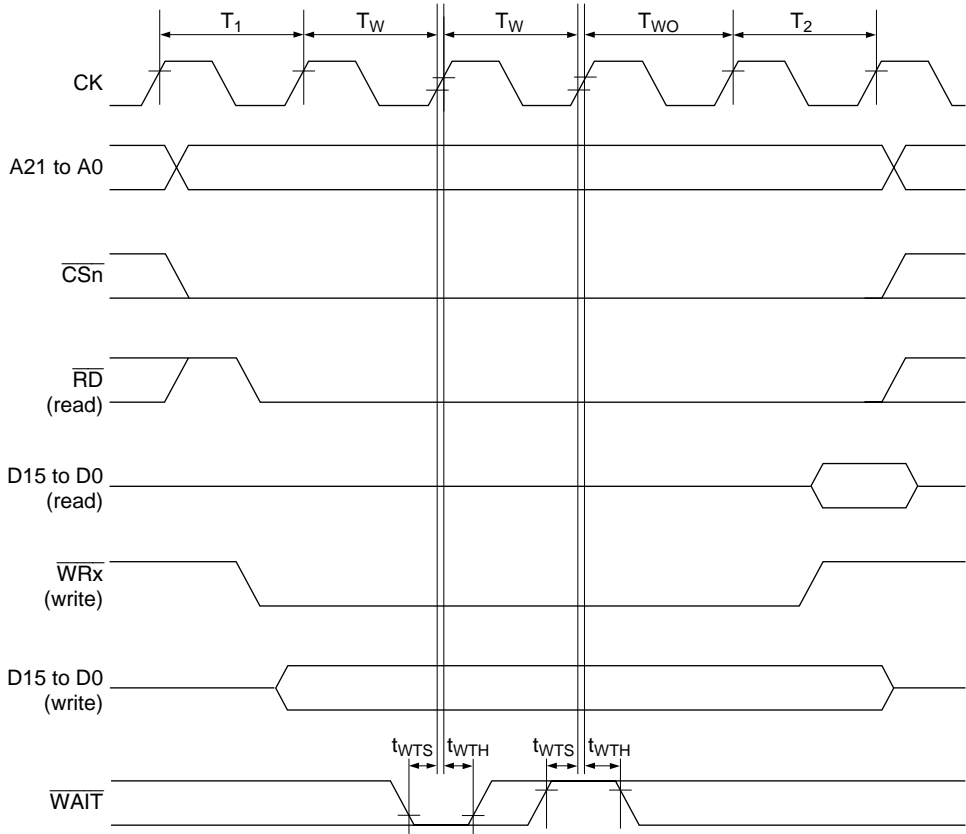
Note:  $t_{RDH}$ : Specified from the negate timing of A21–A0,  $\overline{CSn}$ , or  $\overline{RD}$ , whichever is first.

**Figure 24.8 Basic Cycle (No Waits)**



Note:  $t_{RDH}$ : Specified from the negate timing of A21–A0,  $\overline{CSn}$ , or  $\overline{RD}$ , whichever is first.

**Figure 24.9 Basic Cycle (One Software Wait)**



Note:  $t_{RDH}$ : Specified from the negate timing of A21–A0,  $\overline{CSn}$ , or  $\overline{RD}$ , whichever is first.

**Figure 24.10 Basic Cycle (Two Software Waits + Waits by  $\overline{WAIT}$  Signal)**



### 24.3.5 Advanced Timer Unit Timing and Advance Pulse Controller Timing

Table 24.10 shows advanced timer unit timing and advanced pulse controller timing.

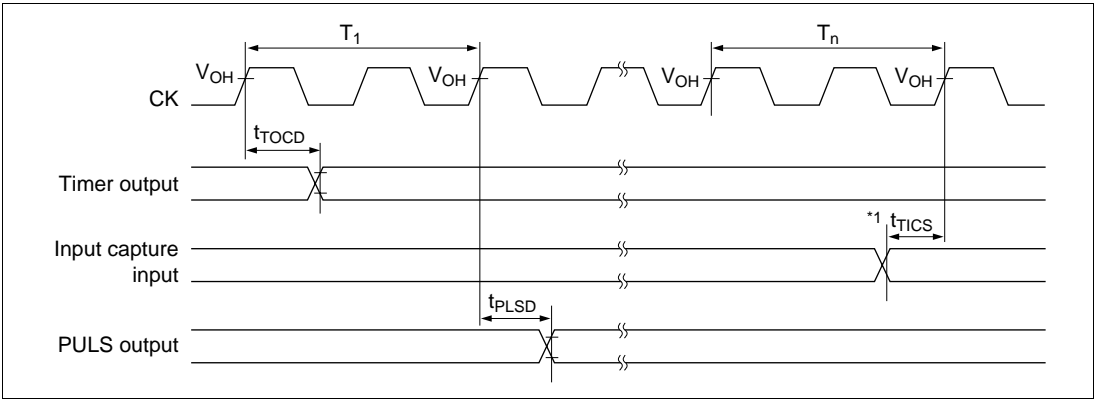
**Table 24.10 Advanced Timer Unit Timing and Advanced Pulse Controller Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

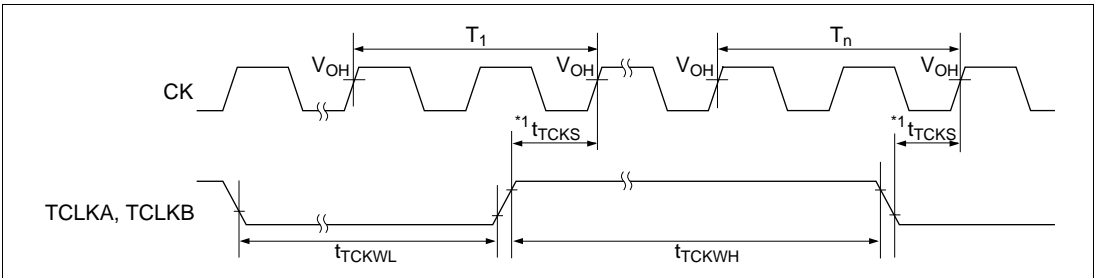
Item	Symbol	Min	Max	Unit	Figures
Output compare output delay time	$t_{TOCD}$	—	100	ns	Figure 24.11
Input capture input setup time	$t_{TICS}$	$24^{*1}$ $24 + t_{cyc}$	—	ns	
PULS output delay time	$t_{PLSD}$	—	100	ns	Figure 24.12
Timer clock input setup time	$t_{TCKS}$	$24^{*1}$ $24 + t_{cyc}$	—	ns	
Timer clock pulse width (single edge specified)	$t_{TCKWH/L}$	3.0	—	$t_{cyc}$	
Timer clock pulse width (both edges specified)	$t_{TCKWH/L}$	5.0	—	$t_{cyc}$	

#### [Operating precautions]

\*1 The timer input signals and timer clock input signals are asynchronous, but judged to have been changed at clock rise with two-state intervals shown in figures 24.11 and 24.12. If the setup times shown here are not provided, recognition is delayed until the clock rise two states after that timing.



**Figure 24.11 ATU Input/Output timing and APC Output timing**



**Figure 24.12 ATU Input timing**

### 24.3.6 I/O Port Timing

Table 24.11 shows I/O port timing.

**Table 24.11 I/O Port Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $PV_{CC1} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $PV_{CC2} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  
 $AV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{ref} = 4.5\text{ V}$  to  $AV_{CC}$ ,  $V_{SS} = PLLV_{SS} = AV_{SS} = 0\text{ V}$ ,  
 $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

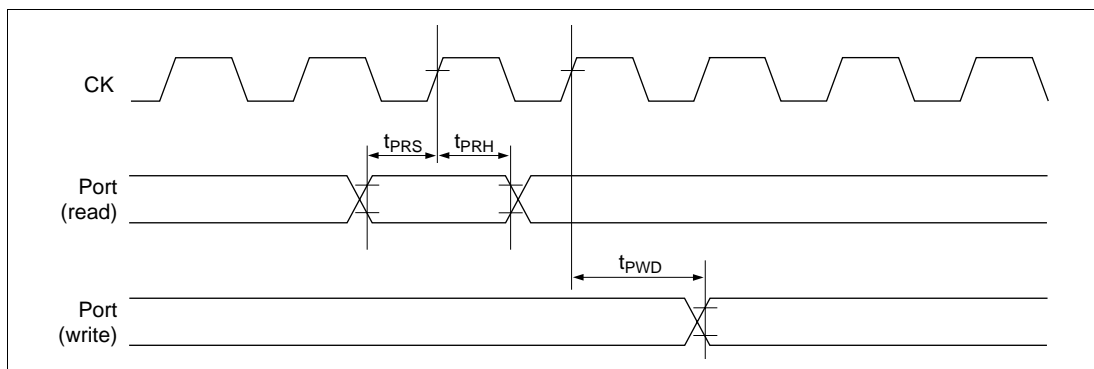
When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
Port output data delay time	$t_{PVD}$	—	100	ns	Figure 24.13
Port input hold time	$t_{PRH}$	$24^{*1}$ $24+t_{cyc}$	—	ns	
Port input setup time	$t_{PRS}$	$24^{*1}$ $24+t_{cyc}$	—	ns	

#### [Operating precautions]

The operation guaranteed voltage range of power supply  $PV_{CC1}$  in MCU single-chip mode is  $5.0\text{ V} \pm 0.5\text{ V}$ . Do not use a voltage outside this range.

\*1 The port input signals are asynchronous, but judged to have been changed at CK clock rise with two-state intervals shown in figure 24.13. If the setup times shown here are not provided, recognition is delayed until the clock rise two states after that timing.



**Figure 24.13 I/O Port Input/Output timing**

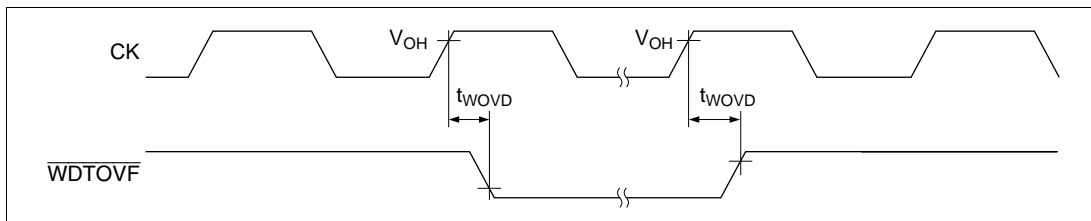
### 24.3.7 Watchdog Timer Timing

Table 24.12 shows watchdog timer timing.

**Table 24.12 Watchdog Timer Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
WDTOVF delay time	$t_{WOVD}$	—	100	ns	Figure 24.14



**Figure 24.14 Watchdog Timer Timing**

## 24.3.8 Serial Communication Interface Timing

Table 24.13 shows serial communication interface timing.

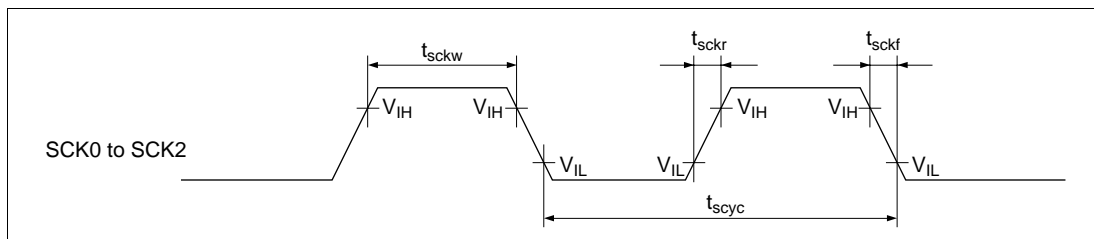
**Table 24.13 Serial Communication Interface Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $PV_{CC1} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  
 $PV_{CC2} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{ref} = 4.5\text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

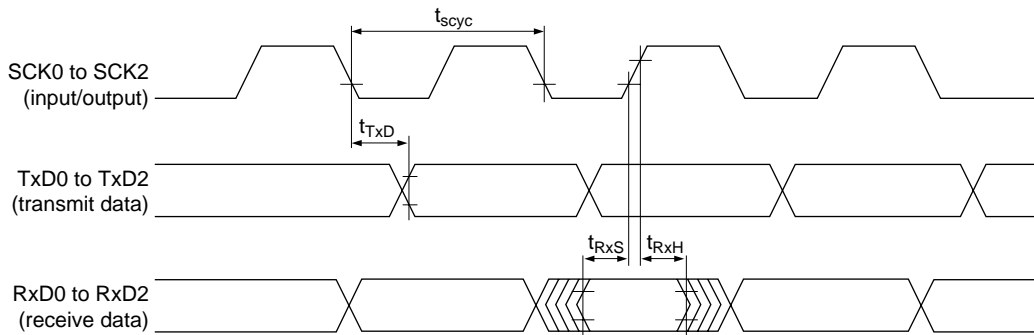
Item	Symbol	Min	Max	Unit	Figures
Clock cycle	$t_{scyc}$	8	—	$t_{cyc}$	Figure 24.15
Clock cycle (clock sync)	$t_{scyc}$	12	—	$t_{cyc}$	
Clock pulse width	$t_{sckw}$	0.4	0.6	$t_{scyc}$	
Input clock rise time	$t_{sckr}$	—	3.0	$t_{cyc}$	
Input clock fall time	$t_{sckf}$	—	3.0	$t_{cyc}$	
Transmit data delay time	$t_{TxD}$	—	100	ns	Figure 24.16
Receive data setup time	$t_{RxS}$	100	—	ns	
Receive data hold time	$t_{RxH}$	100	—	ns	

### [Operating precautions]

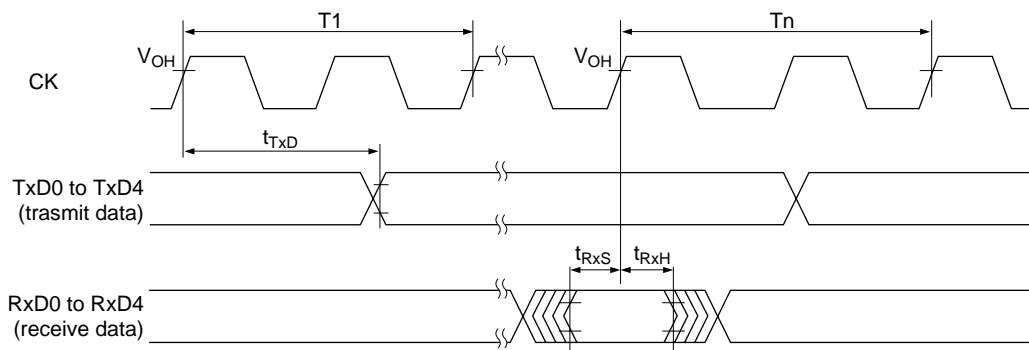
The inputs and outputs are asynchronous in start-stop synchronous mode, but as shown in figure 24.16, the receive data are judged to have been changed at CK clock rise (two-clock intervals). The transmit signals change with a reference of CK clock rise (two-clock intervals).



**Figure 24.15 SCI Input/Output Timing**



SCI input/output timing (clock synchronous mode)



SCI input/output timing (start-stop synchronous mode)

**Figure 24.16 SCI Input/Output Timing**

## 24.3.9 HCAN Timing

Table 24.14 shows HCAN timing.

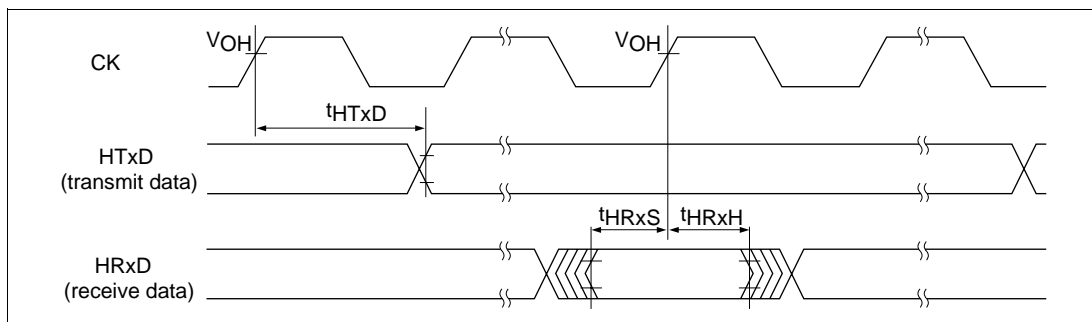
**Table 24.14 HCAN Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V}/3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
Transmit data delay time	$t_{HTxD}$	—	100	ns	Figure 24.17
Receive data setup time	$t_{HRxS}$	100	—	ns	
Receive data hold time	$t_{HRxH}$	100	—	ns	

### [Operating precautions]

The HCAN input signals are asynchronous, but judged to have been changed at CK clock rise (two-clock intervals) shown in figure 24.17. The HCAN output signals are asynchronous, but they change with a reference of CK clock rise (two-clock intervals) shown in figure 24.17.



**Figure 24.17 HCAN Input/Output timing**

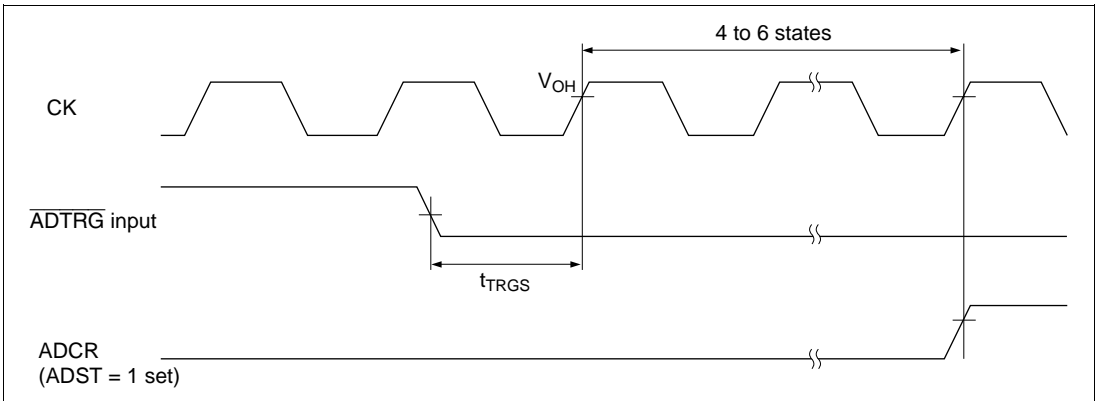
### 24.3.10 A/D Converter Timing

Table 24.15 shows A/D converter timing.

**Table 24.15 A/D Converter Timing**

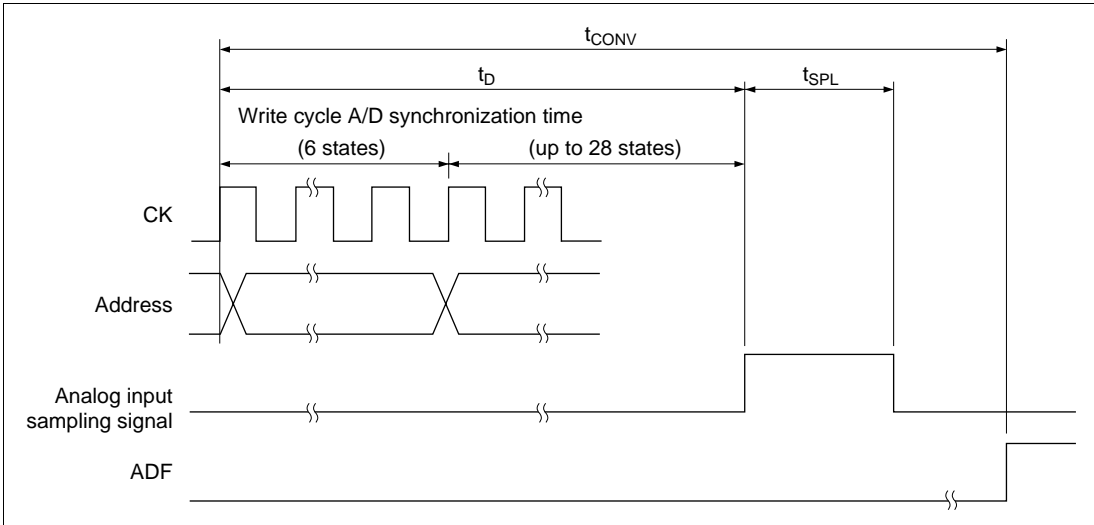
Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V}/3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	CSK = 0: fop = 20 to 40 MHz			CSK = 1: fop = 20 MHz			Unit	Figure
		Min	Typ	Max	Min	Typ	Max		
External trigger input start delay time	$t_{TRGS}$	50	—	—	50	—	—	ns	Figure 24.18
A/D conversion time	$t_{CONV}$	518	—	532	262	—	268	$t_{cyc}$	Figure 24.19
A/D conversion start delay time	$t_D$	20	—	34	12	—	18	$t_{cyc}$	
Input sampling time	$t_{SPL}$	—	128	—	—	64		$t_{cyc}$	



**Figure 24.18 External Trigger Input Timing**





**Figure 24.19 Analog Conversion Timing**

### 24.3.11 AUD Timing

Table 24.16 shows AUD timing.

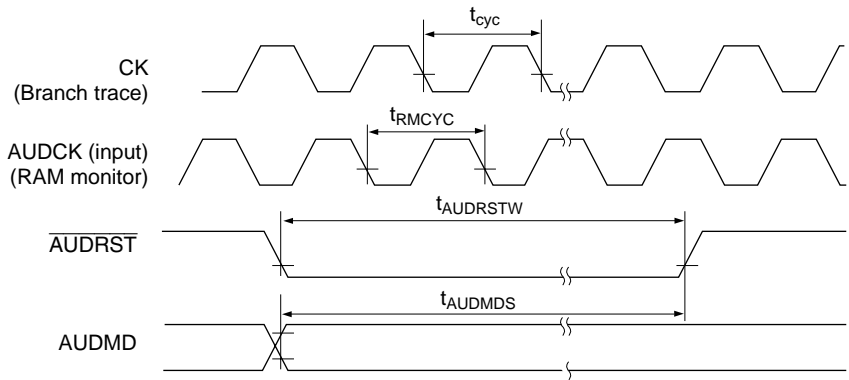
**Table 24.16 AUD Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $PV_{CC1} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  
 $PV_{CC2} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ,  $AV_{ref} = 4.5\text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

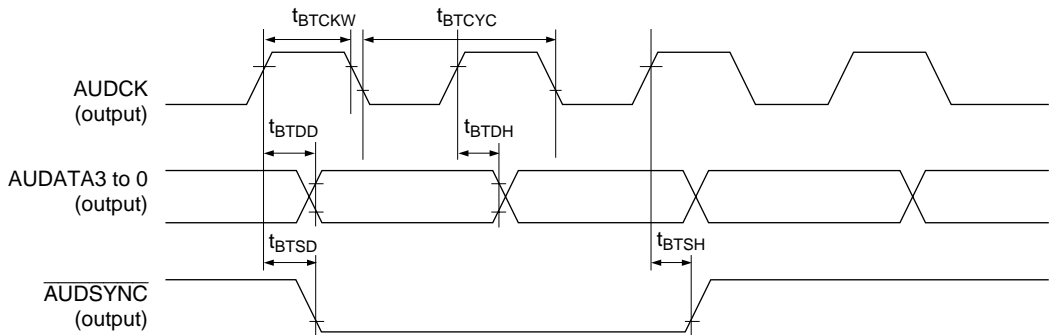
Item	Symbol	Min	Max	Unit	Figures
AUDRST $\bar$ pulse width (Branch trace mode)	$t_{AUDRSTW}$	20	—	$t_{cyc}$	Figure 24.20
AUDRST $\bar$ pulse width (RAM monitor mode)	$t_{AUDRSTW}$	5	—	$t_{RMCYC}$	
AUDMD setup time (Branch trace mode)	$t_{AUDMDS}$	20	—	$t_{cyc}$	
AUDMD setup time (RAM monitor mode)	$t_{AUDMDS}$	5	—	$t_{RMCYC}$	
Branch trace clock cycle	$t_{RTCYC}$	2	2	$t_{cyc}$	Figure 24.21
Branch trace clock duty	$t_{RTCKW}$	40	60	%	
Branch trace data delay time	$t_{RTDD}$	—	40	ns	
Branch trace data hold time	$t_{RTDH}$	0	—	ns	
Branch trace SYNC delay time	$t_{RTSD}$	—	40	ns	
Branch trace SYNC hold time	$t_{RTSH}$	0	—	ns	
RAM monitor clock cycle	$t_{RMCYC}$	100	—	ns	Figure 24.22
RAM monitor clock low pulse width	$t_{RMCKW}$	45	—	ns	
RAM monitor output data delay time	$t_{RMDD}$	7	$t_{RMCYC} - 20$	ns	
RAM monitor output data hold time	$t_{RMDHD}$	5	—	ns	
RAM monitor input data setup time	$t_{RMDS}$	20	—	ns	
RAM monitor input data hold time	$t_{RMDH}$	5	—	ns	
RAM monitor SYNC setup time	$t_{RMSS}$	20	—	ns	
RAM monitor SYNC hold time	$t_{RMSH}$	5	—	ns	

Load conditions: AUDCK (in branch trace):  $C_L = 30\text{ pF}$ : Other than above  $C_L = 100\text{ pF}$

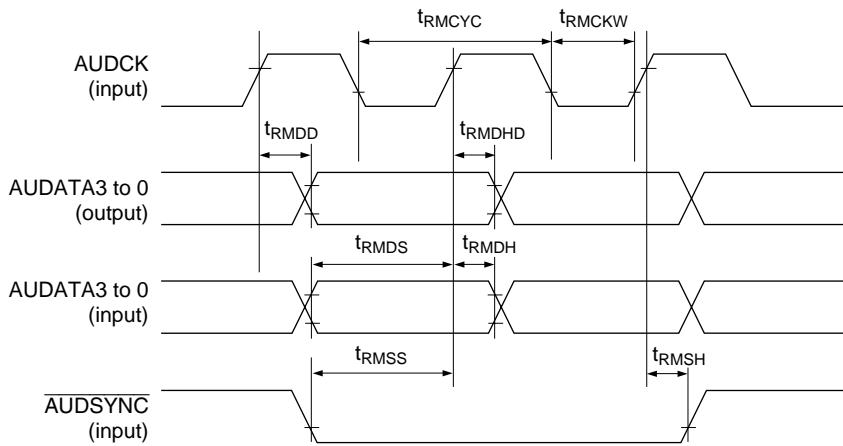
AUDSYNC, AUDATA3 to AUDATA0:  $C_L = 100\text{ pF}$



**Figure 24.20 AUD Reset Timing**



**Figure 24.21 Branch Trace Mode Timing**



**Figure 24.22 RAM Monitor Mode Timing**

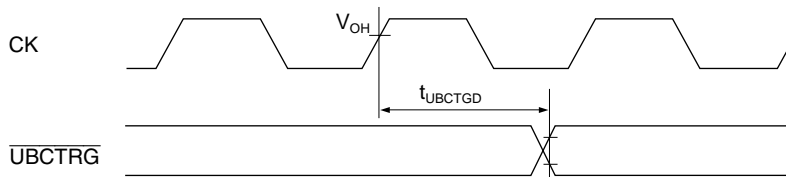
### 24.3.12 UBC Trigger Timing

Table 24.17 shows UBC trigger timing.

**Table 24.17 UBC Trigger Timing**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V} / 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	Symbol	Min	Max	Unit	Figures
$\overline{UBCTR\overline{G}}$ delay time	$t_{UBCTGD}$	—	35	ns	Figure 24.23

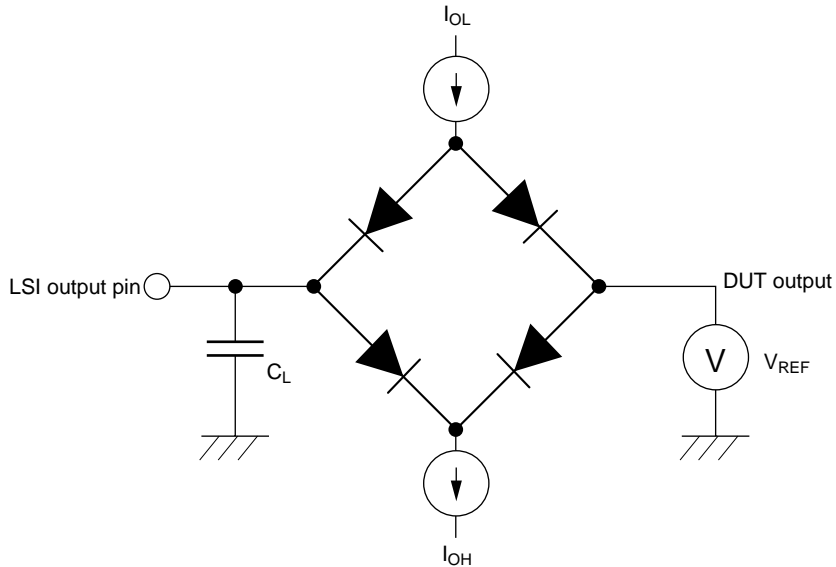


**Figure 24.23 UBC Trigger Timing**

### 24.3.13 Measuring Conditions for AC Characteristics

Input reference levels      High level:  $V_{IH}$  min. value, Low level:  $V_{IL}$  max. value

Output reference level      High level: 2.0 V, Low level: 0.8 V



$C_L$  is a total value that includes the measuring instrument capacitance.

The following  $C_L$  values are used:

30 pF:  $\overline{CK}$ ,  $\overline{CS3}$  to  $\overline{CS0}$ ,  $\overline{BREQ}$ ,  $\overline{BACK}$ ,  $AUDCK$

50 pF:  $A21$  to  $A0$ ,  $D15$  to  $D0$ ,  $\overline{RD}$ ,  $\overline{WRH}$ ,  $\overline{WRL}$

100 pF:  $AUDATA3$  to  $0$ ,  $\overline{AUDSYNC}$

30 pF: All other port output pins and supporting module output pins

$I_{OL}$  and  $I_{OH}$  are the condition for the  $I_{OL} = 1.6$  mA,  $I_{OH} = 200$   $\mu$ A.

**Figure 24.24 Output Test Circuit**

## 24.4 A/D Converter Characteristics

Table 24.18 shows A/D converter characteristics.

**Table 24.18 A/D Converter Characteristics**

Conditions:  $V_{CC} = PLLV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $PV_{CC1} = 5.0 \text{ V} \pm 0.5 \text{ V}/3.3 \text{ V} \pm 0.3 \text{ V}$ ,  
 $PV_{CC2} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ ,  $AV_{ref} = 4.5 \text{ V}$  to  $AV_{CC}$ ,  
 $V_{SS} = PLLV_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .  
 When  $PV_{CC1} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{CC} = PV_{CC1}$ .  
 When writing or erasing flash EEPROM,  $T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .

Item	CSK = 0: fop = 20 to 40 MHz			CSK = 1: fop = 20 MHz			Unit
	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	bit
A/D conversion time	—	—	13.3	—	—	13.4	$\mu\text{s}$
Analog input capacitance	—	—	20	—	—	20	pF
Permitted analog signal source impedance	—	—	3	—	—	3	k $\Omega$
Non-linear error	—	—	$\pm 1.5$	—	—	$\pm 1.5$	LSB
Offset error	—	—	$\pm 1.5$	—	—	$\pm 1.5$	LSB
Full-scale error	—	—	$\pm 1.5$	—	—	$\pm 1.5$	LSB
Quantization error	—	—	$\pm 0.5$	—	—	$\pm 0.5$	LSB
Absolute error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB

# Appendix A On-Chip Supporting Module Registers

## A.1 Address

On-chip peripheral module register addresses and bit names are shown in the following table. 16-bit and 32-bit registers are shown in two and four rows of 8 bits, respectively.

**Table A.1 Address**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFFE400	MCR	MCR7	—	MCR5	—	—	MCR2	MCR1	MCR0	HCAN
H'FFFFFFE401	GSR	—	—	—	—	GSR3	GSR2	GSR1	GSR0	
H'FFFFFFE402	BCR	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0	
H'FFFFFFE403		BCR15	BCR14	BCR13	BCR12	BCR11	BCR10	BCR9	BCR8	
H'FFFFFFE404	MBCR	MBCR7	MBCR6	MBCR5	MBCR4	MBCR3	MBCR2	MBCR1	—	
H'FFFFFFE405		MBCR15	MBCR14	MBCR13	MBCR12	MBCR11	MBCR10	MBCR9	MBCR8	
H'FFFFFFE406	TXPR	TXPR7	TXPR6	TXPR5	TXPR4	TXPR3	TXPR2	TXPR1	—	
H'FFFFFFE407		TXPR15	TXPR14	TXPR13	TXPR12	TXPR11	TXPR10	TXPR9	TXPR8	
H'FFFFFFE408	TXCR	TXCR7	TXCR6	TXCR5	TXCR4	TXCR3	TXCR2	TXCR1	—	
H'FFFFFFE409		TXCR15	TXCR14	TCR13	TXCR12	TXCR11	TSCR10	TXCR9	TXCR8	
H'FFFFFFE40A	TXACK	TXACK7	TXACK6	TXACK5	TXACK4	TXACK3	TXACK2	TXACK1	—	
H'FFFFFFE40B		TXACK15	TXACK14	TXACK13	TXACK12	TXACK11	TXACK10	TXACK9	TXACK8	
H'FFFFFFE40C	ABACK	ABACK7	ABACK6	ABACK5	ABACK4	ABACK3	ABACK2	ABACK1	—	
H'FFFFFFE40D		ABACK15	ABACK14	ABACK13	ABACK12	ABACK11	ABACK10	ABACK9	ABACK8	
H'FFFFFFE40E	RXPR	RXPR7	RXPR6	RXPR5	RXPR4	RXPR3	RXPR2	RXPR1	RXPR0	
H'FFFFFFE40F		RXPR15	RXPR14	RXPR13	RXPR12	RXPR11	RXPR10	RXPR9	RXPR8	
H'FFFFFFE410	RFPR	RFPR7	RFPR6	RFPR5	RFPR4	RFPR3	RFPR2	RFPR1	RFPR0	
H'FFFFFFE411		RFPR15	RFPR14	RFPR13	RFPR12	RFPR11	RFPR10	RFPR9	RFPR8	
H'FFFFFFE412	IRR	IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0	
H'FFFFFFE413		—	—	—	IRR12	—	—	IRR9	IRR8	
H'FFFFFFE414	MBIMR	MBIMR7	MBIMR6	MBIMR5	MBIMR4	MBIMR3	MBIMR2	MBIMR1	MBIMR0	
H'FFFFFFE415		MBIMR15	MBIMR14	MBIMR13	MBIMR12	MBIMR11	MBIMR10	MBIMR9	MBIMR8	
H'FFFFFFE416	IMR	IMR7	IMR6	IMR5	IMR4	IMR3	IMR2	IMR1	—	
H'FFFFFFE417		—	—	—	IMR12	—	—	IMR9	IMR8	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE418	REC									HCAN
H'FFFFE419	TEC									
H'FFFFE41A	UMSR	UMSR7	UMSR6	UMSR5	UMSR4	UMSR3	UMSR2	UMSR1	UMSR0	
H'FFFFE41B		UMSR15	UMSR14	UMSR13	UMSR12	UMSR11	UMSR10	UMSR9	UMSR8	
H'FFFFE41C	LAFML	LAFML7	LAFML6	LAFML5	LAFML4	LAFML3	LAFML2	LAFML1	LAFML0	
H'FFFFE41D		LAFML15	LAFML14	LAFML13	LAFML12	LAFML11	LAFML10	LAFML9	LAFML8	
H'FFFFE41E	LAFMH	LAFMH7	LAFMH6	LAFMH5	—	—	—	LAFMH1	LAFMH0	
H'FFFFE41F		LAFMH15	LAFMH14	LAFMH13	LAFMH12	LAFMH11	LAFMH10	LAFMH9	LAFMH8	
H'FFFFE420	MC0[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE421	MC0[2]									
H'FFFFE422	MC0[3]									
H'FFFFE423	MC0[4]									
H'FFFFE424	MC0[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE425	MC0[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE426	MC0[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE427	MC0[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE428	MC1[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE429	MC1[2]									
H'FFFFE42A	MC1[3]									
H'FFFFE42B	MC1[4]									
H'FFFFE42C	MC1[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE42D	MC1[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE42E	MC1[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE42F	MC1[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE430	MC2[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE431	MC2[2]									
H'FFFFE432	MC2[3]									
H'FFFFE433	MC2[4]									
H'FFFFE434	MC2[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE435	MC2[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	



**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE436	MC2[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	HCAN
H'FFFFE437	MC2[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE438	MC3[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE439	MC3[2]									
H'FFFFE43A	MC3[3]									
H'FFFFE43B	MC3[4]									
H'FFFFE43C	MC3[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE43D	MC3[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE43E	MC3[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE43F	MC3[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE440	MC4[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE441	MC4[2]									
H'FFFFE442	MC4[3]									
H'FFFFE443	MC4[4]									
H'FFFFE444	MC4[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE445	MC4[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE446	MC4[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE447	MC4[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE448	MC5[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE449	MC5[2]									
H'FFFFE44A	MC5[3]									
H'FFFFE44B	MC5[4]									
H'FFFFE44C	MC5[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE44D	MC5[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE44E	MC5[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE44F	MC5[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE450	MC6[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE451	MC6[2]									
H'FFFFE452	MC6[3]									
H'FFFFE453	MC6[4]									

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE454	MC6[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	HCAN
H'FFFFE455	MC6[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE456	MC6[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE457	MC6[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE458	MC7[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE459	MC7[2]									
H'FFFFE45A	MC7[3]									
H'FFFFE45B	MC7[4]									
H'FFFFE45C	MC7[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE45D	MC7[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE45E	MC7[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE45F	MC7[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE460	MC8[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE461	MC8[2]									
H'FFFFE462	MC8[3]									
H'FFFFE463	MC8[4]									
H'FFFFE464	MC8[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE465	MC8[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE466	MC8[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE467	MC8[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE468	MC9[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE469	MC9[2]									
H'FFFFE46A	MC9[3]									
H'FFFFE46B	MC9[4]									
H'FFFFE46C	MC9[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE46D	MC9[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE46E	MC9[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE46F	MC9[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE470	MC10[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE471	MC10[2]									

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE472	MC10[3]									HCAN
H'FFFFE473	MC10[4]									
H'FFFFE474	MC10[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE475	MC10[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE476	MC10[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE477	MC10[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE478	MC11[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE479	MC11[2]									
H'FFFFE47A	MC11[3]									
H'FFFFE47B	MC11[4]									
H'FFFFE47C	MC11[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE47D	MC11[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE47E	MC11[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE47F	MC11[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE480	MC12[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE481	MC12[2]									
H'FFFFE482	MC12[3]									
H'FFFFE483	MC12[4]									
H'FFFFE484	MC12[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE485	MC12[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE486	MC12[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE487	MC12[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE488	MC13[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE489	MC13[2]									
H'FFFFE48A	MC13[3]									
H'FFFFE48B	MC13[4]									
H'FFFFE48C	MC13[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE48D	MC13[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE48E	MC13[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE48F	MC13[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE490	MC14[1]					DLC3	DLC2	DLC1	DLC0	HCAN
H'FFFFE491	MC14[2]									
H'FFFFE492	MC14[3]									
H'FFFFE493	MC14[4]									
H'FFFFE494	MC14[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE495	MC14[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE496	MC14[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE497	MC14[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE498	MC15[1]					DLC3	DLC2	DLC1	DLC0	
H'FFFFE499	MC15[2]									
H'FFFFE49A	MC15[3]									
H'FFFFE49B	MC15[4]									
H'FFFFE49C	MC15[5]	STD_ID2	STD_ID1	STD_ID0	RTR	IDE		EXD_ID17	EXD_ID16	
H'FFFFE49D	MC15[6]	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3	
H'FFFFE49E	MC15[7]	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0	
H'FFFFE49F	MC15[8]	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8	
H'FFFFE4A0	—	—	—	—	—	—	—	—	—	
to										
H'FFFFE4AF										
H'FFFFE4B0	MD0[1]	MSG_DATA_1								
H'FFFFE4B1	MD0[2]	MSG_DATA_2								
H'FFFFE4B2	MD0[3]	MSG_DATA_3								
H'FFFFE4B3	MD0[4]	MSG_DATA_4								
H'FFFFE4B4	MD0[5]	MSG_DATA_5								
H'FFFFE4B5	MD0[6]	MSG_DATA_6								
H'FFFFE4B6	MD0[7]	MSG_DATA_7								
H'FFFFE4B7	MD0[8]	MSG_DATA_8								
H'FFFFE4B8	MD1[1]	MSG_DATA_1								
H'FFFFE4B9	MD1[2]	MSG_DATA_2								
H'FFFFE4BA	MD1[3]	MSG_DATA_3								
H'FFFFE4BB	MD1[4]	MSG_DATA_4								

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE4BC	MD1[5]	MSG_DATA_5								HCAN
H'FFFFE4BD	MD1[6]	MSG_DATA_6								
H'FFFFE4BE	MD1[7]	MSG_DATA_7								
H'FFFFE4BF	MD1[8]	MSG_DATA_8								
H'FFFFE4C0	MD2[1]	MSG_DATA_1								
H'FFFFE4C1	MD2[2]	MSG_DATA_2								
H'FFFFE4C2	MD2[3]	MSG_DATA_3								
H'FFFFE4C3	MD2[4]	MSG_DATA_4								
H'FFFFE4C4	MD2[5]	MSG_DATA_5								
H'FFFFE4C5	MD2[6]	MSG_DATA_6								
H'FFFFE4C6	MD2[7]	MSG_DATA_7								
H'FFFFE4C7	MD2[8]	MSG_DATA_8								
H'FFFFE4C8	MD3[1]	MSG_DATA_1								
H'FFFFE4C9	MD3[2]	MSG_DATA_2								
H'FFFFE4CA	MD3[3]	MSG_DATA_3								
H'FFFFE4CB	MD3[4]	MSG_DATA_4								
H'FFFFE4CC	MD3[5]	MSG_DATA_5								
H'FFFFE4CD	MD3[6]	MSG_DATA_6								
H'FFFFE4CE	MD3[7]	MSG_DATA_7								
H'FFFFE4CF	MD3[8]	MSG_DATA_8								
H'FFFFE4D0	MD4[1]	MSG_DATA_1								
H'FFFFE4D1	MD4[2]	MSG_DATA_2								
H'FFFFE4D2	MD4[3]	MSG_DATA_3								
H'FFFFE4D3	MD4[4]	MSG_DATA_4								
H'FFFFE4D4	MD4[5]	MSG_DATA_5								
H'FFFFE4D5	MD4[6]	MSG_DATA_6								
H'FFFFE4D6	MD4[7]	MSG_DATA_7								
H'FFFFE4D7	MD4[8]	MSG_DATA_8								
H'FFFFE4D8	MD5[1]	MSG_DATA_1								
H'FFFFE4D9	MD5[2]	MSG_DATA_2								

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module	
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
H'FFFFE4DA	MD5[3]	MSG_DATA_3									HCAN
H'FFFFE4DB	MD5[4]	MSG_DATA_4									
H'FFFFE4DC	MD5[5]	MSG_DATA_5									
H'FFFFE4DD	MD5[6]	MSG_DATA_6									
H'FFFFE4DE	MD5[7]	MSG_DATA_7									
H'FFFFE4DF	MD5[8]	MSG_DATA_8									
H'FFFFE4E0	MD6[1]	MSG_DATA_1									
H'FFFFE4E1	MD6[2]	MSG_DATA_2									
H'FFFFE4E2	MD6[3]	MSG_DATA_3									
H'FFFFE4E3	MD6[4]	MSG_DATA_4									
H'FFFFE4E4	MD6[5]	MSG_DATA_5									
H'FFFFE4E5	MD6[6]	MSG_DATA_6									
H'FFFFE4E6	MD6[7]	MSG_DATA_7									
H'FFFFE4E7	MD6[8]	MSG_DATA_8									
H'FFFFE4E8	MD7[1]	MSG_DATA_1									
H'FFFFE4E9	MD7[2]	MSG_DATA_2									
H'FFFFE4EA	MD7[3]	MSG_DATA_3									
H'FFFFE4EB	MD7[4]	MSG_DATA_4									
H'FFFFE4EC	MD7[5]	MSG_DATA_5									
H'FFFFE4ED	MD7[6]	MSG_DATA_6									
H'FFFFE4EE	MD7[7]	MSG_DATA_7									
H'FFFFE4EF	MD7[8]	MSG_DATA_8									
H'FFFFE4F0	MD8[1]	MSG_DATA_1									
H'FFFFE4F1	MD8[2]	MSG_DATA_2									
H'FFFFE4F2	MD8[3]	MSG_DATA_3									
H'FFFFE4F3	MD8[4]	MSG_DATA_4									
H'FFFFE4F4	MD8[5]	MSG_DATA_5									
H'FFFFE4F5	MD8[6]	MSG_DATA_6									
H'FFFFE4F6	MD8[7]	MSG_DATA_7									
H'FFFFE4F7	MD8[8]	MSG_DATA_8									

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFE4F8	MD9[1]	MSG_DATA_1								HCAN
H'FFFFE4F9	MD9[2]	MSG_DATA_2								
H'FFFFE4FA	MD9[3]	MSG_DATA_3								
H'FFFFE4FB	MD9[4]	MSG_DATA_4								
H'FFFFE4FC	MD9[5]	MSG_DATA_5								
H'FFFFE4FD	MD9[6]	MSG_DATA_6								
H'FFFFE4FE	MD9[7]	MSG_DATA_7								
H'FFFFE4FF	MD9[8]	MSG_DATA_8								
H'FFFFE500	MD10[1]	MSG_DATA_1								
H'FFFFE501	MD10[2]	MSG_DATA_2								
H'FFFFE502	MD10[3]	MSG_DATA_3								
H'FFFFE503	MD10[4]	MSG_DATA_4								
H'FFFFE504	MD10[5]	MSG_DATA_5								
H'FFFFE505	MD10[6]	MSG_DATA_6								
H'FFFFE506	MD10[7]	MSG_DATA_7								
H'FFFFE507	MD10[8]	MSG_DATA_8								
H'FFFFE508	MD11[1]	MSG_DATA_1								
H'FFFFE509	MD11[2]	MSG_DATA_2								
H'FFFFE50A	MD11[3]	MSG_DATA_3								
H'FFFFE50B	MD11[4]	MSG_DATA_4								
H'FFFFE50C	MD11[5]	MSG_DATA_5								
H'FFFFE50D	MD11[6]	MSG_DATA_6								
H'FFFFE50E	MD11[7]	MSG_DATA_7								
H'FFFFE50F	MD11[8]	MSG_DATA_8								
H'FFFFE510	MD12[1]	MSG_DATA_1								
H'FFFFE511	MD12[2]	MSG_DATA_2								
H'FFFFE512	MD12[3]	MSG_DATA_3								
H'FFFFE513	MD12[4]	MSG_DATA_4								
H'FFFFE514	MD12[5]	MSG_DATA_5								
H'FFFFE515	MD12[6]	MSG_DATA_6								

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module	
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
H'FFFFE516	MD12[7]	MSG_DATA_7									HCAN
H'FFFFE517	MD12[8]	MSG_DATA_8									
H'FFFFE518	MD13[1]	MSG_DATA_1									
H'FFFFE519	MD13[2]	MSG_DATA_2									
H'FFFFE51A	MD13[3]	MSG_DATA_3									
H'FFFFE51B	MD13[4]	MSG_DATA_4									
H'FFFFE51C	MD13[5]	MSG_DATA_5									
H'FFFFE51D	MD13[6]	MSG_DATA_6									
H'FFFFE51E	MD13[7]	MSG_DATA_7									
H'FFFFE51F	MD13[8]	MSG_DATA_8									
H'FFFFE520	MD14[1]	MSG_DATA_1									
H'FFFFE521	MD14[2]	MSG_DATA_2									
H'FFFFE522	MD14[3]	MSG_DATA_3									
H'FFFFE523	MD14[4]	MSG_DATA_4									
H'FFFFE524	MD14[5]	MSG_DATA_5									
H'FFFFE525	MD14[6]	MSG_DATA_6									
H'FFFFE526	MD14[7]	MSG_DATA_7									
H'FFFFE527	MD14[8]	MSG_DATA_8									
H'FFFFE528	MD15[1]	MSG_DATA_1									
H'FFFFE529	MD15[2]	MSG_DATA_2									
H'FFFFE52A	MD15[3]	MSG_DATA_3									
H'FFFFE52B	MD15[4]	MSG_DATA_4									
H'FFFFE52C	MD15[5]	MSG_DATA_5									
H'FFFFE52D	MD15[6]	MSG_DATA_6									
H'FFFFE52E	MD15[7]	MSG_DATA_7									
H'FFFFE52F	MD15[8]	MSG_DATA_8									
H'FFFFE530	—	—	—	—	—	—	—	—	—	—	—
to											
H'FFFFE7FF											
H'FFFFE800	FLMCR1	FWE	SWE1	ESU1	PSU1	EV1	PV1	E1	P1		FLASH
H'FFFFE801	FLMCR2	FLER	—	—	—	—	—	—	—		



**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFFE802	EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	FLASH
H'FFFFFFE803	EBR2	—	—	EB13* <sup>1</sup>	EB12* <sup>1</sup>	EB11	E10	EB9	EB8	
H'FFFFFFE804	—	—	—	—	—	—	—	—	—	—
to H'FFFFE804										
H'FFFFE800	UBARH	UBA31	UBA30	UBA29	UBA28	UBA27	UBA26	UBA25	UBA24	UBC
H'FFFFE801		UBA23	UBA22	UBA21	UBA20	UBA19	UBA18	UBA17	UBA16	
H'FFFFE802	UBARL	UBA15	UBA14	UBA13	UBA12	UBA11	UBA10	UBA9	UBA8	
H'FFFFE803		UBA7	UBA6	UBA5	UBA4	UBA3	UBA2	UBA1	UBA0	
H'FFFFE804	UBAMRH	UBM31	UBM30	UBM29	UBM28	UBM27	UBM26	UBM25	UBM24	
H'FFFFE805		UBM23	UBM22	UBM21	UBM20	UBM19	UBM18	UBM17	UBM16	
H'FFFFE806	UBAMRL	UBM15	UBM14	UBM13	UBM12	UBM11	UBM10	UBM9	UBM8	
H'FFFFE807		UBM7	UBM6	UBM5	UBM4	UBM3	UBM2	UBM1	UBM0	
H'FFFFE808	UBBR	—	—	—	—	—	—	—	—	
H'FFFFE809		CP1	CP0	ID1	ID0	RW1	RW0	SZ1	SZ0	
H'FFFFE80A	UBCR	—	—	—	—	—	—	—	—	
H'FFFFE80B		—	—	—	—	—	CKS1	CKS0	UBID	
H'FFFFE80C	—	—	—	—	—	—	—	—	—	—
to H'FFFFE80F										
H'FFFFE810	TCSR* <sup>2</sup>	OVF	WT/IT	TME	—	—	CKS2	CKS1	CKS0	WDT
H'FFFFE811	TCNT* <sup>2</sup>									
H'FFFFE812	—	—	—	—	—	—	—	—	—	
H'FFFFE813	RSTCSR* <sup>2</sup>	WOVF	RSTE	RSTS	—	—	—	—	—	
H'FFFFE814	SBYCR	SSBY	HIZ	—	—	—	—	—	—	Power-down mode
H'FFFFE815	—	—	—	—	—	—	—	—	—	—
to H'FFFFE81F										

Notes: 1. Register names differ between the SH7053F and the SH7054F. For details, see sections 20.5.4, Erase Block Register 2 (EBR2), and 21.5.4, Erase Block Register 2 (EBR2).

2. This is the read address. The write address is H'FFFFE810 for TCSR and TCNT, and H'FFFFE812 for RSTCSR. For details, see section 12.2.4, Register Access.

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFEC20	BCR1	—	—	—	—	—	—	—	—	BSC
H'FFFEC21		—	—	—	—	A3SZ	A2SZ	A1SZ	A0SZ	
H'FFFEC22	BCR2	IW31	IW30	IW21	IW20	IW11	IW10	IW01	IW00	
H'FFFEC23		CW3	CW2	CW1	CW0	SW3	SW2	SW1	SW0	
H'FFFEC24	WCR	W33	W32	W31	W30	W23	W22	W21	W20	
H'FFFEC25		W13	W12	W11	W10	W03	W02	W01	W00	
H'FFFEC26	RAMER	—	—	—	—	—	—	—	—	
H'FFFEC27		—	—	—	—	RAMS	RAM2	RAM1	RAM0	
H'FFFEC28	—	—	—	—	—	—	—	—	—	—
to										
H'FFFECAF										
H'FFFECB0	DMAOR	—	—	—	—	—	—	—	—	DMAC
H'FFFECB1		—	—	—	—	—	AE	NMIF	DME	(common)
H'FFFECB2	—	—	—	—	—	—	—	—	—	—
to										
H'FFFECBF										
H'FFFEC0	SAR0									DMAC
H'FFFEC1										(channel 0)
H'FFFEC2										
H'FFFEC3										
H'FFFEC4	DAR0									
H'FFFEC5										
H'FFFEC6										
H'FFFEC7										
H'FFFEC8	DMATCR0	—	—	—	—	—	—	—	—	
H'FFFEC9										
H'FFFECA										
H'FFFECB										
H'FFFEC0	CHCR0	—	—	—	—	—	—	—	—	
H'FFFEC0	CD	—	—	—	RS4	RS3	RS2	RS1	RS0	
H'FFFEC0	CE	—	—	SM1	SM0	—	—	DM1	DM0	
H'FFFEC0	CF	—	—	TS1	TS0	TM	IE	TE	DE	

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFECDD0	SAR1									DMAC
H'FFFECDD1										(channel 1)
H'FFFECDD2										
H'FFFECDD3										
H'FFFECDD4	DAR1									
H'FFFECDD5										
H'FFFECDD6										
H'FFFECDD7										
H'FFFECDD8	DMATCR1	—	—	—	—	—	—	—	—	
H'FFFECDD9										
H'FFFECDDA										
H'FFFECDDB										
H'FFFECDDC	CHCR1	—	—	—	—	—	—	—	—	
H'FFFECDDD		—	—	—	RS4	RS3	RS2	RS1	RS0	
H'FFFECDD E		—	—	SM1	SM0	—	—	DM1	DM0	
H'FFFECDD F		—	—	TS1	TS0	TM	IE	TE	DE	
H'FFFECDE0	SAR2									DMAC
H'FFFECDE1										(channel 2)
H'FFFECDE2										
H'FFFECDE3										
H'FFFECDE4	DAR2									
H'FFFECDE5										
H'FFFECDE6										
H'FFFECDE7										
H'FFFECDE8	DMATCR2	—	—	—	—	—	—	—	—	
H'FFFECDE9										
H'FFFECDEA										
H'FFFECDEB										

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFCECEC	CHCR2	—	—	—	—	—	—	—	RO	DMAC (channel 2)
H'FFFCECED		—	—	—	RS4	RS3	RS2	RS1	RS0	
H'FFFCECEE		—	—	SM1	SM0	—	—	DM1	DM0	
H'FFFCECEF		—	—	TS1	TS0	TM	IE	TE	DE	
H'FFFCECF0	SAR3									DMAC (channel 3)
H'FFFCECF1										
H'FFFCECF2										
H'FFFCECF3										
H'FFFCECF4	DAR3									
H'FFFCECF5										
H'FFFCECF6										
H'FFFCECF7										
H'FFFCECF8	DMATCR3	—	—	—	—	—	—	—	—	
H'FFFCECF9										
H'FFFCECFA										
H'FFFCECFB										
H'FFFCECFC	CHCR3	—	—	—	DI	—	—	—	—	
H'FFFCECFD		—	—	—	RS4	RS3	RS2	RS1	RS0	
H'FFFCECFE		—	—	SM1	SM0	—	—	DM1	DM0	
H'FFFCECFE		—	—	TS1	TS0	TM	IE	TE	DE	
H'FFFED00	IPRA									INTC
H'FFFED01										
H'FFFED02	— to	—	—	—	—	—	—	—	—	
H'FFFED03										
H'FFFED04	IPRC									
H'FFFED05										
H'FFFED06	IPRD									
H'FFFED07										
H'FFFED08	IPRE									
H'FFFED09										

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFFD0A	IPRF									INTC
H'FFFFFFD0B										
H'FFFFFFD0C	IPRG									
H'FFFFFFD0D										
H'FFFFFFD0E	IPRH									
H'FFFFFFD0F										
H'FFFFFFD10	IPRI									
H'FFFFFFD11										
H'FFFFFFD12	IPRJ									
H'FFFFFFD13										
H'FFFFFFD14	IPRK									
H'FFFFFFD15										
H'FFFFFFD16	IPRL									
H'FFFFFFD17										
H'FFFFFFD18	ICR	NMIL	—	—	—	—	—	—	NMIE	
H'FFFFFFD19		IRQ0S	IRQ1S	IRQ2S	IRQ3S	—	—	—	—	
H'FFFFFFD1A	ISR	—	—	—	—	—	—	—	—	
H'FFFFFFD1B		IRQ0F	IRQ1F	IRQ2F	IRQ3F	—	—	—	—	
H'FFFFFFD1C	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFFE										
H'FFFFFFF00	SMR0	C/ $\bar{A}$	CHR	PE	O/ $\bar{E}$	STOP	MP	CKS1	CKS0	SCI (channel 0)
H'FFFFFFF01	BRR0									
H'FFFFFFF02	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFFFFFF03	TDR0									
H'FFFFFFF04	SSR0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'FFFFFFF05	RDR0									
H'FFFFFFF06	SDCR0	—	—	—	—	DIR	—	—	—	
H'FFFFFFF07	—	—	—	—	—	—	—	—	—	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF08	SMR1	C/ $\bar{A}$	CHR	PE	O/ $\bar{E}$	STOP	MP	CKS1	CKS0	SCI (channel 1)
H'FFFFFF09	BRR1									
H'FFFFFF0A	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFFFFF0B	TDR1									
H'FFFFFF0C	SSR1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'FFFFFF0D	RDR1									
H'FFFFFF0E	SDCR1	—	—	—	—	DIR	—	—	—	
H'FFFFFF0F	—	—	—	—	—	—	—	—	—	
H'FFFFFF10	SMR2	C/ $\bar{A}$	CHR	PE	O/ $\bar{E}$	STOP	MP	CKS1	CKS0	SCI (channel 2)
H'FFFFFF11	BRR2									
H'FFFFFF12	SCR2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFFFFF13	TDR2									
H'FFFFFF14	SSR2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'FFFFFF15	RDR2									
H'FFFFFF16	SDCR2	—	—	—	—	DIR	—	—	—	
H'FFFFFF17	—	—	—	—	—	—	—	—	—	
H'FFFFFF18	SMR3	C/ $\bar{A}$	CHR	PE	O/ $\bar{E}$	STOP	MP	CKS1	CKS0	SCI (channel3)
H'FFFFFF19	BRR3									
H'FFFFFF1A	SCR3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFFFFF1B	TDR3									
H'FFFFFF1C	SSR3	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'FFFFFF1D	RDR3									
H'FFFFFF1E	SDCR3	—	—	—	—	DIR	—	—	—	
H'FFFFFF1F	—	—	—	—	—	—	—	—	—	
H'FFFFFF20	SMR4	C/ $\bar{A}$	CHR	PE	O/ $\bar{E}$	STOP	MP	CKS1	CKS0	SCI (channel 4)
H'FFFFFF21	BRR4									
H'FFFFFF22	SCR4	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFFFFF23	TDR4									
H'FFFFFF24	SSR4	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
H'FFFFFF25	RDR4									
H'FFFFFF26	SDCR4	—	—	—	—	DIR	—	—	—	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF027	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF3FF										
H'FFFFFF400	TSTR2	STR7D	STR7C	STR7B	STR7A	STR6D	STR6C	STR6B	STR6A	ATU-II
H'FFFFFF401	TSTR1	STR10	STR5	STR4	STR3	STR1B,2B	STR2A	STR1A	STR0	(common)
H'FFFFFF402	TSTR3	—	—	—	—	—	—	—	STR11	
H'FFFFFF403	—	—	—	—	—	—	—	—	—	
H'FFFFFF404	PSCR1	—	—	—	PSC1E	PSC1D	PSC1C	PSC1B	PSC1A	
H'FFFFFF405	—	—	—	—	—	—	—	—	—	
H'FFFFFF406	PSCR2	—	—	—	PSC2E	PSC2D	PSC2C	PSC2B	PSC2A	
H'FFFFFF407	—	—	—	—	—	—	—	—	—	
H'FFFFFF408	PSCR3	—	—	—	PSC3E	PSC3D	PSC3C	PSC3B	PSC3A	
H'FFFFFF409	—	—	—	—	—	—	—	—	—	
H'FFFFFF40A	PSCR4	—	—	—	PSC4E	PSC4D	PSC4C	PSC4B	PSC4A	
H'FFFFFF40B	—	—	—	—	—	—	—	—	—	
H'FFFFFF40C	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF41F										
H'FFFFFF420	ICR0DH	—	—	—	—	—	—	—	—	ATU-II
H'FFFFFF421	—	—	—	—	—	—	—	—	—	(channel 0)
H'FFFFFF422	ICR0DL	—	—	—	—	—	—	—	—	
H'FFFFFF423	—	—	—	—	—	—	—	—	—	
H'FFFFFF424	ITVRR1	—	—	—	—	ITVE9	ITVE8	ITVE7	ITVE6	
H'FFFFFF425	—	—	—	—	—	—	—	—	—	
H'FFFFFF426	ITVRR2A	ITVA13A	ITVA12A	ITVA11A	ITVA10A	ITVE13A	ITVE12A	ITVE11A	ITVE10A	
H'FFFFFF427	—	—	—	—	—	—	—	—	—	
H'FFFFFF428	ITVRR2B	ITVA13B	ITVA12B	ITVA11B	ITVA10B	ITVE13B	ITVE12B	ITVE11B	ITVE10B	
H'FFFFFF429	—	—	—	—	—	—	—	—	—	
H'FFFFFF42A	TIOR0	IO0D1	IO0D0	IO0C1	IO0C0	IO0B1	IO0B0	IO0A1	IO0A0	
H'FFFFFF42B	—	—	—	—	—	—	—	—	—	
H'FFFFFF42C	TSR0	—	—	—	—	—	—	—	—	
H'FFFFFF42D	—	IIF2B	IIF2A	IIF1	OVF0	ICF0D	ICF0C	ICF0B	ICF0A	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF42E	TIER0	—	—	—	—	—	—	—	—	ATU-II (channel 0)
H'FFFF42F		—	—	—	OVE0	ICE0D	ICE0C	ICE0B	ICE0A	
H'FFFF430	TCNT0H									
H'FFFF431										
H'FFFF432	TCNT0L									
H'FFFF433										
H'FFFF434	ICR0AH									
H'FFFF435										
H'FFFF436	ICR0AL									
H'FFFF437										
H'FFFF438	ICR0BH									
H'FFFF439										
H'FFFF43A	ICR0BL									
H'FFFF43B										
H'FFFF43C	ICR0CH									
H'FFFF43D										
H'FFFF43E	ICR0CL									
H'FFFF43F										
H'FFFF440	TCNT1A									ATU-II (channel 1)
H'FFFF441										
H'FFFF442	TCNT1B									
H'FFFF443										
H'FFFF444	GR1A									
H'FFFF445										
H'FFFF446	GR1B									
H'FFFF447										
H'FFFF448	GR1C									
H'FFFF449										
H'FFFF44A	GR1D									
H'FFFF44B										



**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF44C	GR1E									ATU-II (channel 1)
H'FFFFFF44D										
H'FFFFFF44E	GR1F									
H'FFFFFF44F										
H'FFFFFF450	GR1G									
H'FFFFFF451										
H'FFFFFF452	GR1H									
H'FFFFFF453										
H'FFFFFF454	OCR1									
H'FFFFFF455										
H'FFFFFF456	OSBR1									
H'FFFFFF457										
H'FFFFFF458	TIOR1B	—	IO1D2	IO1D1	IO1D0	—	IO1C2	IO1C1	IO1C0	
H'FFFFFF459	TIOR1A	—	IO1B2	IO1B1	IO1B0	—	IO1A2	IO1A1	IO1A0	
H'FFFFFF45A	TIOR1D	—	IO1H2	IO1H1	IO1H0	—	IO1G2	IO1G1	IO1G0	
H'FFFFFF45B	TIOR1C	—	IO1F2	IO1F1	IO1F0	—	IO1E2	IO1E1	IO1E0	
H'FFFFFF45C	TCR1B	—	—	CKEGB1	CKEGB0	CKSELB3	CKSELB2	CKSELB1	CKSELB0	
H'FFFFFF45D	TCR1A	—	—	CKEGA1	CKEGA0	CKSELA3	CKSELA2	CKSELA1	CKSELA0	
H'FFFFFF45E	TSR1A	—	—	—	—	—	—	—	OVF1A	
H'FFFFFF45F		IMF1H	IMF1G	IMF1F	IMF1E	IMF1D	IMF1C	IMF1B	IMF1A	
H'FFFFFF460	TSR1B	—	—	—	—	—	—	—	OVF1B	
H'FFFFFF461		—	—	—	—	—	—	—	CMF1	
H'FFFFFF462	TIER1A	—	—	—	—	—	—	—	OVE1A	
H'FFFFFF463		IME1H	IME1G	IME1F	IME1E	IME1D	IME1C	IME1B	IME1A	
H'FFFFFF464	TIER1B	—	—	—	—	—	—	—	OVE1B	
H'FFFFFF465		—	—	—	—	—	—	—	CME1	
H'FFFFFF466	TRGMDR	TRGMD	—	—	—	—	—	—	—	
H'FFFFFF467	—	—	—	—	—	—	—	—	—	—
H'FFFFFF47F										

to

H'FFFFFF47F

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF480	TSR3	—	OVF5	IMF5D	IMF5C	IMF5B	IMF5A	OVF4	IMF4D	ATU-II (common in channels 3, 4, and 5)
H'FFFFFF481		IMF4C	IMF4B	IMF4A	OVF3	IMF3D	IMF3C	IMF3B	IMF3A	
H'FFFFFF482	TIER3	—	OVE5	IME5D	IME5C	IME5B	IME5A	OVE4	IME4D	
H'FFFFFF483		IME4C	IME4B	IME4A	OVE3	IME3D	IME3C	IME3B	IME3A	
H'FFFFFF484	TMDR	—	—	—	—	—	T5PWM	T4PWM	T3PWM	
H'FFFFFF485	—	—	—	—	—	—	—	—	—	—
to H'FFFFFF49F										
H'FFFFFF4A0	TCNT3									ATU-II (channel 3)
H'FFFFFF4A1										
H'FFFFFF4A2	GR3A									
H'FFFFFF4A3										
H'FFFFFF4A4	GR3B									
H'FFFFFF4A5										
H'FFFFFF4A6	GR3C									
H'FFFFFF4A7										
H'FFFFFF4A8	GR3D									
H'FFFFFF4A9										
H'FFFFFF4AA	TIOR3B	CCI3D	IO3D2	IO3D1	IO3D0	CCI3C	IO3C2	IO3C1	IO3C0	
H'FFFFFF4AB	TIOR3A	CCI3B	IO3B2	IO3B1	IO3B0	CCI3A	IO3A2	IO3A1	IO3A0	
H'FFFFFF4AC	TCR3	—	—	CKEG1	CKEG0	CKSEL3	CKSEL2	CKSEL1	CKSEL0	
H'FFFFFF4AD	—	—	—	—	—	—	—	—	—	—
to H'FFFFFF4BF										
H'FFFFFF4C0	TCNT4									ATU-II (channel 4)
H'FFFFFF4C1										
H'FFFFFF4C2	GR4A									
H'FFFFFF4C3										
H'FFFFFF4C4	GR4B									
H'FFFFFF4C5										

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF4C6	GR4C									ATU-II (channel 4)
H'FFFFFF4C7										
H'FFFFFF4C8	GR4D									
H'FFFFFF4C9										
H'FFFFFF4CA	TIOR4B	CCI4D	IO4D2	IO4D1	IO4D0	CCI4C	IO4C2	IO4C1	IO4C0	
H'FFFFFF4CB	TIOR4A	CCI4B	IO4B2	IO4B1	IO4B0	CCI4A	IO4A2	IO4A1	IO4A0	
H'FFFFFF4CC	TCR4	—	—	CKEG1	CKEG0	CKSEL3	CKSEL2	CKSEL1	CKSEL0	
H'FFFFFF4CD	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF4DF										
H'FFFFFF4E0	TCNT5									ATU-II (channel 5)
H'FFFFFF4E1										
H'FFFFFF4E2	GR5A									
H'FFFFFF4E3										
H'FFFFFF4E4	GR5B									
H'FFFFFF4E5										
H'FFFFFF4E6	GR5C									
H'FFFFFF4E7										
H'FFFFFF4E8	GR5D									
H'FFFFFF4E9										
H'FFFFFF4EA	TIOR5B	CCI5D	IO5D2	IO5D1	IO5D0	CCI5C	IO5C2	IO5C1	IO5C0	
H'FFFFFF4EB	TIOR5A	CCI5B	IO5B2	IO5B1	IO5B0	CCI5A	IO5A2	IO5A1	IO5A0	
H'FFFFFF4EC	TCR5	—	—	CKEG1	CKEG0	CKSEL3	CKSEL2	CKSEL1	CKSEL0	
H'FFFFFF4ED	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF4EF										
H'FFFFFF500	TCNT6A									ATU-II (channel 6)
H'FFFFFF501										
H'FFFFFF502	TCNT6B									
H'FFFFFF503										
H'FFFFFF504	TCNT6C									
H'FFFFFF505										

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF506	TCNT6D									ATU-II (channel 6)
H'FFFFFF507										
H'FFFFFF508	CYLR6A									
H'FFFFFF509										
H'FFFFFF50A	CYLR6B									
H'FFFFFF50B										
H'FFFFFF50C	CYLR6C									
H'FFFFFF50D										
H'FFFFFF50E	CYLR6D									
H'FFFFFF50F										
H'FFFFFF510	BFR6A									
H'FFFFFF511										
H'FFFFFF512	BFR6B									
H'FFFFFF513										
H'FFFFFF514	BFR6C									
H'FFFFFF515										
H'FFFFFF516	BFR6D									
H'FFFFFF517										
H'FFFFFF518	DTR6A									
H'FFFFFF519										
H'FFFFFF51A	DTR6B									
H'FFFFFF51B										
H'FFFFFF51C	DTR6C									
H'FFFFFF51D										
H'FFFFFF51E	DTR6D									
H'FFFFFF51F										
H'FFFFFF520	TCR6B	—	CKSELD2	CKSELD1	CKSELD0	—	CKSELC2	CKSELC1	CKSELC0	
H'FFFFFF521	TCR6A	—	CKSELB2	CKSELB1	CKSELB0	—	CKSELA2	CKSELA1	CKSELA0	
H'FFFFFF522	TSR6	—	—	—	—	—	—	—	—	
H'FFFFFF523		UD6D	UD6C	UD6B	UD6A	CMF6D	CMF6C	CMF6B	CMF6A	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF524	TIER6	—	—	—	—	—	—	—	—	ATU-II
H'FFFFFF525		—	—	—	—	CME6D	CME6C	CME6B	CME6A	(channel 6)
H'FFFFFF526	PMDR	DTSELD	DTSELC	DTSELB	DTSELA	CNTSELD	CNTSELC	CNTSELB	CNTSELA	
H'FFFFFF527	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF57F										
H'FFFFFF580	TCNT7A									ATU-II
H'FFFFFF581										(channel 7)
H'FFFFFF582	TCNT7B									
H'FFFFFF583										
H'FFFFFF584	TCNT7C									
H'FFFFFF585										
H'FFFFFF586	TCNT7D									
H'FFFFFF587										
H'FFFFFF588	CYLR7A									
H'FFFFFF589										
H'FFFFFF58A	CYLR7B									
H'FFFFFF58B										
H'FFFFFF58C	CYLR7C									
H'FFFFFF58D										
H'FFFFFF58E	CYLR7D									
H'FFFFFF58F										
H'FFFFFF590	BFR7A									
H'FFFFFF591										
H'FFFFFF592	BFR7B									
H'FFFFFF593										
H'FFFFFF594	BFR7C									
H'FFFFFF595										
H'FFFFFF596	BFR7D									
H'FFFFFF597										

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF598	DTR7A									ATU-II (channel 7)
H'FFFFFF599										
H'FFFFFF59A	DTR7B									
H'FFFFFF59B										
H'FFFFFF59C	DTR7C									
H'FFFFFF59D										
H'FFFFFF59E	DTR7D									
H'FFFFFF59F										
H'FFFFFF5A0	TCR7B	—	CKSELD2	CKSELD1	CKSELD0	—	CKSELC2	CKSELC1	CKSELC0	
H'FFFFFF5A1	TCR7A	—	CKSELB2	CKSELB1	CKSELB0	—	CKSELA2	CKSELA1	CKSELA0	
H'FFFFFF5A2	TSR7	—	—	—	—	—	—	—	—	
H'FFFFFF5A3		—	—	—	—	CMF7D	CMF7C	CMF7B	CMF7A	
H'FFFFFF5A4	TIER7	—	—	—	—	—	—	—	—	
H'FFFFFF5A5		—	—	—	—	CME7D	CME7C	CME7B	CME7A	
H'FFFFFF5A6	—	—	—	—	—	—	—	—	—	—
to H'FFFFFF5BF										
H'FFFFFF5C0	TCNT11									ATU-II (channel 11)
H'FFFFFF5C1										
H'FFFFFF5C2	GR11A									
H'FFFFFF5C3										
H'FFFFFF5C4	GR11B									
H'FFFFFF5C5										
H'FFFFFF5C6	TIOR11	—	—	—	IO11B0	—	—	—	IO11A0	
H'FFFFFF5C7	—	—	—	—	—	—	—	—	—	
H'FFFFFF5C8	TCR11	—	—	CKEG1	CKEG0	—	CKSELA2	CKSELA1	CKSELA0	
H'FFFFFF5C9	—	—	—	—	—	—	—	—	—	
H'FFFFFF5CA	TSR11	—	—	—	—	—	—	—	OVF11	
H'FFFFFF5CB		—	—	—	—	—	IMF11B	IMF11A		
H'FFFFFF5CC	TIER11	—	—	—	—	—	—	—	OVE11	
H'FFFFFF5CD		—	—	—	—	—	IME11B	IME11A		

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF5CE	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF5FF										
H'FFFFFF600	TCNT2A									ATU-II
H'FFFFFF601										(channel 2)
H'FFFFFF602	TCNT2B									
H'FFFFFF603										
H'FFFFFF604	GR2A									
H'FFFFFF605										
H'FFFFFF606	GR2B									
H'FFFFFF607										
H'FFFFFF608	GR2C									
H'FFFFFF609										
H'FFFFFF60A	GR2D									
H'FFFFFF60B										
H'FFFFFF60C	GR2E									
H'FFFFFF60D										
H'FFFFFF60E	GR2F									
H'FFFFFF60F										
H'FFFFFF610	GR2G									
H'FFFFFF611										
H'FFFFFF612	GR2H									
H'FFFFFF613										
H'FFFFFF614	OCR2A									
H'FFFFFF615										
H'FFFFFF616	OCR2B									
H'FFFFFF617										
H'FFFFFF618	OCR2C									
H'FFFFFF619										
H'FFFFFF61A	OCR2D									
H'FFFFFF61B										

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF61C	OCR2E									ATU-II (channel 2)
H'FFFFFF61D										
H'FFFFFF61E	OCR2F									
H'FFFFFF61F										
H'FFFFFF620	OCR2G									
H'FFFFFF621										
H'FFFFFF622	OCR2H									
H'FFFFFF623										
H'FFFFFF624	OSBR2									
H'FFFFFF625										
H'FFFFFF626	TIOR2B	—	IO2D2	IO2D1	IO2D0	—	IO2C2	IO2C1	IO2C0	
H'FFFFFF627	TIOR2A	—	IO2B2	IO2B1	IO2B0	—	IO2A2	IO2A1	IO2A0	
H'FFFFFF628	TIOR2D	—	IO2H2	IO2H1	IO2H0	—	IO2G2	IO2G1	IO2G0	
H'FFFFFF629	TIOR2C	—	IO2F2	IO2F1	IO2F0	—	IO2E2	IO2E1	IO2E0	
H'FFFFFF62A	TCR2B	—	—	CKEGB1	CKEGB0	CKSELB3	CKSELB2	CKSELB1	CKSELB0	
H'FFFFFF62B	TCR2A	—	—	CKEGA1	CKEGA0	CKSELA3	CKSELA2	CKSELA1	CKSELA0	
H'FFFFFF62C	TSR2A	—	—	—	—	—	—	—	OVF2A	
H'FFFFFF62D		IMF2H	IMF2G	IMF2F	IMF2E	IMF2D	IMF2C	IMF2B	IMF2A	
H'FFFFFF62E	TSR2B	—	—	—	—	—	—	—	OVF2B	
H'FFFFFF62F		CMF2H	CMF2G	CMF2F	CMF2E	CMF2D	CMF2C	CMF2B	CMF2A	
H'FFFFFF630	TIER2A	—	—	—	—	—	—	—	OVE1A	
H'FFFFFF631		IME2H	IME2G	IME2F	IME2E	IME2D	IME2C	IME2B	IME2A	
H'FFFFFF632	TIER2B	—	—	—	—	—	—	—	OVE2B	
H'FFFFFF633		CME2H	CME2G	CME2F	CME2E	CME2D	CME2C	CME2B	CME2A	
H'FFFFFF634	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF63F										
H'FFFFFF640	DCNT8A									ATU-II (channel 8)
H'FFFFFF641										
H'FFFFFF642	DNCT8B									
H'FFFFFF643										



**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF644	DNCT8C									ATU-II (channel 8)
H'FFFFFF645										
H'FFFFFF646	DCNT8D									
H'FFFFFF647										
H'FFFFFF648	DCNT8E									
H'FFFFFF649										
H'FFFFFF64A	DCNT8F									
H'FFFFFF64B										
H'FFFFFF64C	DCNT8G									
H'FFFFFF64D										
H'FFFFFF64E	DCNT8H									
H'FFFFFF64F										
H'FFFFFF650	DCNT8I									
H'FFFFFF651										
H'FFFFFF652	DCNT8J									
H'FFFFFF653										
H'FFFFFF654	DCNT8K									
H'FFFFFF655										
H'FFFFFF656	DCNT8L									
H'FFFFFF657										
H'FFFFFF658	DCNT8M									
H'FFFFFF659										
H'FFFFFF65A	DCNT8N									
H'FFFFFF65B										
H'FFFFFF65C	DCNT8O									
H'FFFFFF65D										
H'FFFFFF65E	DCNT8P									
H'FFFFFF65F										
H'FFFFFF660	RLDR8									
H'FFFFFF661										

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF662	TCNR	CN8P	CN8O	CN8N	CN8M	CN8L	CN8K	CN8J	CN8I	ATU-II (channel 8)
H'FFFFFF663		CN8H	CN8G	CN8F	CN8E	CN8D	CN8C	CN8B	CN8A	
H'FFFFFF664	OTR	OTEP	OTEO	OTEN	OTEM	OTEL	OTEK	OTEJ	OTEI	
H'FFFFFF665		OTEH	OTEG	OTEF	OTEE	OTED	OTEC	OTEB	OTEA	
H'FFFFFF666	DSTR	DST8P	DST8O	DST8N	DST8M	DST8L	DST8K	DST8J	DST8I	
H'FFFFFF667		DST8H	DST8G	DST8F	DST8E	DST8D	DST8C	DST8B	DST8A	
H'FFFFFF668	TCR8	—	CKSELB2	CKSELB1	CKSELB0	—	CKSELA2	CKSELA1	CKSELA0	
H'FFFFFF669	—	—	—	—	—	—	—	—	—	
H'FFFFFF66A	TSR8	OSF8P	OSF8O	OSF8N	OSF8M	OSF8L	OSF8K	OSF8J	OSF8I	
H'FFFFFF66B		OSF8H	OSF8G	OSF8F	OSF8E	OSF8D	OSF8C	OSF8B	OSF8A	
H'FFFFFF66C	TIER8	OSE8P	OSE8O	OSE8N	OSE8M	OSE8L	OSE8K	OSE8J	OSE8I	
H'FFFFFF66D		OSE8H	OSE8G	OSE8F	OSE8E	OSE8D	OSE8C	OSE8B	OSE8A	
H'FFFFFF66E	RLDENR	RLDEN	—	—	—	—	—	—	—	
H'FFFFFF66F	—	—	—	—	—	—	—	—	—	—
to H'FFFFFF67F										
H'FFFFFF680	ECNT9A									ATU-II (channel 9)
H'FFFFFF681	—	—	—	—	—	—	—	—	—	
H'FFFFFF682	ECNT9B									
H'FFFFFF683	—	—	—	—	—	—	—	—	—	
H'FFFFFF684	ECNT9C									
H'FFFFFF685	—	—	—	—	—	—	—	—	—	
H'FFFFFF686	ECNT9D									
H'FFFFFF687	—	—	—	—	—	—	—	—	—	
H'FFFFFF688	ECNT9E									
H'FFFFFF689	—	—	—	—	—	—	—	—	—	
H'FFFFFF68A	ECNT9F									
H'FFFFFF68B	—	—	—	—	—	—	—	—	—	
H'FFFFFF68C	GR9A									
H'FFFFFF68D	—	—	—	—	—	—	—	—	—	
H'FFFFFF68E	GR9B									

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF68F	—	—	—	—	—	—	—	—	—	ATU-II (channel 9)
H'FFFFFF690	GR9C									
H'FFFFFF691	—	—	—	—	—	—	—	—	—	
H'FFFFFF692	GR9D									
H'FFFFFF693	—	—	—	—	—	—	—	—	—	
H'FFFFFF694	GR9E									
H'FFFFFF695	—	—	—	—	—	—	—	—	—	
H'FFFFFF696	GR9F									
H'FFFFFF697	—	—	—	—	—	—	—	—	—	
H'FFFFFF698	TCR9A	—	TRG3BENEGSELB1	EGSELB0	—	TRG3AENEGSELA1	EGSELA0			
H'FFFFFF699	—	—	—	—	—	—	—	—	—	
H'FFFFFF69A	TCR9B	—	TRG3DENEGSELD1	EGSELD0	—	TRG3CENEGSELC1	EGSELC0			
H'FFFFFF69B	—	—	—	—	—	—	—	—	—	
H'FFFFFF69C	TCR9C	—	—	EGSELF1	EGSELF0	—	—	EGSELE1	EGSELE0	
H'FFFFFF69D	—	—	—	—	—	—	—	—	—	
H'FFFFFF69E	TSR9	—	—	—	—	—	—	—	—	
H'FFFFFF69F	—	—	—	CMF9F	CMF9E	CMF9D	CMF9C	CMF9B	CMF9A	
H'FFFFFF6A0	TIER9	—	—	—	—	—	—	—	—	
H'FFFFFF6A1	—	—	—	CME9F	CME9E	CME9D	CME9C	CME9B	CME9A	
H'FFFFFF6A2	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF6BF										
H'FFFFFF6C0	TCNT10AH									ATU-II (channel 10)
H'FFFFFF6C1										
H'FFFFFF6C2	TCNT10AL									
H'FFFFFF6C3										
H'FFFFFF6C4	TCNT10B									
H'FFFFFF6C5	—	—	—	—	—	—	—	—	—	
H'FFFFFF6C6	TCNT10C									
H'FFFFFF6C7										

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF6C8	TCNT10D									ATU-II (channel 10)
H'FFFFFF6C9	—	—	—	—	—	—	—	—	—	
H'FFFFFF6CA	TCNT10E									
H'FFFFFF6CB										
H'FFFFFF6CC	TCNT10F									
H'FFFFFF6CD										
H'FFFFFF6CE	TCNT10G									
H'FFFFFF6CF										
H'FFFFFF6D0	ICR10AH									
H'FFFFFF6D1										
H'FFFFFF6D2	ICR10AL									
H'FFFFFF6D3										
H'FFFFFF6D4	OCR10AH									
H'FFFFFF6D5										
H'FFFFFF6D6	OCR10AL									
H'FFFFFF6D7										
H'FFFFFF6D8	OCR10B									
H'FFFFFF6D9	—	—	—	—	—	—	—	—	—	
H'FFFFFF6DA	RLD10C									
H'FFFFFF6DB										
H'FFFFFF6DC	GR10G									
H'FFFFFF6DD										
H'FFFFFF6DE	TCNT10H									
H'FFFFFF6DF	—	—	—	—	—	—	—	—	—	
H'FFFFFF6E0	NCR10									
H'FFFFFF6E1	—	—	—	—	—	—	—	—	—	
H'FFFFFF6E2	TIOR10	RLDEN	CCS	PIM1	PIM0	—	IO10G2	IO10G1	IO10G0	
H'FFFFFF6E3	—	—	—	—	—	—	—	—	—	
H'FFFFFF6E4	TCR10	TRG2BEN	TRG1BEN	TRG2AEN	TRG1AEN	TRG0DEN	NCE	CKEG1	CKEG0	
H'FFFFFF6E5	—	—	—	—	—	—	—	—	—	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF6E6	TCCLR10									ATU-II (channel 10)
H'FFFFFF6E7										
H'FFFFFF6E8	TSR10	—	—	—	—	—	—	—	—	
H'FFFFFF6E9		—	—	—	—	CMF10G	CMF10B	ICF10A	CMF10A	
H'FFFFFF6EA	TIER10	—	—	—	—	—	—	—	—	
H'FFFFFF6EB		—	—	—	IREG	CME10G	CME10B	ICE10A	CME10A	
H'FFFFFF6EC	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF6FF										
H'FFFFFF700	POPCR	PULS7 ROE	PULS6 ROE	PULS5 ROE	PULS4 ROE	PULS3 ROE	PULS2 ROE	PULS1 ROE	PULS0 ROE	APC
H'FFFFFF701		PULS7 SOE	PULS6 SOE	PULS5 SOE	PULS4 SOE	PULS3 SOE	PULS2 SOE	PULS1 SOE	PULS0 SOE	
H'FFFFFF702	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF707										
H'FFFFFF708	SYSCR	—	—	—	—	—	—	AUDSRST	RAME	Power-down mode
H'FFFFFF709	—	—	—	—	—	—	—	—	—	
H'FFFFFF70A	—	—	—	—	—	—	—	—	—	
H'FFFFFF70B	MSTCR*3	—	—	—	—	MSTOP3	—	—	MSTOP0	
H'FFFFFF70C	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF70F										
H'FFFFFF710	CMSTR	—	—	—	—	—	—	—	—	CMT
H'FFFFFF711		—	—	—	—	—	—	STR1	STR0	
H'FFFFFF712	CMCSR0	—	—	—	—	—	—	—	—	
H'FFFFFF713		CMF	CMIE	—	—	—	—	CKS1	CKS0	
H'FFFFFF714	CMCNT0									
H'FFFFFF715										
H'FFFFFF716	CMCOR0									
H'FFFFFF717										

Note: 3. This is the read address. The write address is H'FFFFFF70A. For details, see section 23.2.4, Notes on Register Access.

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF718	CMCSR1	—	—	—	—	—	—	—	—	CMT
H'FFFFFF719		CMF	CMIE	—	—	—	—	CKS1	CKS0	
H'FFFFFF71A	CMCNT1									
H'FFFFFF71B										
H'FFFFFF71C	CMCOR1									
H'FFFFFF71D										
H'FFFFFF71E	—	—	—	—	—	—	—	—	—	
H'FFFFFF71F	—	—	—	—	—	—	—	—	—	
H'FFFFFF720	PAIOR	PA15IOR	PA14IOR	PA13IOR	PA12IOR	PA11IOR	PA10IOR	PA9IOR	PA8IOR	Port A
H'FFFFFF721		PA7IOR	PA6IOR	PA5IOR	PA4IOR	PA3IOR	PA2IOR	PA1IOR	PA0IOR	
H'FFFFFF722	PACRH	—	PA15MD	—	PA14MD	—	PA13MD	—	PA12MD	
H'FFFFFF723		—	PA11MD	—	PA10MD	—	PA9MD	—	PA8MD	
H'FFFFFF724	PACRL	—	PA7MD	—	PA6MD	—	PA5MD	—	PA4MD	
H'FFFFFF725		—	PA3MD	—	PA2MD	—	PA1MD	—	PA0MD	
H'FFFFFF726	PADR	PA15DR	PA14DR	PA13DR	PA12DR	PA11DR	PA10DR	PA9DR	PA8DR	
H'FFFFFF727		PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR	
H'FFFFFF728	PHIOR	PH15IOR	PH14IOR	PH13IOR	PH12IOR	PH11IOR	PH10IOR	PH9IOR	PH8IOR	Port H
H'FFFFFF729		PH7IOR	PH6IOR	PH5IOR	PH4IOR	PH3IOR	PH2IOR	PH1IOR	PH0IOR	
H'FFFFFF72A	PHCR	PH15MD	PH14MD	PH13MD	PH12MD	PH11MD	PH10MD	PH9MD	PH8MD	
H'FFFFFF72B		PH7MD	PH6MD	PH5MD	PH4MD	PH3MD	PH2MD	PH1MD	PH0MD	
H'FFFFFF72C	PHDR	PH15DR	PH14DR	PH13DR	PH12DR	PH11DR	PH10DR	PH9DR	PH8DR	
H'FFFFFF72D		PH7DR	PH6DR	PH5DR	PH4DR	PH3DR	PH2DR	PH1DR	PH0DR	
H'FFFFFF72E	ADTRGR1	EXTRG	—	—	—	—	—	—	—	A/D
H'FFFFFF72F	—	—	—	—	—	—	—	—	—	—
H'FFFFFF730	PBIOR	PB15IOR	PB14IOR	PB13IOR	PB12IOR	PB11IOR	PB10IOR	PB9IOR	PB8IOR	Port B
H'FFFFFF731		PB7IOR	PB6IOR	PB5IOR	PB4IOR	PB3IOR	PB2IOR	PB1IOR	PB0IOR	
H'FFFFFF732	PBCRH	PB15MD1	PB15MD0	PB14MD1	PB14MD0	—	PB13MD	PB12MD1	PB12MD0	
H'FFFFFF733		PB11MD1	PB11MD0	PB10MD1	PB10MD0	PB9MD1	PB9MD0	PB8MD1	PB8MD0	
H'FFFFFF734	PBCRL	PB7MD1	PB7MD0	PB6MD1	PB6MD0	PB5MD1	PB5MD0	PB4MD1	PB4MD0	
H'FFFFFF735		—	PB3MD	—	PB2MD	—	PB1MD	—	PB0MD	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF736	PBIR	PB15IR	PB14IR	PB13IR	—	PB11IR	PB10IR	PB9IR	PB8IR	Port B
H'FFFFFF737		PB7IR	PB6IR	PB5IR	PB4IR	PB3IR	PB2IR	PB1IR	PB0IR	
H'FFFFFF738	PBDR	PB15DR	PB14DR	PB13DR	PB12DR	PB11DR	PB10DR	PB9DR	PB8DR	
H'FFFFFF739		PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR	
H'FFFFFF73A	PCIOR	—	—	—	—	—	—	—	—	Port C
H'FFFFFF73B		—	—	—	PC4IOR	PC3IOR	PC2IOR	PC1IOR	PC0IOR	
H'FFFFFF73C	PCCR	—	—	—	—	—	—	—	PC4MD	
H'FFFFFF73D		—	PC3MD	—	PC2MD	—	PC1MD	—	PC0MD	
H'FFFFFF73E	PCDR	—	—	—	—	—	—	—	—	
H'FFFFFF73F		—	—	—	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR	
H'FFFFFF740	PDIOR	—	—	PD13IOR	PD12IOR	PD11IOR	PD10IOR	PD9IOR	PD8IOR	Port D
H'FFFFFF741		PD7IOR	PD6IOR	PD5IOR	PD4IOR	PD3IOR	PD2IOR	PD1IOR	PD0IOR	
H'FFFFFF742	PDCRH	—	—	—	—	PD13MD1	PD13MD0	—	PD12MD	
H'FFFFFF743		—	PD11MD	—	PD10MD	—	PD9MD	—	PD8MD	
H'FFFFFF744	PDCRL	—	PD7MD	—	PD6MD	—	PD5MD	—	PD4MD	
H'FFFFFF745		—	PD3MD	—	PD2MD	—	PD1MD	—	PD0MD	
H'FFFFFF746	PDDR	—	—	PD13DR	PD12DR	PD11DR	PD10DR	PD9DR	PD8DR	
H'FFFFFF747	PDDR	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR	
H'FFFFFF748	PFIOR	PF15IOR	PF14IOR	PF13IOR	PF12IOR	PF11IOR	PF10IOR	PF9IOR	PF8IOR	Port F
H'FFFFFF749		PF7IOR	PF6IOR	PF5IOR	PF4IOR	PF3IOR	PF2IOR	PF1IOR	PF0IOR	
H'FFFFFF74A	PFCRH	CKHIZ	PF15MD	—	PF14MD	—	PF13MD	—	PF12MD	
H'FFFFFF74B		—	PF11MD	—	PF10MD	—	PF9MD	—	PF8MD	
H'FFFFFF74C	PFCRL	—	PF7MD	—	PF6MD	PF5MD1	PF5MD0	—	PF4MD	
H'FFFFFF74D		—	PF3MD	—	PF2MD	—	PF1MD	—	PF0MD	
H'FFFFFF74E	PFDR	PF15DR	PF14DR	PF13DR	PF12DR	PF11DR	PF10DR	PF9DR	PF8DR	
H'FFFFFF74F		PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR	
H'FFFFFF750	PEIOR	PE15IOR	PE14IOR	PE13IOR	PE12IOR	PE11IOR	PE10IOR	PE9IOR	PE8IOR	Port E
H'FFFFFF751		PE7IOR	PE6IOR	PE5IOR	PE4IOR	PE3IOR	PE2IOR	PE1IOR	PE0IOR	
H'FFFFFF752	PECR	PE15MD	PE14MD	PE13MD	PE12MD	PE11MD	PE10MD	PE9MD	PE8MD	
H'FFFFFF753		PE7MD	PE6MD	PE5MD	PE4MD	PE3MD	PE2MD	PE1MD	PE0MD	

**Table A.1 Address (cont)**

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF754	PEDR	PE15DR	PE14DR	PE13DR	PE12DR	PE11DR	PE10DR	PE9DR	PE8DR	Port E
H'FFFFFF755		PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR	
H'FFFFFF756	—	—	—	—	—	—	—	—	—	—
to H'FFFFFF75F										
H'FFFFFF760	PGIOR	—	—	—	—	—	—	—	—	Port G
H'FFFFFF761		—	—	—	—	PG3IOR	PG2IOR	PG1IOR	PG0IOR	
H'FFFFFF762	PGCR	—	—	—	—	—	—	—	—	
H'FFFFFF763		PG3MD1	PG3MD0	PG2MD1	PG2MD0	—	PG1MD	PG0MD1	PG0MD0	
H'FFFFFF764	PGDR	—	—	—	—	—	—	—	—	
H'FFFFFF765		—	—	—	—	PG3DR	PG2DR	PG1DR	PG0DR	
H'FFFFFF766	PJIOR	PJ15IOR	PJ14IOR	PJ13IOR	PJ12IOR	PJ11IOR	PJ10IOR	PJ9IOR	PJ8IOR	Port J
H'FFFFFF767		PJ7IOR	PJ6IOR	PJ5IOR	PJ4IOR	PJ3IOR	PJ2IOR	PJ1IOR	PJ0IOR	
H'FFFFFF768	PJCRH	—	PJ15MD	—	PJ14MD	—	PJ13MD	—	PJ12MD	
H'FFFFFF769		—	PJ11MD	—	PJ10MD	—	PJ9MD	—	PJ8MD	
H'FFFFFF76A	PJCRL	—	PJ7MD	—	PJ6MD	—	PJ5MD	—	PJ4MD	
H'FFFFFF76B		—	PJ3MD	—	PJ2MD	—	PJ1MD	—	PJ0MD	
H'FFFFFF76C	PJDR	PJ15DR	PJ14DR	PJ13DR	PJ12DR	PJ11DR	PJ10DR	PJ9DR	PJ8DR	
H'FFFFFF76D		PJ7DR	PJ6DR	PJ5DR	PJ4DR	PJ3DR	PJ2DR	PJ1DR	PJ0DR	
H'FFFFFF76E	ADTRGR0	EXTRG	—	—	—	—	—	—	—	A/D
H'FFFFFF76F	—	—	—	—	—	—	—	—	—	
H'FFFFFF770	PKIOR	PK15IOR	PK14IOR	PK13IOR	PK12IOR	PK11IOR	PK10IOR	PK9IOR	PK8IOR	Port K
H'FFFFFF771		PK7IOR	PK6IOR	PK5IOR	PK4IOR	PK3IOR	PK2IOR	PK1IOR	PK0IOR	
H'FFFFFF772	PKCRH	—	PK15MD	—	PK14MD	—	PK13MD	—	PK12MD	
H'FFFFFF773		—	PK11MD	—	PK10MD	—	PK9MD	—	PK8MD	
H'FFFFFF774	PKCRL	—	PK7MD	—	PK6MD	—	PK5MD	—	PK4MD	
H'FFFFFF775		—	PK3MD	—	PK2MD	—	PK1MD	—	PK0MD	
H'FFFFFF776	PKIR	PK15IR	PK14IR	PK13IR	PK12IR	PK11IR	PK10IR	PK9IR	PK8IR	
H'FFFFFF777		PK7IR	PK6IR	PK5IR	PK4IR	PK3IR	PK2IR	PK1IR	PK0IR	
H'FFFFFF778	PKDR	PK15DR	PK14DR	PK13DR	PK12DR	PK11DR	PK10DR	PK9DR	PK8DR	
H'FFFFFF779	PKDR	PK7DR	PK6DR	PK5DR	PK4DR	PK3DR	PK2DR	PK1DR	PK0DR	



**Table A.1 Address (cont)**

Address	Register		Bit Names							Module	
	Abbr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1		Bit 0
H'FFFFFF77A	—	—	—	—	—	—	—	—	—	—	—
to											
H'FFFFFF7FF											
H'FFFFFF800	ADDR0H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D	
H'FFFFFF801	ADDR0L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF802	ADDR1H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF803	ADDR1L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF804	ADDR2H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF805	ADDR2L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF806	ADDR3H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF807	ADDR3L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF808	ADDR4H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF809	ADDR4L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF80A	ADDR5H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF80B	ADDR5L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF80C	ADDR6H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF80D	ADDR6L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF80E	ADDR7H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF80F	ADDR7L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF810	ADDR8H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF811	ADDR8L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF812	ADDR9H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF813	ADDR9L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF814	ADDR10H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF815	ADDR10L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF816	ADDR11H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FFFFFF817	ADDR11L	AD1	AD0	—	—	—	—	—	—		
H'FFFFFF818	ADCSR0	ADF	ADIE	ADM1	ADM0	CH3	CH2	CH1	CH0		
H'FFFFFF819	ADCR0	TRGE	CKS	ADST	ADCS	—	—	—	—		
H'FFFFFF81A	—	—	—	—	—	—	—	—	—		
to											
H'FFFFFF81F											

**Table A.1 Address (cont)**

Address	Register	Bit Names								Module
	Abbr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFFFF820	ADDR12H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D
H'FFFFFF821	ADDR12L	AD1	AD0	—	—	—	—	—	—	
H'FFFFFF822	ADDR13H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'FFFFFF823	ADDR13L	AD1	AD0	—	—	—	—	—	—	
H'FFFFFF824	ADDR14H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'FFFFFF825	ADDR14L	AD1	AD0	—	—	—	—	—	—	
H'FFFFFF826	ADDR15H	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
H'FFFFFF827	ADDR15L	AD1	AD0	—	—	—	—	—	—	Port K
H'FFFFFF828	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF837										
H'FFFFFF838	ADCSR1	ADF	ADIE	ADM1	ADM0	CH3	CH2	CH1	CH0	A/D
H'FFFFFF839	ADCR1	TRGE	CKS	ADST	ADCS	—	—	—	—	
H'FFFFFF83A	—	—	—	—	—	—	—	—	—	—
to										
H'FFFFFF85F										

## A.2 Register States in Reset and Power-Down States

**Table A.2 Register States in Reset and Power-Down States**

Type	Name	Reset State	Power-Down State		
		Power-On	Hardware Standby	Software Standby	Sleep
CPU	R0 to R15	Initialized	Initialized	Held	Held
	SR				
	GBR				
	VBR				
	MACH, MACL				
	PR				
	PC				
Interrupt controller (INTC)	IPRA, IPRC to IPRL	Initialized	Initialized	Held	Held
	IOR				
	ISR				
User break controller (UBC)	UBARH, UBARL	Initialized	Initialized	Held	Held
	UBAMRH, UBAMRL				
	UBBR				
	UBCR				
Bus state controller (BSC)	BCR1, BCR2	Initialized	Initialized	Held	Held
	WCR				
Direct memory access controller (DMAC)	SAR0 to SAR3	Undefined	Undefined	Undefined	Held
	DAR0 to DAR3				
	DMATCR0 to DMATCR3	Initialized	Initialized	Initialized	
	CHCR0 to CHCR3				
	DMAOR				
Advanced timer unit-II (ATU-II)	BFR6A to BFR6D, BFR7A to BFR7D	Initialized	Initialized	Initialized	Held
	CYLR6A to CYLR6D, CYLR7A to CYLR7D				
	DCNT8A to DCNT8P				
	DSTR				

**Table A.2 Register States in Reset and Power-Down States (cont)**

Type	Name	Reset State	Power-Down State		
		Power-On	Hardware Standby	Software Standby	Sleep
Advanced timer unit-II (ATU-II)	DTR6A to DTR6D, DTR7A to DTR7D	Initialized	Initialized	Initialized	Held
	ECNT9A to ECNT9F				
	GR1A to GR1H, GR2A to GR2H, GR3A to GR3D, GR4A to GR4D, GR5A to GR5D, GR9A to GR9F, GR10G, GR11A, GR11B				
	ICR0A to ICR0D, ICR10A				
	ITVRR1, ITVRR2A, ITVRR2B				
	NCR10				
	OCR1, OCR2A to OCR2H, OCR10AH, OCR10AL, OCR10B				
	OSBR1, OSBR2				
	OTR				
	PMDR				
	PSCR1 to PSCR4				
	PSTR				
	RLD10C				
	RLDENR				
	RLDR8				
	TCCLR10				
TCNR					

**Table A.2 Register States in Reset and Power-Down States (cont)**

Type	Name	Reset State	Power-Down State		
		Power-On	Hardware Standby	Software Standby	Sleep
Advanced timer unit-II (ATU-II)	TCNT0H, TCNT0L, TCNT1A, TCNT1B, TCNT2A, TCNT2B, TCNT3 to TCNT5, TCNT6A to TCNT6D, TCNT7A to TCNT7D, TCNT10AH, TCNT10AL, TCNT10B to TCNT10H, TCNT11	Initialized	Initialized	Initialized	Held
	TCR1A, TCR1B, TCR2A, TCR2B, TCR3 to TCR5, TCR6A, TCR6B, TCR7A, TCR7B, TCR8, TCR9A to TCR9C, TCR10, TCR11				
	TIER0, TIER1A, TIER1B, TIER2A, TIER2B, TIER3, TIER6 to TIER11				
	TIOR0, TIOR1A to TIOR1D, TIOR2A to TIOR2D, TIOR3A, TIOR3B, TIOR4A, TIOR4B, TIOR5A, TIOR5B, TIOR10, TIOR11				
	TMDR				
	TNCT10E				
	TRGMDR				
	TSR0, TSR1A, TSR1B, TSR2A, TSR2B, TSR3, TSR6 to TSR11				
	TSTR1 to TSTR3				
	Advanced pulse controller (APC)	POPCR	Initialized	Initialized	Held

**Table A.2 Register States in Reset and Power-Down States (cont)**

Type	Name	Reset State	Power-Down State		
		Power-On	Hardware Standby	Software Standby	Sleep
Watchdog timer (WDT)	TCNT	Initialized	Initialized	Initialized	Held
	TCSR			*	
	RSTCSR			Initialized	
Serial communication interface (SCI)	SMR0 to SMR4	Initialized	Initialized	Held	Held
	BRR0 to BRR4				
	SCR0 to SCR4				
	TDR0 to TDR4			Initialized	
	SSR0 to SSR4				
	RDR0 to RDR4				
	SDCR0 to SDCR4			Held	
A/D converter	ADDR0(H/L) to ADDR15(H/L)	Initialized	Initialized	Initialized	Held
	ADSCR0, ADCSR1				
	ADCR0, ADCR1				
	ADTRGR			Held	
Compare match timer (CMT)	CMSTR	Initialized	Initialized	Initialized	Held
	CMCSR0, CMCSR1				
	CMCNT0, CMCNT1				
	CMCOR0, CMCOR1				
Pin function controller (PFC)	PAIOR, PBIOR, PCIOR, PDIOR, PEIOR, PFIOR, PGIOR, PHIOR, PJIOR, PKIOR  PACRH, PACRL, PBCRH, PBCRL, PBIR, PCCR, PDCRH, PDCRL, PECR, PFCRH, PFCRL, PGCR, PHCR, PJCRH, PJCRL, PKCRH, PKCRL, PKIR	Initialized	Initialized	Held	Held

**Table A.2 Register States in Reset and Power-Down States (cont)**

Type	Name	Reset State	Power-Down State		
		Power-On	Hardware Standby	Software Standby	Sleep
I/O ports	PADR, PBDR, PCDR, PDDR, PEDR, PFDR, PGDE, PHDR, PJDR, PKDR	Initialized	Initialized	Held	Held
Flash ROM	FLMCR1	Initialized	Initialized	Initialized	Held
	FLMCR2			Initialized/ Held	
	EBR1, EBR2			Initialized	
	RAMER			Held	
Power-down modes	SBYCR	Initialized	Initialized	Held	Held
	SYSCR				
	MSTCR				
Hitachi controller area network (HCAN)	MCR	Initialized	Initialized	Initialized	Held
	GSR				
	BCR				
	MBCR				
	TXPR				
	TXCR				
	TXACK				
	ABACK				
	RXPR				
	RFPR				
	IRR				
	MBIMR				
	IMR				
	REC				
	TEC				
	UMSR				
	LAFML				
LAFMH					

**Table A.2 Register States in Reset and Power-Down States (cont)**

<b>Type</b>	<b>Name</b>	<b>Reset State</b>	<b>Power-Down State</b>		
		<b>Power-On</b>	<b>Hardware Standby</b>	<b>Software Standby</b>	<b>Sleep</b>
Hitachi controller area network (HCAN)	MC0 [1:8] to MC15 [1:8]	Undefined	Undefined	Undefined	Held
	MD0 [1:8] to MD15 [1:8]				

Note: \* Bits 7 to 5 (OVF, WT/IT, TME) are initialized, and Bits 2 to 0 (CKS2 to CKS0) are held.



# Appendix B Pin States

Tables B.1, B.2, and B.3 show the SH7052F/SH7053F/SH7054F pin states.

**Table B.1 Pin States (1)**

		Pin State									
		Reset State				Power-Down State					
		Power-On									
Type	Pin Name	ROMless Expanded Mode		Expanded Mode with ROM	Single-Chip Mode	Hardware Standby	Software Standby	H-UDI Module Standby	AUD Module Standby	Bus-Released State	
		8 Bits	16 Bits								
Clock	CK* <sup>2</sup>	O				Z	H* <sup>1</sup>	O	O	O	
	XTAL	O				Z	O	O	O	O	
	EXTAL	I				Z	I	I	I	I	
	PLLCAP	I				I	I	I	I	I	
System control	RES	I				Z	I	I	I	I	
	FWE	I				I	I	I	I	I	
	HSTBY	I				I	I	I	I	I	
	MD0	I				I	I	I	I	I	
	MD1	I				I	I	I	I	I	
	MD2	I				I	I	I	I	I	
	WDTOVF	O				Z	O* <sup>1</sup>	O	O	O	
	BREQ	—				Z	Z	I	I	I	
	BACK	—				Z	Z	O	O	L	
Interrupt	NMI	I				Z	I	I	I	I	
	IRQ0 to IRQ3	—				Z	Z	I	I	I	
Address bus	A0 to A21	O		—		Z	Z	O	O	Z	
Data bus	D0 to D7	Z		—		Z	Z	I/O	I/O	Z	
	D8 to D15	—	Z	—		Z	Z	I/O	I/O	Z	
Bus control	WAIT	I			—	Z	Z	I	I	I	
	WRH, WRL	H			—	Z	Z	O	O	Z	
	RD	H			—	Z	Z	O	O	Z	
	CS0	H			—	Z	Z	O	O	Z	
	CS1 to CS3	—				Z	Z	O	O	Z	
Port control	POD	—				Z	Z	I	I	I	
ATU	TIOA to TIOD	—				Z	Z	I	I	I	
	TIO1A to TIO1H	—				Z	K* <sup>1</sup>	I/O	I/O	I/O	
	TIO2A to TIO2H	—				Z	K* <sup>1</sup>	I/O	I/O	I/O	
	TIO3A to TIO3D	—				Z	K* <sup>1</sup>	I/O	I/O	I/O	

**Table B.2 Pin States (2)**

		Pin State								
		Reset State			Power-Down State					
		Power-On								
Type	Pin Name	ROMless Expanded Mode		Expanded Mode with ROM	Single-Chip Mode	Hardware Standby	Software Standby	H-UDI Module Standby	AUD Module Standby	Bus-Released State
		8 Bits	16 Bits							
ATU	TIO4A to TIO4D	—				Z	K*1	I/O	I/O	I/O
	TIO5A to TIO5D	—				Z	K*1	I/O	I/O	I/O
	TO6A to TO6D	—				Z	O*1	O	O	O
	TO7A to TO7D	—				Z	O*1	O	O	O
	TO8A to TO8P	—				Z	O*1	O	O	O
	TI9A to TI9F	—				Z	Z	I	I	I
	TI10	—				Z	Z	I	I	I
	TCLKA, TCLKB	—				Z	Z	I	I	I
SCI	SCK0 to SCK2	—				Z	K*1	I/O	I/O	I/O
	TxD0 to TxD4	—				Z	O*1	O	O	O
	RxD0 to RxD4	—				Z	Z	I	I	I
A/D converter	AN0 to AN15	Z				Z	Z	I	I	I
	ADTRG0	—				Z	Z	I	I	I
	ADEND	—				Z	O*1	O	O	O
	AVref	I				I	I	I	I	I
APC	PULS0 to PULS7	—				Z	O*1	O	O	O
HCAN	HTxD	—				Z	O*1	O	O	O
	HRxD	—				Z	Z	I	I	I
UBC	UBCTRĠ	—				Z	O*1	O	Z	O
I/O port	PA0 to PA15	Z				Z	K*1	I/O	I/O	I/O
	PB0 to PB15	Z				Z	K*1	I/O	I/O	I/O
	PC0 to PC4	Z				Z	K*1	I/O	I/O	I/O
	PD0 to PD13	Z				Z	K*1	I/O	I/O	I/O
	PE0 to PE15	—		Z		Z	K*1	I/O	I/O	I/O
	PF0 to PF5	—		Z		Z	K*1	I/O	I/O	I/O
	PF6 to PF10	—			Z	Z	K*1	I/O	I/O	I/O
	PH11 to PH15	Z				Z	K*1	I/O	I/O	I/O
	PG0 to PG3	Z				Z	K*1	I/O	I/O	I/O
	PH0 to PH7	—		Z		Z	K*1	I/O	I/O	I/O
	PH8 to PH15	Z	—	Z		Z	K*1	I/O	I/O	I/O
	PJ0 to PJ15	Z				Z	K*1	I/O	I/O	I/O
	PK0 to PK15	Z				Z	K*1	I/O	I/O	I/O

**Table B.3 Pin States (3)**

Type	Pin Name	Pin State			
		Hardware Standby AUD Module Standby	AUD Reset (AUDRST = L)	Software Standby AUDSRST = 1 / Normal Operation	No Connection
AUD	AUDRST	Z	LI	HI	Pulled down internally
	AUDMD	Z	I	I	Pulled up internally
	AUDATA0 to AUDATA3	Z	AUDMD = H : I AUDMD = L : HO	AUDMD = H : I/O AUDMD = L : O	Pulled up internally
	AUDCK	Z	AUDMD = H : I AUDMD = L : HO	AUDMD = H : I/O AUDMD = L : O	Pulled up internally
	AUDSYNC	Z	AUDMD = H : I AUDMD = L : HO	AUDMD = H : I/O AUDMD = L : O	Pulled up internally

**Legend:**

—: Not initial value

I: Input

O: Output

H: High-level

L: Low-level

Z: High impedance

K: Input pins become high-impedance, output pins retain their state.

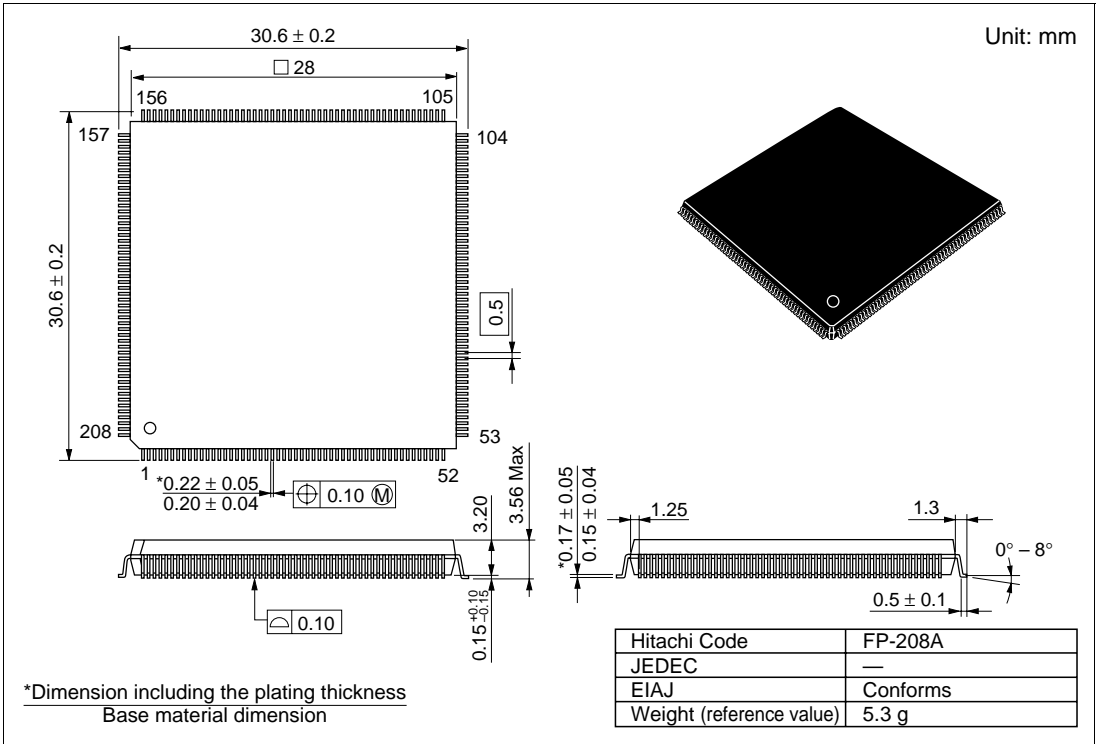
- Notes: 1. When the port impedance bit (HIZ) in the standby control register (SBYCR) is set to 1, output pins become high-impedance.  
 2. When the CKHIZ bit in PFCRH is set to 1, becomes high-impedance unconditionally.

# Appendix C Product Code Lineup

**Table C.1 SH7052F/SH7053F/SH7054F Product Code Lineup**

<b>Product Type</b>	<b>Product Code</b>	<b>Mark Code</b>	<b>Package</b>
SH7052      F-ZTAT version	HD64F7052F40	HD64F7052F40	208-pin plastic QFP (FP-208A)
SH7053	HD64F7053F40	HD64F7053F40	
SH7054	HD64F7054F40	HD64F7054F40	

# Appendix D Package Dimensions



**Figure D.1 Package Dimensions (FP-208A)**



---

**SH7052 F-ZTAT™, SH7053 F-ZTAT™, SH7054 F-ZTAT™  
Hardware Manual**

Publication Date: 1st Edition, March 1999

3rd Edition, November 2000

Published by: Electronic Devices Sales & Marketing Group  
Semiconductor & Integrated Circuits  
Hitachi, Ltd.

Edited by: Technical Documentation Group  
Hitachi Kodaira Semiconductor Co., Ltd.

Copyright © Hitachi, Ltd., 1999. All rights reserved. Printed in Japan.