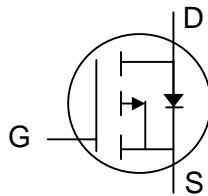


# P-channel Enhancement-mode Power MOSFET

- Low gate-charge
- Simple drive requirement
- Fast switching

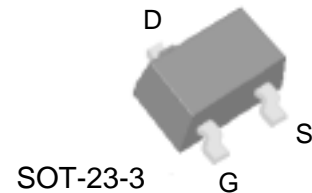
 **Pb-free; RoHS compliant.**



$V_{DSS}$	-30V
$R_{DS(ON)}$	80mΩ
$I_D$	-3.2A

## DESCRIPTION

The SSM2305AGN is in a SOT-23-3 package, which is widely used for lower power commercial and industrial surface mount applications. This device is suitable for low-voltage applications such as DC/DC converters and general switching applications.



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	± 12	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	-3.2	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	-2.6	A
$I_{DM}$	Pulsed Drain Current <sup>1,2</sup>	-10	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1.38	W
	Linear Derating Factor	0.01	W/°C
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

## THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	90	°C/W

**ELECTRICAL CHARACTERISTICS (at T<sub>j</sub> = 25°C unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	-	-0.1	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-3.2A	-	-	60	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3.0A	-	-	80	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2.0A	-	-	150	mΩ
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-1.0A	-	-	250	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.5	-	-1.2	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3.0A	-	9	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>J</sub> =25°C)	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	-	-	-1	uA
	Drain-Source Leakage Current (T <sub>J</sub> =70°C)	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = ± 12V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =-3.2A	-	10	18	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-24V	-	1.8	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =-4.5V	-	3.6	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =-15V	-	7	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =-3.2A	-	15	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =-10V	-	21	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =4.6Ω	-	15	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	735	1325	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =-25V	-	100	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	80	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =-1.2A, V <sub>GS</sub> =0V	-	-	-1.2	V
trr	Reverse Recovery Time	I <sub>S</sub> =-3.2A, V <sub>GS</sub> =0V,	-	24	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	19	-	nC

**Notes:**

- 1.Pulse width limited by maximum junction temperature.
- 2.Pulse width ≤300us, duty cycle ≤2%.
- 3.Surface-mounted on 1 in<sup>2</sup> copper pad on FR4 board ; 270°C/W when mounted on minimum copper pad.

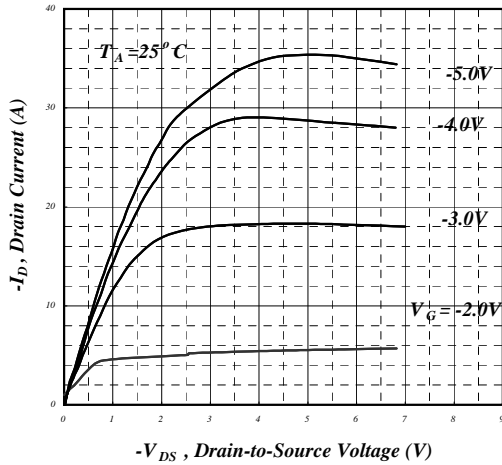


Fig 1. Typical Output Characteristics

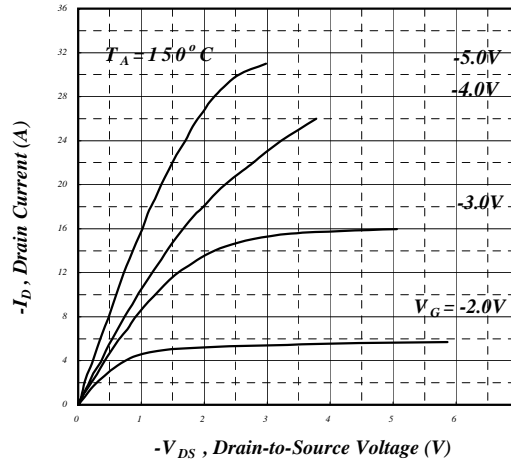


Fig 2. Typical Output Characteristics

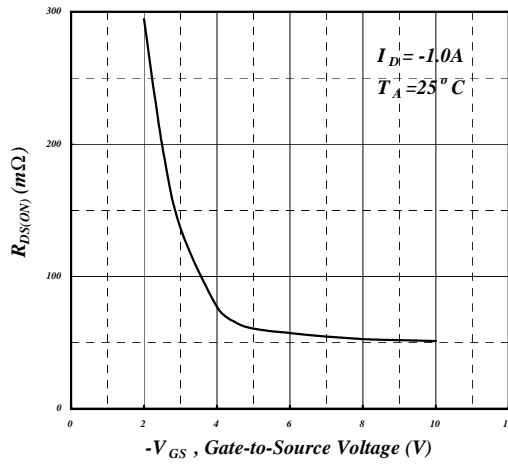


Fig 3. On-Resistance vs. Gate Voltage

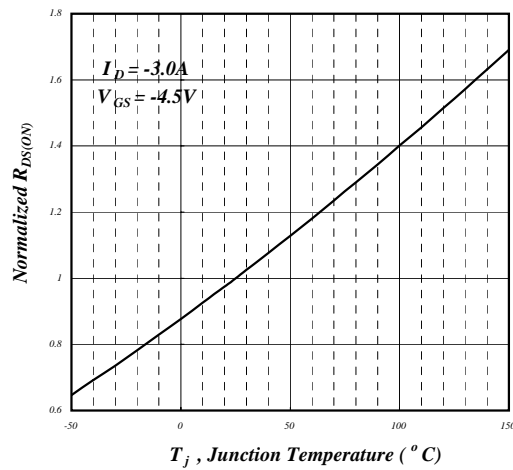


Fig 4. Normalized On-Resistance vs. Junction Temperature

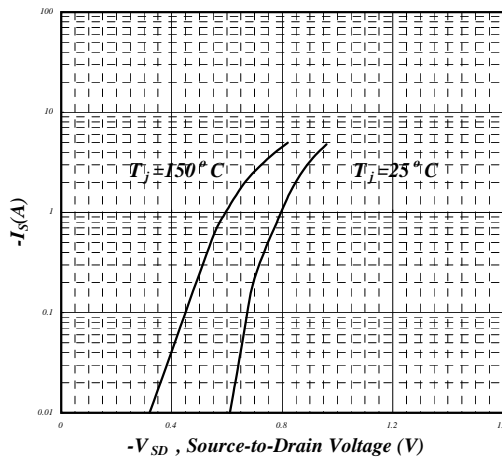


Fig 5. Forward Characteristic of Reverse Diode

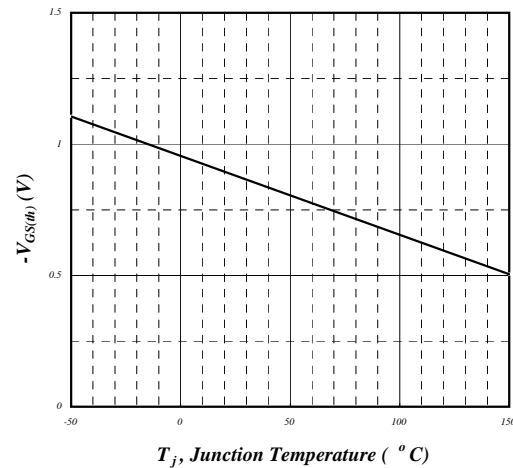


Fig 6. Gate Threshold Voltage vs. Junction Temperature

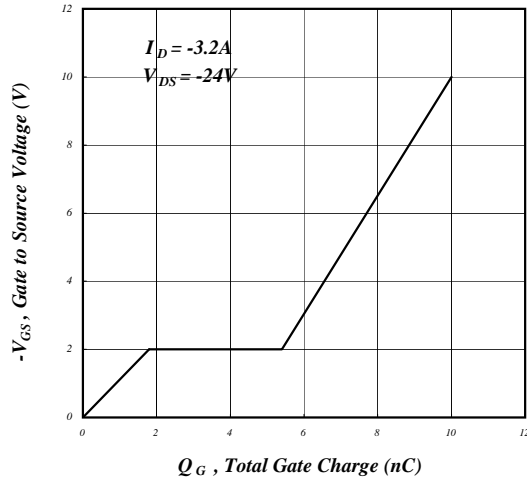


Fig 7. Gate Charge Characteristics

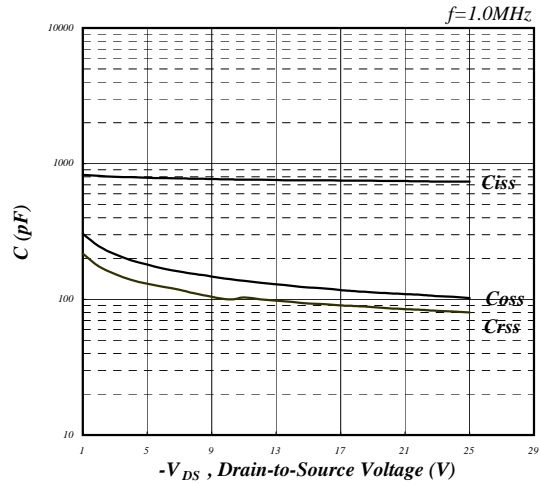


Fig 8. Typical Capacitance Characteristics

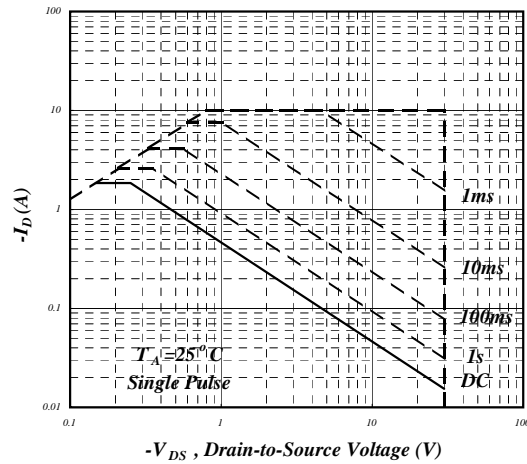


Fig 9. Maximum Safe Operating Area

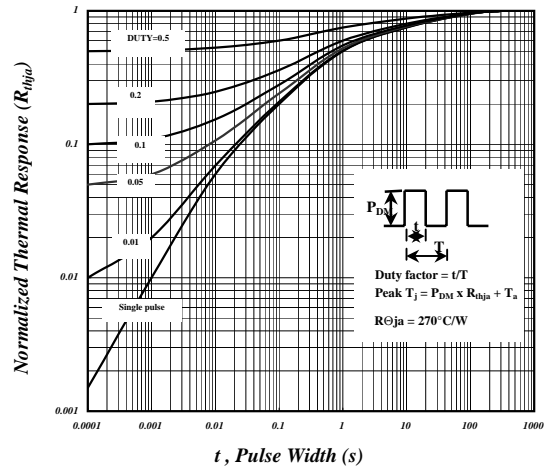


Fig 10. Effective Transient Thermal Impedance

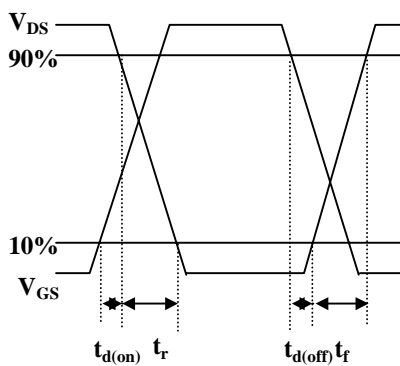


Fig 11. Switching Time Circuit

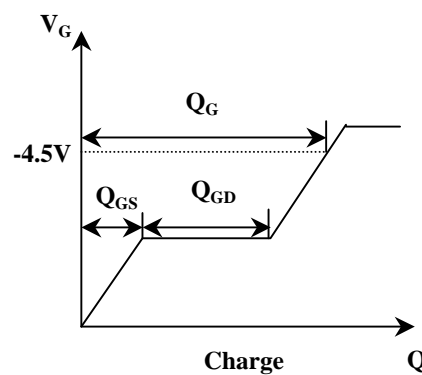


Fig 12. Gate Charge Circuit

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