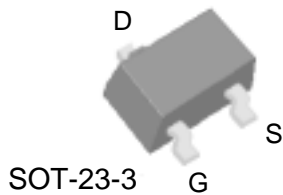


# N-channel Enhancement-mode Power MOSFET

## PRODUCT SUMMARY

$BV_{DSS}$	30V
$R_{DS(ON)}$	42m $\Omega$
$I_D$	4.7A

 **Pb-free; RoHS-compliant SOT-23-3**



## DESCRIPTION

The SSM2316GN achieves fast switching performance with low gate charge without a complex drive circuit. It is suitable for low voltage applications such as DC/DC converters and general load-switching circuits.

The SSM2316GN is supplied in an RoHS-compliant SOT-23-3 package, which is widely used for lower power commercial and industrial surface mount applications.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Continuous drain current <sup>3</sup> , $T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	4.7	A
		3.7	A
$I_{DM}$	Pulsed drain current <sup>1,2</sup>	10	A
$P_D$	Total power dissipation <sup>3</sup> , $T_A = 25^\circ\text{C}$	1.38	W
	Linear derating factor	0.01	W/ $^\circ\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Maximum thermal resistance, junction-ambient <sup>3</sup>	90	$^\circ\text{C}/\text{W}$

### Notes:

1. Pulse width must be limited to avoid exceeding the maximum junction temperature of 150 $^\circ\text{C}$ .
2. Pulse width <300us, duty cycle <2%.
3. Mounted on a square inch of copper pad on FR4 board ; 270 $^\circ\text{C}/\text{W}$  when mounted on the minimum pad area required for soldering.

**ELECTRICAL CHARACTERISTICS** (at  $T_j = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown voltage temperature coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	-	0.02	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static drain-source on-resistance	$V_{GS}=10V, I_D=4A$	-	-	42	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=2A$	-	-	72	$\text{m}\Omega$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward transconductance	$V_{DS}=10V, I_D=4A$	-	5	-	S
$I_{DSS}$	Drain-source leakage current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
		$V_{DS}=24V, V_{GS}=0V, T_j = 70^\circ\text{C}$	-	-	10	$\mu A$
$I_{GSS}$	Gate-source leakage current	$V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$Q_g$	Total gate charge <sup>2</sup>	$I_D=4A$	-	5	8	nC
$Q_{gs}$	Gate-source charge	$V_{DS}=24V$	-	1	-	nC
$Q_{gd}$	Gate-drain ("Miller") charge	$V_{GS}=4.5V$	-	3	-	nC
$t_{d(on)}$	Turn-on delay time <sup>2</sup>	$V_{DS}=15V$	-	7	-	ns
$t_r$	Rise time	$I_D=1A$	-	8	-	ns
$t_{d(off)}$	Turn-off delay time	$R_G=3.3\Omega, V_{GS}=10V$	-	12	-	ns
$t_f$	Fall time	$R_D=15\Omega$	-	3	-	ns
$C_{iss}$	Input capacitance	$V_{GS}=0V$	-	270	430	pF
$C_{oss}$	Output capacitance	$V_{DS}=25V$	-	70	-	pF
$C_{rss}$	Reverse transfer capacitance	$f=1.0\text{MHz}$	-	60	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	1.4	2.1	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward voltage <sup>2</sup>	$I_S=1.2A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse recovery time	$I_S=4A, V_{GS}=0V,$	-	14	-	ns
$Q_{rr}$	Reverse recovery charge	$di/dt=100A/\mu s$	-	9	-	nC

**Notes:**

1. Pulse width must be limited to avoid exceeding the maximum junction temperature of  $150^\circ\text{C}$ .

2. Pulse width  $<300\mu s$ , duty cycle  $<2\%$ .

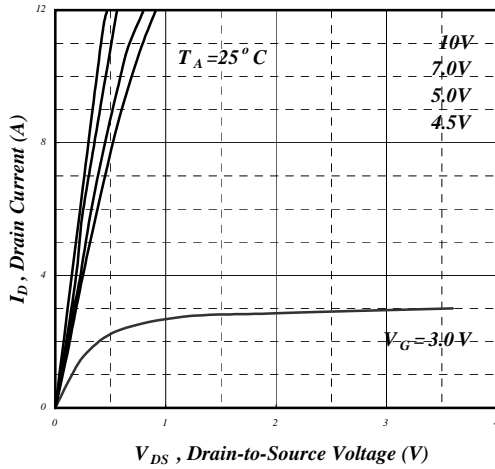


Fig 1. Typical Output Characteristics

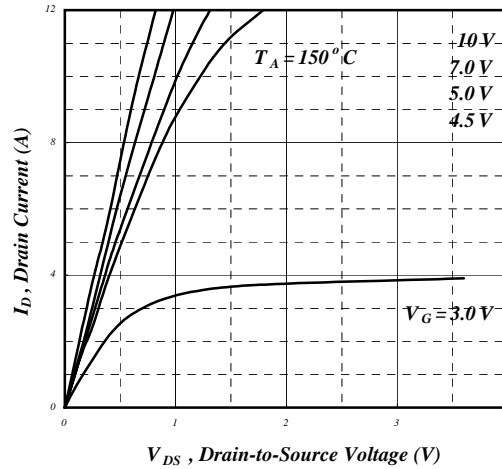


Fig 2. Typical Output Characteristics

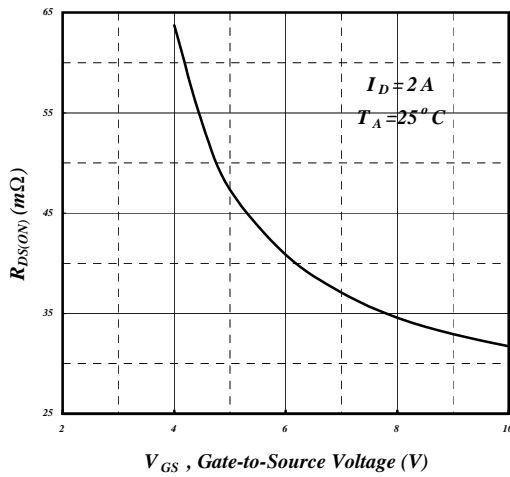


Fig 3. On-Resistance vs. Gate Voltage

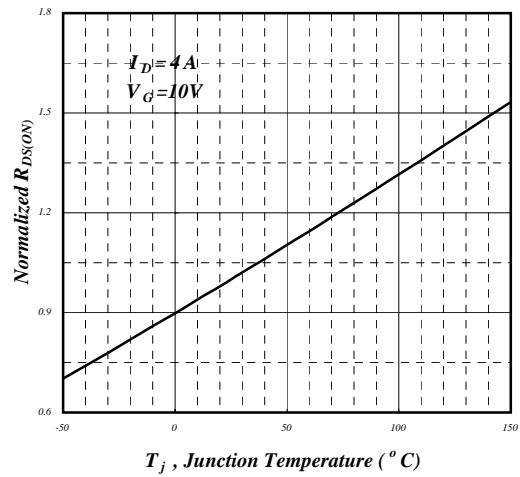


Fig 4. Normalized On-Resistance vs. Junction Temperature

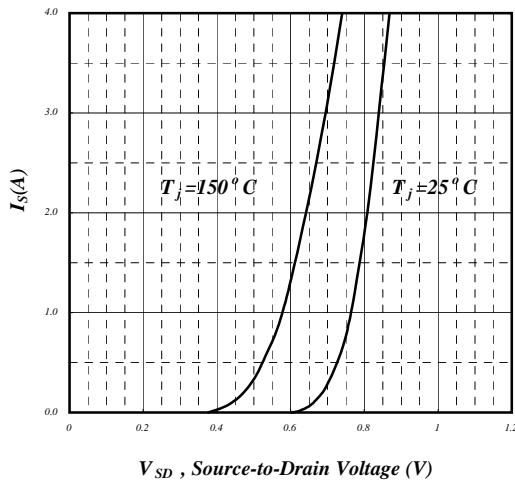


Fig 5. Forward Characteristic of Reverse Diode

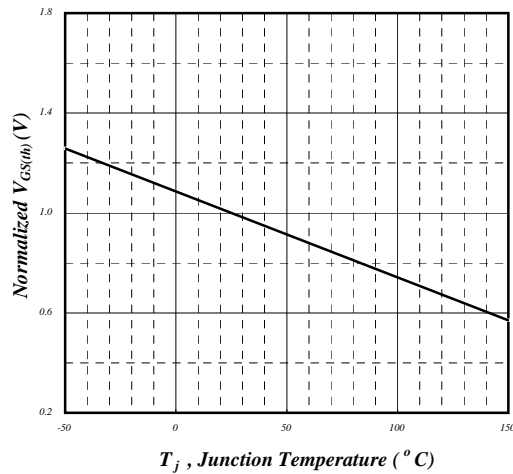


Fig 6. Gate Threshold Voltage vs. Junction Temperature

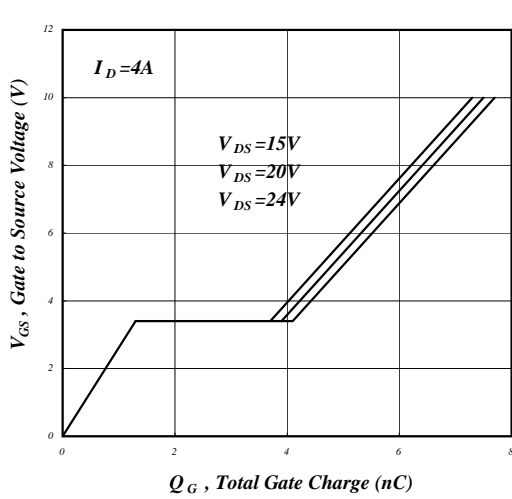


Fig 7. Gate Charge Characteristics

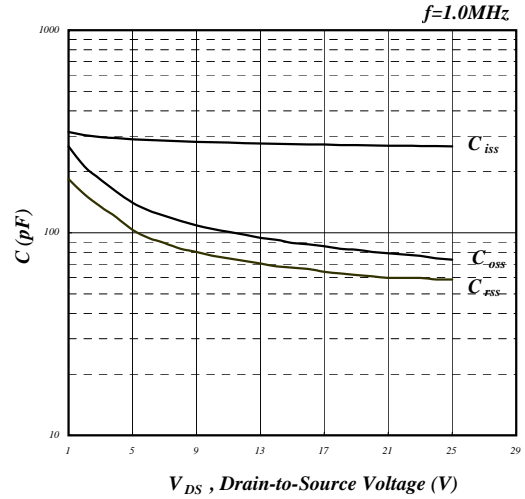


Fig 8. Typical Capacitance Characteristics

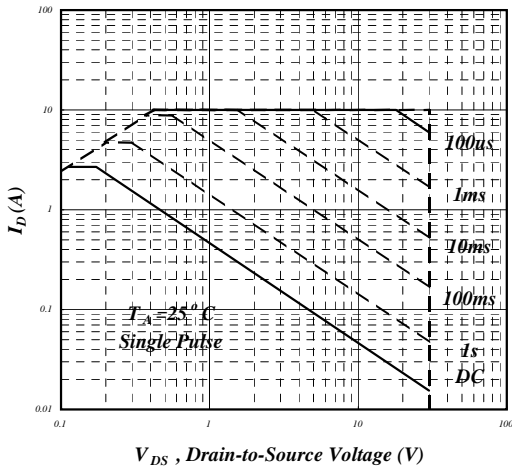


Fig 9. Maximum Safe Operating Area

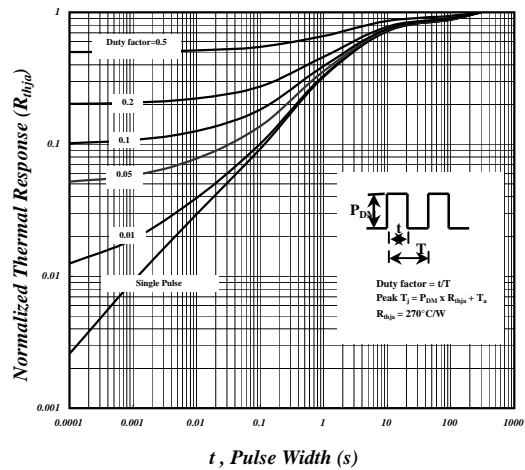


Fig 10. Effective Transient Thermal Impedance

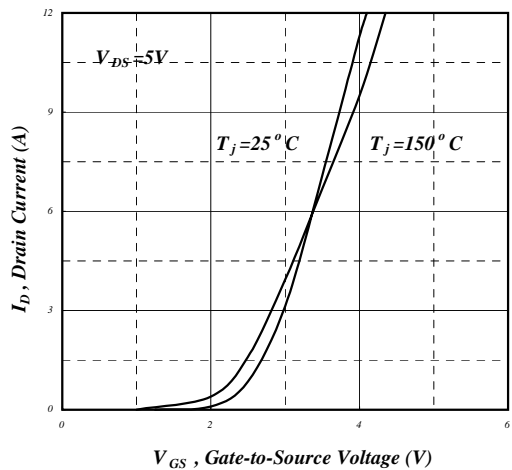


Fig 11. Transfer Characteristics

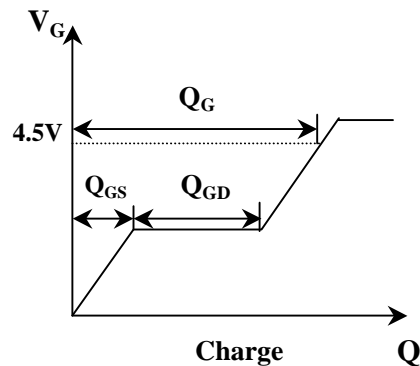
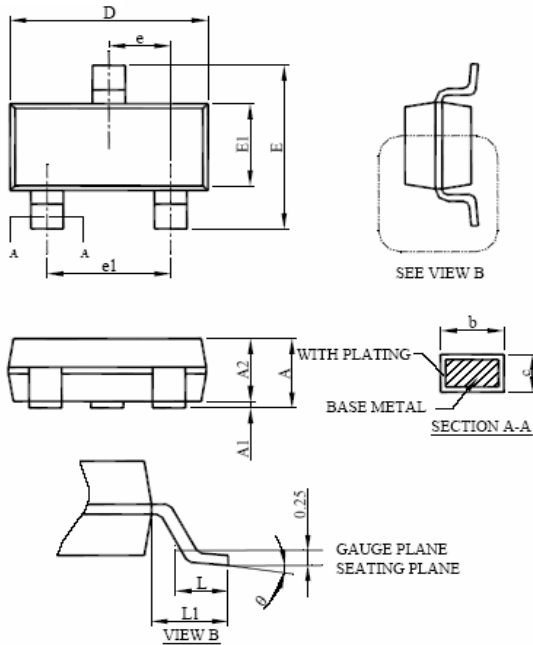


Fig 12. Gate Charge Circuit

## PHYSICAL DIMENSIONS

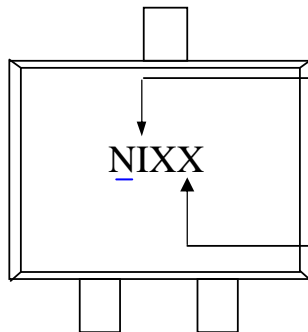
### SOT-23-3



SYMBOL	SOT-23-3	
	MILLIMETERS	
	MIN.	MAX.
A	0.89	1.45
A1	0	0.15
A2	0.70	1.30
b	0.30	0.50
c	0.08	0.25
D	2.65	3.10
E	2.10	3.00
E1	1.19	2.30
e	0.95BSC	
e1	1.90BSC	
L	0.30	0.60
L1	0.60REF	
$\Theta$	0°	8°

\*Dimensions do not include mold protrusions.

## PART MARKING



PART NUMBER CODE: NI = SSM2316GN

First character is underlined to indicate Pb-free part

XX = DATE/LOT CODE - contact SSC for information on decoding this.

## PACKING: Moisture sensitivity level MSL3

3000 pcs in antistatic tape on a reel packed in a moisture barrier bag (MBB).

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