Filterless, High Efficiency, Mono 3 W Class-D Audio Amplifier

SSM2319

FEATURES

Filterless Class-D amplifier with ultraefficient spread-spectrum Σ-Δ modulation
Internal modulator synchronization (SYNC)
3 W into 3 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with <1% total harmonic distortion (THD)
90% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Signal-to-noise ratio (SNR): 98 dB
Single-supply operation: 2.5 V to 5.5 V
Ultralow shutdown current: 20 nA
Short-circuit and thermal protection with autorecovery
Available in 9-ball, 1.5 mm × 1.5 mm WLCSP
Pop-and-click suppression
Built-in resistors reduce board component count
Default fixed 12 dB or user-adjustable gain setting

APPLICATIONS

Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2319 is a fully integrated, high efficiency Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 3 W of continuous output power with <1% THD + N driving a 3 Ω load from a 5.0 V supply.

The SSM2319 features a high efficiency, low noise modulation scheme that does not require any external LC output filters. The modulation continues to provide high efficiency even at low output power. It operates with 90% efficiency at 1.4 W into 8 Ω or 85% efficiency at 3 W into 3 Ω from a 5.0 V supply and has an SNR of 98 dB. Spread-spectrum pulse density modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

SYNC can be activated in the event that end users are concerned about clock intermodulation (beating effect) of several amplifiers in close proximity.

The SSM2319 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The device also includes pop-and-click suppression circuitry. This minimizes voltage glitches at the output during turn-on and turn-off, reducing audible noise on activation and deactivation.

The default gain of the SSM2319 is 12 dB, but users can reduce the gain by using a pair of external resistors (see the Gain section).

The SSM2319 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 9-ball, 1.5 mm × 1.5 mm wafer level chip scale package (WLCSP).

FUNCTIONAL BLOCK DIAGRAM

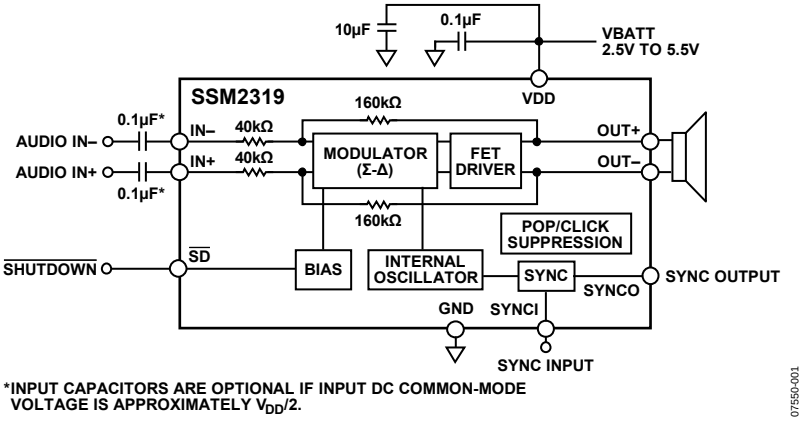

Figure 1.

Rev. 0

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REVISION HISTORY

8/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω +33 µH, SYNCI = GND (standalone mode), unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_{OUT}	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.41		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.72		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.33		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.77		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.91		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.42		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.53		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.28		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.56		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.17[1]		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.6		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.72		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.1[1]		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.52		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.68		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.7[1]		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.9		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.85		W
Efficiency	η	P_{OUT} = 1.4 W, 8 Ω, V_{DD} = 5.0 V		93		%
Total Harmonic Distortion + Noise	THD + N	P_{OUT} = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.06		%
		P_{OUT} = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.02		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} – 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, output referred		57		dB
Average Switching Frequency	f_{SW}			300		kHz
Differential Output Offset Voltage	V_{OOS}	G = 12 dB		2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating/ground	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac GND, C_{IN} = 0.1 µF		60		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		3.6		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		3.2		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		2.7		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 5.0 V		3.7		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 3.6 V		3.3		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 2.5 V		2.8		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Av			12		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = VDD		40		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		28		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac grounded, A_V = 12 dB, A weighting		40		μV
Signal-to-Noise Ratio	SNR	P_{OUT} = 1.4 W, R_L = 8 Ω		98		dB
SYNC OPERATIONAL FREQUENCY			5		12	MHz

[1] Although the SSM2319 has good audio quality above 3 W, continuous output power beyond 3 W must be avoided due to device packaging limitations.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Susceptibility	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-Ball, 1.5 mm × 1.5 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

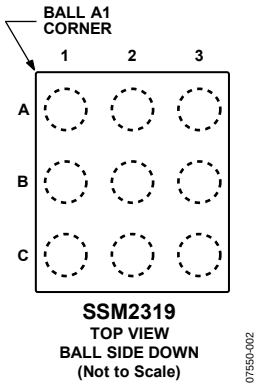


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	IN−	Inverting Input.
1B	IN+	Noninverting Input.
1C	GND	Ground.
2A	$\overline{SD}$	Shutdown Input. Active low digital input.
2B	SYNCI	SYNC Input.
2C	VDD	Power Supply.
3A	SYNCO	SYNC Output.
3B	OUT−	Inverting Output.
3C	OUT+	Noninverting Output.

TYPICAL PERFORMANCE CHARACTERISTICS

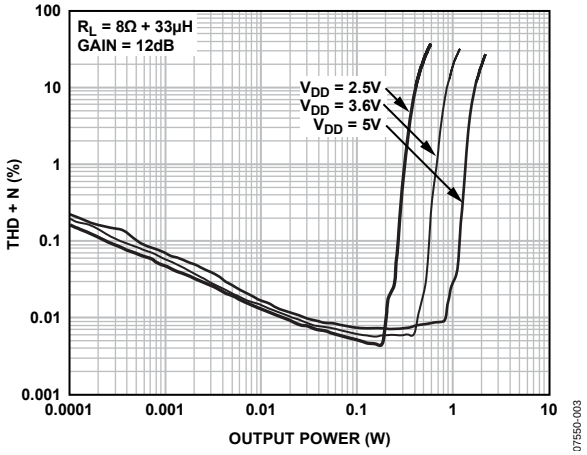


Figure 3. THD + N vs. Output Power into R_L = 8 Ω + 33 µH, Gain = 12 dB

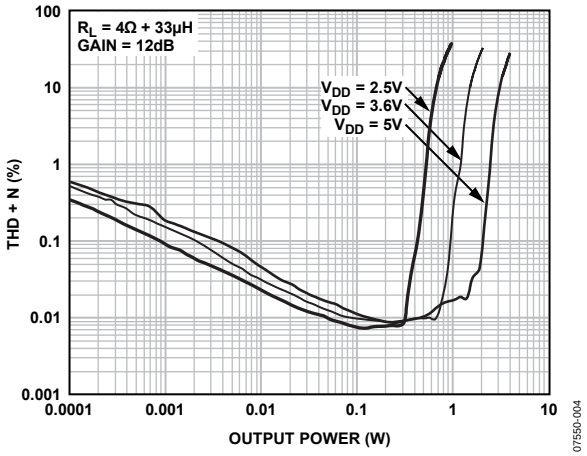


Figure 4. THD + N vs. Output Power into R_L = 4 Ω + 33 µH, Gain = 12 dB

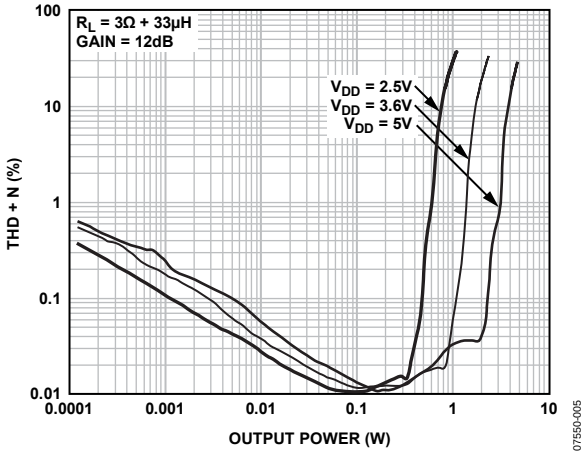


Figure 5. THD + N vs. Output Power into R_L = 3 Ω + 33 µH, Gain = 12 dB

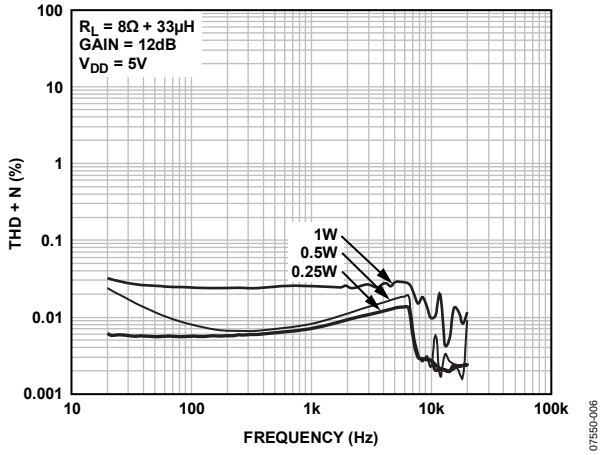


Figure 6. THD + N vs. Frequency, R_L = 8 Ω + 33 µH, Gain = 12 dB, V_{DD} = 5 V

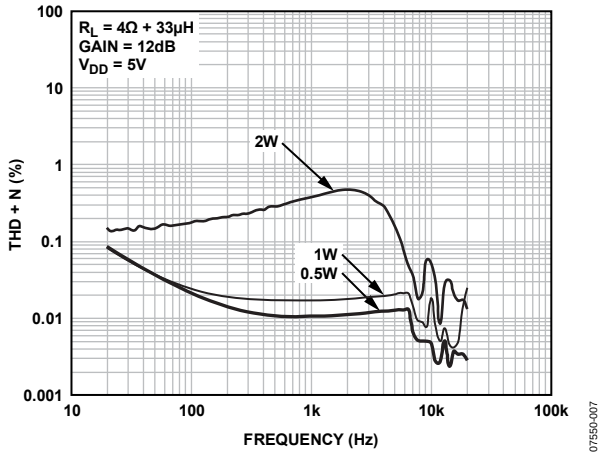


Figure 7. THD + N vs. Frequency, R_L = 4 Ω + 33 µH, Gain = 12 dB, V_{DD} = 5 V

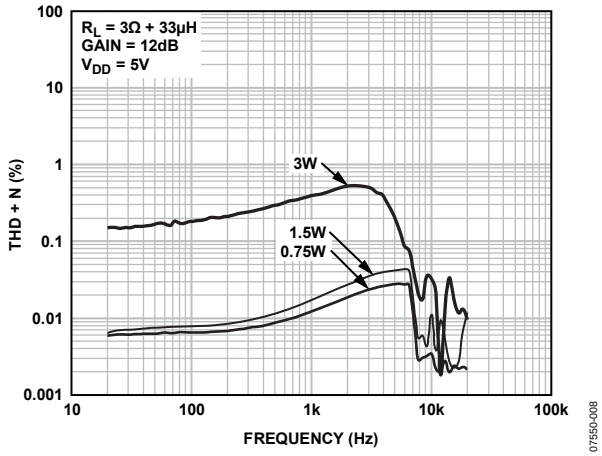


Figure 8. THD + N vs. Frequency, R_L = 3Ω + 33 µH, Gain = 12 dB, V_{DD} = 5 V

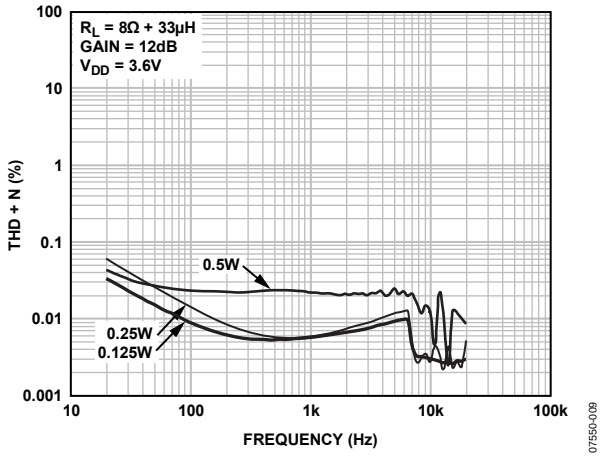


Figure 9. THD + N vs. Frequency, R_L = 8 Ω + 33 µH, Gain = 12 dB, V_{DD} = 3.6 V

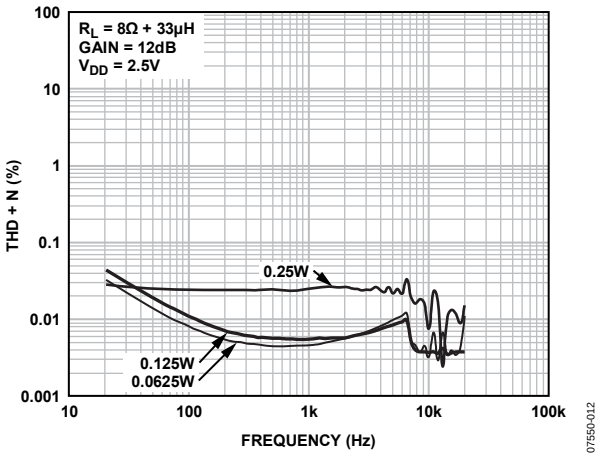


Figure 12. THD + N vs. Frequency, R_L = 8 Ω + 33 µH, Gain = 12 dB, V_{DD} = 2.5 V

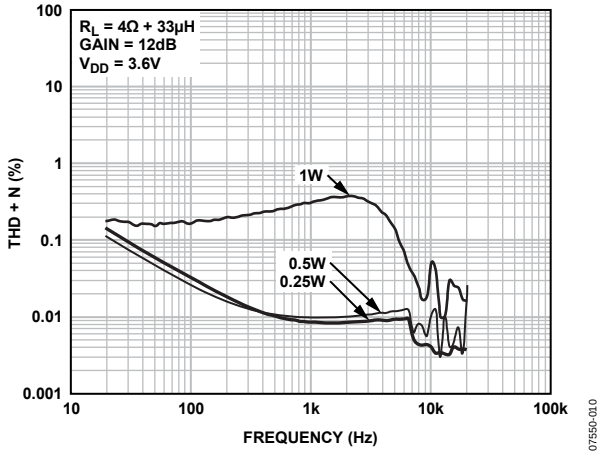


Figure 10. THD + N vs. Frequency, R_L = 4 Ω + 33 µH, Gain = 12 dB, V_{DD} = 3.6 V

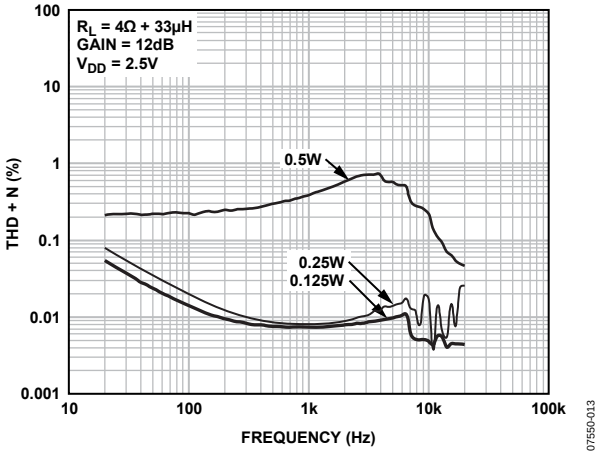


Figure 13. THD + N vs. Frequency, R_L = 4 Ω + 33 µH, Gain = 12 dB, V_{DD} = 2.5 V

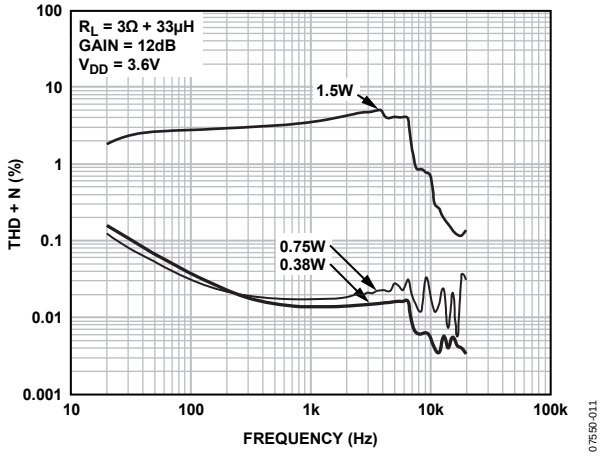


Figure 11. THD + N vs. Frequency, R_L = 3 Ω + 33 µH, Gain = 12 dB, V_{DD} = 3.6 V

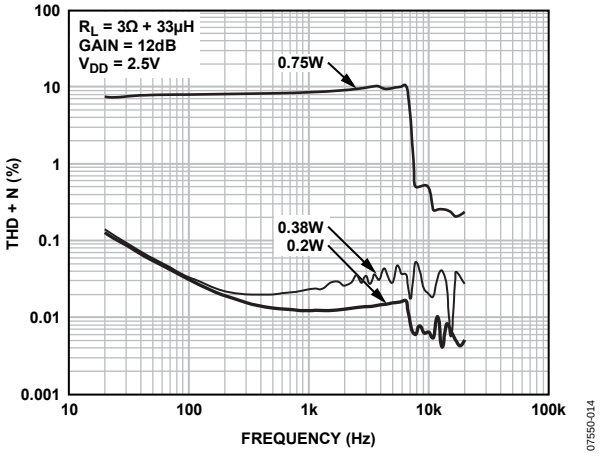


Figure 14. THD + N vs. Frequency, R_L = 3 Ω + 33 µH, Gain = 12 dB, V_{DD} = 2.5 V

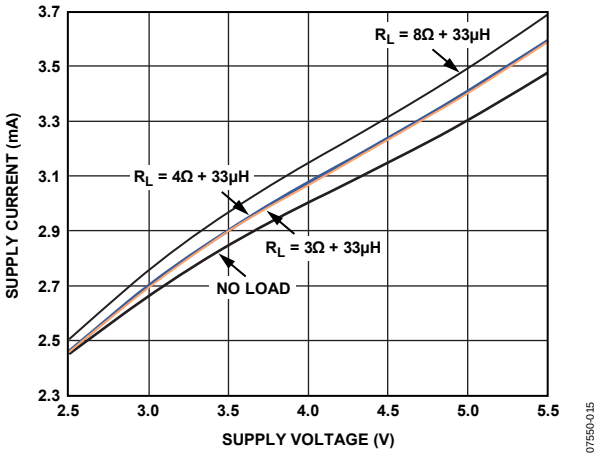


Figure 15. Supply Current vs. Supply Voltage

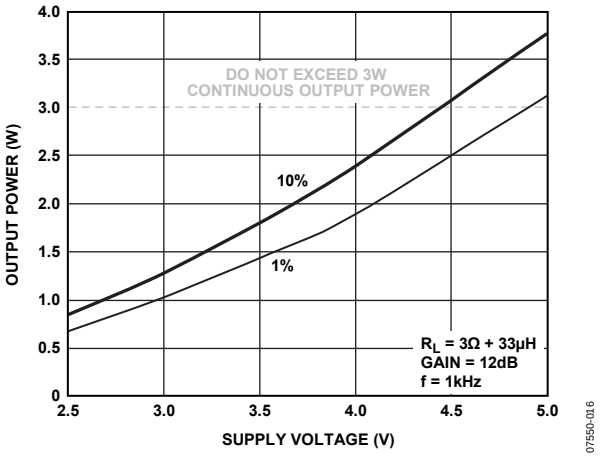


Figure 16. Maximum Output Power vs. Supply Voltage, $R_L = 3\ \Omega + 33\ \mu H$, Gain = 12 dB

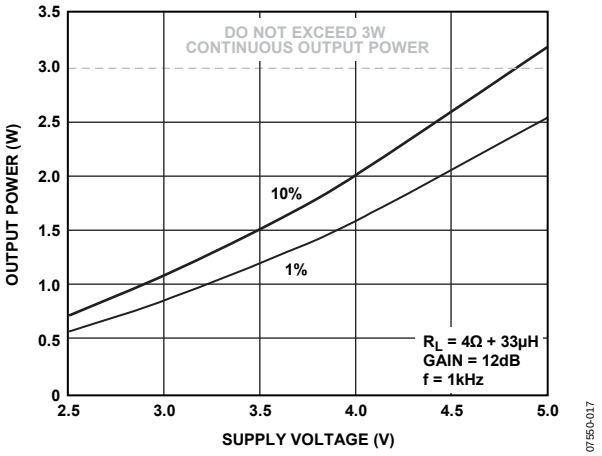


Figure 17. Maximum Output Power vs. Supply Voltage, $R_L = 4\ \Omega + 33\ \mu H$, Gain = 12 dB

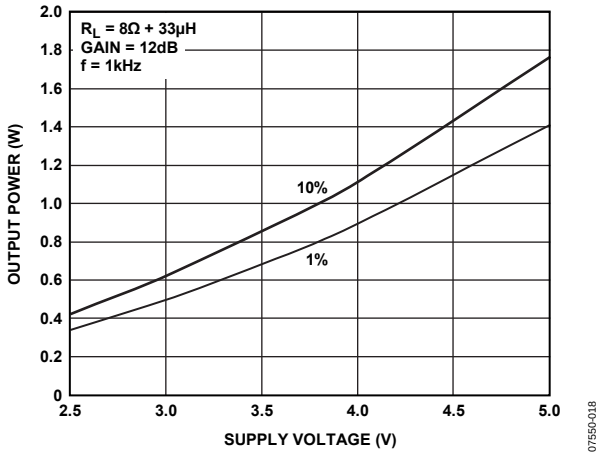


Figure 18. Maximum Output Power vs. Supply Voltage, $R_L = 8\ \Omega + 33\ \mu H$, Gain = 12 dB

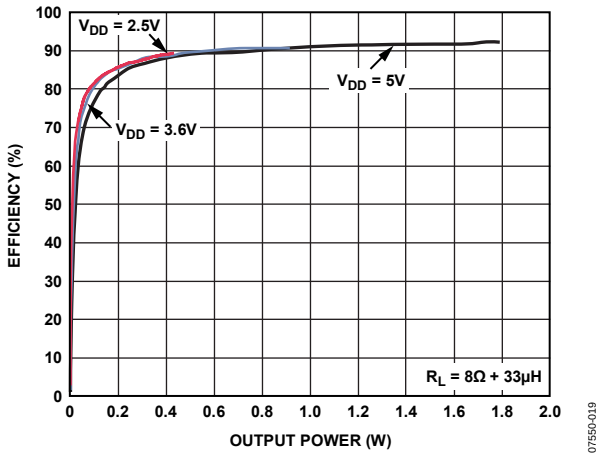


Figure 19. Efficiency vs. Output Power into $R_L = 8\ \Omega + 33\ \mu H$

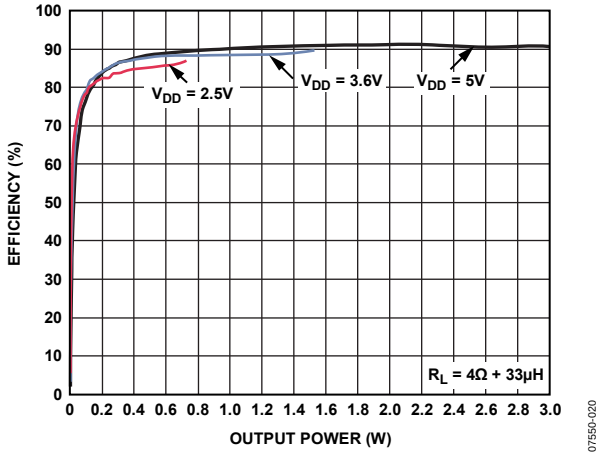


Figure 20. Efficiency vs. Output Power into $R_L = 4\ \Omega + 33\ \mu H$

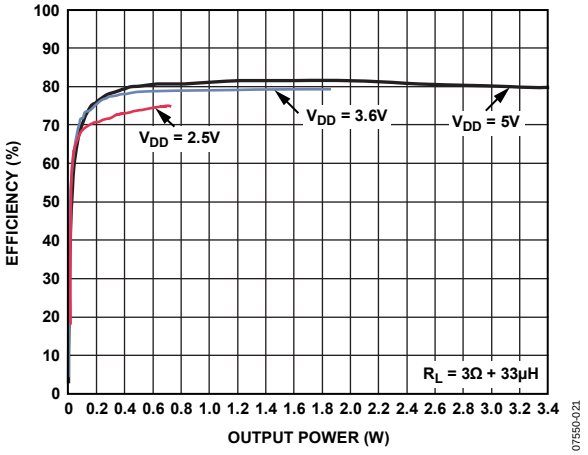


Figure 21. Efficiency vs. Output Power into R_L = 3 Ω + 33 µH

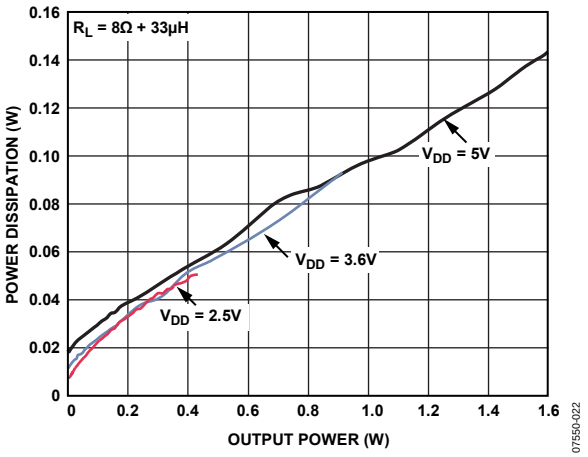


Figure 22. Power Dissipation vs. Output Power into R_L = 8 Ω + 33 µH

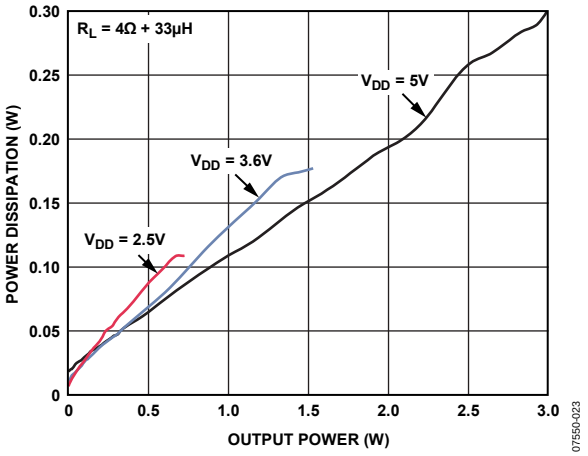


Figure 23. Power Dissipation vs. Output Power into R_L = 4 Ω + 33 µH

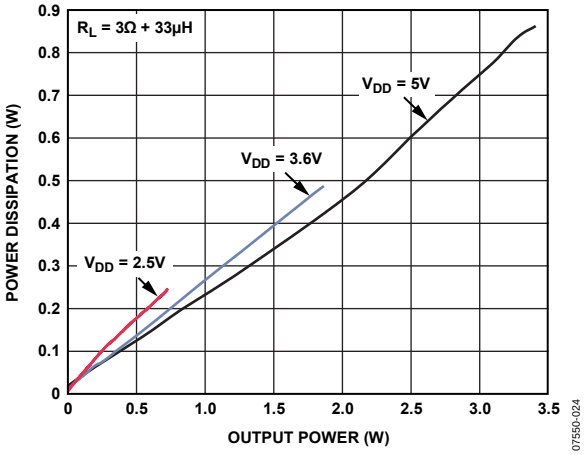


Figure 24. Power Dissipation vs. Output Power into R_L = 3 Ω + 33 µH

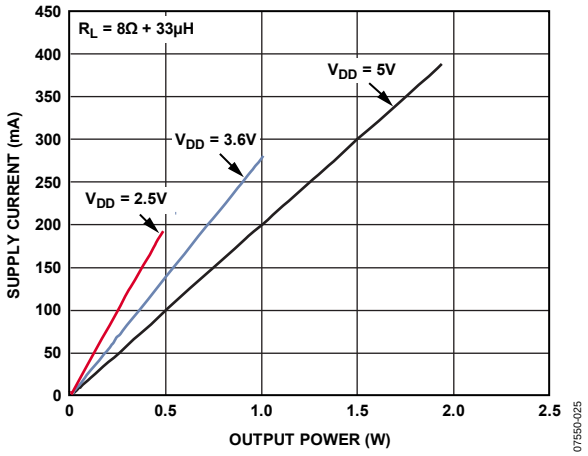


Figure 25. Supply Current vs. Output Power into R_L = 8 Ω + 33 µH

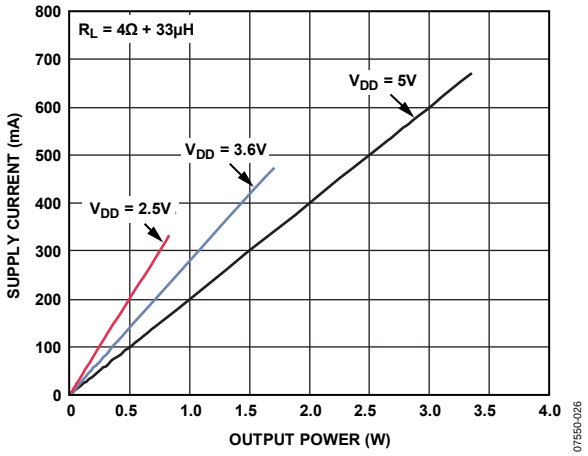


Figure 26. Supply Current vs. Output Power into R_L = 4 Ω + 33 µH

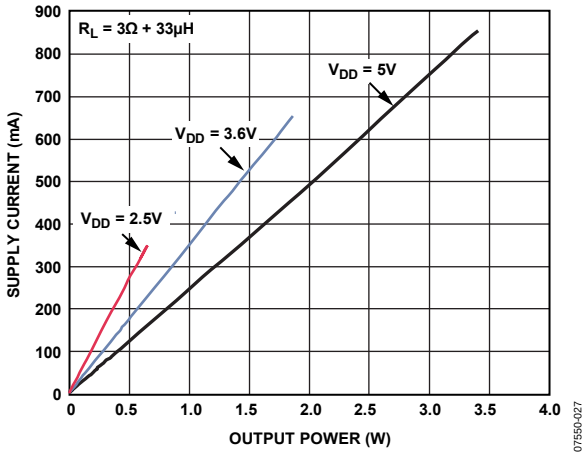


Figure 27. Supply Current vs. Output Power into R_L = 3 Ω + 33 µH

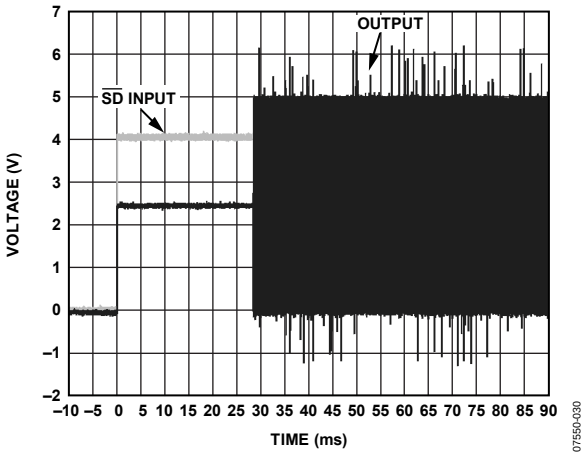


Figure 30. Turn-On Response

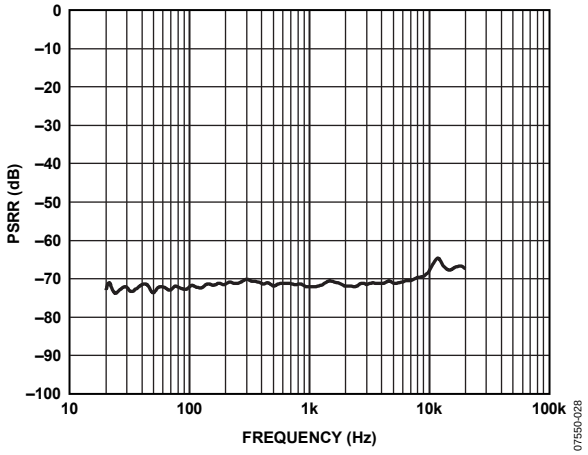


Figure 28. Power Supply Rejection Ratio (PSRR) vs. Frequency

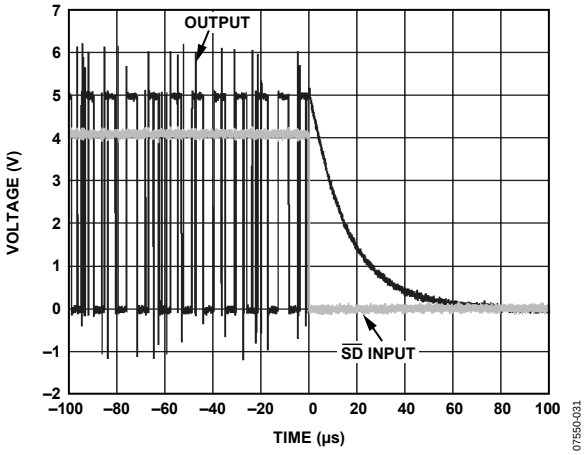


Figure 31. Turn-Off Response

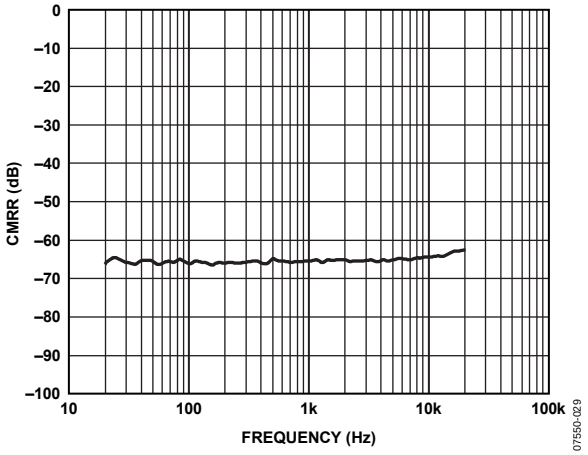


Figure 29. Common-Mode Rejection Ratio (CMRR) vs. Frequency

TYPICAL APPLICATION CIRCUITS

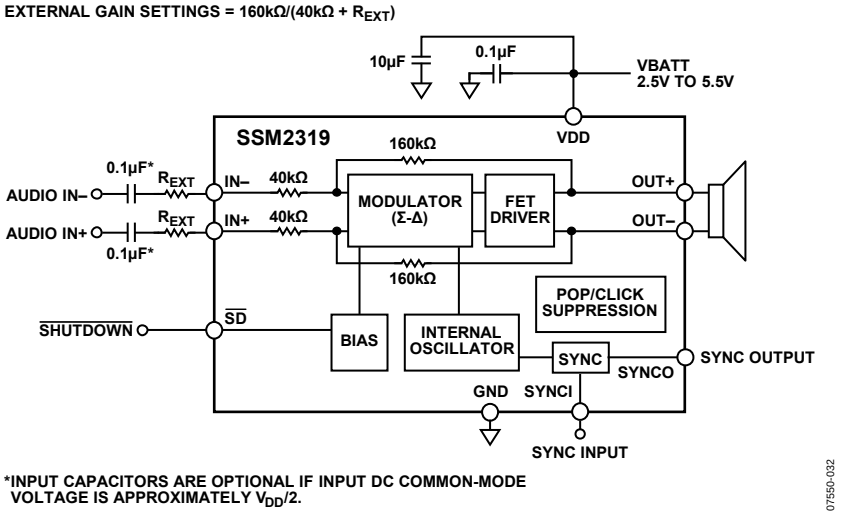


Figure 32. Differential Input Configuration, User-Adjustable Gain

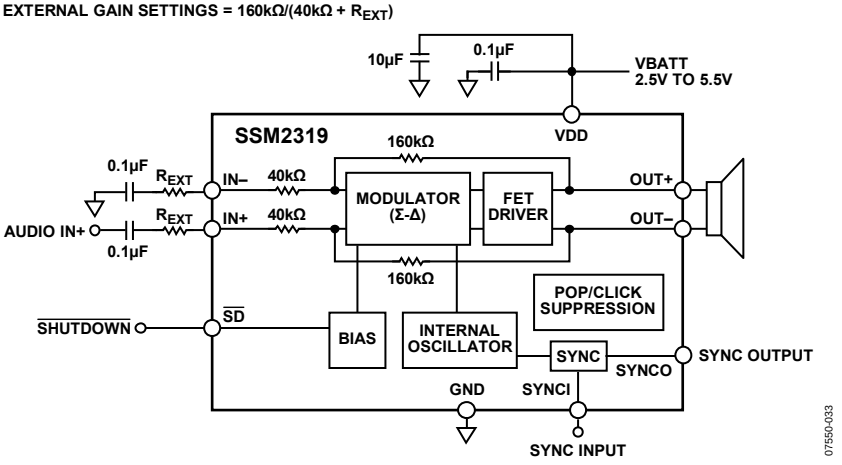
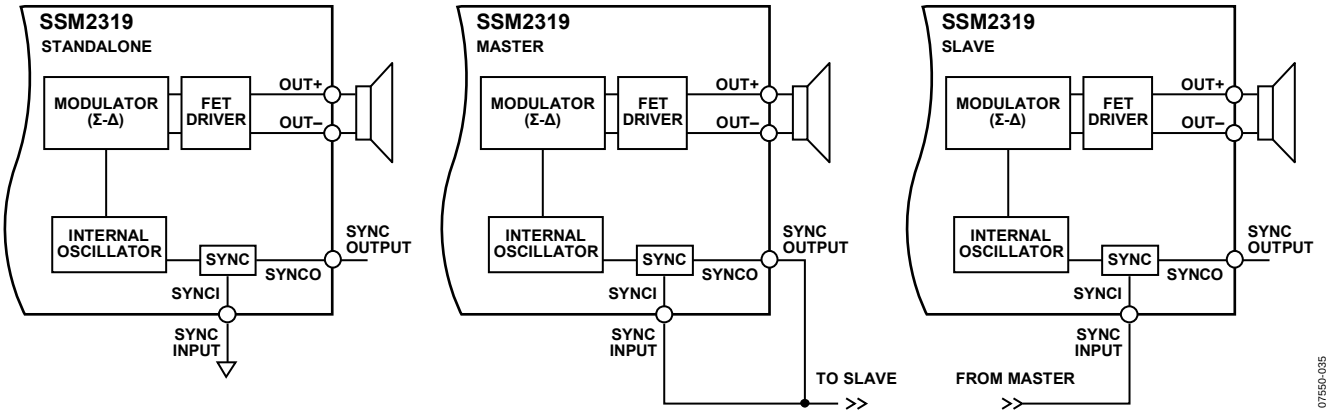


Figure 33. Single-Ended Input Configuration, User-Adjustable Gain



NOTES
1. TRACE LENGTH FROM SYNCI TO SYNCO IS LESS THAN 1mm.

Figure 34. Synchronization Operation Modes

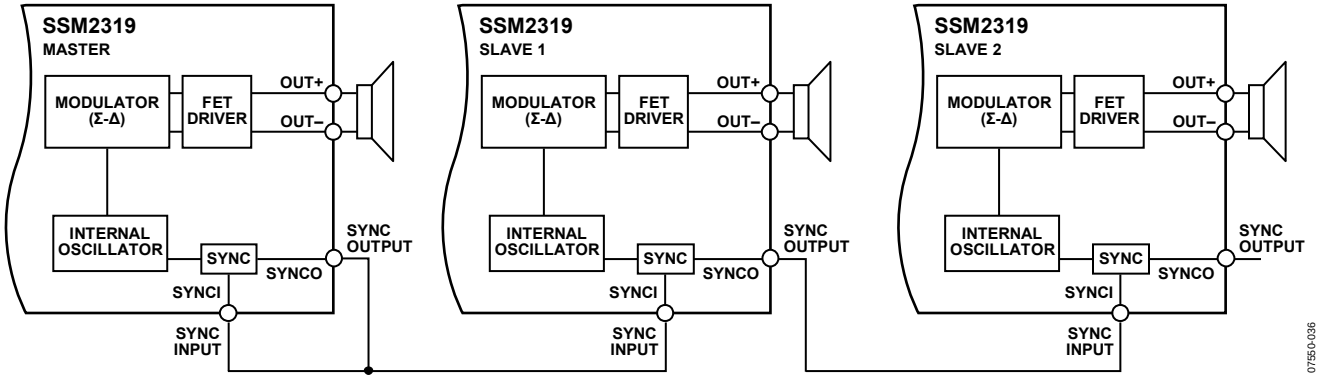


Figure 35. Typical SYNC Master-Slave Daisy-Chain Configuration

THEORY OF OPERATION

OVERVIEW

The SSM2319 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external components count, conserving board space and, thus, reducing systems cost. The SSM2319 does not require an output filter. Instead, it relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2319 uses a Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation reduces the amplitude of spectral components at high frequencies, reducing EMI emission that may otherwise be radiated by speakers and long cable traces. Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM2319 amplifiers.

The SSM2319 also offers protection circuits for overcurrent and temperature protection.

GAIN

The SSM2319 has a default gain of 12 dB that can be reduced by using a pair of external resistors with a value calculated as follows:

$$External\ Gain\ Settings = 160\ k\Omega/(40\ k\Omega + R_{EXT})$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of the audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode. For example, audible transient sources include system power-up/power-down, mute/unmute, an input source change, and a sample rate change. The SSM2319 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM2319 uses 3-level Σ-Δ output modulation. Each output is able to swing from GND to VDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, there are always noise sources present. Due to the constant presence of noise, a differential pulse is generated in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

However, most of the time, the output differential voltage is 0 V, due to the Analog Devices, Inc., patented 3-level, Σ-Δ output modulation feature. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 36 depicts 3-level Σ-Δ output modulation with and without input stimulus.

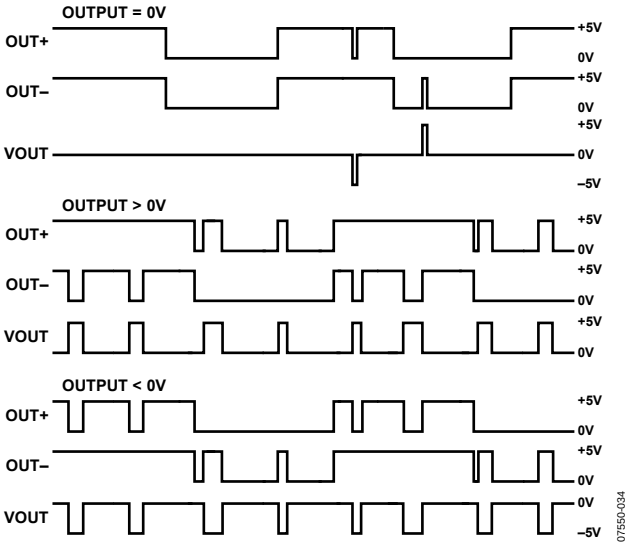


Figure 36. 3-Level Σ-Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power continues to increase, care must be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and to the supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layouts isolate critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more when compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and, similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes or analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2319 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if using a single-ended source. If high-pass filtering is needed at the input, the input capacitor, along with the input resistor of the SSM2319, form a high-pass filter whose corner frequency is determined by

$$f_C = 1/\{2\pi \times (40\ \text{k}\Omega + R_{EXT}) \times C_{IN}\}$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the PSRR performance.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality, low ESL, low ESR capacitor, usually of around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transients noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2319 helps to maintain efficient performance.

SYNCRONIZATION (SYNC) OPERATION

SYNC is the feature that allows an external clock signal to control the modulator of the SSM2319. The SSM2319 can act in standalone mode, act as a master device, or act as a slave device. Although the inherent random switching frequency of the Analog Devices patented 3-level PDM modulation virtually eliminates the need for SYNC, this feature can be activated in the event that end users are concerned about clock intermodulation (beating effect) of several amplifiers in close proximity.

Another use for the SYNC feature is its ability to adjust modulator frequency to move harmonic interference to a less sensitive frequency band in certain applications with very delicate interference requirements.

Although the synchronization frequency operates from 5 MHz to 12 MHz, the optimal operating range is 6 MHz to 9 MHz.

Modulator synchronization is initiated after the internal shut-down signal is released. SYNCO buffers the internal oscillator clock with a delay of 127 clock cycles.

When synchronizing several SSM2319 amplifiers, configure them in a daisy-chain configuration, as shown in Figure 35. Using this configuration causes a small delay in the SYNCO-to-SYNCO transitions of multiple SSM2319s, preventing large surges of instantaneous current and reducing excessive loading of the power supply.

When configuring one device to act as a master device, it is mandatory that the connection from SYNCO to SYCNI be less than 1 mm. As in many digital systems, to maintain signal integrity when interfacing several clocking systems, users must insert series dumping resistors close to the SYNCO pin if long trace lengths are used for synchronization connections. A typical value used is 750 Ω. The series dumping resistor should be placed as close to the SYNCO pin as possible. If careful layout practices are followed to minimize signal trace routing from the SYNCO pin of one device to the SYNCI pin of another, a dumping resistor is not necessary. If the SYNC feature is not used, or if the SYNC feature is not interfacing the SYNCO pin to an external device, it is recommended that the SYNCO pin be floated.

Operating Modes

The SYNC operating modes include the following:

- Initial SYNC startup. An internal reference signal, REF, is released after one complete internal clock cycle (MCLK). After REF is released, another internal signal, MOD, waits 127 internal clock cycles. This operates as a training signal to determine the SYNCI/SYNCO connection. During this time, SYNCO is the internal clock signal.
- SYNCI = GND or VDD. SYNCO stops generating pulses. The modulator is controlled by an internal clock signal, as shown in Figure 37.

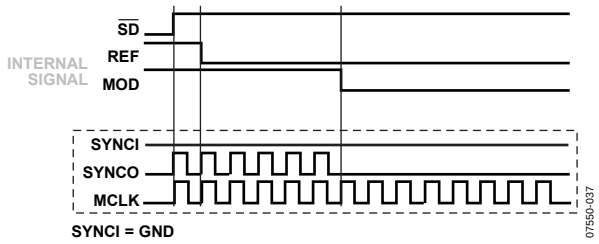


Figure 37. SYNCI = GND or VDD

- SYNCI = SYNCO. SYNCO is the delayed clock signal of SYNCI, as shown in Figure 38.

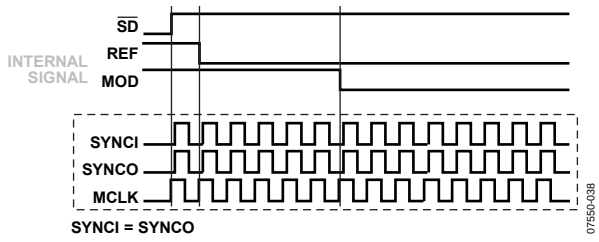


Figure 38. SYNCI = SYNCO

- SYNCI = external clock. SYNCO is a buffered clock output sourced from an external clock signal. One clock cycle after the internal modulator detect signal is released, an irregular pulse appears on MCLK before the first buffered output signal begins on SYNCO, as shown in Figure 39.

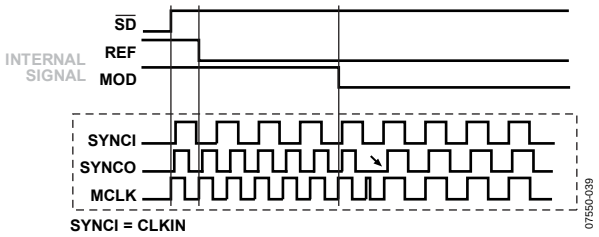


Figure 39. SYNCI = External Clock

- SYNCI = GND, transitions to clock. When the SYNCI pin is connected to GND first but then transitions to a clock signal, SYNCO generates several internal clock signals before finally being synchronized to the external clock signal, as shown in Figure 40.

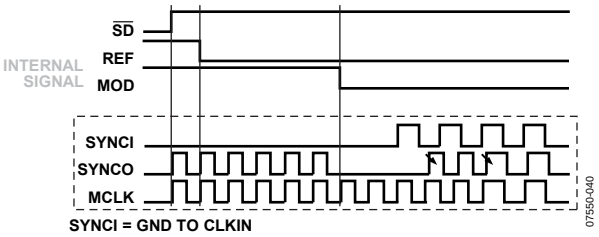


Figure 40. SYNCI = GND to Clock Input

- SYNCI = CLK, transitions to GND. When SYNCI is connected to a clock signal but then transitions to GND, the SYNCO pin immediately stops generating a clock signal. After a short clock loss detect time, the internal modulator synchronizes to the internal clock signal, as shown in Figure 41.

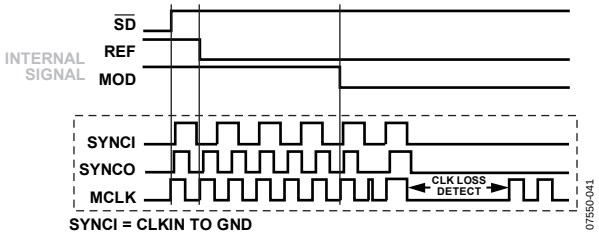


Figure 41. SYNCI = Clock Input to GND

OUTLINE DIMENSIONS

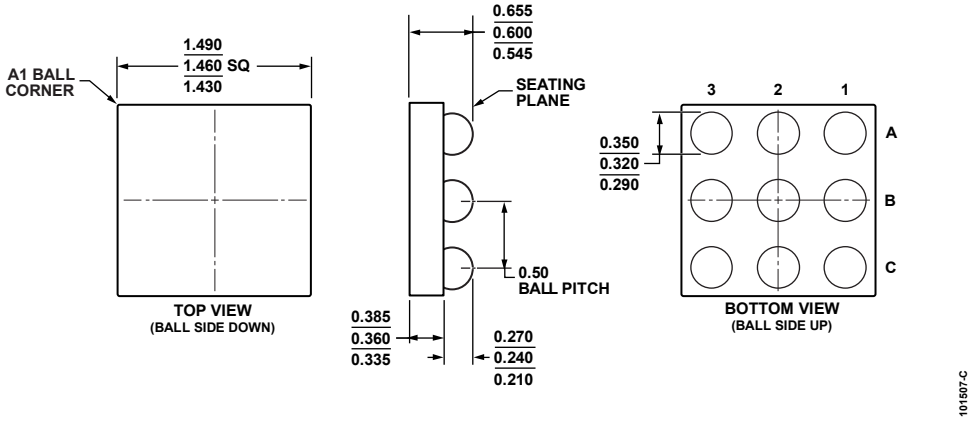


Figure 42. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SSM2319CBZ-R2[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
SSM2319CBZ-REEL[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
SSM2319CBZ-REEL7[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
EVAL-SSM2319Z[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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