Filterless High Efficiency Mono 3 W Class-D Audio Amplifier

Preliminary Technical Data

SSM2375

FEATURES

Filterless Class-D amplifier with spread-spectrum Σ-Δ modulation
3 W into 3 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with <1% total harmonic distortion (THD)
93% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
>100 dB signal-to-noise ratio (SNR)
High PSRR @ 217 Hz: 80dB
Flexible gain adjustment pin: 0dB to 12dB in 3dB steps
Fixed Input Impedance, 80kΩ
User-selectable ultralow EMI emissions mode
Single-supply operation from 2.5 V to 5.5 V
20 nA shutdown current
Short-circuit and thermal protection with auto recovery
Available in 9-ball, 1.5 mm × 1.5 mm WLCSP
Pop-and-click suppression

APPLICATIONS

Mobile phones
MP3 players
Portable electronics

GENERAL DESCRIPTION

The SSM2375 is a fully integrated, high efficiency Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 3 W of continuous output power with less than 1% THD + N driving an 3 Ω load from a 5.0 V supply.

The SSM2375 features a high efficiency, low noise modulation scheme that requires no external LC output filters. The modulation operates with high efficiency even at low output power. It operates with 93% efficiency at 1.4 W into 8 Ω or 85% efficiency at 3 W into 3 Ω from a 5.0 V supply and has an SNR of >100 dB.

Spread-spectrum pulse density modulation (PDM) is used to provide lower EMI-radiated emissions compared with other Class-D architectures. The inherent randomized nature of spread-spectrum PDM eliminates clock intermodulation (beating effect) of several amplifiers in close proximity.

The SSM2375 includes an optional modulation select pin (ultralow EMI emission mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz and can pass FCC Class B radiated emissions testing with 50cm unshielded speaker cable without any external filtering. The device also includes a highly flexible gain select pin that only requires one series resistor in order to select between 0dB, 3dB, 6dB, 9dB, or 12dB. The benefit of this is to improve gain matching between multiple SSM2375 devices within a single application as compared to using external resistors to set gain.

The SSM2375 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The device also includes pop-and-click suppression circuitry. This minimizes voltage glitches at the output during turn-on and turn-off, reducing audible noise on activation and deactivation.

Other included features to simplify system level integration of the SSM2375 are input low pass filtering to suppress out of band DAC noise interference to the PDM modulator and fixed input impedance to simplify component selection across multiple platform production builds.

The SSM2375 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a halogen-free 9-ball, 1.5 mm × 1.5 mm wafer level chip scale package (WLCSP).

Rev. PrC

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FUNCTIONAL BLOCK DIAGRAM

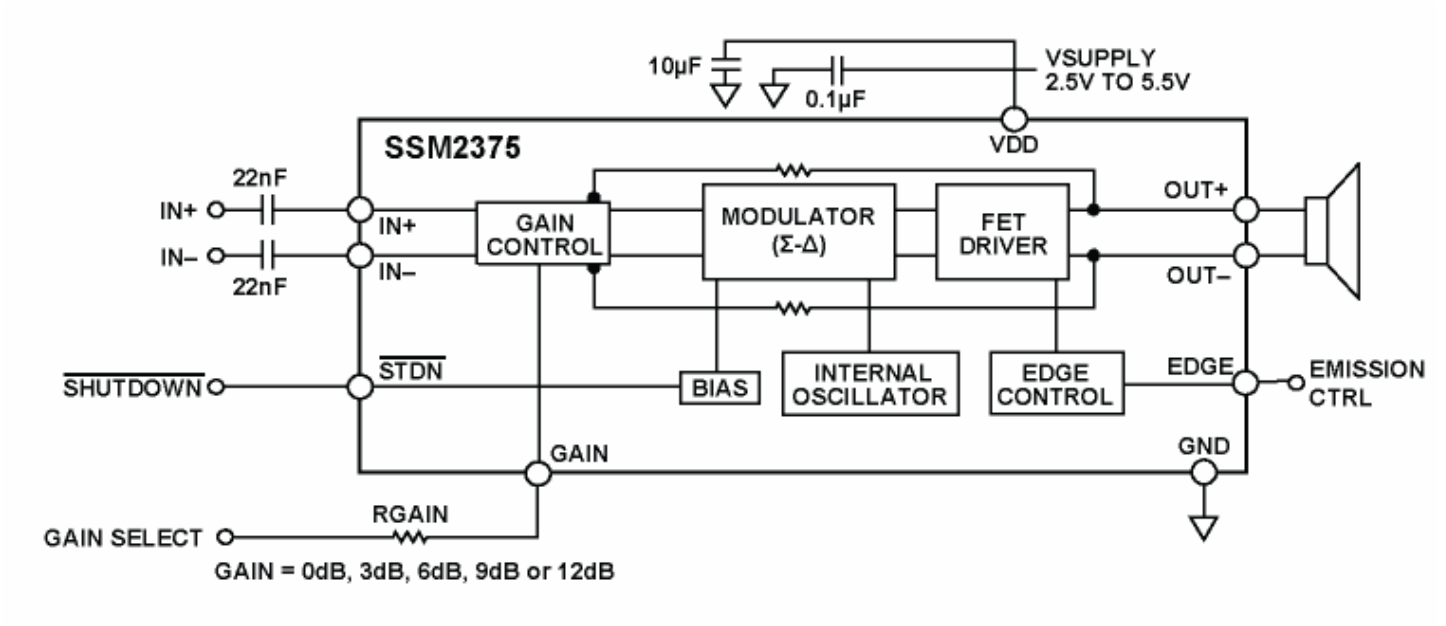

Figure 1.

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SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω +33 µH, EDGE = GND, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_{OUT}	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.42		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.72		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.33		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.77		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.91		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5V		0.42		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.52		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.28		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.56		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.17[1]		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.6		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.72		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.2[1]		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.52		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5V		0.68		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.7[1]		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.9		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.85		W
Efficiency	η	P_{OUT} = 1.4 W, 8 Ω, V_{DD} = 5.0 V		93		%
Total Harmonic Distortion + Noise	THD + N	P_{OUT} = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.01		%
		P_{OUT} = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.01		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} – 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, output referred		55		dB
Average Switching Frequency	f_{SW}			250		kHz
Differential Output Offset Voltage	V_{OOS}	G = 6 dB		0.1	5.0	mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating/ground		78		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac GND, C_{IN} = 0.1 µF		80		dB
		V_{RIPPLE} = 100 mV at 1 kHz, inputs ac GND, C_{IN} = 0.1 µF		80		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		3.0		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		2.7		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		2.5		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 5.0 V		3.1		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 3.6 V		2.8		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 2.5 V		2.6		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Av		0		12	dB
Input Impedance	Z_{IN}	$\overline{SD}$ = VDD, Fixed Input Impedance (0-12dB)		80		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}		1.35			V
Input Voltage Low	V_{IL}				0.35	V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		12.5		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 5 V, f = 20 Hz to 20 kHz, inputs are ac grounded, A_V = 6 dB, A weighting		30		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 1.4 W, R_L = 8 Ω		100		dB

[1] Although the SSM2375 has good audio quality above 3 W, continuous output power beyond 3 W must be avoided due to device packaging limitations.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Susceptibility	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-ball, 1.5 mm × 1.5 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

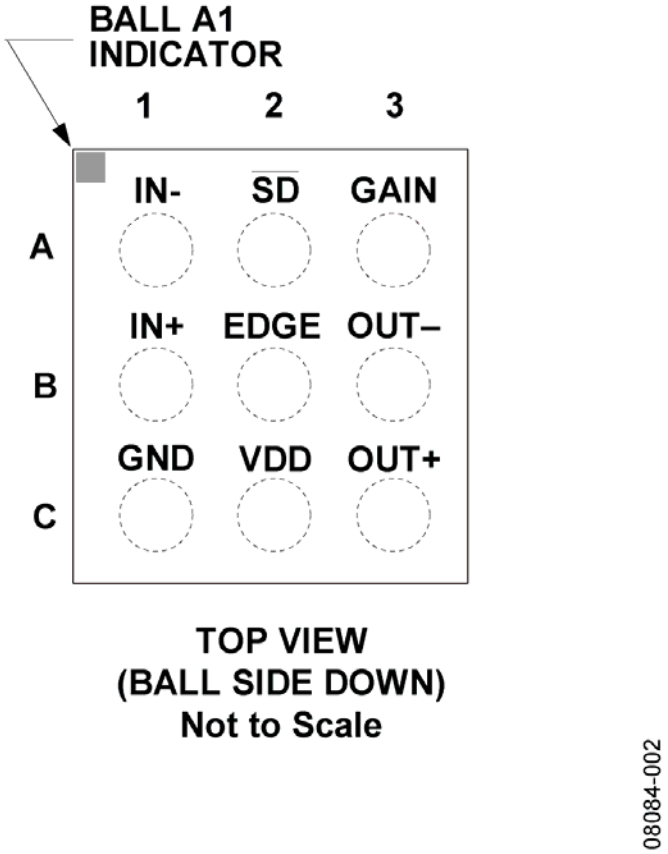

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	IN–	Inverting Input.
1B	IN+	Noninverting Input.
1C	GND	Ground.
2A	$\overline{SD}$	Shutdown Input. Active low digital input.
2B	EDGE	Edge Rate Control. Active high.
2C	VDD	Power Supply.
3A	GAIN	Gain Control Pin
3B	OUT–	Inverting Output.
3C	OUT+	Noninverting Output.

TYPICAL PERFORMANCE CHARACTERISTICS

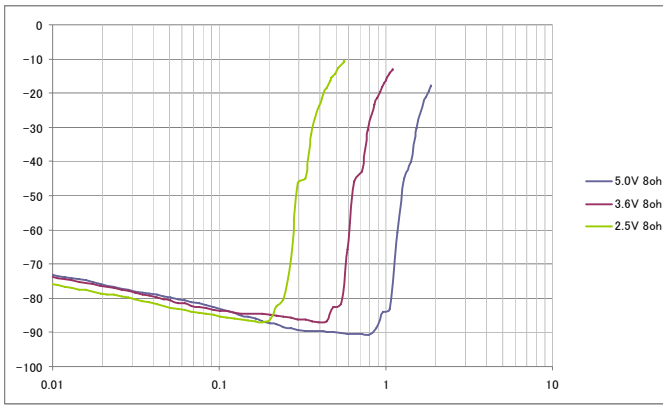

Figure 3. THD + N vs. Output Power into 8 Ω + 33 µH

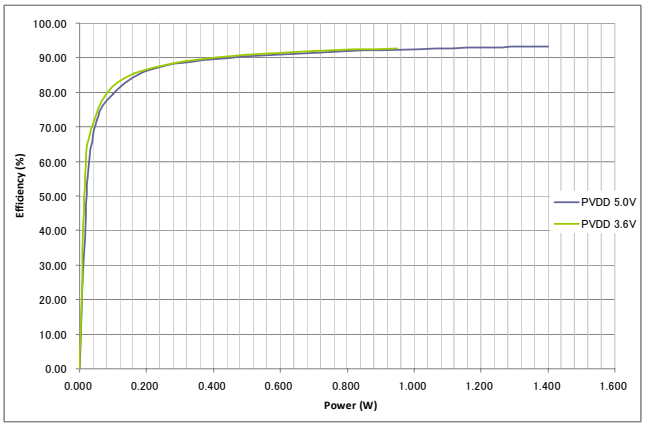

Figure 4. Efficiciency into 8Ω + 33 µH load

TYPICAL APPLICATION CIRCUITS

TBD

THEORY OF OPERATION

OVERVIEW

The SSM2375 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing systems cost. The SSM2375 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2375 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM2375 amplifiers. The SSM2375 also integrates overcurrent and temperature protection.

GAIN SELECTION

In addition, preset gain of SSM2375 can be set from 0dB to 12 dB in 3dB steps with one external resistor (optional). The external resistor is used to select 9dB and 12dB gain settings, as shown below in *Table 5*.

Table 5. Gain Function Descriptions

Gain Setting	GAIN Pin Configuration
12dB	Tie to VDD through 47k Ω
9dB	Tie to GND through 47k Ω
6dB	Tie to VDD
3dB	Open
0dB	Tie to GND

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers may occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal.

The SSM2375 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation from the $\overline{SD}$ control pin.

EMI NOISE

The SSM2375 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. For applications having difficulty passing FCC Class B emission tests, the SSM2375 includes a modulation select pin (ultralow EMI emission mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. Figure 5 shows SSM2375 EMI emission tests performed in a certified FCC Class-B laboratory in normal emissions mode (EDGE = GND). Figure 6 shows SSM2375 EMI emission with EDGE = V_{DD}, placing the device in low emissions mode.

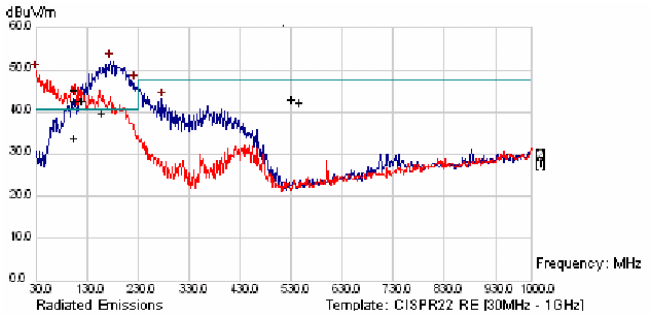

Figure 5. EMI Emissions from SSM2375, 50 cm Cable, 5V V_{DD}, EDGE = GND

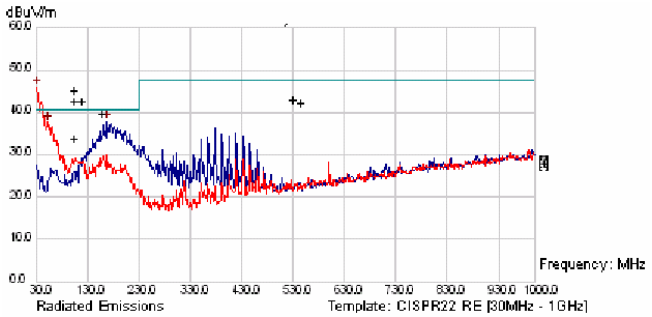

Figure 6. EMI Emissions from SSM2375, 50cm Cable, 5V V_{DD}, EDGE = V_{DD}

The measurements for Figure 5 and Figure 6 were taken in an FCC-certified EMI laboratory with a 1 kHz input signal, producing 0.5 W output power into an 8 Ω load from a 5 V supply. Cable length was 50 cm, unshielded twisted pair speaker cable. Note that reducing the supply voltage greatly reduces radiated emissions.

OUTPUT MODULATION DESCRIPTION

The SSM2375 uses three-level, Σ-Δ output modulation. Each output can swing from GND to V_{DD} and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, there are always noise sources present.

Due to this constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated. However, most of the time, output differential voltage is 0 V, due to the Analog Devices three-level,

Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse is generated to follow input voltage. The differential pulse density is increased by raising the input signal level. Figure 7 depicts three-level, Σ-Δ output modulation with and without input stimulus.

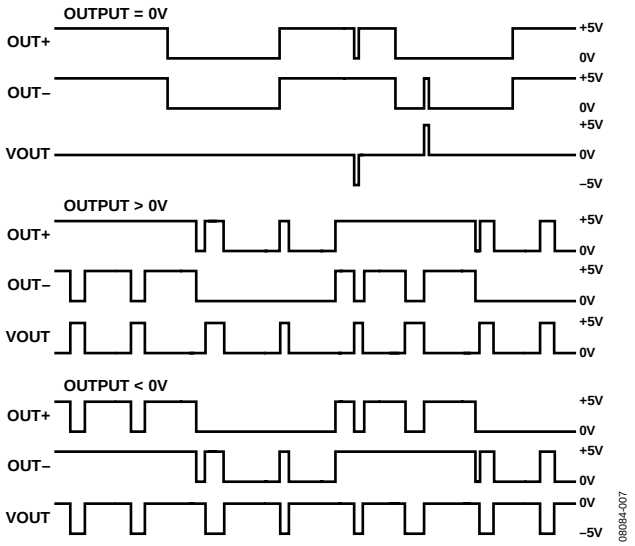

Figure 7. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power continues to increase, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz. or 2 oz. copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal.

To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances. In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be directly beneath the analog power plane, and, similarly, the digital ground plane should be directly beneath the digital power plane. There should be no overlap between analog and digital ground planes or between analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2375 does not require input coupling capacitors if the input signal is biased from 1.0 V to VDD − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the SSM2375 form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the DC PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with a good quality, low ESL, low ESR capacitor, greater than 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2375 helps to maintain efficient performance.

OUTLINE DIMENSIONS

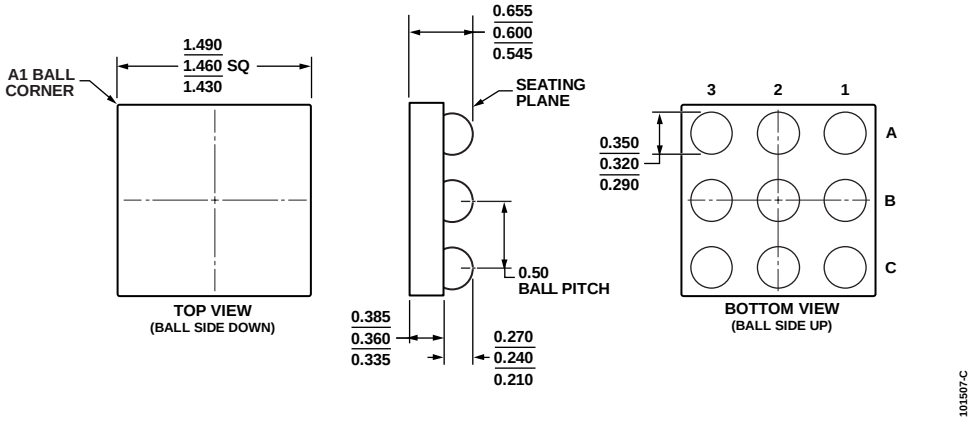

Figure 8. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-2)
Dimensions shown in millimeters

PR09011-0-3/10(PrC)