Low Power Audio Codec

Preliminary Technical Data

SSM2602

FEATURES

Stereo, 24-bit analog-to-digital and digital-to-analog converters
DAC SNR: 98 dB (A-weighted), THD: −80 dB at 48 kHz, 3.3 V
ADC SNR: 90 dB (A-weighted), THD: −80 dB at 48 kHz, 3.3 V
Highly efficient headphone amplifier
Complete stereo/mono or microphone/line interface
Low power
- **7 mW stereo playback (1.8 V/1.8 V supplies)**
- **14 mW record and playback (1.8 V/1.8 V supplies)**

Low supply voltages
- **Analog: 1.8 V to 3.6 V**
- **Digital core: 1.8 V to 3.6 V**
- **Digital I/O: 1.8 V/3.6 V**

256 f_S/384 f_S or USB master clock rate: 12 MHz, 24 MHz
Audio sample rates: 8 kHz,16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz
28-lead, 5 mm × 5 mm LFCSP (QFN) package

APPLICATIONS

Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2602 is a low power, high quality stereo audio codec for portable digital audio applications with stereo programmable gain amplifier (PGA) line and monaural microphone inputs. It features two 24-bit analog-to-digital converter (ADC) channels and two 24-bit digital-to-audio (DAC) converter channels.

The SSM2602 can operate as a master or a slave. It offers various master clock frequencies, including 12 MHz or 24 MHz for USB devices; standard 256 f_S rates, such as 12.288 MHz and 24.576 MHz; and many common audio-sampling rates, such as 96 kHz, 88.2 kHz, 48 kHz, 44.1 kHz, 32 kHz, 16 kHz, and 8 kHz.

The SSM2602 can operate at power supplies as low as 1.8 V for the analog circuitry and 1.5 V for the digital circuitry. The maximum voltage supply is 3.6 V for all supplies.

The SSM2602 software-programmable output options provide the user with many application options, such as speaker driver, headphone driver, or both. Its volume control functions provide a large range of gain control of the audio signal.

The SSM2602 is specified over the industrial temperature range of −40°C to +85°C. It is available in a 28-lead, 5 mm × 5 mm lead frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

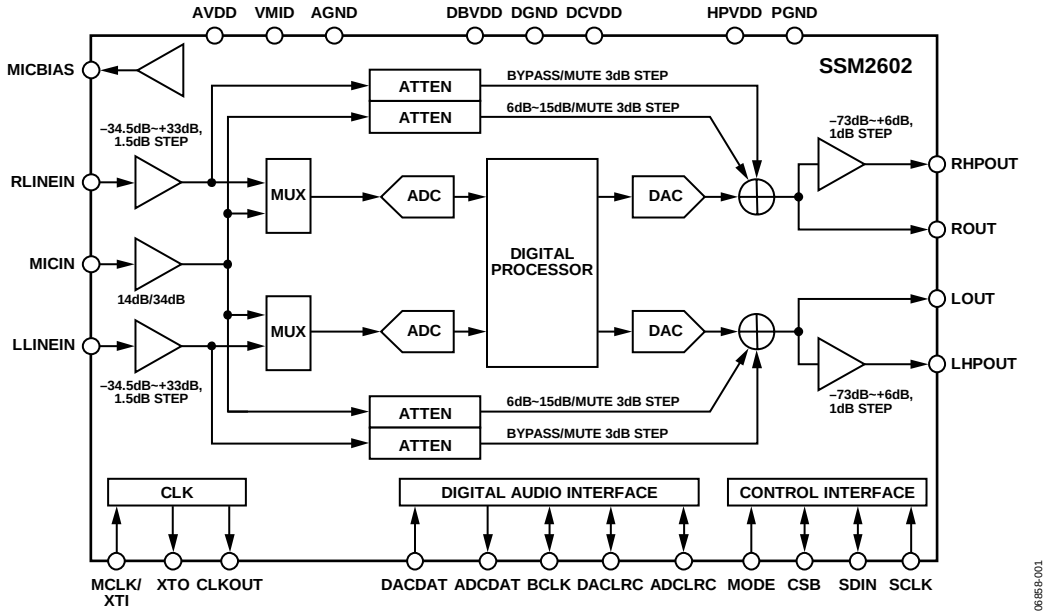

Figure 1.

Rev. PrB

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REVISION HISTORY

9/07—Revision PrB: Preliminary Version

SPECIFICATIONS

T_A = 25°C, AVDD = DVDD = 3.3 V, PVDD = 3.3 V, 1 kHz signal, f_S = 48 kHz, PGA gain = 0 dB, 24-bit audio data, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
OPERATING CONDITIONS					
Analog Voltage Supply (AVDD)	1.8	3.3	3.6	V	
Digital Power Supply	1.5	3.3	3.6	V	
Ground (AGND, PGND, DGND)		0		V	
POWER CONSUMPTION					
Power-Up					
Stereo Record (1.8 V)		7		mW	
Stereo Record (3.3 V)		22		mW	
Stereo Playback (1.8 V)		7		mW	
Stereo Playback (3.3 V)		22		mW	
Power-Down			40	µW	
LINE INPUT					
Input Signal Level (0 dB)		1 × AVDD/3.3		V rms	
Input Impedance		200		kΩ	PGA gain = 0 dB
		10		kΩ	PGA gain = +33 dB
		480		kΩ	PGA gain = −34.5 dB
Input Capacitance		10		pF	
Signal-to-Noise Ratio (A-weighted)	85	90		dB	PGA gain = 0 dB, AVDD = 3.3 V
		87		dB	PGA gain = 0 dB, AVDD = 1.8 V
Total Harmonic Distortion (THD)		−80		dB	−1 dBFS input, AVDD = 3.3 V
		−75		dB	−1 dBFS input, AVDD = 1.8 V
Channel Separation		80		dB	
Programmable Gain	−34.5	0	33.5	dB	
Gain Step		1.5		dB	
Mute Attenuation		−80		dB	
MICROPHONE INPUT					
Input Signal Level		1		V rms	
Signal-to-Noise Ratio (A-weighted)		85		dB	Microphone gain = 0 dB (R_{SOURCE} = 40 kΩ)
Total Harmonic Distortion		−70		dB	0 dBFS input, 0 dB gain
Power Supply Rejection Ratio		50		dB	
Mute Attenuation		80		dB	
Input Resistance		10		kΩ	
Input Capacitance		10		pF	
MICROPHONE BIAS					
Bias Voltage		0.75 × AVDD		V	
Bias Current Source			3	mA	
Noise in the Signal Bandwidth		40		nV/√Hz	20 Hz to 20 kHz
LINE OUTPUT					
DAC					−1 dBFS input DAC + line output
Full-Scale Output		1 × AVDD/3.3		V rms	
Signal-to-Noise Ratio (A-Weighted)		100		dB	AVDD = 3.3 V
		98			AVDD = 1.8 V
THD + N		−80		dB	AVDD = 3.3 V
		−75			AVDD = 1.8 V
Power Supply Rejection Ratio		50		dB	
Channel Separation		80		dB	

Parameter	Min	Typ	Max	Unit	Conditions
HEADPHONE OUTPUT					
Full-Scale Output Voltage		1 × AVDD/3.3		V rms	
Maximum Output Power		30		mW	R_L = 32 Ω
		60		mW	R_L = 16 Ω
Signal-to-Noise Ratio (A-Weighted)	92	100		dB	
THD + N		−50		dB	P_{OUT} = 10 mW
		−55		dB	P_{OUT} = 20 mW
Power Supply Rejection Ratio		50		dB	
Mute Attenuation		80		dB	
LINE INPUT TO LINE OUTPUT					
Full-Scale Output Voltage		1 × AVDD/3.3		V rms	
Signal-to-Noise Ratio (A-Weighted)		96		dB	
Total Harmonic Distortion		−80		dB	
Power Supply Rejection		50		dB	
MICROPHONE INPUT TO HEADPHONE OUTPUT					
Full-Scale Output Voltage		1 × AVDD/3.3		V rms	
Signal-to-Noise Ratio (A-Weighted)		98		dB	
Power Supply Rejection Ratio		50		dB	
Programmable Attenuation	6		15	dB	
Gain Step		3		dB	
Mute Attenuation		80		dB	

RECOMMENDED OPERATING CONDITIONS

Table 2.

Parameter	Min	Typ	Max	Unit
Analog Voltage Supply (AVDD)	1.8	3.3	3.6	V
Digital Power Supply	1.5	3.3	3.6	V
Ground (AGND, PGND, DGND		0		V

DIGITAL FILTER CHARACTERISTICS

Table 3.

Parameter	Min	Typ	Max	Unit	Conditions
ADC FILTER					
Pass Band	0		0.445 f_S	Hz	±0.04 dB
		0.5 f_S		Hz	−6 dB
Pass-Band Ripple			±0.04	dB	
Stop Band	0.555 f_S			Hz	
Stop-Band Attenuation	−60			dB	f > 0.567 f_S
High-Pass Filter Corner Frequency		3.7		Hz	−3 dB
		10.4		Hz	−0.5 dB
		21.6		Hz	−0.1 dB
DAC FILTER					
Pass Band	0		0.445 f_S	Hz	±0.03 dB
		0.5 f_S		Hz	−6 dB
Pass-Band Ripple			±0.04	dB	
Stop Band	0.555 f_S			Hz	
Stop-Band Attenuation	−58			dB	f > 0.565 f_S

TIMING CHARACTERISTICS

Table 4.

	Limit			
Parameter	**t_{MIN}**	**t_{MAX}**	**Unit**	**Description**
f_{SCLK}	0	550	kHz	SCLK frequency
t_{SCLKPL}	1.3		µs	SCLK low pulse width
t_{SCLKPH}	600		ns	SCLK high pulse width
t_{SCH}	600		ns	Hold time (start condition)
t_{SCS}	600		ns	Setup time (start condition)
t_{DS}	100		ns	Data setup time
$t_{SDIN-SCLKR}$		300	ns	SDIN, SCLK rise time
$t_{SDIN-SCLKF}$		300	ns	SDIN, SCLK fall time
t_{HCS}	600		ns	Setup time (hold condition)
t_{DH}		900	ns	Data hold time

TIMING DIAGRAMS

TBD

ABSOLUTE MAXIMUM RATINGS

At 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
Supply Voltage	5 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead, 5 mm × 5 mm LFCSP	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

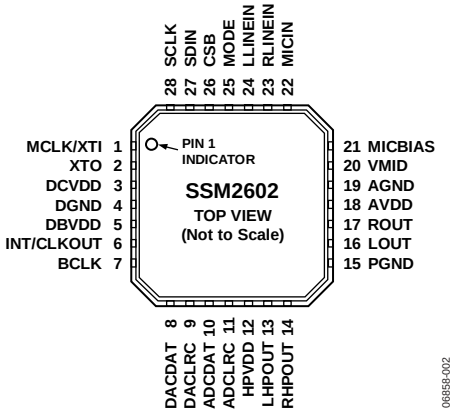

Figure 2. Pin Configuration of SSM2602

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	MCLK/XTI	Digital Input	Master Clock Input/Crystal Input
2	XTO	Digital Output	Crystal Output
3	DCVDD	Digital Supply	Digital Core Supply
4	DGND	Digital Ground	Digital Ground
5	DBVDD	Digital Supply	Digital I/O Supply
6	CLKOUT	Digital Output	Buffered Clock Output
7	BCLK	Digital Input/Output	Digital Audio Bit Clock. This pin is pulled down when the ACTIVE register is set to 0.
8	DACDAT	Digital Input	DAC Digital Audio Data Input
9	DACLRC	Digital Input/Output	DAC Sample Rate Clock (from Left and Right Channels). This pin is pulled down when the ACTIVE register is set to 0.
10	ADCDAT	Digital Output	ADC Digital Audio Data Output
11	ADCLRC	Digital Input/Output	ADC Sample Rate Clock (from Left and Right Channels). This pin is pulled down when the ACTIVE register is set to 0.
12	HPVDD	Analog Supply	Headphone Supply
13	LHPOUT	Analog Output	Left-Channel Headphone Output
14	RHPOUT	Analog Output	Right-Channel Headphone Output
15	PGND	Analog Ground	Headphone Ground
16	LOUT	Analog Output	Left-Channel Line Output
17	ROUT	Analog Output	Right-Channel Line Output
18	AVDD	Analog Supply	Analog Supply
19	AGND	Analog Ground	Analog Ground
20	VMID	Analog Output	Middle Voltage Decoupling Capacitor
21	MICBIAS	Analog Output	Microphone Bias
22	MICIN	Analog Input	Microphone Input Signal
23	RLINEIN	Analog Input	Right-Channel Line/Microphone Input
24	LLINEIN	Analog Input	Left-Channel Line/Microphone Input
25	MODE	Digital Input	Control Interface Selection to Select I²C®/SPI
26	CSB	Digital Input	3-Wire MPU Chip Select/2-Wire MPU Interface Address Selection, Active Low. This pin is pulled up when the ACTIVE register is set to 0.
27	SDIN	Digital Input/Output	3-Wire MPU Data Input/2-Wire MPU Data Input/Output
28	SCLK	Digital Input	3-Wire MPU Clock Input/2-Wire MPU Clock Input

TYPICAL PERFORMANCE CHARACTERISTICS

CONVERTER FILTER RESPONSE

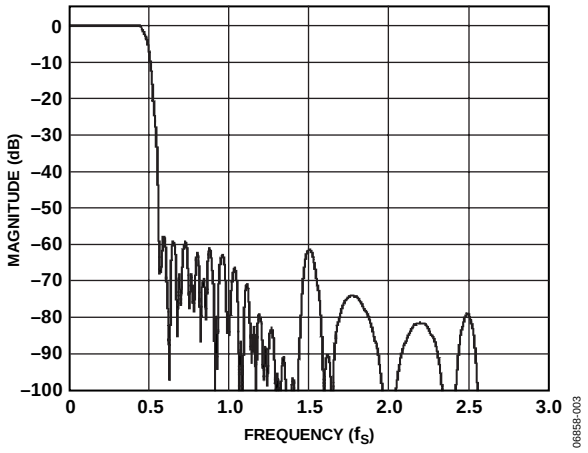

Figure 3. ADC Digital Filter Frequency Response

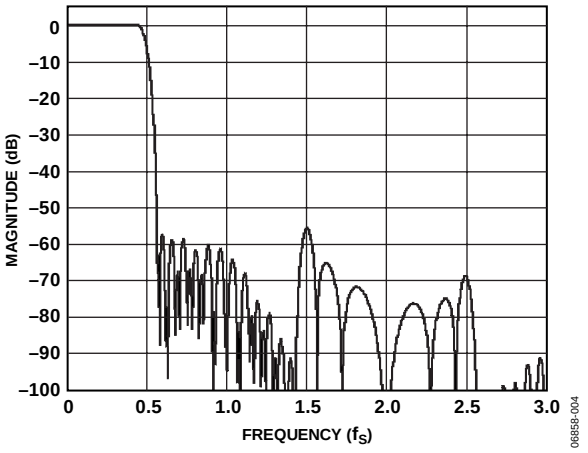

Figure 5. DAC Digital Filter Frequency Response

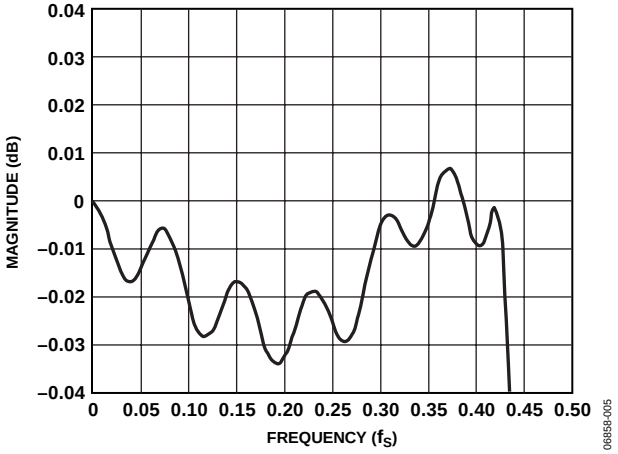

Figure 4. ADC Digital Filter Ripple

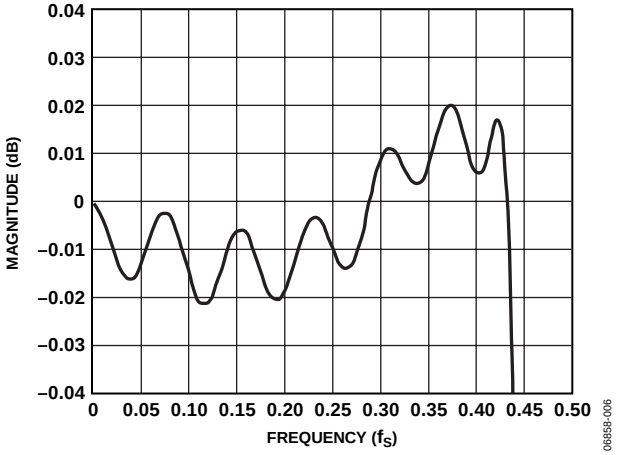

Figure 6. DAC Digital Filter Ripple

DIGITAL DE-EMPHASIS CHARACTERISTICS

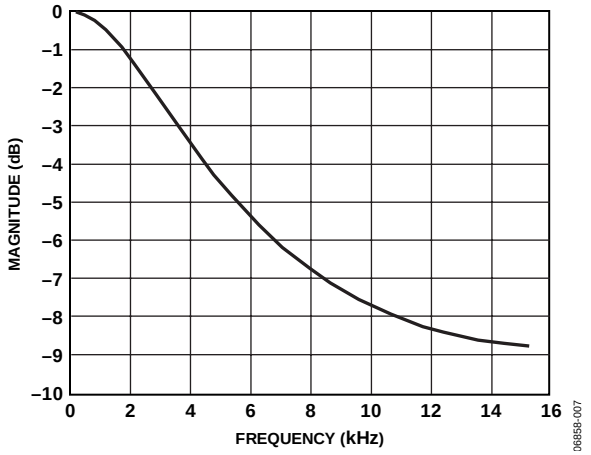

Figure 7. De-Emphasis Frequency Response (32 kHz)

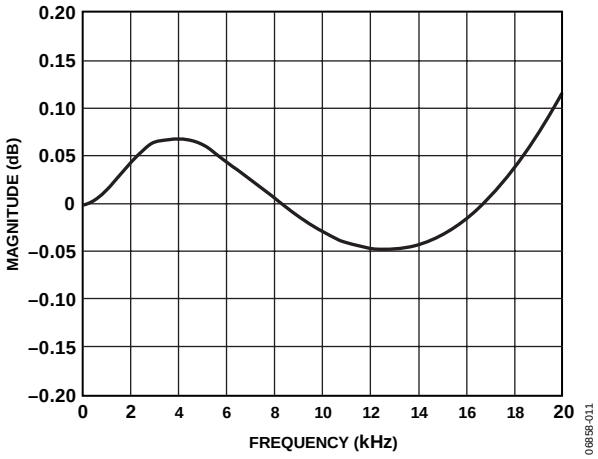

Figure 10. De-Emphasis Error (44.1 kHz)

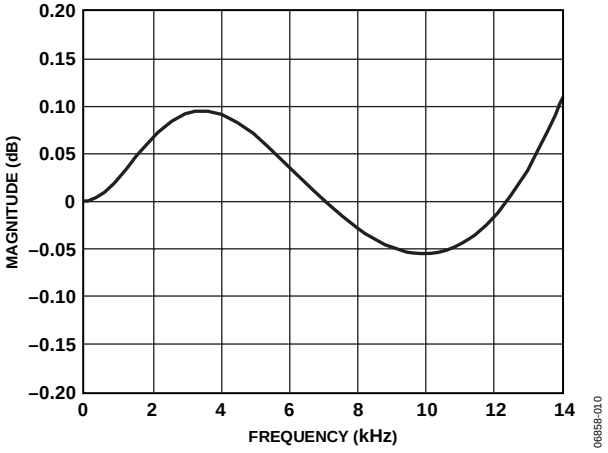

Figure 8. De-Emphasis Error (32 kHz)

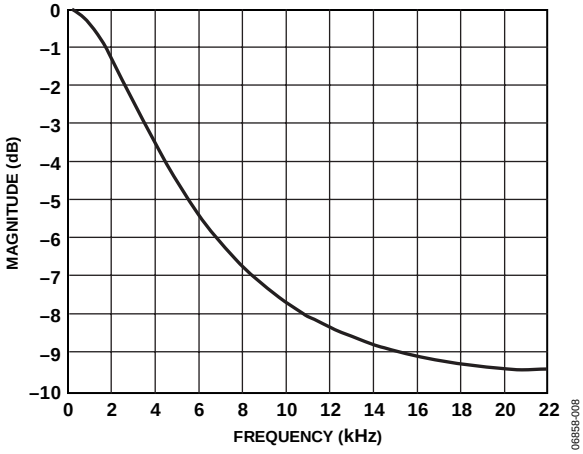

Figure 11. De-Emphasis Frequency Response (48 kHz)

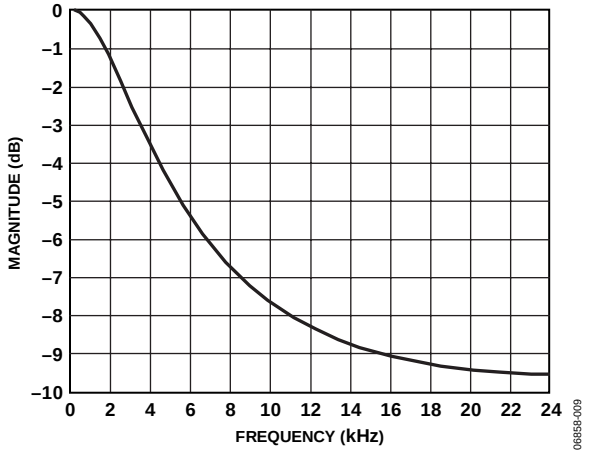

Figure 9. De-Emphasis Frequency Response (44.1 kHz)

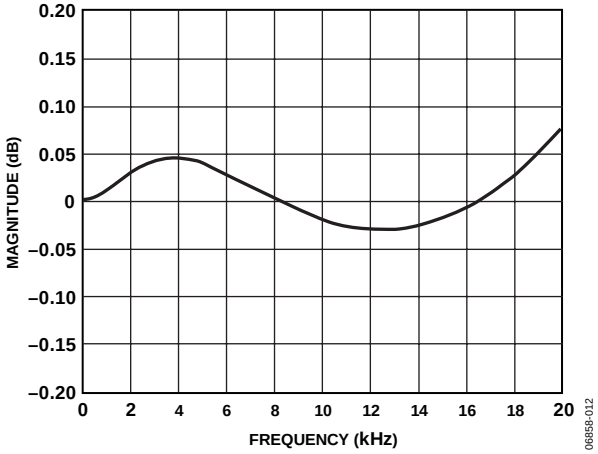

Figure 12. De-Emphasis Error (48 kHz)

THEORY OF OPERATION

ADC HIGH-PASS FILTER

DC offset can be removed by using the SSM2602 adjustable digital high-pass filter (see Table 3 for characteristics).

Digital Filter Characteristics

The ADC and DAC employ separate digital filters.

AUTOMATIC LEVEL CONTROL (ALC)

Codec has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

Decay (Gain Ramp-Up) Time

This is the time for the PGA gain to ramp up through 90% of its range. The time for the recording level to return to its target value therefore depends on both the decay time and the gain adjustment required. If the gain adjustment is small, the time to return to the target value will be less than the decay time.

Attack (Gain Ramp-Down) Time

This is the time for the PGA gain to ramp down through 90% of its range. The time for the recording level to return to its target value therefore depends on both the attack time and the gain adjustment required. If the gain adjustment is small, the time to return to the target value will be less than the attack time.

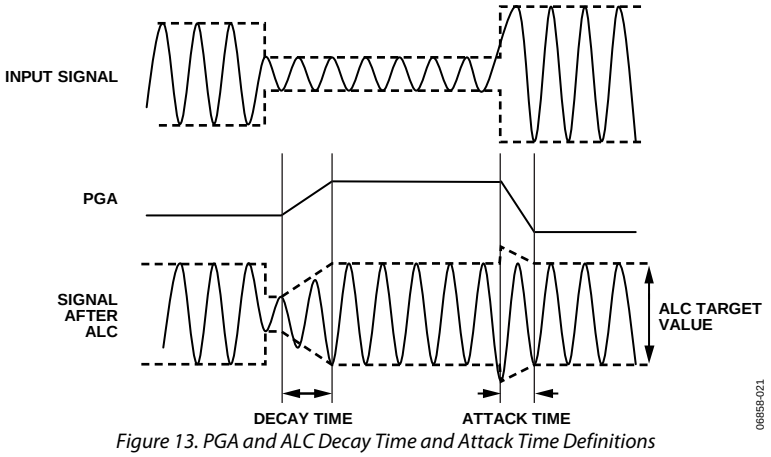

Figure 13. PGA and ALC Decay Time and Attack Time Definitions

ANALOG INTERFACE

Microphone Input

High impedance input MIC

TBD

Headphone Output

TBD

Sidetone Insertion

TBD

DIGITAL AUDIO INTERFACE

The digital audio input can support various communication protocols:

- Right justified
- Left justified
- I²S mode
- Digital-signal processor (DSP) mode

The mode selection is performed by writing to the FORMAT [1:0] bits of the digital audio interface register (Register R7). All modes are MSB first and operate with data of 16 to 32 bits.

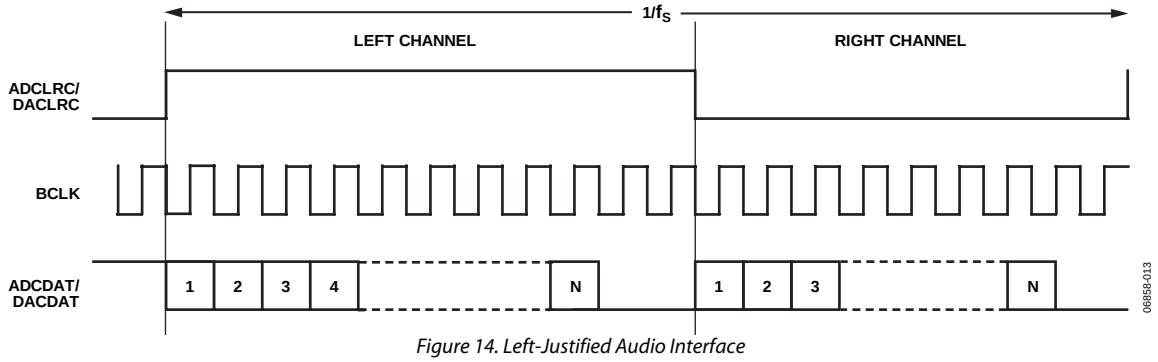

Figure 14. Left-Justified Audio Interface

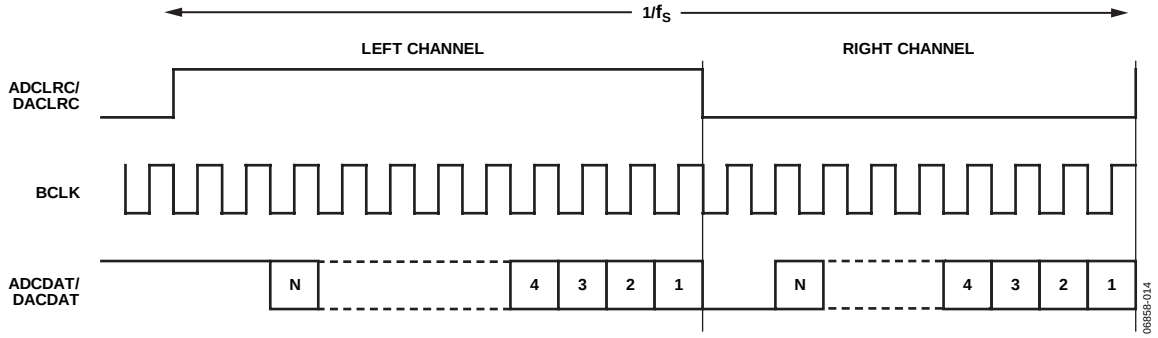

Figure 15. Right-Justified Audio Interface

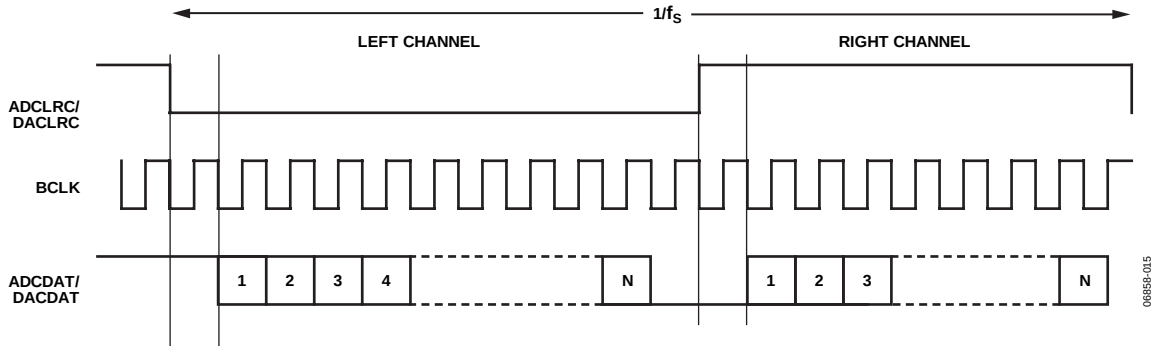

Figure 16. I²S Audio Interface

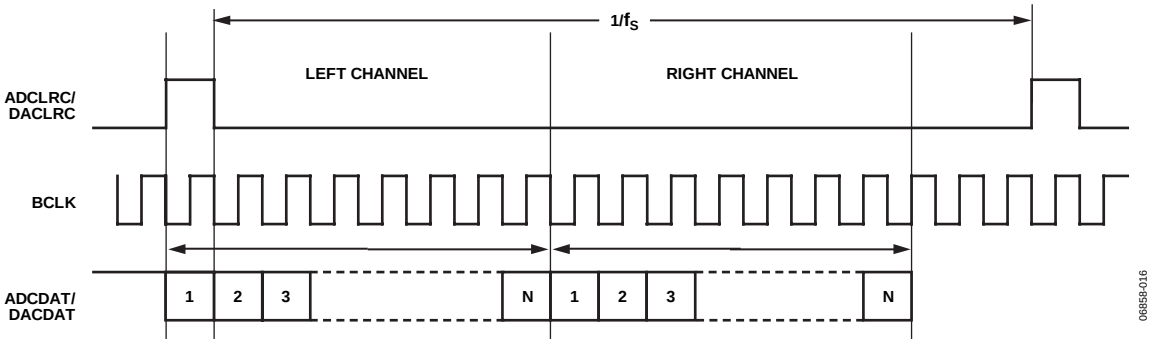

Figure 17. DSP/Pulse Code Modulation (PCM) Mode Audio Interface Submode 1 (SM1) [Bit LRP = 0]

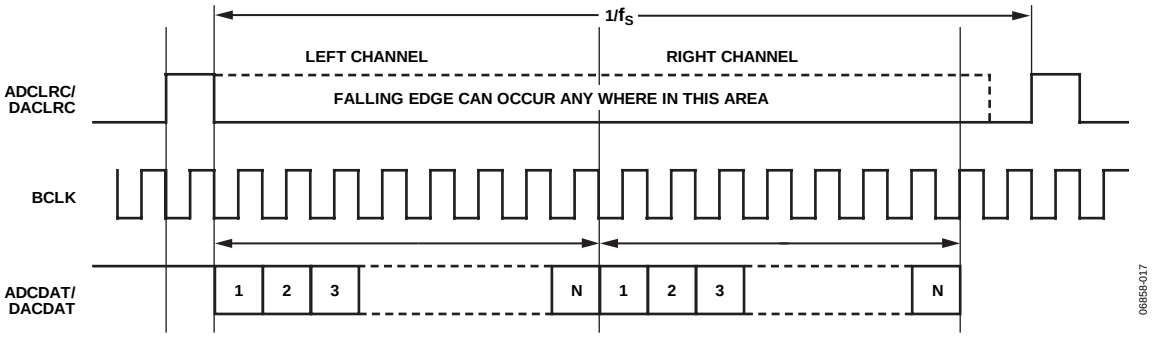

Figure 18. DSP/PCM Mode Audio Interface Submode 2 (SM2) [Bit LRP = 1]

SOFTWARE CONTROL INTERFACE

The software control interface can be operated with a 3-wire (SPI) or 2-wire (I^2C) interface. Selection of the interface format is achieved by setting the state of the MODE pin.

Table 8. Selecting the Interface Format

MODE Pin Setting	Interface
0	2-wire (I^2C) interface
1	3-wire (SPI) interface

In 3-wire (SPI) mode, SDIN is used for the program data, SCLK is used to clock in the program data, and CSB is used to latch in the program data. In 2-wire (I^2C) mode, SDIN is used for serial data, SCLK is used for the serial clock, and the state of the CSB pin allows the user to select one of two addresses (see Table 9).

Table 9. Selecting the Address

CSB Pin Setting	Address
0	0011010
1	0011011

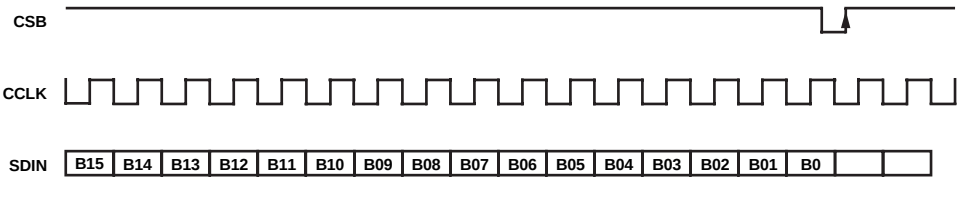

Figure 19. SPI Serial Interface

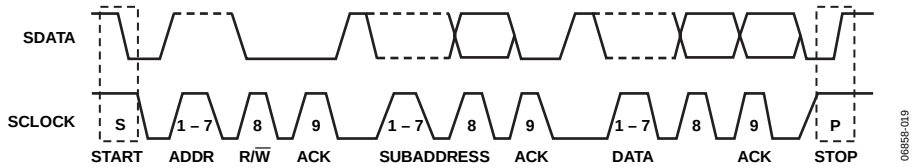

Figure 20. SSM2602 2-Wire I^2C Generalized Clocking Diagram

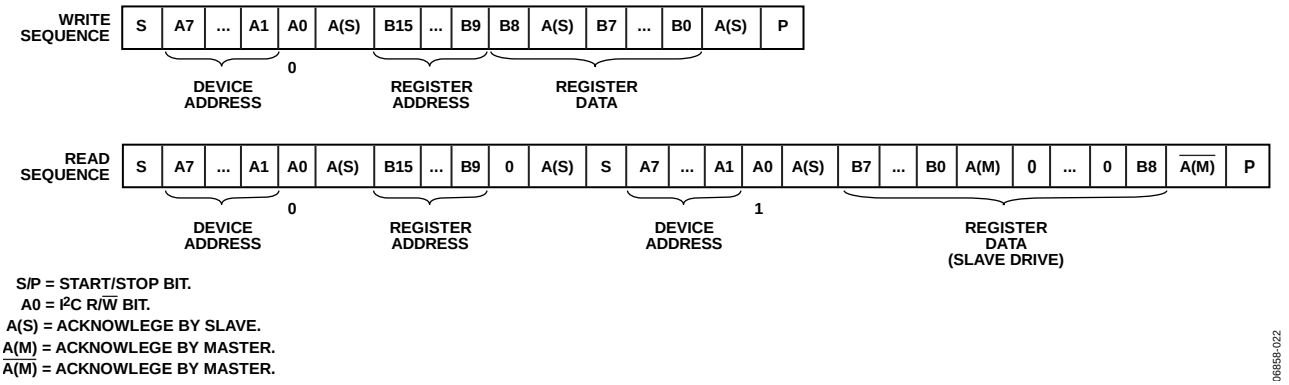

Figure 21. SSM2602 I^2C Write and Read Sequences

APPLICATIONS

TBD

TYPICAL APPLICATION CIRCUITS

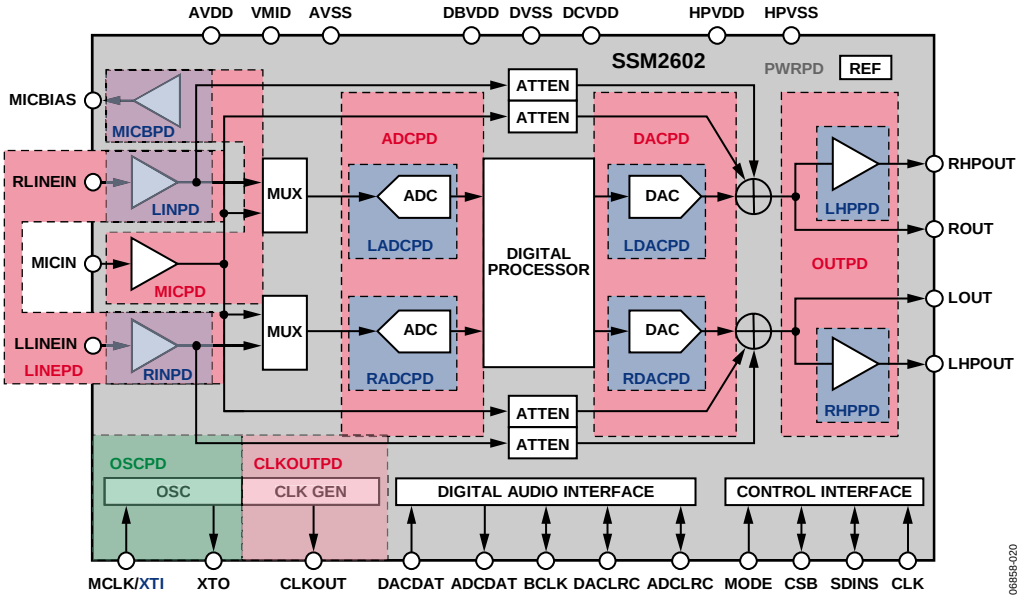

Figure 22. SSM2602 Power Management Functional Location Diagram

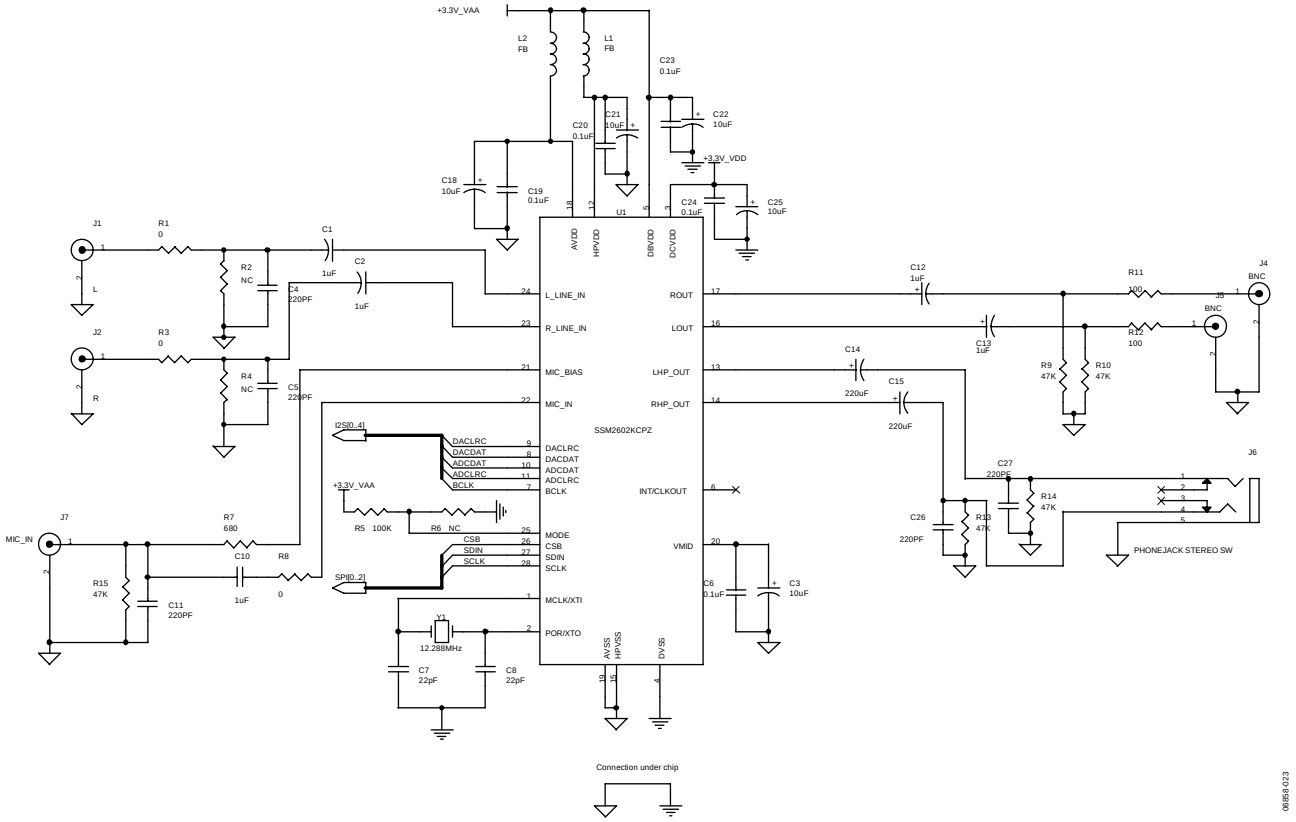

Figure 23. SSM2602 Typical Application Circuit

REGISTER MAP

Table 10. Register Map

Reg.	Address	Name	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
R0	0x00	Left-Channel ADC Input Volume	LRINBOTH	LINMUTE	0	LINVOL [5:0]						010010111
R1	0x01	Right-Channel ADC Input Volume	RLINBOTH	RINMUTE	0	RINVOL [5:0]						010010111
R2	0x02	Left-Channel DAC Volume	LRHPBOTH	LZCEN	LHPVOL [6:0]							001111001
R3	0x03	Right-Channel DAC Volume	RLHPBOTH	RZCEN	RHPVOL [6:0]							001111001
R4	0x04	Analog Audio Path	MICBOOST2	SIDETONE_ATT [1:0]		SIDETONE_EN	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST	000001010
R5	0x05	Digital Audio Path	0	0	0	0	HPOR	DACMU	DEEMPH [1:0]		ADCHPD	000001000
R6	0x06	Power Management	0	PWROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	010011111
R7	0x07	Digital Audio I/F	0	BCLKINV	MS	LRSWAP	LRP	WL [1:0]		FORMAT [1:0]		000001010
R8	0x08	Sampling Rate	0	CLKODIV2	CLKDIV2	SR [3:0]				BOSR	USB	000000000
R9	0x09	Active	0	0	0	0	0	0	0	0	ACTIVE	000000000
R15	0x0F	Software Reset	RESET [8:0]									000000000
R16	0x10	ALC Control 1	ALCSEL [1:0]		MAXGAIN [2:0]			ALCL [3:0]				001111011
R17	0x11	ALC Control 2	0	DCY [3:0]				ATK [3:0]				000110010
R18	0x12	Noise Gate	0	NGTH [4:0]					NGG [1:0]		NGAT	000000000

REGISTER MAP DETAILS

LEFT-CHANNEL ADC INPUT VOLUME, ADDRESS 0x00

Table 11. Left-Channel ADC Input Volume Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
LRINBOTH	LINMUTE	0	LINVOL [5:0]					

Table 12. Descriptions of Left-Channel ADC Input Volume Register Bits

Bit Name	Description	Settings
LRINBOTH	Left-channel line input volume update	0 = store LINVOL in intermediate latch (default) 1 = update left- and right-channel gains
LINMUTE	Left-channel input mute	0 = disable mute 1 = enable mute (default)
LINVOL [5:0]	Left-channel PGA volume control	00 0000 = 34.5 dB … 1.5 dB step down 01 0111 = 0 dB (default) … 1.5 dB step down 01 1111 = 12 dB 10 0000 = 13.5 dB 10 0001 = 15 dB 10 0010 = 16.5 dB 10 0011 = 18 dB 10 0100 = 19.5 dB 10 0101 = 21 dB 10 0110 = 22.5 dB 10 0111 = 24 dB 10 1000 = 25.5 dB 10 1001 = 27 dB 10 1010 = 28.5 dB 10 1011 = 30 dB 10 1100 = 31.5 dB 10 1101 = 33 dB 11 1111 to 10 1101 = 33 dB

RIGHT-CHANNEL ADC INPUT VOLUME, ADDRESS 0x01

Table 13. Right-Channel Input Volume Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
RLINBOTH	RINMUTE	0	RINVOL [5:0]					

Table 14. Descriptions of Right Input Volume Register Bits

Bit Name	Description	Settings
RLINBOTH	Right-channel line input volume update	0 = store RINVOL in intermediate latch (default) 1 = update left- and right-channel gains
RINMUTE	Right-channel input mute	0 = disable mute 1 = enable mute (default)
RINVOL [5:0]	Right-channel PGA volume control	00 0000 = 34.5 dB … 1.5 dB step down 01 0111 = 0 dB (default) … 1.5 dB step down 01 1111 = 12 dB 10 0000 = 13.5 dB 10 0001 = 15 dB 10 0010 = 16.5 dB 10 0011 = 18 dB 10 0100 = 19.5 dB 10 0101 = 21 dB 10 0110 = 22.5 dB 10 0111 = 24 dB 10 1000 = 25.5 dB 10 1001 = 27 dB 10 1010 = 28.5 dB 10 1011 = 30 dB 10 1100 = 31.5 dB 10 1101 = 33 dB 11 1111 to 10 1101 = 33 dB

LEFT-CHANNEL DAC VOLUME, ADDRESS 0x02

Table 15. Left-Channel DAC Volume Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
LRHPBOTH	LZCEN	LHPVOL [6:0]						

Table 16. Descriptions of Left-Channel DAC Volume Register Bits

Bit Name	Description	Settings
LRHPBOTH	Right-channel headphone volume update	0 = store LHPVOL in intermediate latch (default) 1 = update left- and right-channel gains
LZCEN	Left-channel zero cross detect enable	0 = disable (default) 1 = enable
LHPVOL [6:0]	Left-channel headphone volume control	000 0000 to 010 1111 = mute 011 0000 = −73 dB … 111 1001 = 0 dB (default) … 1 dB steps down to 111 1111 = +6 dB

RIGHT-CHANNEL DAC VOLUME, ADDRESS 0x03

Table 17. Right-Channel DAC Volume Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
RLHPBOTH	RZCEN	RHPVOL [6:0]						

Table 18. Descriptions of Right-Channel DAC Volume Register Bits

Bit Name	Description	Settings
RLHPBOTH	Right-channel headphone volume update	0 = store RHPVOL in intermediate latch (default) 1 = update left- and right-channel gains
RZCEN	Right-channel zero cross detect enable	0 = disable (default) 1 = enable
RHPVOL [6:0]	Right-channel headphone volume control	000 0000 to 010 1111 = mute 011 0000 = −73 dB … 111 1001 = 0 dB (default) … 1 dB steps down to 111 1111 = +6 dB

ANALOG AUDIO PATH, ADDRESS 0x04

Table 19. Analog Audio Path Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
MICBOOST2	SIDETONE_ATT [1:0]		SIDETONE_EN	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST

Table 20. Descriptions of Analog Audio Path Register Bits

Bit Name	Description	Settings
MICBOOST2	Additional microphone amplifier gain booster control	0 = 0 dB (default) 1 = 20 dB
SIDETONE_ATT [1:0]	Microphone sidetone gain control	00 = −6 dB (default) 01 = −9 dB 10 = −12 dB 11 = −15 dB
SIDETONE_EN		0 = sidetone disable (default) 1 = sidetone enable
DACSEL	DAC select	0 = do not select DAC (default) 1 = select DAC
BYPASS	Line input bypass to line output	0 = bypass disable 1 = bypass enable (default)
INSEL	Microphone/line level boost	0 = microphone input select to ADC (default) 1 = line input select to ADC
MUTEMIC	Microphone mute control	0 = mute disable 1 = mute enable (default)
MICBOOST	Primary microphone amplifier gain booster control	0 = 0 dB (default) 1 = 20 dB

DIGITAL AUDIO PATH CONTROL, ADDRESS 0x05

Table 21. Digital Audio Path Control Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	HPOR	DACMU	DEEMPH [1:0]		ADCHPD

Table 22. Descriptions of Digital Audio Path Control Register Bits

Bit Name	Description	Settings
HPOR	Store dc offset when high-pass filter is disabled	0 = store offset disable (default) 1 = store offset enable
DACMU	DAC digital mute	0 = no mute (signal active) 1 = mute (default)
DEEMPH [1:0]	De-emphasis control	00 = no de-emphasis (default) 01 = 32 kHz sampling rate 10 = 44.1 kHz sampling rate 11 = 48 kHz sampling rate
ADCHPD	ADC high-pass filter control	0 = ADC high-pass filter disable (default) 1 = ADC high-pass filter enable

POWER MANAGEMENT, ADDRESS 0x06

Table 23. Power Management Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	PWROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD

Table 24.

Bit Name	Description	Settings
PWROFF	Whole chip power-down control	0 = power up 1 = power down (default)
CLKOUTPD	Clock output power-down control	0 = power up (default) 1 = power down
OSCPD	Crystal power-down control	0 = power up (default) 1 = power down
OUTPD	Output power-down control	0 = power up 1 = power down (default)
DACPD	DAC power-down control	0 = power up 1 = power down (default)
ADCPD	ADC power-down control	0 = power up 1 = power down (default)
MICPD	Microphone input power-down control	0 = power up 1 = power down (default)
LINEINPD	Line input power-down control	0 = power up 1 = power down (default)

POWER CONSUMPTION

Table 25.

Mode	PWROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	AVDD (3.3 V)	HPVDD (3.3 V)	DCVDD (1.5 V)	DBVDD (1.5 V)	Unit
Record and Playback	0	0	0	0	0	0	0	0	8.36	1.7	TBD	TBD	mA
Playback Only													
Oscillator Enabled	0	0	0	0	0	1	1	1	3.1	1.7	TBD	TBD	mA
External Clock	0	1	1	0	0	1	1	1	3.1	1.7	TBD	TBD	mA
Record Only													
Line Clock	0	0	0	1	1	0	1	0	3.15	-	TBD	TBD	mA
Line Oscillator	0	0	1	1	1	0	1	0	3.15	-	TBD	TBD	mA
Microphone 1	0	0	0	1	1	0	0	1	3.45	-	TBD	TBD	mA
Microphone 2	0	0	1	1	1	0	0	1	3.45		TBD	TBD	mA
Sidetone (Microphone to Headphone Output)													
External Clock	0	0	1	0	1	1	0	1	2.24	1.7	TBD	TBD	mA
Internally Generated Clock	0	0	1	0	1	1	0	1	2.24	1.7	TBD	TBD	mA
Analog Bypass (Line Input or Line Output)													
External Line	0	0	1	0	1	1	1	0	1.94	1.7	TBD	TBD	mA
Internally Generated Line	0	0	1	0	1	1	1	0	1.94	1.7	TBD	TBD	mA
Power-Down													
External Clock	1	1	1	1	1	1	1	1	TBD	TBD	TBD	TBD	mA
Oscillator	1	1	1	1	1	1	1	1	TBD	TBD	TBD	TBD	mA

DIGITAL AUDIO I/F, ADDRESS 0x07

Table 26. Digital Audio I/F Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	BCLKINV	MS	LRSWAP	LRP	WL [1:0]		FORMAT [1:0]	

Table 27. Descriptions of Digital Audio I/F Register Bits

Bit Name	Description	Settings
BCLKINV	BCLK inversion control	0 = BCLK not inverted (default) 1 = BCLK inverted
MS	Master mode enable	0 = enable slave mode (default) 1 = enable master mode
LRSWAP	Swap DAC data control	0 = output left- and right-channel data as normal (default) 1 = swap left- and right-channel DAC data in audio interface
LRP	Polarity control for clocks in right justified, left justified, and I^2S modes	0 = normal DACLRC and ADCLRC (default), or DSP Submode 1 1 = invert DACLRC and ADCLRC polarity, or DSP Submode 2
WL [1:0]	Data-word length control	00 = 16 bits 01 = 20 bits 10 = 24 bits (default) 11 = 32 bits
FORMAT [1:0]	Digital audio input format control	00 = right justified 01 = left justified 10 = I^2S format (default) 11 = DSP mode

SAMPLING RATE, ADDRESS 0x08

Table 28. Sampling Rate Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	CLKODIV2	CLKDIV2	SR [3:0]				BOSR	USB

Table 29. Descriptions of Sampling Rate Register Bits

Bit Name	Description	Settings
CLKODIV2	CLKOUT divider select	0 = CLKOUT is core clock (default) 1 = CLKOUT is core clock divided by 2
CLKDIV2	Core clock divide select	0 = core clock is MCLK (default) 1= core clock is MCLK divided by 2
SR [3:0]	Clock setting condition	See Table 30 and Table 31.
BOSR	Base oversampling rate	USB mode: 0 = 250 f_S (default) 1 = 272 f_S Normal mode: 0 = 256 f_S (default) 1 = 384 f_S
USB	USB mode select	0 = USB mode disable (default) 1 = USB mode enable

Table 30. Sampling Rate Lookup Table, USB Disabled

Sampling Rate Register Setting								
BOSR	SR3	SR2	SR1	SR0	Normal/USB	MCLK (MHz)	ADC Sampling Rate (kHz)	DAC Sampling Rate (kHz)
0	0	0	0	0	0	12.288	48	48
1					0	18.432		
0	0	0	0	1	0	12.288	48	8
1					0	18.432		
0	0	0	1	0	0	12.288	8	48
1					0	18.432		
0	0	0	1	1	0	12.288	8	8
1					0	18.432		
0	0	1	0	0	0	12.288	12	12
1					0	18.432		
0	0	1	0	1	0	12.288	16	16
1					0	18.432		
0	0	1	1	0	0	12.288	32	32
1					0	18.432		
0	0	1	1	1	0	12.288	96	96
1					0	18.432		
0	1	0	0	0	0	11.2896	44.1	44.1
1					0	16.9344		
0	1	0	0	1	0	11.2896	44.1	8.02
1					0	16.9344		
0	1	0	1	0	0	11.2896	8.02	44.1
1					0	16.9344		
0	1	0	1	1	0	11.2896	8.02	8.02
1					0	16.9344		
0	1	1	0	0	0	11.2896	11	11
1					0	16.9344		
0	1	1	0	1	0	11.2896	22	22
1					0	16.9344		
0	1	1	1	0	0	11.2896	24	24
1					0	16.9344		
0	1	1	1	1	0	11.2896	88.2	88.2
1					0	16.9344		

Table 31. Sampling Rate Lookup Table, USB Enabled

Sampling Rate Register Setting								
BOSR	SR3	SR2	SR1	SR0	Normal/USB	MCLK (MHz)	ADC Sampling Rate (kHz)	DAC Sampling Rate (kHz)
0	0	0	0	0	1	12	48	48
1	1	0	0	0	1	12	44.1	44.1
0	0	0	0	1	1	12	48	8
1	1	0	0	1	1	12	44.1	8.02
0	0	0	1	0	1	12	8	48
1	1	0	1	0	1	12	8.02	44.1
0	0	0	1	1	1	12	8	8
1	1	0	1	1	1	12	8.02	8.02
0	0	1	0	0	1	12	12	12
0	0	1	0	1	1	12	16	16
0	1	1	0	0	1	12	11	11
0	1	1	0	1	1	12	22	22
0	1	1	1	0	1	12	24	24

Sampling Rate Register Setting					Normal/USB	MCLK (MHz)	ADC Sampling Rate (kHz)	DAC Sampling Rate (kHz)
BOSR	SR3	SR2	SR1	SR0				
0	0	1	1	0	1	12	32	32
0	0	1	1	1	1	12	96	96
1	1	1	1	1	1	12	88.2	88.2

ACTIVE, ADDRESS 0x09

Table 32. Active Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	ACTIVE

Table 33. Descriptions of Active Register Bit

Bit Name	Description	Settings
ACTIVE	Digital core activation control	0 = disable digital core (default) 1 = activate digital core

RESET, ADDRESS 0x0F

Table 34. Reset Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET [8:0]								

Table 35. Descriptions of Reset Register Bits

Bit Name	Description	Settings
RESET [8:0]	Write to RESET register to set all control registers to default setting.	0 = reset (default)

ALC CONTROL 1, ADDRESS 0x10

Table 36. ALC Control 1 Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
ALCSEL [1:0]		MAXGAIN [2:0]			ALCL [[3:0]			

Table 37. Descriptions of ALC Control 1 Register Bits

Bit Name	Description	Settings
ALCSEL [1:0]	ALC selection	00: ALC disabled (default) 01: ALC enabled, right channel only 10: ALC enabled, left channel only 11: N/A
MAXGAIN [2:0]	PGA maximum gain	000: −12 dB 001: −6 dB … 6 dB steps up to 111: 30 dB (default)
ALCL [3:0]	ALC target level	0000: −28.5 dBFS 0001: −27 dBFS … 1011: −12 dBFS (default) … 1.5 dB steps up to 1111: −6 dBFS

ALC CONTROL 2, ADDRESS 0x11

Table 38. ALC Control 2 Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	DCY [3:0]				ATK [3:0]			

Table 39. Descriptions of ALC Control 2 Register Bits

Bit Name	Description	Settings
DCY [3:0]	Decay (release) time control	0000: 24 ms 0001: 48 ms 0010: 96 ms 0011: 192 ms (default) … 24 ms steps up to 1010: 24.576 sec
ATK [3:0]	ALC attack time control	0000: 6 ms 0001: 12 ms 0010: 24 ms (default) … 6 ms steps up to 1010: 6.144 sec

NOISE GATE, ADDRESS 0x12

Table 40. Noise Gate Register Bit Map

D8	D7	D6	D5	D4	D3	D2	D1	D0
0	NGTH [4:0]					NGG [1:0]		NGAT

Table 41. Descriptions of Noise Gate Register Bits

Bit Name	Description	Settings
NGTH [4:0]	Noise gate threshold	00000: −76.5 dBFS (default) 00001: −75 dBFS … 1.5 dB steps up to 11110: −31.5 dBFS 11111: −30 dBFS
NGG [1:0]	Noise gate type	X0: hold PGA gain constant (default)[1] 01: mute output 11: reserved
NGAT	Noise enable	0: noise disable (default) 1: noise enable

[1] X = don't care.

OUTLINE DIMENSIONS

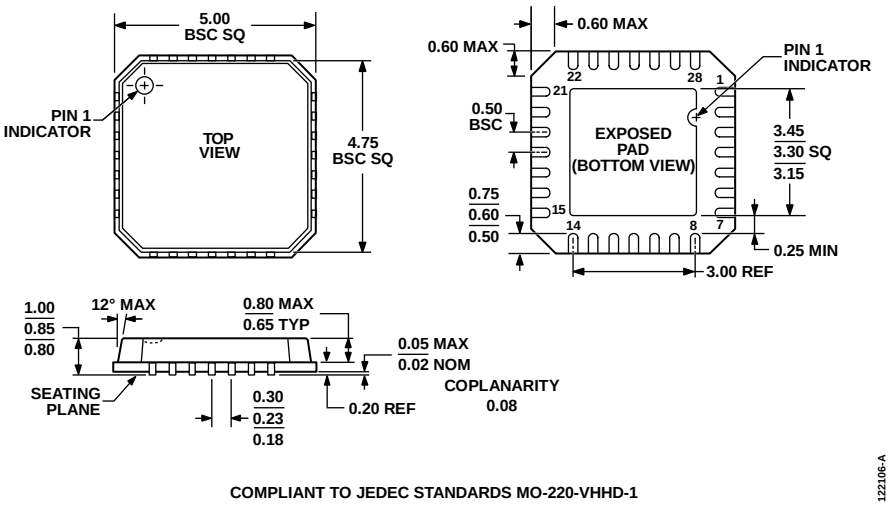

Figure 24. 28-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-28-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SSM2602CPZ-R2[1]	−40°C to +85°C	28-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-28-4
SSM2602CPZ-REEL[1]	−40°C to +85°C	28-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-28-4
SSM2602CPZ-REEL7[1]	−40°C to +85°C	28-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-28-4
SSM2602-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

PR06858-0-9/07(PrB)