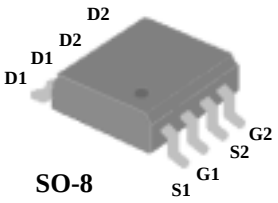
N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

PRODUCT SUMMARY

Simple Drive Requirement
Low On-resistance
Fast Switching



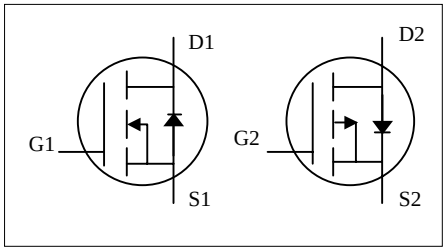
SO-8

N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	28mΩ
	I_D	7A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	50mΩ
	I_D	-5.3A

DESCRIPTION

The advanced power MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Pb-free; RoHS-compliant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current[3]	7	-5.3	A
I_D@T_A=70℃	Continuous Drain Current[3]	5.8	-4.7	A
I_{DM}	Pulsed Drain Current[1]	20	-20	A
P_D@T_A=25℃	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

THERMAL DATA

Symbol	Parameter		Value	Unit
Rthj-amb	Thermal Resistance Junction-ambient[3]	Max.	62.5	℃/W

N-CH ELECTRICAL CHARACTERISTICS

@Tj=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=1mA	-	0.02	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=7A	-	-	28	mΩ
		V_{GS}=4.5V, I_D=5A	-	-	42	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=7A	-	13	-	S
I_{DSS}	Drain-Source Leakage Current (T_j=25°C)	V_{DS}=30V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=24V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=7A	-	8.4	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=24V	-	2.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	4.7	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=15V	-	6	-	ns
t_r	Rise Time	I_D=1A	-	5.2	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	18.8	-	ns
t_f	Fall Time	R_D=15Ω	-	4.4	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	645	-	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	150	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	95	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=1.2V	-	-	1.7	A
V_{SD}	Forward On Voltage[2]	T_j=25℃, I_S=7A, V_{GS}=0V	-	-	1.2	V

P-CH ELECTRICAL CHARACTERISTICS

@Tj=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D=-1mA	-	-0.03	-	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-5.3A	-	-	50	mΩ
		V_{GS}=-4.5V, I_D=-4.2A	-	-	90	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-5.3A	-	8.5	-	S
I_{DSS}	Drain-Source Leakage Current (Tj=25°C)	V_{DS}=-30V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (Tj=70°C)	V_{DS}=-24V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}= ± 20V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-5.3A	-	20	-	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	3.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-10V	-	2	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-15V	-	12	-	ns
t_r	Rise Time	I_D=-1A	-	20	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=6Ω,V_{GS}=-10V	-	45	-	ns
t_f	Fall Time	R_D=15Ω	-	27	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	790	-	pF
C_{oss}	Output Capacitance	V_{DS}=-15V	-	440	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	120	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	V_D=V_G=0V , V_S=-1.2V	-	-	-1.7	A
V_{SD}	Forward On Voltage[2]	T_j=25℃, I_S=-2.6A, V_{GS}=0V	-	-	-1.2	V

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

3.Surface mounted on 1 in^2 copper pad of FR4 board ; 135℃/W when mounted on Min. copper pad.

N-Channel

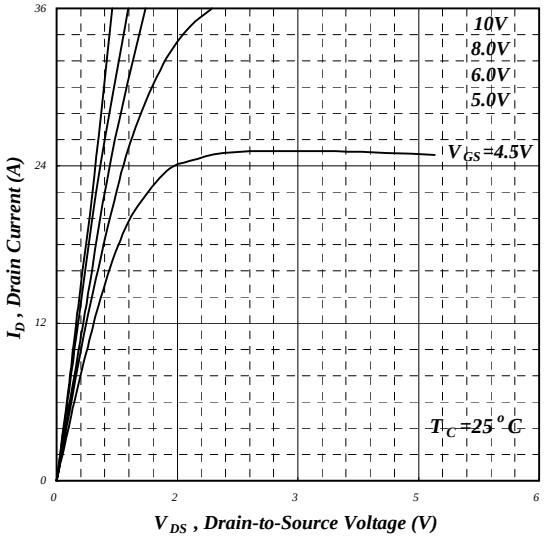


Fig 1. Typical Output Characteristics

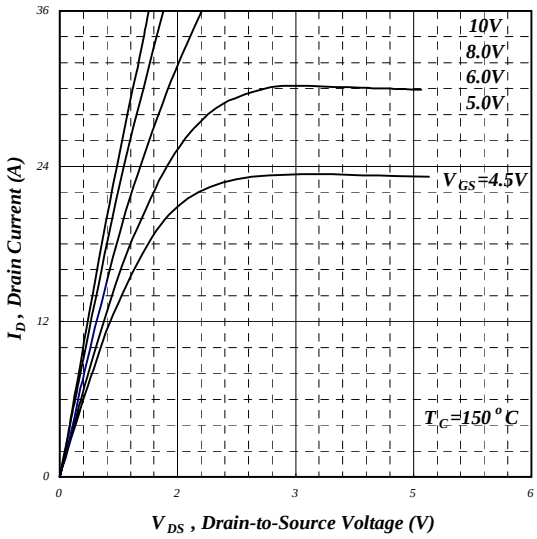


Fig 2. Typical Output Characteristics

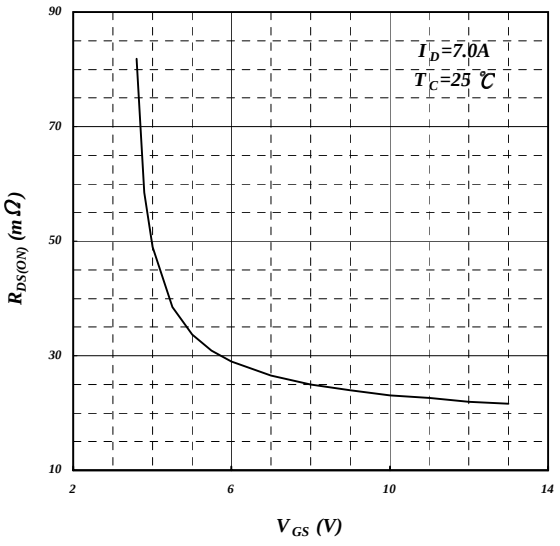


Fig 3. On-Resistance v.s. Gate Voltage

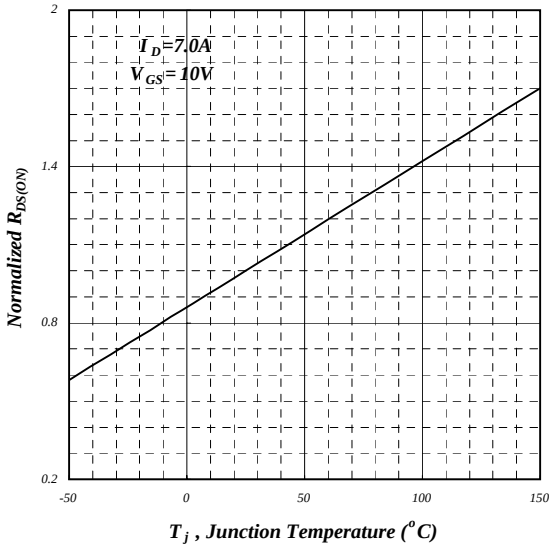


Fig 4. Normalized On-Resistance v.s. Junction Temperature

N-Channel

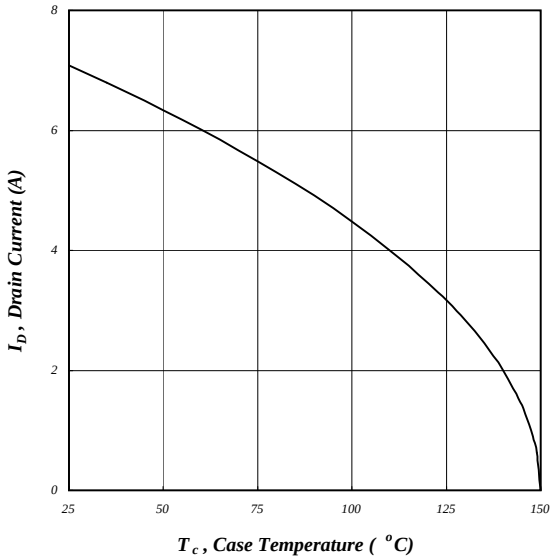


Fig 5. Maximum Drain Current v.s. Case Temperature

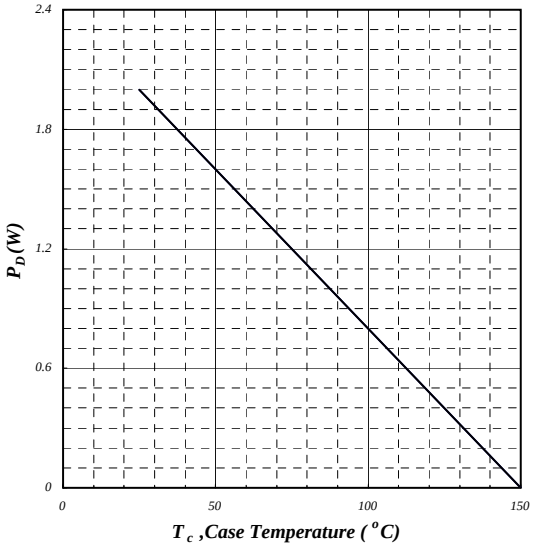


Fig 6. Typical Power Dissipation

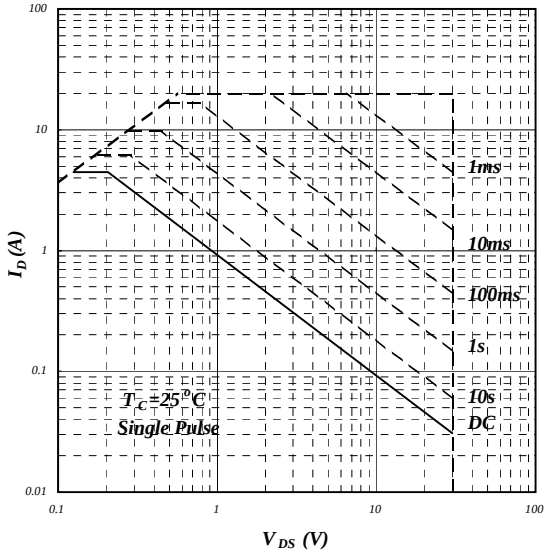


Fig 7. Maximum Safe Operating Area

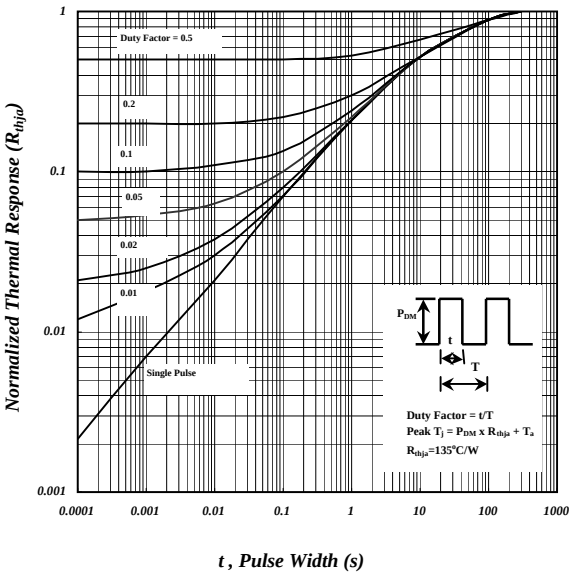


Fig 8. Effective Transient Thermal Impedance

N-Channel

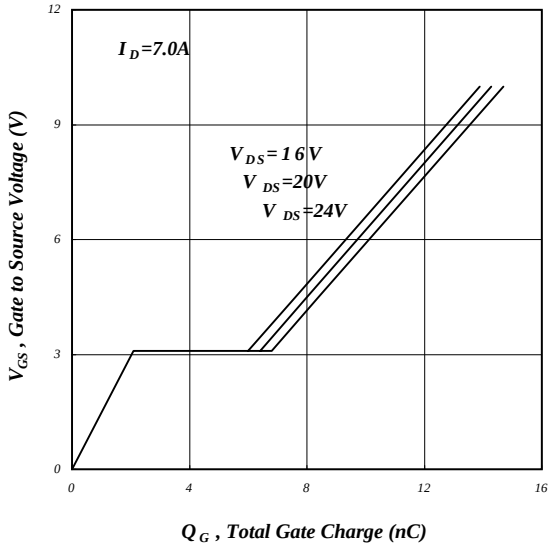


Fig 9. Gate Charge Characteristics

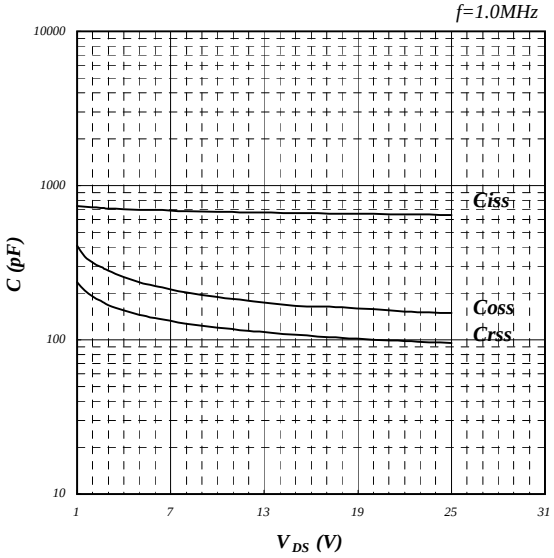


Fig 10. Typical Capacitance Characteristics

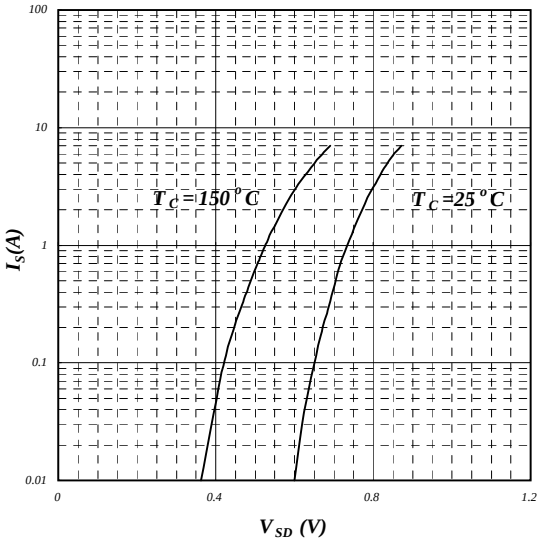


Fig 11. Forward Characteristic of Reverse Diode

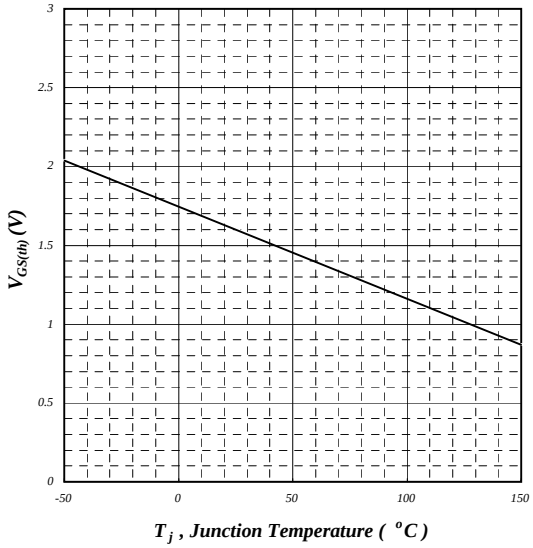


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

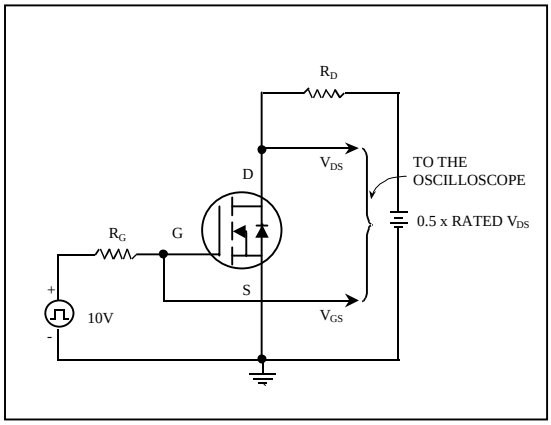


Fig 13. Switching Time Circuit

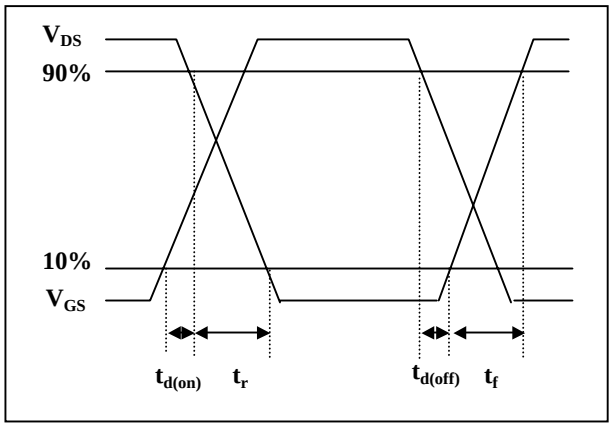


Fig 14. Switching Time Waveform

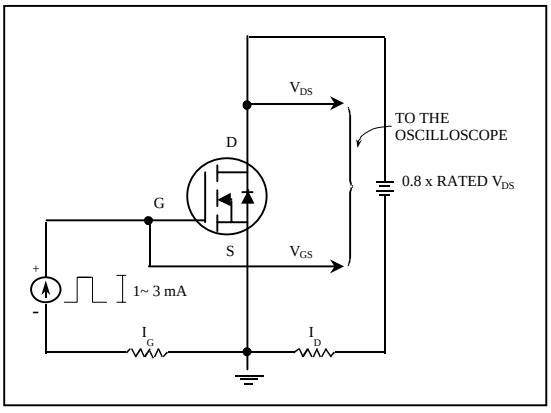


Fig 15. Gate Charge Circuit

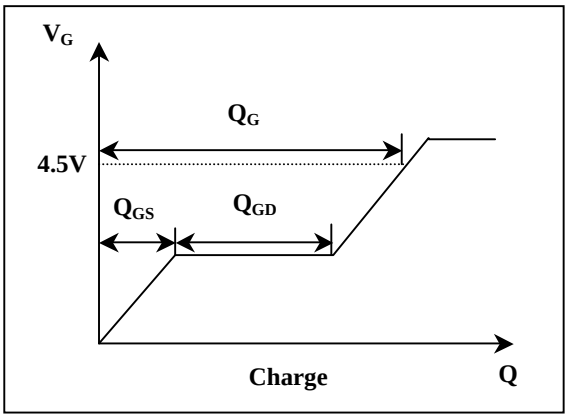


Fig 16. Gate Charge Waveform

P-Channel

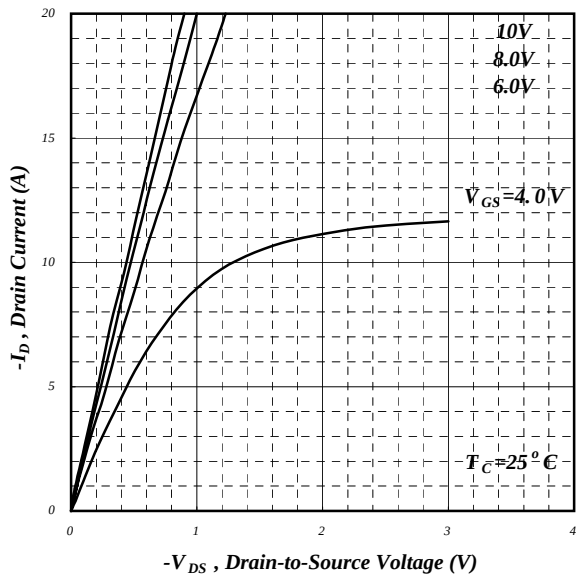


Fig 1. Typical Output Characteristics

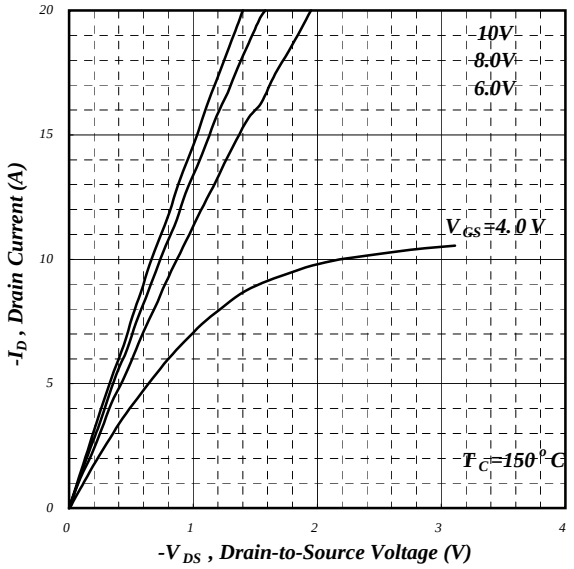


Fig 2. Typical Output Characteristics

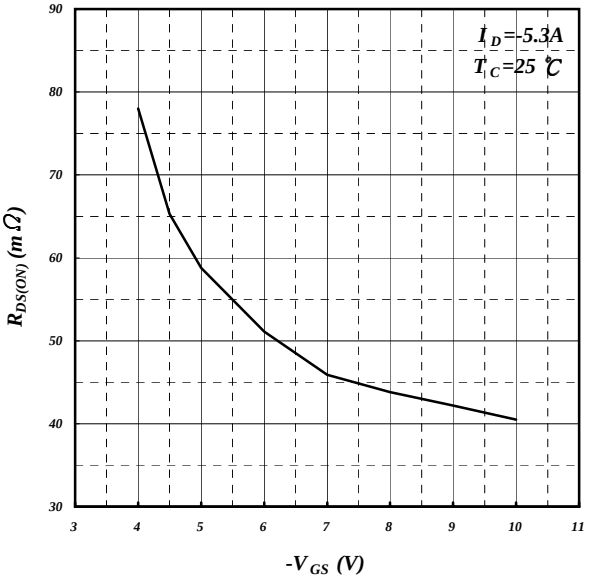


Fig 3. On-Resistance v.s. Gate Voltage

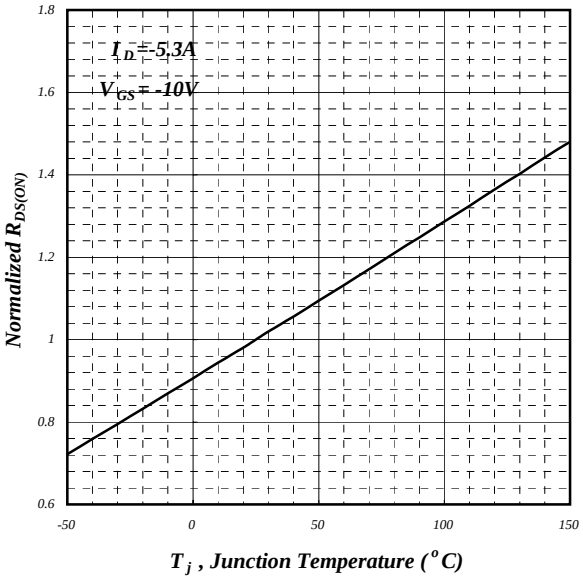


Fig 4. Normalized On-Resistance v.s. Junction Temperature

P-Channel

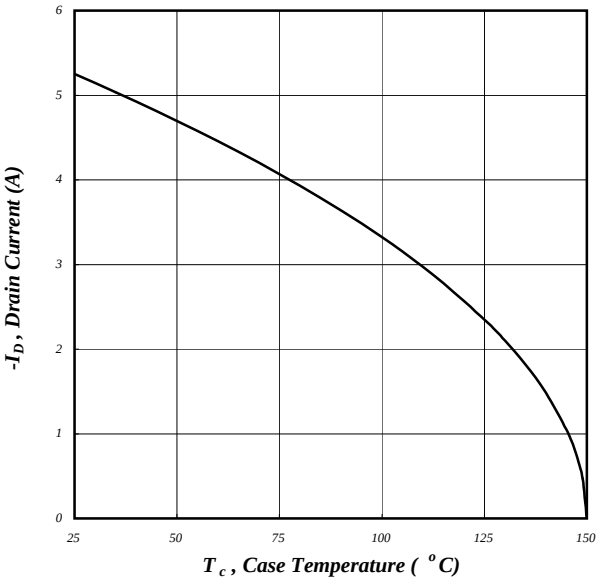


Fig 5. Maximum Drain Current v.s. Case Temperature

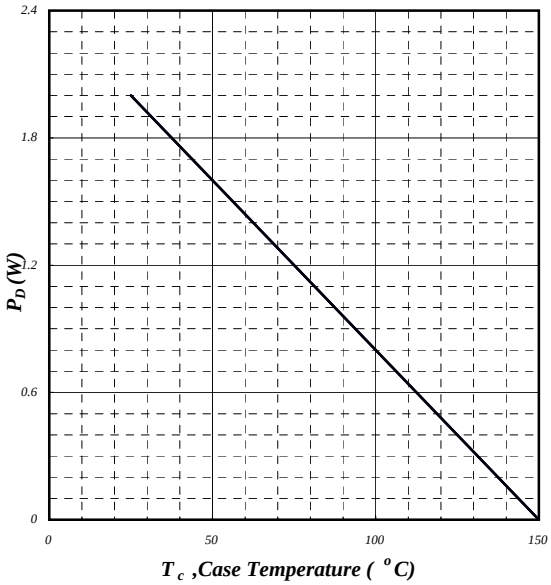


Fig 6. Typical Power Dissipation

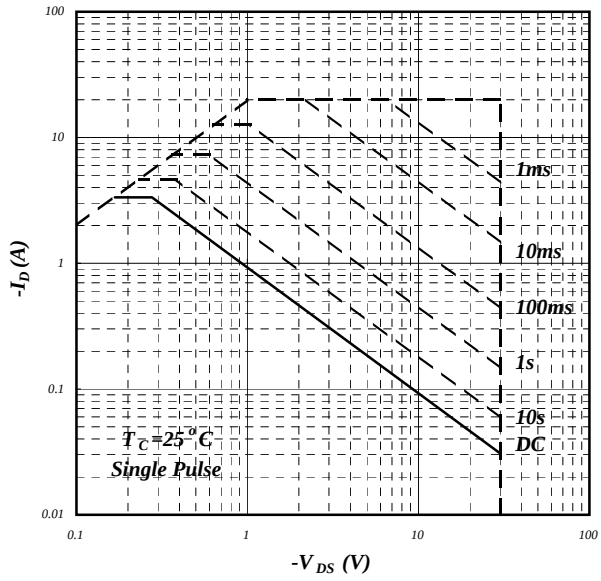


Fig 7. Maximum Safe Operating Area

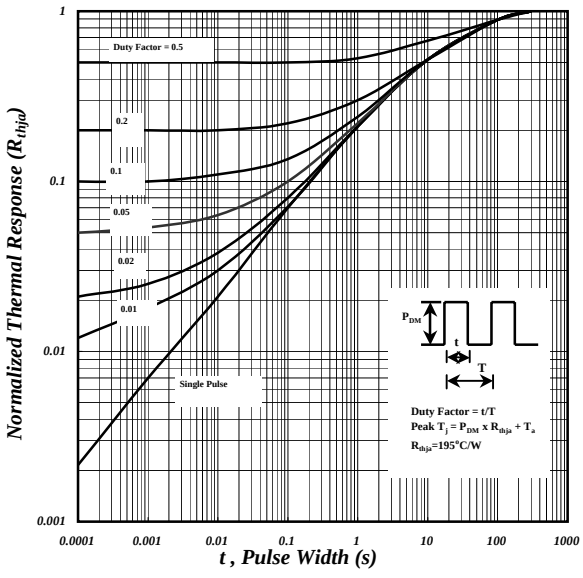


Fig 8. Effective Transient Thermal Impedance

P-Channel

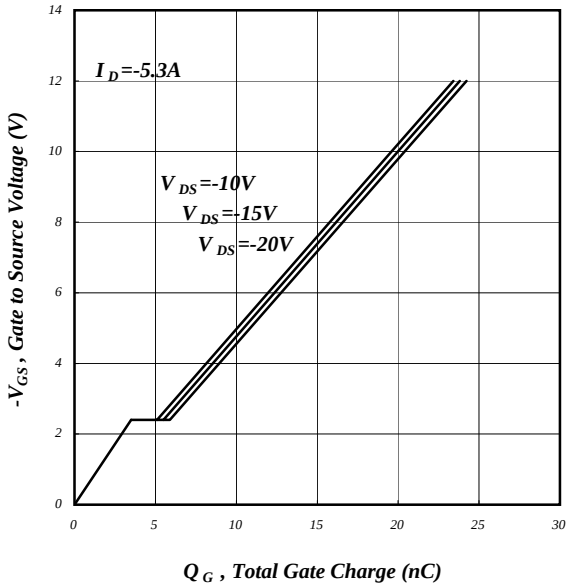


Fig 9. Gate Charge Characteristics

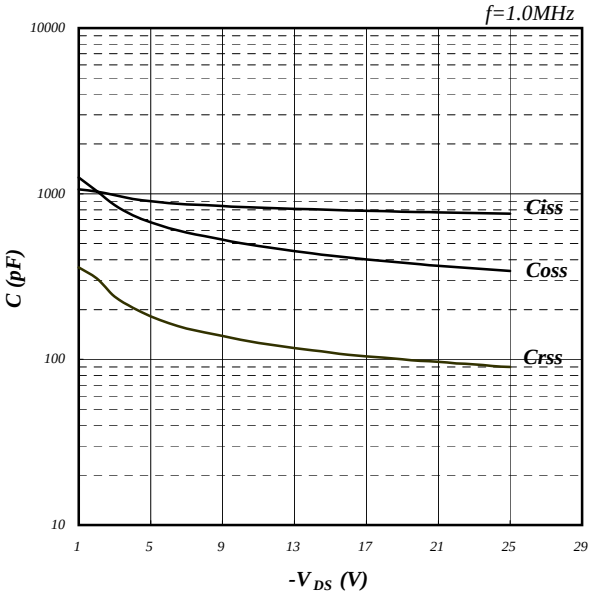


Fig 10. Typical Capacitance Characteristics

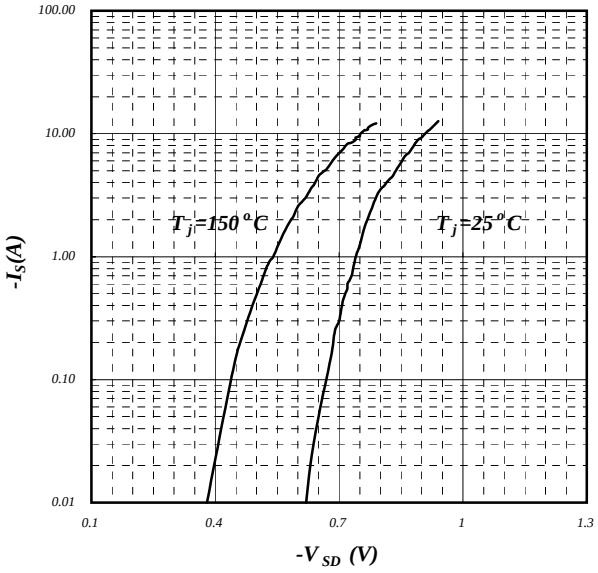


Fig 11. Forward Characteristic of Reverse Diode

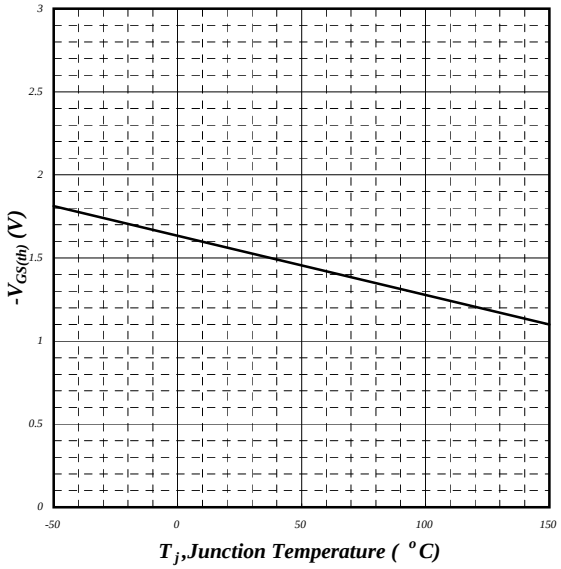


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

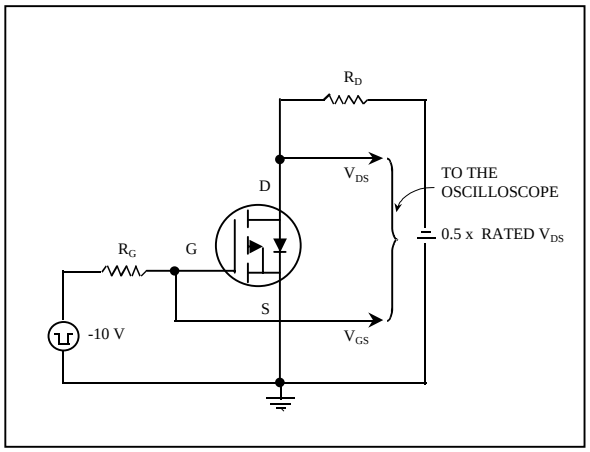


Fig 13. Switching Time Circuit

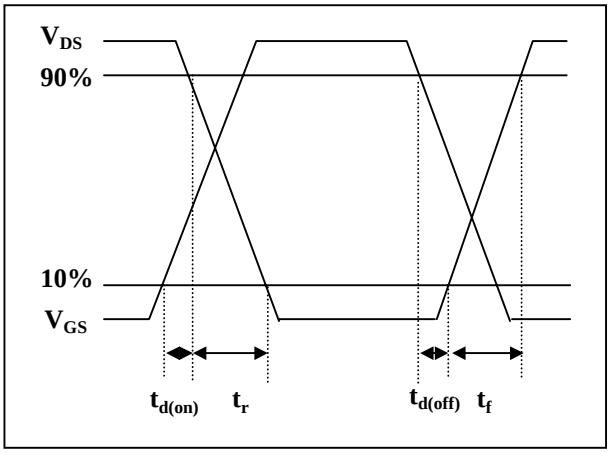


Fig 14. Switching Time Waveform

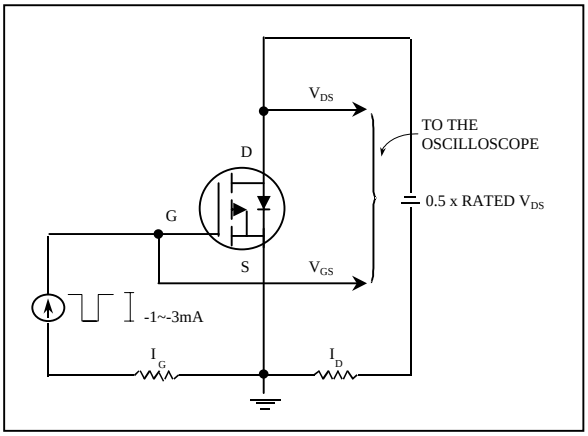


Fig 15. Gate Charge Circuit

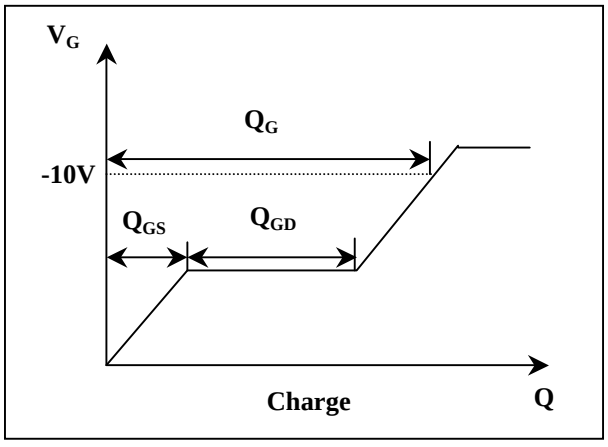


Fig 16. Gate Charge Waveform