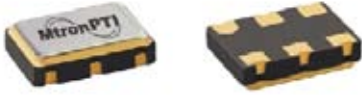
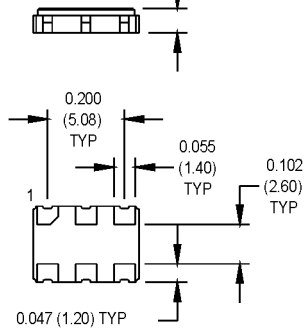
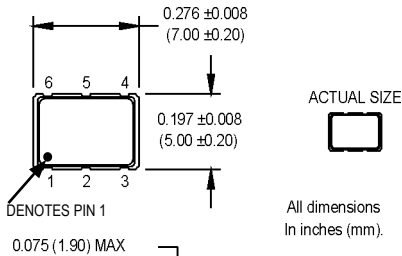


# UVCJ Series

## 5x7 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillators



- Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz
- Ideal for 10 and 40 Gigabit Ethernet and Optical Carrier applications



### Pad Connections

Pad	Function
1	Enable/Disable for "B" or "S" Output Type or N/C for "U" Output Type
2	N/C
3	Ground
4	Output Q
5	Complementary Output $\bar{Q}$
6	+ Vdd

### Ordering Information

Product Series	UVCJ	1	8	B	L	N	00.0000 MHz
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C	6: -20°C to +70°C	7: -0°C to +85°C	8: 0°C to +50°C		
Stability	3: ±100 ppm	4: ±50 ppm	6: ±25 ppm	8: ±20 ppm			
Output Type	B: Complementary, Enable (Enable High)	S: Complementary, Enable (Enable Low)	U: Complementary Output				
Symmetry/Output Logic Type	L: 45/55% LVDS	P: 45/55% PECL	H: 40/60% LVDS	Q: 40/60% PECL			
Package/Lead Configurations	N: Leadless Ceramic (6 pads)						
Frequency (customer specified)							

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	0.75		700	MHz		
Operating Temperature	T <sub>A</sub>	(See ordering information)					
Storage Temperature	T <sub>S</sub>	-55		+125	°C		
Frequency Stability	ΔF/F	(See ordering information)					
Aging						See Note 1	
1st Year		-3/-5		+3/+5	ppm	<52 MHz/ ≥52 MHz	
Thereafter (per year)		-1/-2		+1/-2	ppm	<52 MHz/ ≥52 MHz	
Input Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V		
Input Current	I <sub>cc</sub>						
0.75 to 24 MHz				70/30	mA	PECL/LVDS	
24 to 700 MHz				100/60	mA	PECL/LVDS	
Output Type						PECL/LVDS	
Load		50 Ohms to V <sub>cc</sub> - 2 VDC 100 Ohm differential load					See Note 2 PECL Waveform LVDS Waveform
Symmetry (Duty Cycle)		(See ordering information)					@ 50% of waveform
Output Skew				200	ps	PECL	
Differential Voltage		250	350	450	mV	LVDS	
Logic "1" Level	V <sub>oh</sub>	V <sub>cc</sub> -1.02			V	LVPECL	
Logic "0" Level	V <sub>ol</sub>			V <sub>cc</sub> -1.63	V	LVPECL	
Rise/Fall Time	Tr/Tf		0.35 0.50	0.55 1.0	ns ns	@ 20/80% LVPECL @ 20/80% LVDS	
Enable Function		80% V <sub>cc</sub> min or N/C output active 20% V <sub>cc</sub> max: output disables to high-Z					Output Option B
		PECL low, GND, or N/C – output active PECL high 0 output disables to high-Z					Output Option S
Start up Time			5		ms		
Phase Jitter (Typical)	φ <sub>J</sub>		0.35 2.85 1.95 1.30		ps RMS ps RMS ps RMS ps RMS	See Note 3 Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz Integrated 12 kHz – 20 MHz	

1. PECL load - see Load Circuit Diagram. LVDS load - see load circuit diagram. Consult factory with nonstandard output load requirements.
2. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% V<sub>dd</sub> and 90% V<sub>dd</sub> with HCMOS load.
3. Consult factory for phase jitter at other specific frequencies.

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