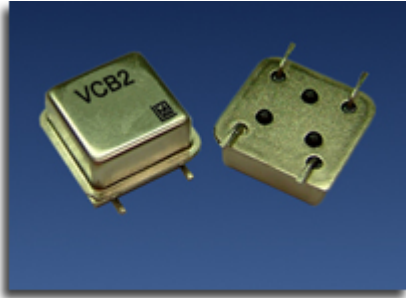
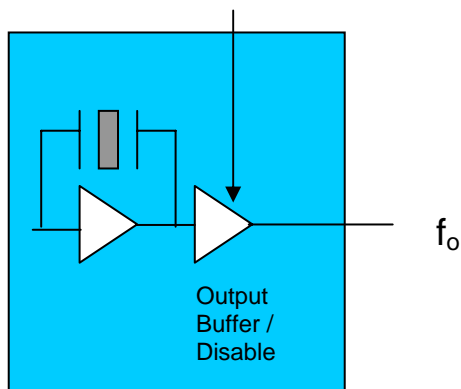



VCB2 series 3.3, 5.0 volt CMOS Oscillator



The VCB2 Crystal Oscillator



Features

- CMOS output
- Output frequencies to 160 MHz
- Tri-state output for board test and debug
- 0/70 or -40/85 °C operating temperature
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, Gigabit Ethernet
- Storage Area Network
- Digital Video
- Broadband Access
- Microprocessors/DSP/FPGA

Description

Vectron's VCB2 Crystal Oscillator (XO) is quartz stabilized square wave generator with a CMOS output, operating off a 3.3 or 5.0 volt supply.

The VCB2 uses fundamental or 3rd overtone crystals, for output frequencies < 80MHz, resulting in low jitter performance, typically 0.5ps rms in the 12 kHz to 20MHz band.

Performance Characteristics

Table 1. Electrical Performance, 5V option

| Parameter | Symbol | Min | Typical | Maximum | Units |
|---|--------------|--------------------|---|--------------------|-------|
| Frequency | f_O | 0.032768 | | 160.000 | MHz |
| Operating Supply Voltage ¹ | V_{DD} | 4.5 | 5.0 | 5.5 | V |
| Absolute Maximum Supply Voltage | | -0.7 | | 7.0 | V |
| Supply Current, Output Enabled | I_{DD} | | | | mA |
| 0.032768 to 2.0 MHz | | | | 10 | |
| 2.01 to 30 MHz | | | | 15 | |
| 30.01 to 50 MHz | | | | 40 | |
| 50.01 to 160.00 MHz | | | | 50 | |
| Output Logic Levels | | | | | |
| Output Logic High ² | V_{OH} | $0.9 \cdot V_{DD}$ | | | V |
| Output Logic Low ² | V_{OL} | | | $0.1 \cdot V_{DD}$ | V |
| Output Rise/Fall Time ² | t_R/t_F | | | | ns |
| 0.032768 to 2.00 MHz | | | | 10 | |
| 2.01 to 20.00 MHz | | | | 8 | |
| 20.01 to 160.00 MHz | | | | 5 | |
| Duty Cycle ³ (ordering option) | SYM | | 40/60 or 45/55 | | % |
| Operating Temperature (ordering option) | T_{OP} | | 0/70 or -40/85 | | °C |
| Storage Temperature | T_{STOR} | -55 | | 125 | °C |
| Stability ⁴ (ordering option) | $\Delta F/T$ | | $\pm 20, \pm 25, \pm 32, \pm 50, \pm 100$ | | ppm |
| Output Enable/Disable ⁵ | E/D | | | | V |
| Output Enabled | | 4.0 | | | |
| Output Disabled | | | | 0.8 | |
| Start-up time | T_{SU} | | | 10 | ms |

1. A 0.01 μ F and a 0.1 μ F capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions under which these parameters are tested and specified.
3. Symmetry is measured defined as On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
5. Output will be enabled if enable/disable is left open.

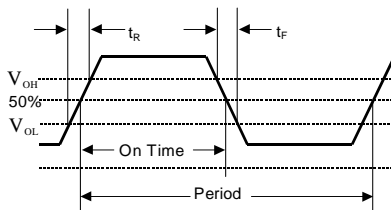


Figure 1. Output Waveform

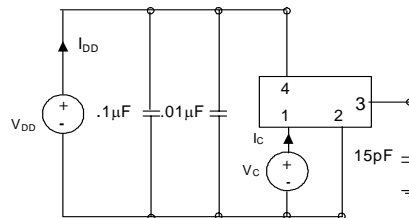


Figure 2. Typical Output Test Conditions (25±5°C)

VCB2 Data Sheet

| Table 2. Electrical Performance, 3.3V option | | | | | |
|--|--------------|--------------------|---|--------------------|-------|
| Parameter | Symbol | Min | Typical | Maximum | Units |
| Frequency | f_O | 0.032768 | | 160.000 | MHz |
| Operating Supply Voltage ¹ | V_{DD} | 2.97 | 3.3 | 3.63 | V |
| Absolute Maximum Operating Voltage | | -0.5 | | 5.0 | V |
| Supply Current, Output Enabled | I_{DD} | | | | mA |
| 0.032786 to 2.0 MHz | | | | 8 | |
| 2.01 to 30 MHz | | | | 10 | |
| 30.01 to 50 MHz | | | | 20 | |
| 50.01 to 160 MHz | | | | 35 | |
| Output Logic Levels | | | | | |
| Output Logic High ² | V_{OH} | $0.9 \cdot V_{DD}$ | | | V |
| Output Logic Low ² | V_{OL} | | | $0.1 \cdot V_{DD}$ | V |
| Output Rise/Fall Time ² | t_R/t_F | | | | ns |
| 0.032768 to 2.00 MHz | | | | 12 | |
| 2.01 to 20.00 MHz | | | | 10 | |
| 20.01 to 160.00 MHz | | | | 6 | |
| Duty Cycle ³ (ordering option) | SYM | | 40/60 or 45/55 | | % |
| Operating Temperature (ordering option) | T_{OP} | | 0/70 or -40/85 | | °C |
| Storage Temperature | T_{STOR} | -55 | | 125 | °C |
| Stability ⁴ (ordering option) | $\Delta F/T$ | | $\pm 20, \pm 25, \pm 32, \pm 50, \pm 100$ | | ppm |
| Output Enable/Disable ⁵ | E/D | | | | V |
| Output Enabled | | 2.0 | | | |
| Output Disabled | | | | 0.5 | |
| Start-up time | T_{SU} | | | 10 | ms |

1. A 0.01 μ F and a 0.1 μ F capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 3 defines these parameters. Figure 4 illustrates the operating conditions under which these parameters are tested and specified. For $f_O > 90$ MHz, rise and fall time is measured 20 to 80%.
3. Symmetry is measured defined as On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
5. Output will be enabled if enable/disable is left open.

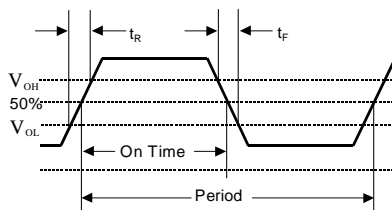


Figure 3. Output Waveform

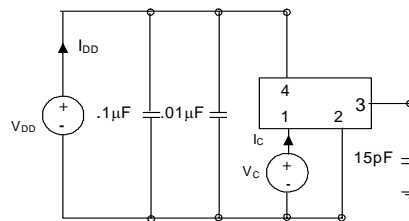


Figure 4. Typical Output Test Conditions (25±5°C)

Enable/Disable Functional Description

Under normal operation the Enable/Disable is left open or set to a logic high state. When the E/D is set to a logic low, the oscillator stops and the output is in a high impedance state. This helps reduce power consumption as well as facilitating board testing and troubleshooting.

Tri-state Functional Description

Under normal operation the tri-state is left open or set to a logic high state. When the tri-state is set to a logic low, the oscillator remains active but the output buffer is in a high impedance state. This helps facilitate board testing and troubleshooting.

Table 3. Outline Diagrams and Pin Out

| Pin # | Symbol | Function |
|-------|-----------|---------------------------------|
| 1 | E/D or NC | Tri-state, Enable/Disable or NC |
| 2 | GND | Electrical and Case Ground |
| 3 | f_o | Output Frequency |
| 4 | V_{DD} | Supply Voltage |

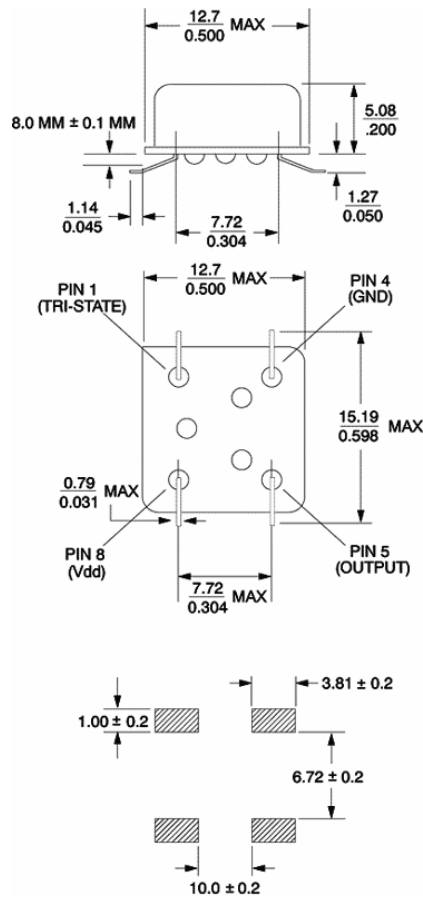


Figure 5, Package drawing

VCB2 Data Sheet

Reliability

The VCB2 qualification tests have included:

Table 4. Environmental Compliance

| Parameter | Conditions |
|------------------------|-------------------------|
| Mechanical Shock | MIL-STD-883 Method 2022 |
| Mechanical Vibration | MIL-STD-883 Method 2007 |
| Temperature Cycle | MIL-STD-883 Method 1010 |
| Gross and Fine Leak | MIL-STD-883 Method 1014 |
| Resistance to Solvents | MIL-STD-883 Method 2015 |

Handling Precautions

Although ESD protection circuitry has been designed into the the VCB2, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

Table 5. ESD Ratings

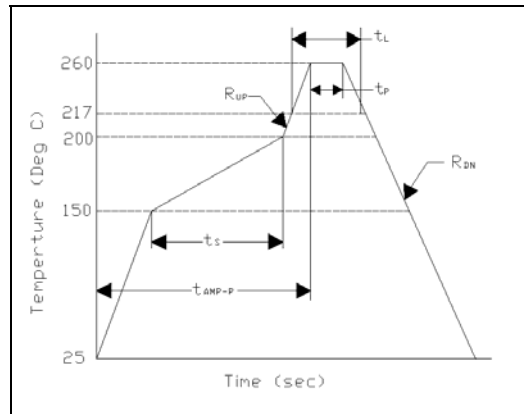
| Model | Minimum | Conditions |
|----------------------|---------|-------------------------|
| Human Body Model | 1000 | MIL-STD-883 Method 3115 |
| Charged Device Model | 1500 | JESD 22-C101 |

Suggested IR profile

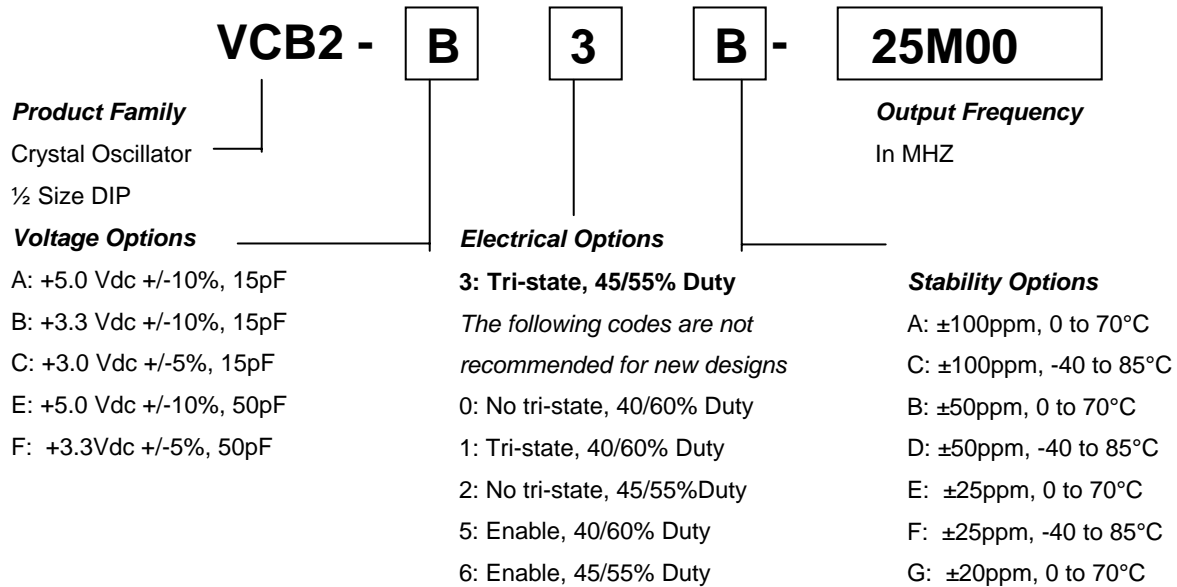
Devices are built using lead free epoxy and can also be subjected to standard lead free IR reflow conditions, Table 6 shows max temperatures and lower temperatures. A peak temperature of 240°C minimum should be used to reflow the lead solder.

Table 6. Reflow Profile (IPC/JEDEC J-STD-020B)

| Parameter | Symbol | Value |
|--------------------------|-------------|--------------------------|
| Preheat Time | t_s | 150 sec Min, 200 sec Max |
| Ramp Up | R_{UP} | 3 °C/sec Max |
| Time Above 217 °C | t_L | 60 sec Min, 150 sec Max |
| Time To Peak Temperature | t_{AMB-P} | 480 sec Max |
| Time At 260 °C (max) | t_P | 10 sec Max |
| Time At 240 °C (max) | t_{p2} | 60 sec Max |
| Ramp Down | R_{DN} | 6 °C/sec Max |



Ordering Information:



Note: Not all combinations are available.

Tri-state with a 45/55% is the most common Electrical code and is recommended for most applications.

Devices will be shipped in Anti Static Tubes

For Additional Information, Please Contact:



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