512Kx16 SRAM/FLASH MODULE, SMD 5962-96901

FEATURES

- Access Times of 35ns (SRAM) and 90ns (FLASH)
- Access Times of 70ns (SRAM) and 120ns (FLASH)
- Packaging
  - 66 pin, PGA Type, 1.385" square HIP, Hermetic Ceramic HIP (Package 402)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880") square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (FIGURE 2)
- 512Kx16 SRAM
- 512Kx16 5V FLASH
- Organized as 512Kx16 of SRAM and 512Kx16 of Flash Memory with separate Data Busses
- Both blocks of memory are User Configurable as 1Mx8
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

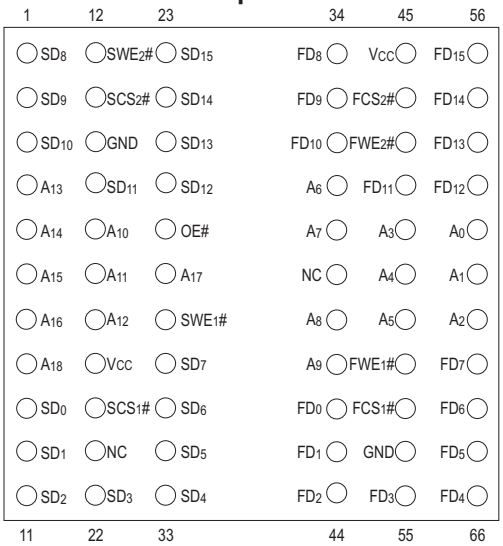
FLASH MEMORY FEATURES

- 100,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

Note: Programming information available upon request.

FIGURE 1 – PIN CONFIGURATION FOR WSF512K16-XH2X

Top View



Pin Description

FD0-15	Flash Data Inputs/Outputs
SD0-15	SRAM Data Inputs/Outputs
A0-18	Address Inputs
SWE1-2#	SRAM Write Enable
SCS1-2#	SRAM Chip Selects
OE#	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected
FWE1-2#	Flash Write Enable
FCS1-2#	Flash Chip Select

Block Diagram

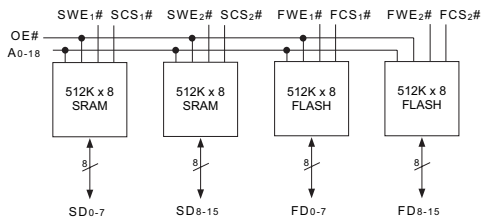
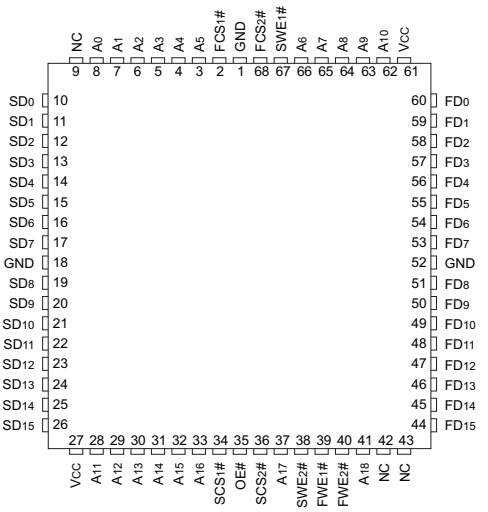


FIGURE 2 – PIN CONFIGURATION FOR WSF512K16-XG2X

Top View



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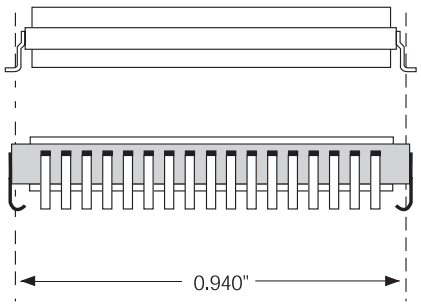
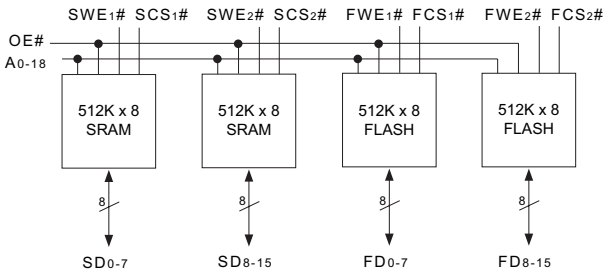
NC	Not Connected
FWE1-2#	Flash Write Enable
FCS1-2#	Flash Chip Select



The WEDC 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	7.0	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

Parameter	
Flash Data Retention	20 years
Flash Endurance (write/erase cycles)	100,000

NOTES: 1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

SRAM TRUTH TABLE

SCS#	OE#	SWE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

T_A = +25°C

Test	Symbol	Condition	Max	Unit
OE# Capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	50	pF
F/S WE1-2# Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	20	pF
F/S CS1-2# Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	20	pF
Address Input Capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	SCS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
SRAM Operating Supply Current x 16 Mode	I_{CCx16}	SCS# = V_{IL}, OE# = FCS# = V_{IH}, f = 5MHz, V_{CC} = 5.5		330	mA
Standby Current	I_{SB}	FCS# = SCS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		45	mA
SRAM Output Low Voltage	V_{OL}	I_{OL} = 6mA, V_{CC} = 4.5		0.4	V
SRAM Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		V
Flash V_{CC} Active Current for Read (1)	I_{CC1}	FCS# = V_{IL}, OE# = SCS# = V_{IH}		130	mA
Flash V_{CC} Active Current for Program or Erase (2)	I_{CC2}	FCS# = V_{IL}, OE# = SCS# = V_{IH}		150	mA
Flash Output Low Voltage	V_{OL}	I_{OL} = 8.0mA, V_{CC} = 4.5		0.45	V
Flash Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Flash Low V_{CC} Lock Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

SRAM AC CHARACTERISTICS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-35		-70		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		70		ns
Address Access Time	t_{AA}		35		70	ns
Output Hold from Address Change	t_{OH}	0		5		ns
Chip Select Access Time	t_{ACS}		35		70	ns
Output Enable to Output Valid	t_{OE}		25		35	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	4		10		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		15		25	ns
Output Disable to Output in High Z	t_{OHZ}[1]		15		25	ns

1. This parameter is guaranteed by design but not tested.

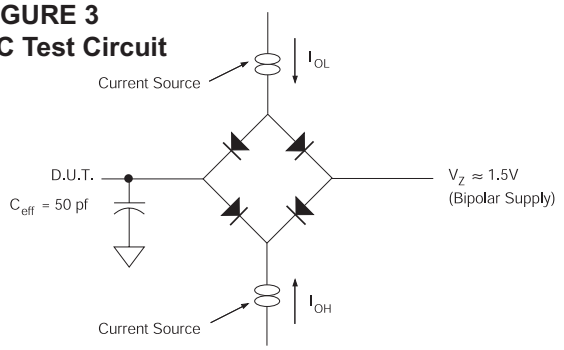
SRAM AC CHARACTERISTICS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-35		-70		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		70		ns
Chip Select to End of Write	t_{CW}	25		60		ns
Address Valid to End of Write	t_{AW}	25		60		ns
Data Valid to End of Write	t_{DW}	20		30		ns
Write Pulse Width	t_{WP}	25		50		ns
Address Setup Time	t_{AS}	0		0		ns
Address Hold Time	t_{AH}	0		5		ns
Output Active from End of Write	t_{OW1}	0		5		ns
Write Enable to Output in High Z	t_{WHZ1}		15		25	ns
Data Hold from Write Time	t_{DH}	0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 3
AC Test Circuit

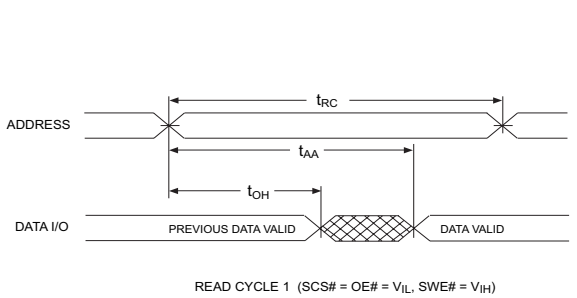


AC TEST CONDITIONS

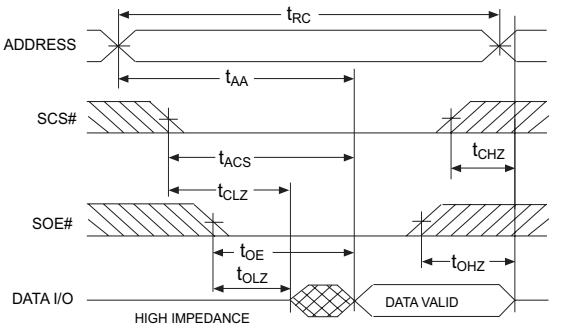
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes: V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIGURE 4 – SRAM TIMING WAVEFORM — READ CYCLE

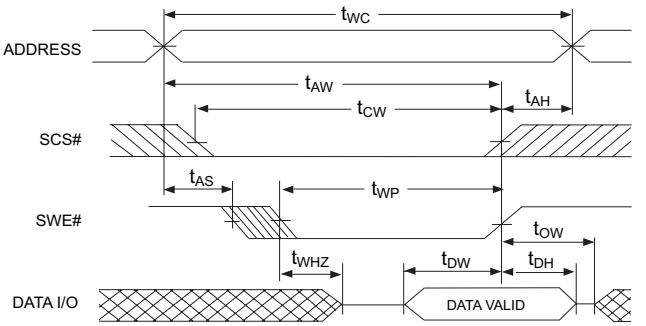


READ CYCLE 1 (SCS# = OE# = V_{IL}, SWE# = V_{IH})



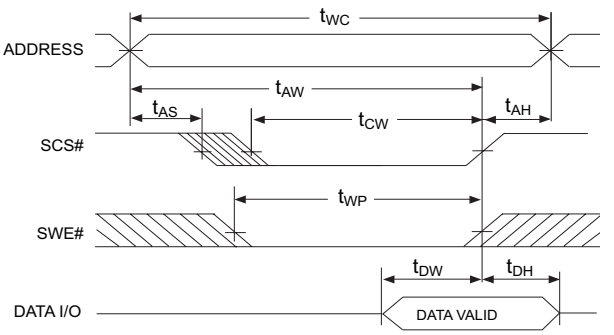
READ CYCLE 2 (SWE# = V_{IH})

FIGURE 5 – SRAM WRITE CYCLE — SWE# CONTROLLED



WRITE CYCLE 1, SWE# CONTROLLED

FIGURE 6 – SRAM WRITE CYCLE — SCS# CONTROLLED



WRITE CYCLE 2, SCS# CONTROLLED

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FWE# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15	sec
Read Recovery Time Before Write	t_{GHWL}		0		0		µs
V_{CC} Set-up Time		t_{VCS}	50		50		µs
Chip Programming Time				11		11	sec
Chip Select Hold Time		t_{OEH}	10		10		ns
Chip Erase Time (3)				64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7ns.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90		-120		Unit
			Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	90		120		ns
Address Access Time	t_{AVQV}	t_{ACC}		90		120	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		90		120	ns
OE# to Output Valid	t_{GLQV}	t_{OE}		35		50	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		30	ns
OE# High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		30	ns
Output Hold from Address, CS# or OE# Change, whichever is first	t_{AXQX}	t_{OH}	0		0		ns

1. Guaranteed by design, not tested.

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-970		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		ns
FWE# Setup Time	t_{WLEL}	t_{WS}	0		0		ns
FCS# Pulse Width	t_{ELEH}	t_{CP}	45		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		ns
FCS# Pulse Width High	t_{EHEL}	t_{CPH}	20		20		ns
Duration Of Programming Operation (1)	t_{WHWH1}			300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15	sec
Read Recovery Time	t_{GHEL}		0		0		ns
Chip Programming Time				11		11	sec
Chip Erase Time (3)				64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7ns.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIGURE 7 – AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS

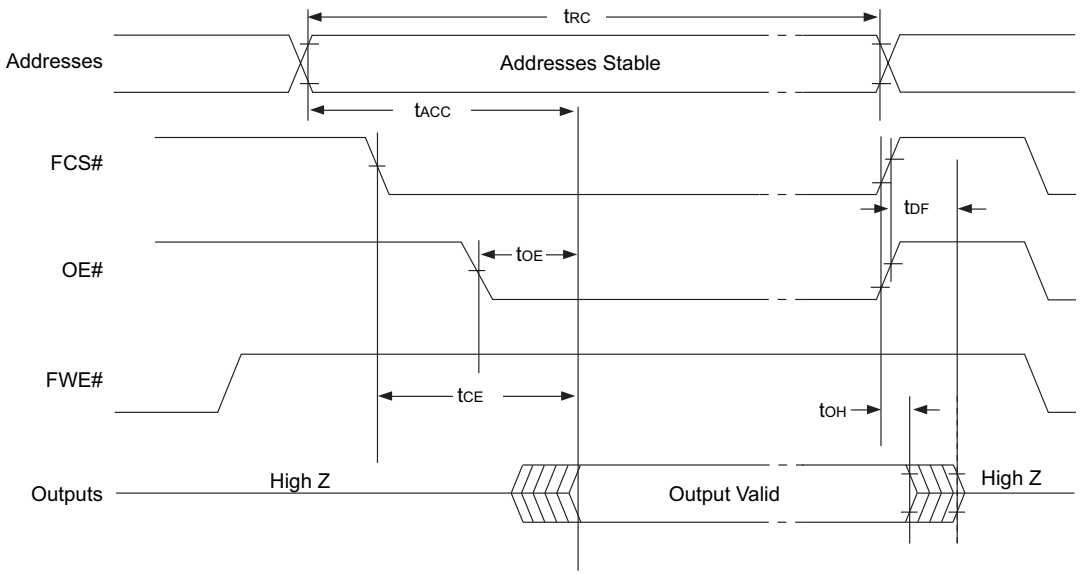
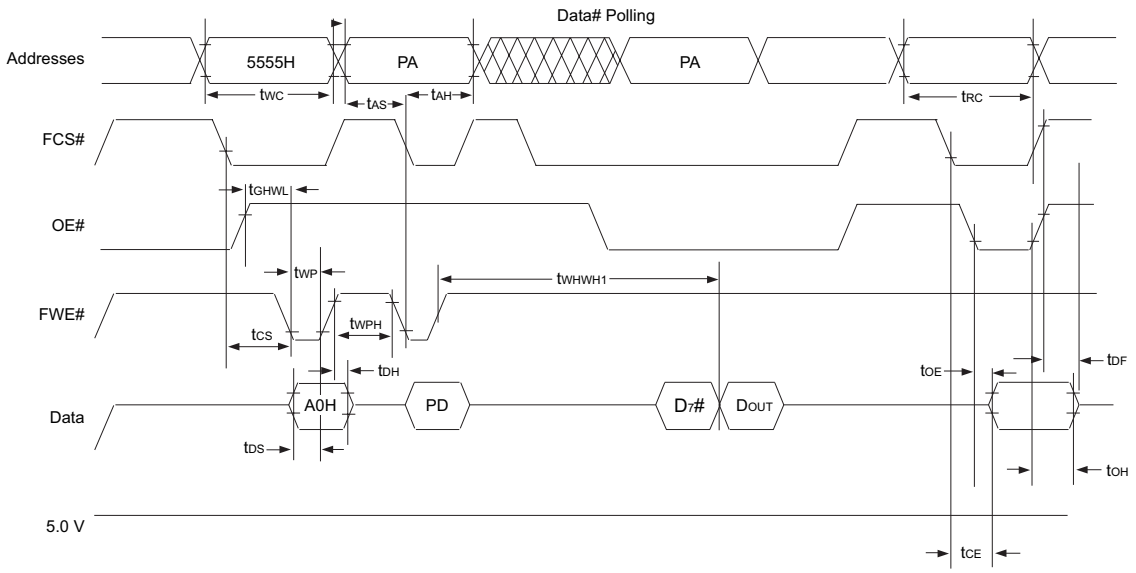
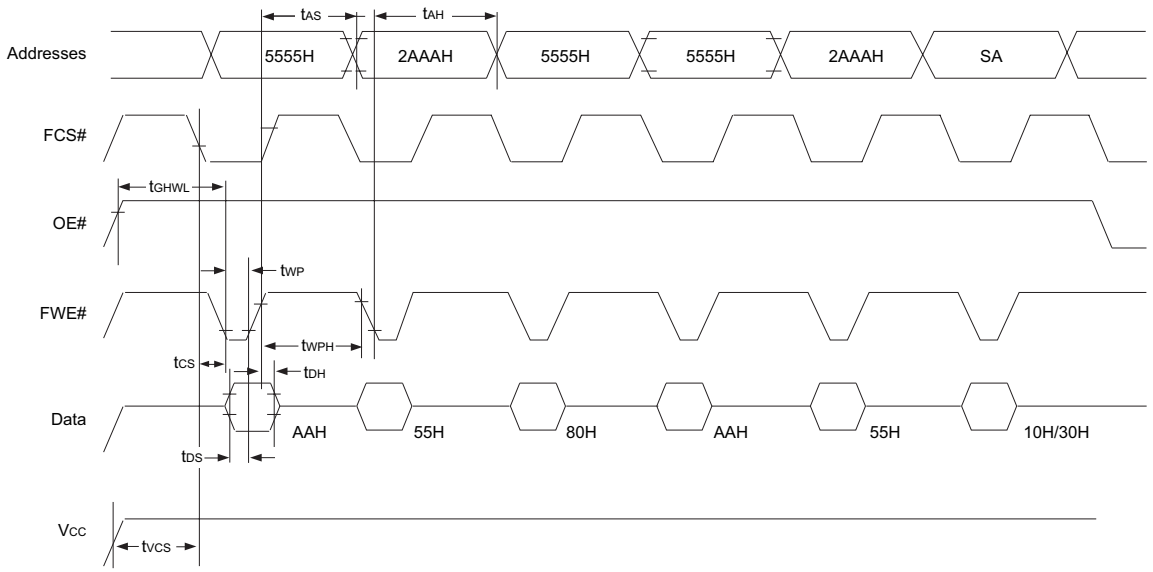


FIGURE 8 – WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FWE# CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIGURE 9 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



Note: SA is the sector address for Sector Erase.

FIGURE 10 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY

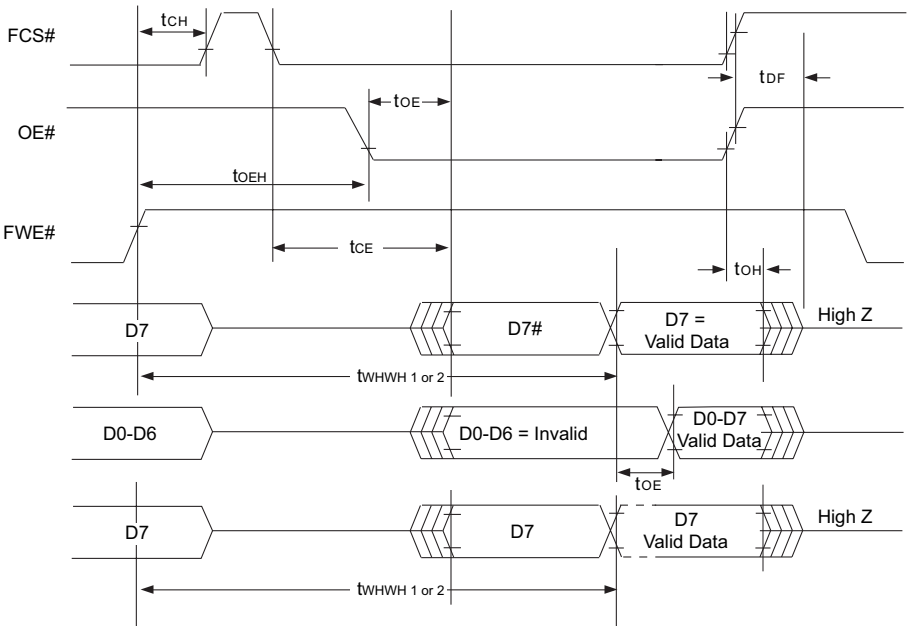
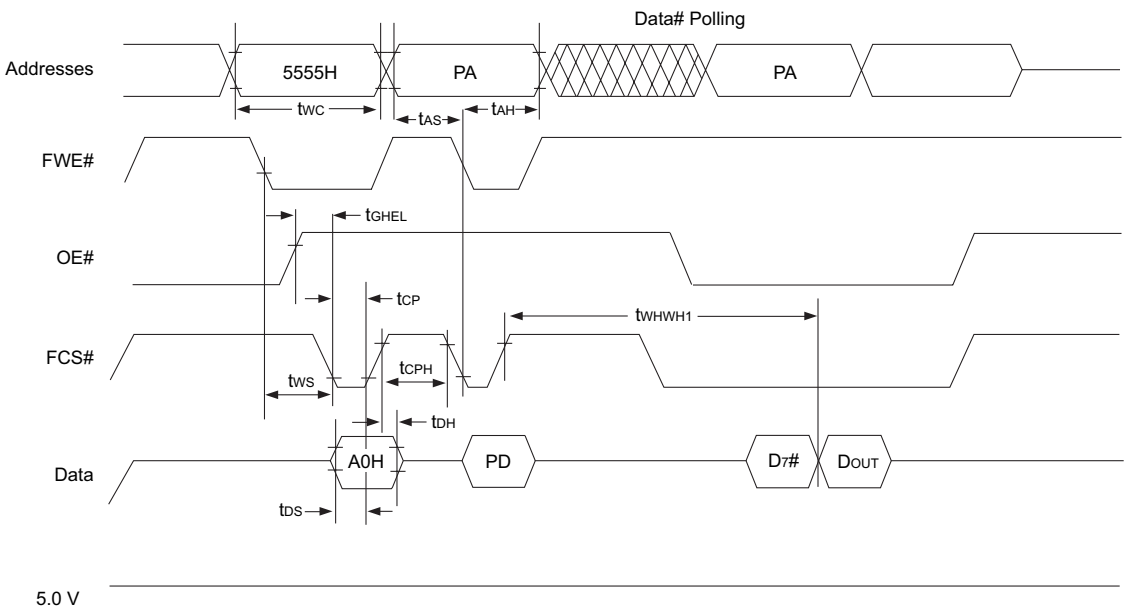
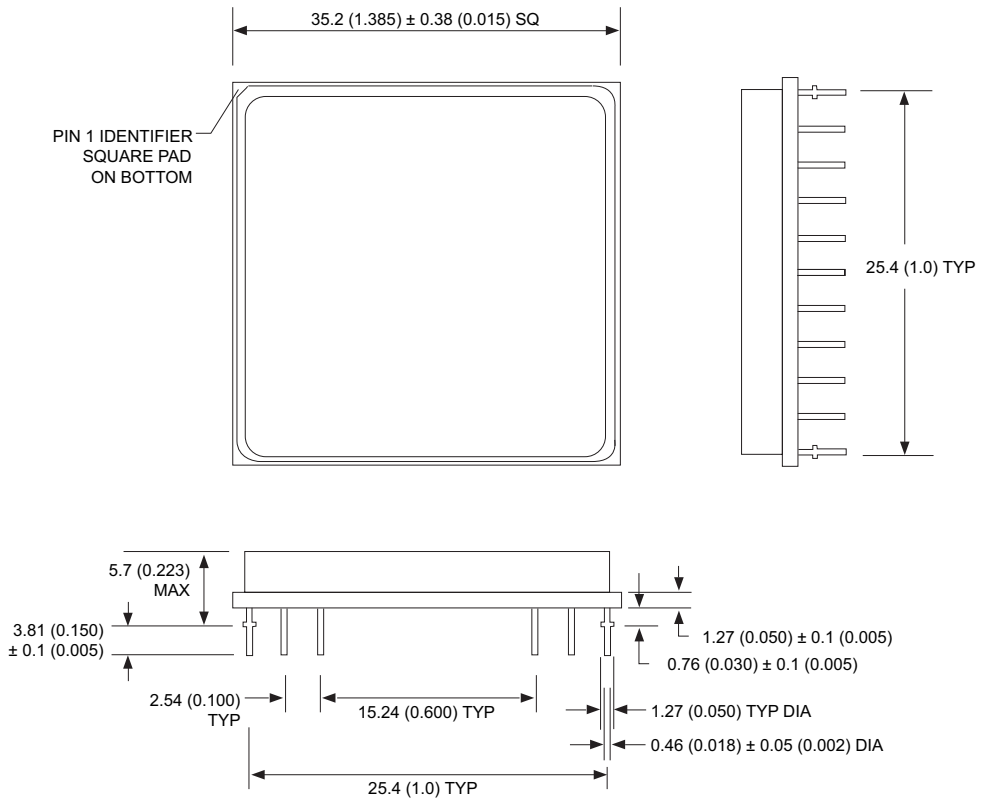


FIGURE 11 – WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, CS# CONTROLLED



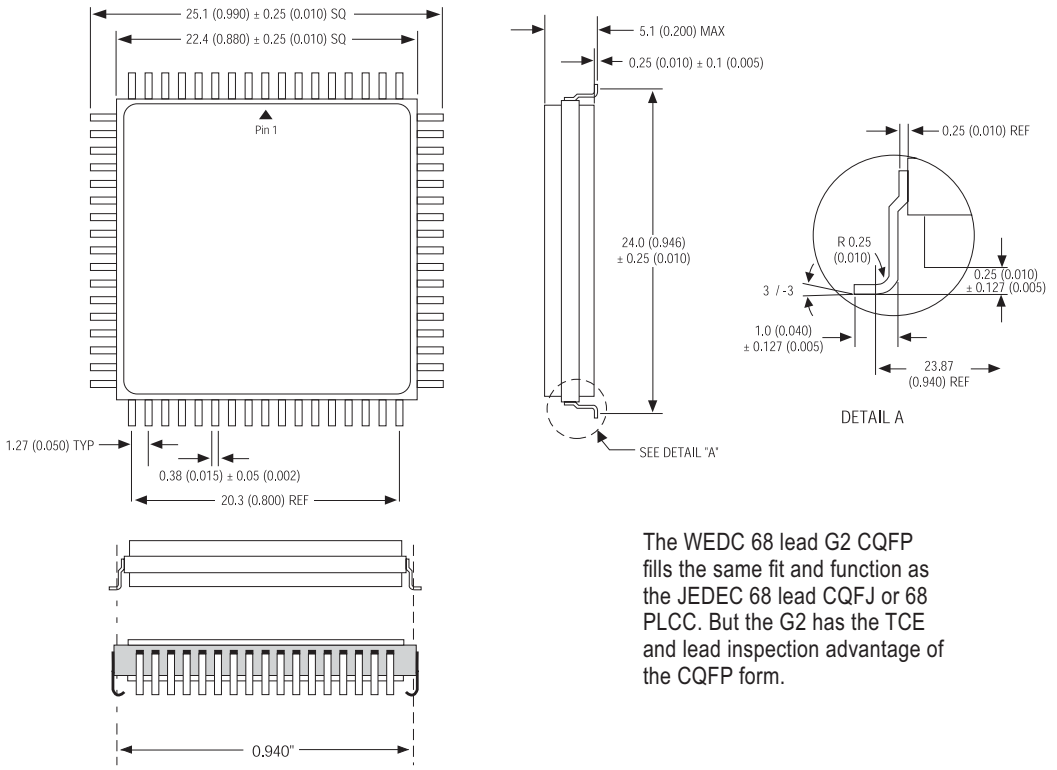
NOTES:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)



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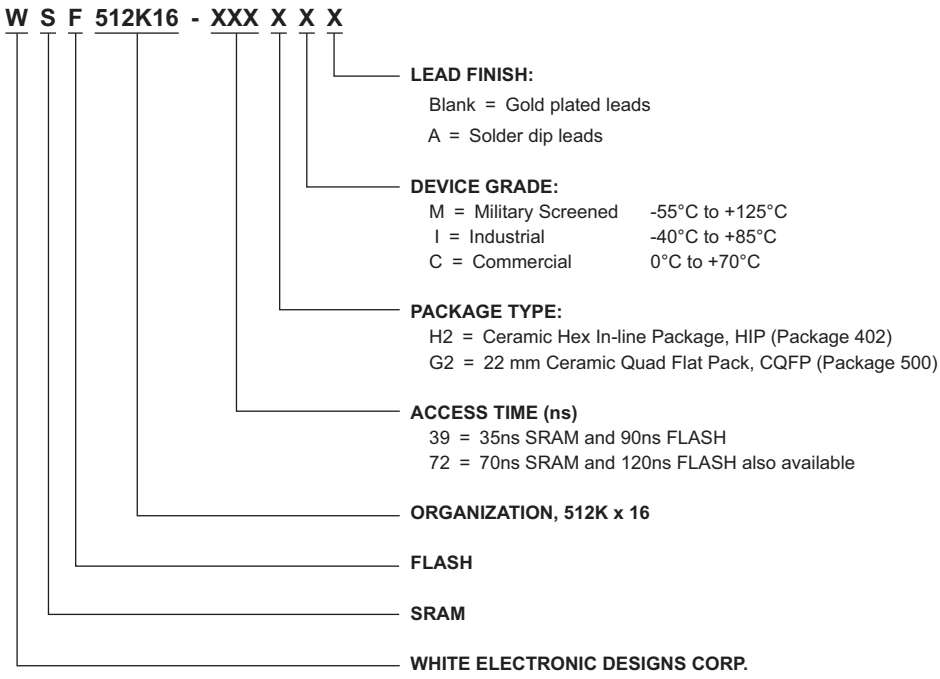
ORDERING INFORMATION



DEVICE TYPE	SRAM SPEED	FLASH SPEED	PACKAGE	SMD NO.
512K x 16 Mixed Module	70ns	120ns	66 pin HIP (H2)	5962-96901 01HXX
512K x 16 Mixed Module	35ns	90ns	66 pin HIP (H2)	5962-96901 02HXX
512K x 16 Mixed Module	70ns	120ns	68 lead CQFP/J (G2)	5962-96901 01HMX
512K x 16 Mixed Module	35ns	90ns	68 lead CQFP/J (G2)	5962-96901 02HMX