

ICs for use with Crystal Oscillators

GENERAL DESCRIPTION

The XC2164 series are high frequency, low current consumption CMOS ICs with built-in crystal oscillator and divider circuits. For fundamental oscillation, output is selectable from any one of the following values for f_0 : $f_0/1$, $f_0/2$, $f_0/4$, and $f_0/8$. With oscillation capacitors and a feedback resistor built-in, it is possible to configure a stable fundamental oscillator or 3rd overtone oscillator using only an external crystal. Also the series has stand-by function built-in and the type, which suspends the oscillation completely (XC2164A~D type) or the type suspends only an output (XC2164K~N type) are available. The XC2164 series are integrated into SOT-26 packages. The series is also available in chip form.

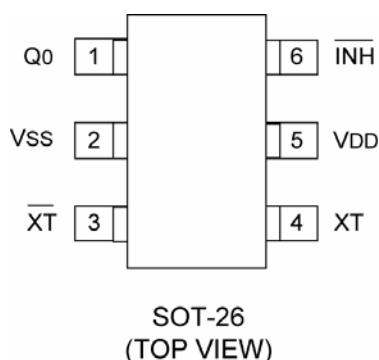
APPLICATIONS

- Crystal oscillation modules
- Clocks for micro computer, DSPs
- Communication equipment
- Various system clocks

FEATURES

- Oscillation Frequency** : 4MHz ~ 30MHz (Fundamental)
20MHz ~ 125MHz (3rd Overtone)
- Divider Ratio** : Selectable from $f_0/1$, $f_0/2$, $f_0/4$, $f_0/8$ ($f_0/2$, $f_0/4$, $f_0/8$ are fundamental only)
- Output** : 3-State
- Operating Voltage Range** : $3.3V \pm 10\%$, $5.0V \pm 10\%$
- Low Power Consumption** : Stand-by function included
Selectable from Chip Enable type and Output Enable type
- CMOS**
- Built-in Oscillation Feedback Resistor**
- Built- in Oscillation Capacitors C_g , C_d**
- Packages** : SOT-26, Chip Form (1.3x0.8mm)

PIN CONFIGURATION



PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
1	Q_0	Clock Output
2	V_{SS}	Ground
3	$/XT$	Crystal Oscillator Connection (Output)
4	XT	Crystal Oscillator Connection (Input)
5	V_{DD}	Power Supply
6	$/INH$	Stand-by Control*

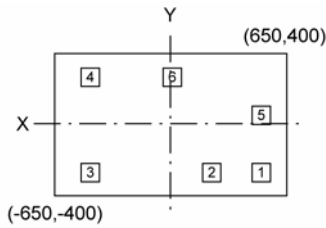
*Stand-by control pin has a pull-up resistor built-in. unit [μm]

$/INH$, Q_0 PIN FUNCTION

$/INH$	Q_0
"H" or OPEN	Clock Output
"L"	High impedance

H = High level
L = Low level

PAD LAYOUT FOR CHIP FORM



Size (Chip) : 1.3x0.8mm
 Thickness (Chip) : XC2164xx1xxT : 280±20 μm
 : XC2164xx1xxF : 200±20 μm
 Backside (Chip) : V_{DD} Level
 Aperture (Pad) : 100x100 μm

PAD DIMENSIONS

PIN NUMBER	PIN NAME	PAD DIMENSIONS	
		X	Y
1	Q ₀	514	- 264
2	V _{SS}	222	- 264
3	/ XT	- 450	- 264
4	XT	- 450	264
5	V _{DD}	514	27
6	/ INH	47	264

unit [μm]

PRODUCT CLASSIFICATION

Ordering Information

XC2164

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
	Divider Ratio & /INH Pin Function	A	: Chip Enable: f0/1
		B	: Chip Enable: f0/2 (Fundamental only)
		C	: Chip Enable: f0/4 (Fundamental only)
		D	: Chip Enable: f0/8 (Fundamental only)
		K	: Output Enable: f0/1
		L	: Output Enable: f0/2 (Fundamental only)
		M	: Output Enable: f0/4 (Fundamental only)
		N	: Output Enable: f0/8 (Fundamental only)
	Chip Surface Treatment	5	: Not polyimide coating on the chip surface (SOT-26 only)
		6	: Polyimide coating on the chip surface (Chip form only)
	Duty Level	1	: CMOS (V _{DD} /2) *TTL: Fundamental 4MHz to 30MHz
	Frequency Range & R _f , C _g , C _d Values	(Table 1)	: 3rd Overtone, built-in type
		(Table 2)	: Fundamental, built-in type
	Packages	C	: Chip form
		M	: SOT-26
	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed
		T	: Chip tray (Wafer thickness : 280 ± 20 μm)
		F	: Chip tray (Wafer thickness : 200 ± 20 μm)

Table 1: 3rd Overtone, Built-In Type

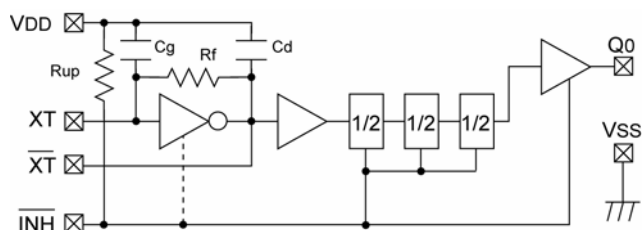
SYMBOL	FREQUENCY RANGE		R _f (k Ω)	C _g (pF)	C _d (pF)
	3.3V ±10%	5.0V ±10%			
A	-	20MHz to 30MHz	9.0	21.5	21.5
B	20MHz to 30MHz	30MHz to 40MHz	6.5	20.0	20.0
C	30MHz to 40MHz	40MHz to 50MHz	5.0	16.0	16.0
D	40MHz to 50MHz	50MHz to 65MHz	3.5	14.0	14.0
E	50MHz to 65MHz	65MHz to 80MHz	2.8	12.5	12.5
F	65MHz to 80MHz	80MHz to 95MHz	2.5	10.0	10.0
H	80MHz to 95MHz	95MHz to 110MHz	2.2	8.0	8.0
K	95MHz to 110MHz	110MHz to 125MHz	2.0	7.0	7.0
L	110MHz to 125MHz	-	2.3	5.5	5.5

Table 2: Fundamental, Built-In Type

SYMBOL	FREQUENCY RANGE		R _f (k Ω)	C _g (pF)	C _d (pF)
	3.3V ±10%	5.0V ±10%			
M, V	4MHz to 30MHz	4MHz to 30MHz	3.5/7.0	20.0	20.0
T	4MHz to 30MHz	4MHz to 30MHz	3.5/7.0	35.0	35.0

(*)R_f = 3.5M @V_{DD} = 5.0V Operation
 R_f = 7.0 M @V_{DD} = 3.3V Operation

BLOCK DIAGRAM



Built-in oscillation capacitors, oscillation feedback resistor

ABSOLUTE MAXIMUM RATINGS

Ta=25

PARAMETER	SYMBOL	CONDITIONS	UNITS
Supply Voltage	V _{DD}	V _{SS} - 0.3 ~ V _{SS} + 7.0	V
Input Voltage	V _{IN}	V _{SS} - 0.3 ~ V _{DD} + 0.3	V
Power Dissipation	P _d	250*	mW
Operating Temperature Range	T _{opr}	- 40 ~ + 85	
Storage Temperature Range	T _{stg}	- 65 ~ + 150 (Chip Form)	
		- 55 ~ + 125 (SOT-26)	

** When implemented on a glass epoxy PCB. (SOT-26 package)

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

XC2164Ax1M, T, V / XC2164Kx1M, T, V (Fundamental)

5.0V operation (unless otherwise stated, V_{DD}=5.0V, No Load, Ta= -30~+80)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Operating Voltage	V _{DD}		4.5	5.0	5.5	V	
"H" Level Input Voltage	V _{IH}		2.4	-	-	V	
"L" Level Input Voltage	V _{IL}		-	-	0.4	V	
"H" Level Output Voltage	V _{OH}	CMOS: V _{DD} =4.5V, I _{OH} = - 16mA	3.9	4.2	-	V	
"L" Level Output Voltage	V _{OL}	CMOS: V _{DD} =4.5V, I _{OH} =16mA	-	0.3	0.4	V	
Supply Current 1	I _{DD1}	/INH=Open, Q ₀ =Open f=30MHz	XC2164Ax1M, V	-	11	(15)	mA
			XC2164Ax1T	-	11	(15)	
			XC2164Kx1M, V	-	11	(15)	
			XC2164Kx1T	-	11	(15)	
Supply Current 2	I _{DD2}	/INH="L", Q ₀ =Open f=30MHz	XC2164Ax1M, V	-	5	(8)	μA
			XC2164Ax1T	-	5	(8)	
			XC2164Kx1M, V	-	(T.B.D.*)	(T.B.D.*)	mA
			XC2164Kx1T	-	9	(14)	
Input Pull-Up Resistance 1	R _{UP1}	/INH="L"	0.5	1.0	2.0	M	
Input Pull-Up Resistance 2	R _{UP2}	/INH=0.7 V _{DD}	25	50	100	k	
Internal Oscillation Feedback Resistance	R _f		-	3.5	-	M	
Output Disable Leak Current	I _{OZ}	/INH="L"	-	-	10	μA	

* T.B.D.: To be determined

XC2164Ax1M, XC2164Kx1M (Fundamental)

3.3V operation (unless otherwise stated, V_{DD}=3.3V, No Load, Ta= -30~+80)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Operating Voltage	V _{DD}		2.97	3.30	3.63	V	
"H" Level Input Voltage	V _{IH}		2.4	-	-	V	
"L" Level Input Voltage	V _{IL}		-	-	0.4	V	
"H" Level Output Voltage	V _{OH}	CMOS: V _{DD} =2.97V, I _{OH} = - 8mA	2.5	-	-	V	
"L" Level Output Voltage	V _{OL}	CMOS: V _{DD} =2.97V, I _{OH} =8mA	-	-	0.4	V	
Supply Current 1	I _{DD1}	/INH=Open, Q ₀ =Open, f=30MHz	XC2164Ax1M	-	5	(8)	mA
			XC2164Kx1M	-	5	(8)	
Supply Current 2	I _{DD2}	/INH="L", Q ₀ =Open, f=30MHz	XC2164Ax1M	-	2	(4)	μA
			XC2164Kx1M	-	(T.B.D.*)	(T.B.D.*)	mA
Input Pull-Up Resistance 1	R _{UP1}	/INH="L"	1.0	2.0	4.0	M	
Input Pull-Up Resistance 2	R _{UP2}	/INH=0.7 V _{DD}	35	70	140	k	
Internal Oscillation Feedback Resistance	R _f		-	7.0	-	M	
Output Disable Leak Current	I _d	/INH="L"	-	-	10	μA	

* T.B.D.: To be determined

ELECTRICAL CHARACTERISTICS (Continued)

DC Electrical Characteristics (Continued)

XC2164Ax1T, V / XC2164Kx1T, V (Fundamental)

3.3V operation (unless otherwise stated, V_{DD}=3.3V, No Load, T_a= -30~+80)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Operating Voltage	V _{DD}		2.50	3.30	3.63	V	
"H" Level Input Voltage	V _{IH}		2.4	-	-	V	
"L" Level Input Voltage	V _{IL}		-	-	0.4	V	
"H" Level Output Voltage	V _{OH}	CMOS: 2.97V, I _{OH} = - 8mA	2.5	-	-	V	
"L" Level Output Voltage	V _{OL}	CMOS: 2.97V, I _{OH} =8mA	-	-	0.4	V	
Supply Current 1	I _{DD1}	/INH=Open, Q ₀ =Open, f=30MHz	XC2164Ax1T	-	4	(6.5)	mA
			XC2164Ax1V	-	5	(8)	
			XC2164Kx1T	-	4	(6.5)	
			XC2164Kx1V	-	5	(8)	
Supply Current 2	I _{DD2}	/INH="L", Q ₀ =Open, f=30MHz	XC2164Ax1T	-	2	(4)	μ A
			XC2164Ax1V	-	2	(4)	mA
			XC2164Kx1T	-	(T.B.D.*)	(T.B.D.*)	
			XC2164Kx1V	-	(T.B.D.*)	(T.B.D.*)	
Input Pull-Up Resistance 1	R _{UP1}	/INH="L"	1.0	2.0	4.0	M	
Input Pull-Up Resistance 2	R _{UP2}	/INH=0.7 V _{DD}	35	70	140	k	
Internal Oscillation Feedback Resistance	R _f		-	7.0	-	M	
Output Disable Leakage Current	I _{OZ}	/INH="L"	-	-	10	μ A	

* T.B.D.: To be determined

Comparative Chart of Oscillation Frequency vs. Supply Voltage, and Negative Resistance Value

SYMBOL	OSCILLATION FREQUENCY vs. SUPPLY VOLTAGE		NEGATIVE RESISTANCE VALUE	
	V _{DD} =3.3V±10%	V _{DD} =5.0V±10%	V _{DD} =3.3V	V _{DD} =5.0V
M	± 4.3ppm	± 4.5ppm	- 130	- 220
V	± 1.2ppm	± 2.1ppm	- 150	- 250
T	± 9.4ppm	± 7.0ppm	- 660	- 760

(The designed value when 30MHz crystal is used.)

ELECTRICAL CHARACTERISTICS (Continued)

DC Electrical Characteristics (Continued)

XC2164Ax1A ~ XC2164Ax1K (3rd Overtone)

5.0V Operation (Unless otherwise stated, V_{DD}=5.0V, No Load, T_a= -30~+80)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Operating Voltage	V _{DD}		4.5	5.0	5.5	V	
"H" Level Input Voltage	V _{IH}		2.4	-	-	V	
"L" Level Input Voltage	V _{IL}		-	-	0.4	V	
"H" Level Output Voltage	V _{OH}	CMOS: 4.5V, I _{OH} = -16mA	3.9	4.2	-	V	
"L" Level Output Voltage	V _{OL}	CMOS: 4.5V, I _{OH} =16mA	-	0.3	0.4	V	
Supply Current 1	I _{DD1}	/INH=Open, Q ₀ =Open	XC2164Ax1A, f ₀ =30MHz	-	17.0	(23)	mA
			XC2164Ax1B, f ₀ =40MHz	-	17.0	(23)	
			XC2164Ax1C, f ₀ =55MHz	-	19.0	(26)	
			XC2164Ax1D, f ₀ =70MHz	-	23.0	(32)	
			XC2164Ax1E, f ₀ =85MHz	-	24.0	(32)	
			XC2164Ax1F, f ₀ =100MHz	-	30.0	(40)	
			XC2164Ax1H, f ₀ =110MHz	-	30.0	(40)	
XC2164Ax1K, f ₀ =125MHz	-	30.0	(40)				
Supply Current 2	I _{DD2}	/INH="L", Q ₀ =Open	-	5.0	(8)	μ A	
Input Pull-Up Resistance 1	R _{UP1}	/INH="L"	0.5	1.0	2.0	M	
Input Pull-Up Resistance 2	R _{UP2}	/INH=0.7 V _{DD}	25	50	100	k	
Internal Oscillation Feedback Resistance	R _f	XC2164Ax1A	-	9.0	-	k	
		XC2164Ax1B	-	6.5	-		
		XC2164Ax1C	-	5.0	-		
		XC2164Ax1D	-	3.5	-		
		XC2164Ax1E	-	2.8	-		
		XC2164Ax1F	-	2.5	-		
		XC2164Ax1H	-	2.2	-		
XC2164Ax1K	-	2.0	-				
Output Disable Leak Current	I _{oz}	/INH="L"	-	-	10	μ A	

ELECTRICAL CHARACTERISTICS (Continued)

DC Electrical Characteristics (Continued)

XC2164Ax1B, C, E, F, H, K, L (3rd Overtone)

3.3V Operation (unless otherwise stated, V_{DD}=3.3V, No Load, T_a= -30~+80)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Operating Voltage	V _{DD}		2.97	3.30	3.63	V	
"H" Level Input Voltage	V _{IH}		2.4	-	-	V	
"L" Level Input Voltage	V _{IL}		-	-	0.4	V	
"H" Level Output Voltage	V _{OH}	CMOS: 2.97V, I _{OH} = - 8mA	2.5	-	-	V	
"L" Level Output Voltage	V _{OL}	CMOS: 2.97V, I _{OH} =8mA	-	-	0.4	V	
Supply Current 1	I _{DD1}	/INH=Open, Q ₀ =Open	XC2164Ax1B, f ₀ =30MHz	-	4.5	(7)	mA
			XC2164Ax1C, f ₀ =40MHz	-	5.0	(8)	
			XC2164Ax1E, f ₀ =70MHz	-	8.0	(13)	
			XC2164Ax1F, f ₀ =85MHz	-	8.5	(13)	
			XC2164Ax1H, f ₀ =100MHz	-	9.5	(15)	
			XC2164Ax1K, f ₀ =110MHz	-	10.0	(15)	
Supply Current 2	I _{DD2}	/INH="L", Q ₀ =Open	-	2.0	-	μA	
Input Pull-Up Resistance 1	R _{UP1}	/INH="L"	1.0	2.0	4.0	M	
Input Pull-Up Resistance 2	R _{UP2}	/INH=0.7 V _{DD}	35	70	140	k	
Internal Oscillation Feedback Resistance	R _f	XC2164Ax1B	-	6.5	-	k	
		XC2164Ax1C	-	5.0	-		
		XC2164Ax1E	-	2.8	-		
		XC2164Ax1F	-	2.5	-		
		XC2164Ax1H	-	2.2	-		
		XC2164Ax1K	-	2.0	-		
XC2164Ax1L	-	2.3	-				
Output Disable Leak Current	I _{OZ}	/INH="L"	-	-	10	μA	

XC2164Ax1D (3rd Overtone)

3.3V Operation (Unless otherwise stated, V_{DD}=3.3V, Oscillation Frequency f₀=48MHz, T_a= -30~+80)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V _{DD}		2.70	3.30	3.63	V
'H' Level Input Voltage	V _{IH}		2.4	-	-	V
'L' Level Input Voltage	V _{IL}		-	-	0.4	V
'H' Level Output Voltage	V _{OH}	CMOS: 2.97V, I _{OH} = - 8mA	2.5	-	-	V
'L' Level Output Voltage	V _{OL}	CMOS: 2.97V, I _{OH} =8mA	-	-	0.4	V
Supply Current 1	I _{DD1}	/INH=Open, Q ₀ =Open		6.5	(10)	mA
Supply Current 2	I _{DD2}	/INH = 'L', Q ₀ =Open	-	2.0	-	μA
Input Pull-Up Resistance 1	R _{UP1}	/INH = 'L'	1.0	2.0	4.0	M
Input Pull-Up Resistance 2	R _{UP2}	/INH = 0.7V _{DD}	35	70	140	k
Internal Oscillation Feedback Resistance	R _f	XC2164Ax1D	-	3.5	-	k
Output Disable Leak Current	I _{OZ}	/INH = 'L'	-	-	10	μA

SWITCHING CHARACTERISTICS

XC2164Ax1M, T, V (Fundamental) <Chip Enable>

(unless otherwise stated, $V_{DD}=3.3V$ or $5.0V$, $T_a=-30\sim+80$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time ^(*)	tr	CMOS: $C_L=15pF$, $0.1V_{DD}\rightarrow 0.9V_{DD}$	-	1.5	-	ns
		TTL: Load=10TTL, $0.4V\rightarrow 2.4V$	-	1.5	-	ns
Output Fall Time ^(*)	tf	CMOS: $C_L=15pF$, $0.9V_{DD}\rightarrow 0.1V_{DD}$	-	1.5	-	ns
		TTL: Load=10TTL, $2.4V\rightarrow 0.4V$	-	1.5	-	ns
Output Duty Cycle	DUTY	CMOS: $C_L=15pF$ @ $0.5V_{DD}$	45	-	55	%
		TTL: Load=10TTL @ $1.4V$	45	-	55	%
Output Disable Delay Time ^(*)	tplz	$f_0=4MHz$, $C_L=15pF$	-	-	100	ns
Output Enable Delay Time ^(*)	tplz	$f_0=4MHz$, $C_L=15pF$	-	-	6	ms
Oscillation Start Time ^(*)	tosc_on	$f_0=4MHz$, $C_L=15pF$	-	-	6	ms

*1: the values are the designed values.

XC2164Ax1A to L (3rd Overtone) <Chip Enable>

(unless otherwise stated, $V_{DD}=3.3V$ or $5.0V$, $T_a=-30\sim+80$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time ^(*)	tr	CMOS: $C_L=15pF$, $0.1V_{DD}\rightarrow 0.9V_{DD}$	-	1.5	-	ns
		TTL: Load=10TTL, $0.4V\rightarrow 2.4V$	-	1.5	-	ns
Output Fall Time ^(*)	tf	CMOS: $C_L=15pF$, $0.9V_{DD}\rightarrow 0.1V_{DD}$	-	1.5	-	ns
		TTL: Load=10TTL, $2.4V\rightarrow 0.4V$	-	1.5	-	ns
Output Duty Cycle	DUTY	CMOS: $C_L=15pF$ @ $0.5V_{DD}$	45	-	55	%
		TTL: Load=10TTL @ $1.4V$	45	-	55	%
Output Disable Delay Time ^(*)	tplz	$f_0=20MHz$, $C_L=15pF$	-	-	100	ns
Output Enable Delay Time ^(*)	tplz	$f_0=20MHz$, $C_L=15pF$	-	-	6	ms
Oscillation Start Time ^(*)	tosc_on	$f_0=20MHz$, $C_L=15pF$	-	-	6	ms

*1: the values are the designed values.

XC2164Kx1M, T, V (Fundamental) <Output Enable>

(unless otherwise stated, $V_{DD}=3.3V$ or $5.0V$, $T_a=-30\sim+80$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time ^(*)	tr	CMOS: $C_L=15pF$, $0.1V_{DD}\rightarrow 0.9V_{DD}$	-	1.5	-	ns
		TTL: Load=10TTL, $0.4V\rightarrow 2.4V$	-	1.5	-	ns
Output Fall Time ^(*)	tf	CMOS: $C_L=15pF$, $0.9V_{DD}\rightarrow 0.1V_{DD}$	-	1.5	-	ns
		TTL: Load=10TTL, $2.4V\rightarrow 0.4V$	-	1.5	-	ns
Output Duty Cycle	DUTY	CMOS: $C_L=15pF$ @ $0.5V_{DD}$	45	-	55	%
		TTL: Load=10TTL @ $1.4V$	45	-	55	%
Output Disable Delay Time ^(*)	tplz	$f_0=4MHz$, $C_L=15pF$	-	-	100	ns
Output Enable Delay Time ^(*)	tplz	$f_0=4MHz$, $C_L=15pF$	-	-	10	μs
Oscillation Start Time ^(*)	tosc_on	$f_0=4MHz$, $C_L=15pF$	-	-	6	ms

*1: the values are the designed values.

* The values shown are preliminary so that the values may be changed without a prior announcement.

SWITCHING WAVEFORMS

Switching Time

(1) CMOS Output

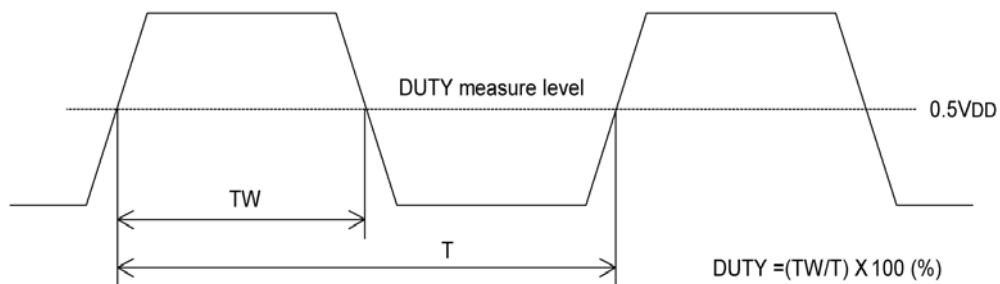


(2) TTL Output

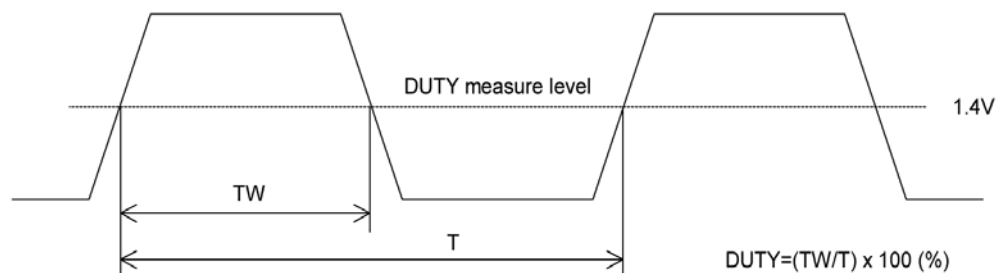


Duty Cycle

(1) CMOS Output

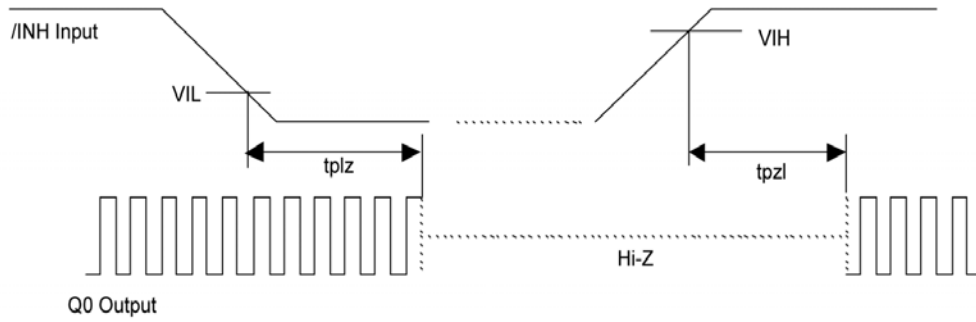


(2) TTL Output



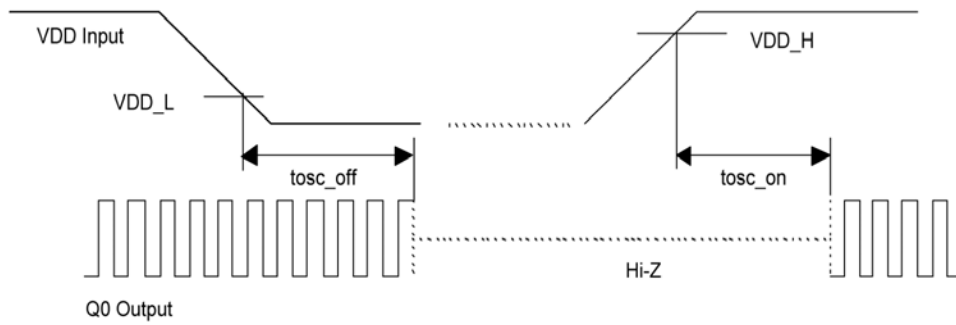
SWITCHING WAVEFORMS (Continued)

(3) Output Disable Delay Time, Output Enable Delay Time *)The /INH pin input waveform: less than $t_r=t_f=10\text{ns}$, VDD input



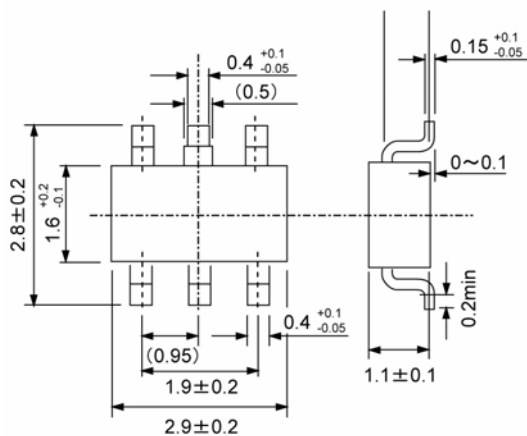
(4) Oscillation Start Time: t_{osc_on}

*)The VDD pin input waveform : less than $t_r=t_f=10\text{ns}$, /INH=Open



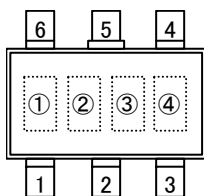
PACKAGING INFORMATION

SOT-26



MARKING RULE

SOT-26



SOT-26
(TOP VIEW)

Represents product series

MARK
4

Represents divider ratio

<Chip Enable>

MARK	RATIO	MARK	RATIO
A	f0/1	C	f0/4
B	f0/2	D	f0/8

*B, C, D: fundamental only

<Output Enable>

MARK	RATIO	MARK	RATIO
K	f0/1	M	f0/4
L	f0/2	N	f0/8

*L, M, N: fundamental only

Represents recommended frequency & Rf, Cg & Cd values

* Please refer to the ordering information, SYMBOL to

Represents assembly lot number

(Based on internal standards)

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