XC9101 Series

PWM Controlled Step-Up DC/DC Controllers

◆Input Voltage Range : 2.5V ~ 20V
◆Output Voltage Range
: 2.5V ~ 16V
(Fixed Voltage Type)
: 30V + (Adjustable Type)
◆Oscillation Frequency Range
: 100kHz ~ 600kHz
◆Output Current : up to 1.5A
◆Ceramic Capacitor Compatible
◆MSOP-8A Package

■Applications

- ●Mobile, Cordless phones
- ●Palm top computers, PDAs
- ●Portable games
- ●Cameras, Digital cameras
- ●Laptops

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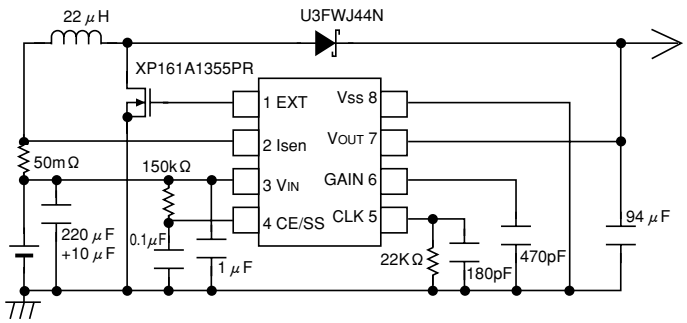
■General Description

The XC9101 series are step-up multiple current and voltage feedback DC/DC controller ICs. Current sense, clock frequencies and amp feedback gain can all be externally regulated.
A stable power supply is possible with output currents of up to 1.5A.
With output voltage fixed internally, VOUT is selectable in 0.1V steps within a 2.5V - 16.0V range (± 2.5%).
For output voltages outside this range, we recommend the FB version which has a 0.9V internal reference voltage. Using this version, the required output voltage can be set-up using 2 external resistors.
Switching frequencies can also be set-up externally within a range of 100~600 kHz and therefore frequencies suited to your particular application can be selected.
With the current sense function, peak currents (which flow through the driver transistor and the coil) can be controlled. Soft-start time can be adjusted using external resistor and capacitor.
During shutdown (CE pin =L), consumption current can be reduced to as little as 0.5μA (TYP.) or less.

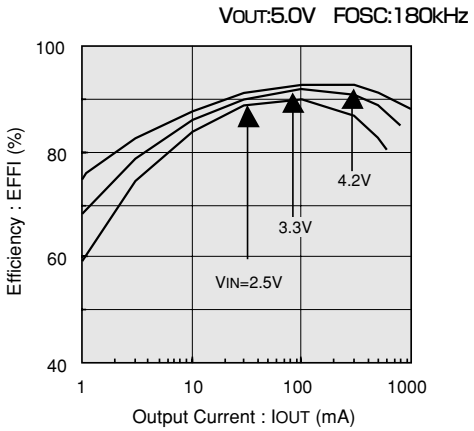
■Features

- ●**Stable Operations via Current & Voltage Multiple Feedback**
- ●**Unlimited Options for Peripheral Selection**
- ●**Current Protection Circuit**
- ●**Ceramic Capacitor Compatible**

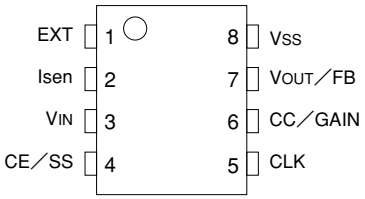
■Typical Application Circuit



■Typical Performance Characteristic



■Pin Configuration



MSOP-8A
(TOP VIEW)

■Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION
1	EXT	Driver
2	Isen	Current Sense
3	VIN	Power Input
4	CE／SS	CE/Soft Start
5	CLK	Clock Input
6	CC／GAIN	Phase Compensation
7	VOUT／FB	Voltage Sense
8	VSS	Ground

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■Product Classification

●Ordering Information

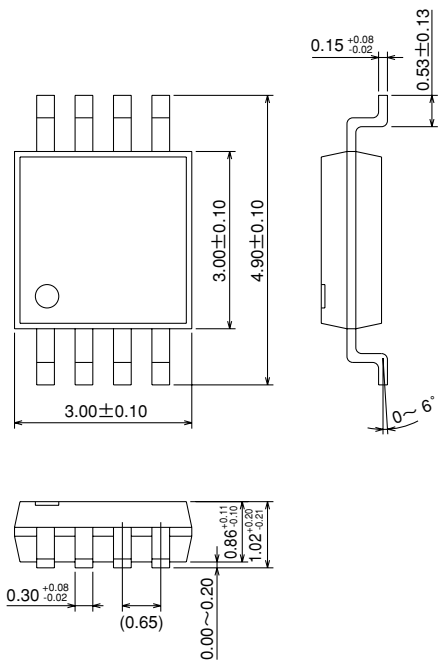
X C 9 1 0 1 ①②③④⑤⑥

DISIGNATOR	SYMBOL	VOUT/FB	Soft-start
①	C	VOUT (Fixed Voltage Type)	Soft-start externally set-up
	D	FB	Soft-start externally set-up
②③	Number	Output Voltage : For voltages above 10V, see below : 10=A, 11=B, 12=C, 13=D, 14=E, 15=F, 16=H e.g. VOUT=2.3V→②=2, ③=3 VOUT=13.5V→②=D, ③=5 FB products→②=0, ③=9 fixed	
④	A	Adjustable Frequency	
⑤	K	MSOP-8A	
⑥	R	Embossed tape. Standard Feed	
	L	Embossed tape. Reverse Feed	

The standard output voltages of the XC9101C series are 2.5V, 3.3V, and 5.0V.
Voltages other than those listed are semi-custom.

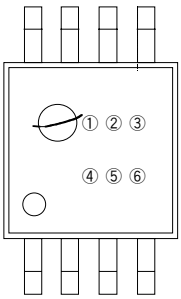
■Packaging Information

●MSOP-8A



■Marking

MSOP-8A



① Represents the product series

DESIGNATOR	PRODUCT NAME
4	XC9101***AK*

② Represents product type, DC/DC converter

DESIGNATOR	TYPE	PRODUCT NAME
C	VOUT, CE PIN	XC9101C**AK*
D	FB, CE PIN	XC9101D09AK*

③ Represents integral number of output voltage, or FB type

DESIGNATOR	VOLTAGE（V）	PRODUCT NAME	DESIGNATOR	VOLTAGE（V）	PRODUCT NAME
2	2. X	XC9101C2*AK*	A	10. X	XC9101CA*AK*
3	3. X	XC9101C3*AK*	B	11. X	XC9101CB*AK*
4	4. X	XC9101C4*AK*	C	12. X	XC9101CC*AK*
5	5. X	XC9101C5*AK*	D	13. X	XC9101CD*AK*
6	6. X	XC9101C6*AK*	E	14. X	XC9101CE*AK*
7	7. X	XC9101C7*AK*	F	15. X	XC9101CF*AK*
8	8. X	XC9101C8*AK*	H	16. X	XC9101CH*AK*
9	9. X	XC9101C9*AK*			
0	FB products	XC9101D09AK*			

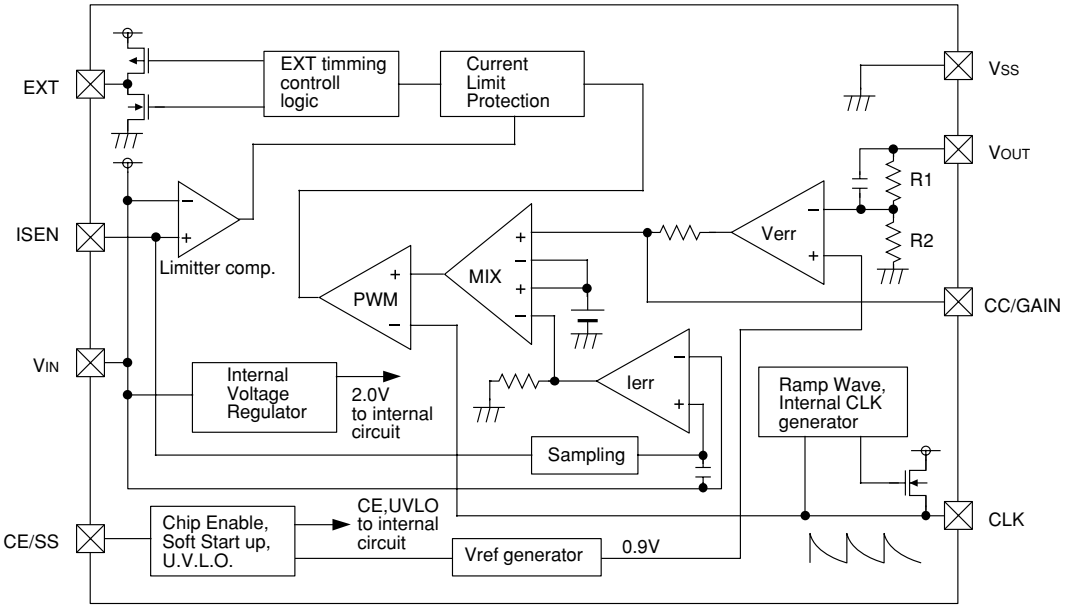
④ Represents decimal number of output voltage

DESIGNATOR	VOLTAGE（V）	PRODUCT NAME
0	X. 0	XC9101C*0AK*
3	X. 3	XC9101C*3AK*
9	FB products	XC9101D09AK*

⑤ Represents oscillation frequency's control type

DESIGNATOR	TYPE	PRODUCT NAME
A	Adjustable Frequency	XC9101***AK*

■Block Diagram



■Absolute Maximum Ratings

Ta=25℃

PARAMETER	SYMBOL	RATINGS	UNITS
EXT Pin Voltage	VEXT	−0.3～VDD+0.3	V
Isen Pin Voltage	VIsen	−0.3～+22	V
VIN Pin Voltage	VIN	−0.3～+22	V
CE/SS Pin Voltage	VCE	−0.3～+22	V
CLK Pin Voltage	VCLK	−0.3～VDD+0.3	V
CC/GAIN Pin Voltage	VCC	−0.3～VDD+0.3	V
VOUT/FB Pin Voltage	VOUT/FB	−0.3～+22	V
EXT Pin Current	IEXT	±100	mA
Continuous Total Power Dissipation	Pd	150	mW
Operating Ambient Temperature	Topr	−40～+85	℃
Storage Temperature	Tstg	−55～+125	℃

■Electrical Characteristics

XC9101C33AKR

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PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	3.218	3.300	3.382	V	①
Maximum Operating Voltage	VINmax		20	—	—	V	①
Minimum Operating Voltage	VINmin		—	—	2.5	V	①
Supply Current 1	IDD1	VIN=2.5V VOUT=CE=Set Output Voltage×0.95V		150	255	μA	②
Supply Current 2	IDD2	VIN=2.5V, CE=VIN VOUT=Set Output Voltage×1.05V		90	176	μA	②
Stand-by Current	ISTB	VIN=2.5V, CE=VOUT=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	$\frac{\Delta FOSC}{\Delta VIN \cdot FOSC}$	VIN=2.5V～20V		±5		%	③
Frequency Temperature Fluctuation	$\frac{\Delta FOSC}{\Delta Topr \cdot FOSC}$	VIN=2.5V Topr=−40～+85℃		±5		%	③
Maximum Duty Cycle	MAXDTY	VOUT=Set Voltage×0.95V	79	85	89	%	④
Minimum Duty Cycle	MINDTY	VOUT=Set Voltage×1.05V			0	%	④
Current Limiter Voltage	ILIM	VIN pin voltage−ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN=2.5V, ISEN=2.5V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE=VIN=2.5V, VOUT=0V	−0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE=0V, VIN=2.5V, VOUT=0V	−0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, VOUT=0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, VOUT=0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	EXT=VIN−0.4V, CE=VIN=2.5V VOUT=Set voltage×0.95V		31	58	Ω	④
EXT "Low" ON Resistance	REXTL	EXT=0.4V, CE=VIN=2.5V VOUT=Set voltage×1.05		27	45	Ω	④
Efficiency *1	EFFI			88		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V→2.5V	5	10	20	ms	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 2.5V unless specified

*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

*2 : The capacity range of the capacitor used to set the external CLK frequency is 150 ~ 220pF

XC9101C50AKR

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	4.875	5.000	5.125	V	①
Maximum Operating Voltage	VINmax		20	—	—	V	①
Minimum Operating Voltage	VINmin		—	—	2.5	V	①
Supply Current 1	IDD1	VIN=3.0V VOUT=CE=Set Output Voltage×0.95V		160	270	μA	②
Supply Current 2	IDD2	VIN=3.0V, CE=VIN VOUT=Set Output Voltage×1.05V		90	176	μA	②
Stand-by Current	ISTB	VIN=3.0V, CE=VOUT=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	ΔFOSC / ΔVIN・FOSC	VIN=2.5V～20V		±5		%	③
Frequency Temperature Fluctuation	ΔFOSC / ΔTopr・FOSC	VIN=3.0V Topr=−40～+85℃		±5		%	③
Maximum Duty Cycle	MAXDTY	VOUT=Set Voltage×0.95V	79	85	89	%	④
Minimum Duty Cycle	MINDTY	VOUT=Set Voltage×1.05V			0	%	④
Current Limiter Voltage	ILIM	VIN pin voltage−ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN=3.0V, ISEN=3.0V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE=VIN=3.0V, VOUT=0V	−0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE=0V, VIN=3.0V, VOUT=0V	−0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, VOUT=0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, VOUT=0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	EXT=VIN−0.4V, CE=VIN=3.0V VOUT=Set voltage×0.95V		27	51	Ω	④
EXT "Low" ON Resistance	REXTL	EXT=0.4V, CE=VIN=3.0V VOUT=Set voltage×1.05V		25	37	Ω	④
Efficiency *1	EFFI			87		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V→3.0V		5		ms	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 3.0V unless specified

*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100

*2 : The capacity range of the capacitor used to set the external CLK frequency is 150 ~ 220pF

XC9101D09AKR

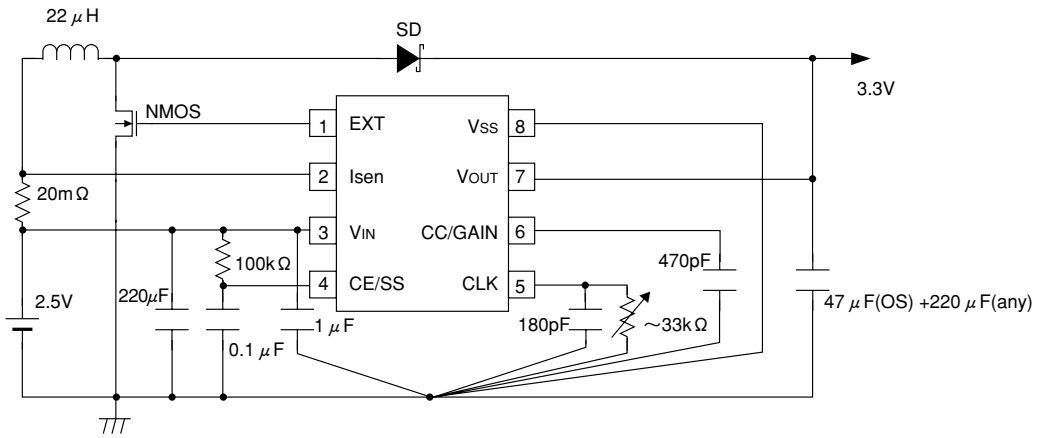
Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Output Voltage	VOUT	IOUT=300mA	0.8775	0.9	0.9225	V	①
Maximum Operating Voltage	VINmax		20	—	—	V	①
Minimum Operating Voltage	VINmin		—	—	2.5	V	①
Supply Current 1	IDD1	VIN=2.5V, VIN=CE, FB=0.9×0.95V		150	255	μA	②
Supply Current 2	IDD2	VIN=2.5V, CE=VIN, VOUT=0.9×1.05V		90	176	μA	②
Stand-by Current	ISTB	VIN=2.5V, CE=FB=VSS		0.5	2.0	μA	②
CLK Oscillation Frequency	FOSC	RT=10.0kΩ, CT=220pF	280	330	380	kHz	③
Frequency Input Stability	ΔFOSC / ΔVIN·FOSC	VIN=2.5V～20V		±5		%	③
Frequency Temperature Fluctuation	ΔFOSC / ΔTopr·FOSC	VIN=2.5V Topr=−40～+85℃		±5		%	③
Maximum Duty Cycle	MAXDTY	VOUT=0.9×0.95V	79	85	89	%	④
Minimum Duty Cycle	MINDTY	VOUT=0.9×1.05V			0	%	④
Current Limiter Voltage	ILIM	VIN pin voltage−ISEN pin voltage	90	150	220	mV	⑥
ISEN Current	IISEN	VIN=2.5V, ISEN=2.5V	4.5	7	13	μA	⑥
CE "High" Current	ICEH	CE=VIN=2.5V, FB=0V	−0.1	0	0.1	μA	⑤
CE "Low" Current	ICEL	CE=0V, VIN=2.5V, FB=0V	−0.1	0	0.1	μA	⑤
CE "High" Voltage	VCEH	Existence of CLK Oscillation, VOUT=0V, CE : Voltage applied	0.6			V	⑤
CE "Low" Voltage	VCEL	Disappearance of CLK Oscillation, VOUT=0V, CE : Voltage applied			0.2	V	⑤
EXT "High" ON Resistance	REXTH	EXT=VIN−0.4V, CE=VIN VOUT=Set voltage×0.95V		31	58	Ω	④
EXT "Low" ON Resistance	REXTL	EXT=0.4V, CE=VIN VOUT=Set voltage×1.05V		27	45	Ω	④
Efficiency *1	EFFI			88		%	①
Soft-Start Time	TSS	Connect CSS and RSS, CE : 0V→2.5V	5	10	20	ms	①
CC/GAIN Pin Output Impedance	RCCGAIN			400		kΩ	⑦

VIN = 2.5V unless specified
External Components : RFB1=200kΩ, RFB2=100kΩ, CFB=82pF
*1 : EFFI = {[(Output Voltage) × (Output Current)] ÷ [(Input Voltage) × (Input Current)]} × 100
*2 : The capacity range of the capacitor used to set the external CLK frequency is 150 ~ 220pF

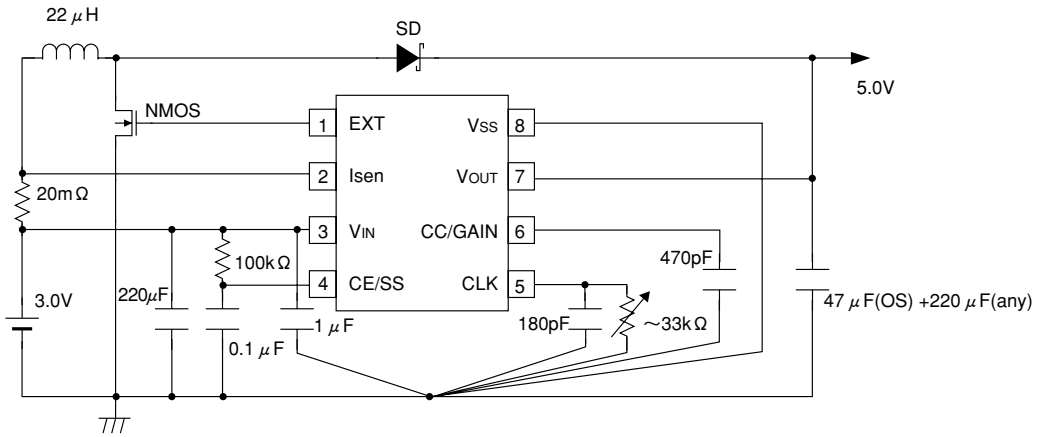
■Typical Application Circuits

XC9101C33AKR



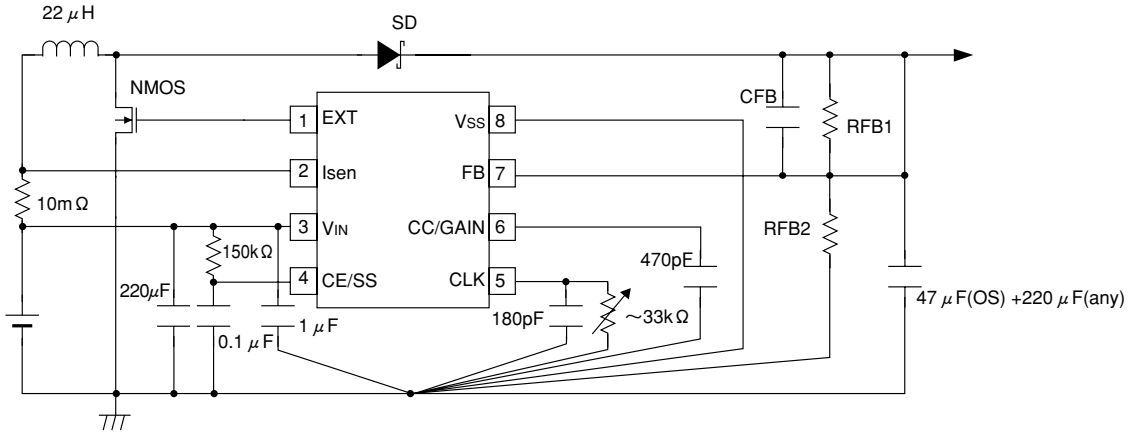
NMOS : XP161A1355PR
Coil : 22μH(CR105 SUMIDA)
Resistor : 20mΩ for Isen (NPR1 KOA), 33kΩ(trimmer) for CLK, 100kΩ for SS
Capacitors : 180pF(ceramic) for CLK, 470pF(ceramic) for CC/GAIN, 0.1μF(ceramic) for SS,1μF(ceramic) for Bypass
47μF(OS)+220μF(any) for CL, 220μF(any) for C_{IN}
SD : U3FWJ44N (TOSHIBA)

XC9101C50AKR



NMOS : XP161A1355PR
Coil : 22μH(CR105 SUMIDA)
Resistor : 20mΩ for Isen (NPR1 KOA), 33kΩ(trimmer) for CLK, 100kΩ for SS
Capacitors : 180pF(ceramic) for CLK, 470pF(ceramic) for CC/GAIN, 0.1μF(ceramic) for SS,1μF(ceramic) for Bypass
47μF(OS)+220μF(any) for CL, 220μF(any) for C_{IN}
SD : U3FWJ44N (TOSHIBA)

XC9101D09AKR



NMOS : XP161A11A1PR
Coil : 22μH(CDRH127 SUMIDA)
Resistor : 10mΩ for Isen (NPR1 KOA), 33kΩ(trimmer) for CLK, 150kΩ for SS
Capacitors : 180pF(ceramic) for CLK, 470pF(ceramic) for CC/GAIN, 0.1μF(ceramic) for SS,1μF(ceramic) for Bypass
47μF(OS)+220μF(any) for CL, 220μF(any) for C_{IN}
SD : U5FWJ44N (TOSHIBA)
V_{OUT} : 16V
RFB1 : 560kΩ
RFB2 : 33kΩ
CFB : 27pF

V_{OUT} : 20V
RFB1 : 470kΩ
RFB2 : 22kΩ
CFB : 33pF

■Operational Explanation

Step-up DC/DC converter controllers of the XC9101 series carry out pulse width modulation (PWM) according to the multiple feedback signals of the output voltage and coil current.
The internal circuits consist of different blocks that operate at V_{IN} or the stabilized power (2.0 V) of the internal regulator. The output setting voltage of the type C controller and the FB pin voltage (Vref = 0.9 V) of type D controller have been adjusted and set by laser-trimming.

<Clock>

With regard to clock pulses, a capacitor and resistor connected to the CLK pin generate ramp waveforms whose top and bottom are 0.7V and 0.15V, respectively. The frequency can be set within a range of 100 to 600 kHz externally (refer to the "Functional Settings" section for further information). The clock pulses are processed to generate a signal used for synchronizing internal sequence circuits.

<Verr amplifier>

The Verr amplifier is designed to monitor the output voltage. A fraction of the voltage applied to internal resistors R1, R2 in the case of a type C controller, and the voltage at the FB pin in the case of a type D controller, are fed back and compared with the reference voltage. In response to feedback of a voltage lower than the reference voltage, the output voltage of the Verr amplifier increases.
The output of the Verr amplifier enters the mixer via resistor (RVerr). This signal works as a pulse width control signal during PWM operations. By connecting an external capacitor and resistor through the CE/GAIN pin, it is possible to set the gain and frequency characteristics of Verr amplifier signals (refer to the "Functional Settings" section for further information).

<Ierr amplifier>

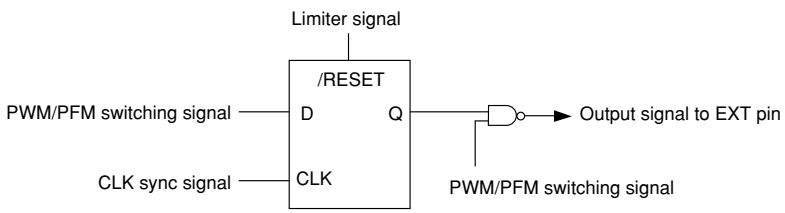
The Ierr amplifier monitors the coil current. The potential difference between the V_{IN} and Isen pins is sampled at each switching operation. Then the potential difference is amplified or held, as necessary, and input to the mixer. The Ierr amplifier outputs a signal ensuring that the greater the potential difference between the V_{IN} and Isen pins, the smaller the switching current. The gain and frequency characteristics of this amplifier are fixed internally.

<Mixer and PWM>

The mixer modulates the signal sent from Verr by the signal from Ierr. The modulated signal enters the PWM comparator for comparison with the sawtooth pulses generated at the CLK pin. If the signal is greater than the sawtooth waveforms, a signal is sent to the output circuit to turn on the external switch.

<Current Limiter>

The current flowing through the coil is monitored by the limiter comparator via the V_{IN} and Isen pins. The limiter comparator outputs a signal when the potential difference between the V_{IN} and Isen pins reaches about 150 mV or more. This signal is converted to a logic signal and handled as a DFF reset signal for the internal limiter circuit. When a reset signal is input, a signal is output immediately at the EXT pin to turn off the MOS switch. When the limiter comparator sends a signal to enable data acceptance, a signal to turn on the MOS switch is output at the next clock pulse. If at this time the potential difference between the V_{IN} and Isen pins is large, operation is repeated to turn off the MOS switch again. DFF operates in synchronization with the clock signal of the CLK pin.



<Soft Start>

The soft start function is made available by attaching a capacitor and resistor to the CE/SS pin. The Vref voltage applied to the Verr amplifier is restricted by the start-up voltage of the CE/SS pin. This ensures that the Verr amplifier operates with its two inputs in balance, thereby preventing the ON-TIME signal from becoming stronger than necessary. Consequently, soft start time needs to be set sufficiently longer than the time set to CLK. The start-up time of the CE/SS pin equals the time set for soft start (refer to the "Functional Settings" section for further information).
The soft start function operates when the voltage at the CE/SS pin is between 0V to 1.55V. If the voltage at the CE/SS pin doesn't start from 0V but from a mid level voltage when the power is switched on, the soft start function will become ineffective and the possibilities of large rush currents and ripple voltages occuring will be increased.

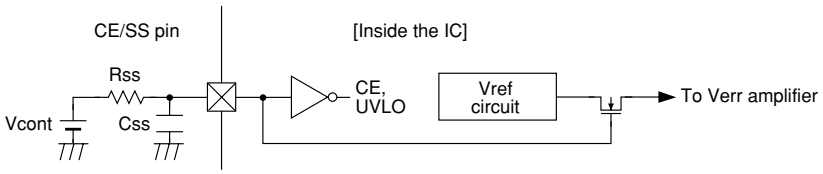
●Functional Settings

1. Soft Start

CE and soft start (SS) functions are commonly assigned to the CE/SS pin. The soft start function is effective until the voltage at the CE pin reaches approximately 1.55 V rising from 0 V. Soft start time is approximated by the equation below according to values of Vcont, Rss, and Css.

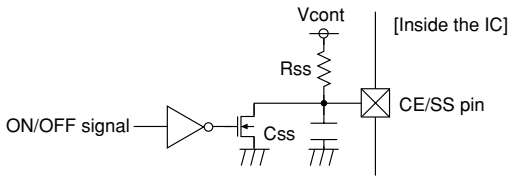
T = -Css × Rss × ln((Vcont - 1.55)/Vcont)

Example: When C_{SS} = 0.1 μF, R_{SS} = 470 kΩ, and Vcont = 5 V, T = -0.1 e^{-6} × 470 e^{3} × ln ((5 - 1.55)/5) = 17.44 ms.

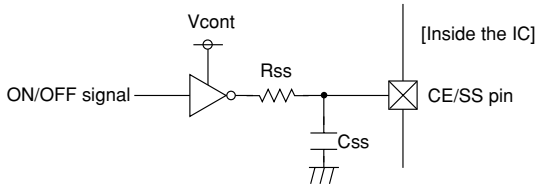


Set the soft start time to a value sufficiently longer than the period of a clock pulse.

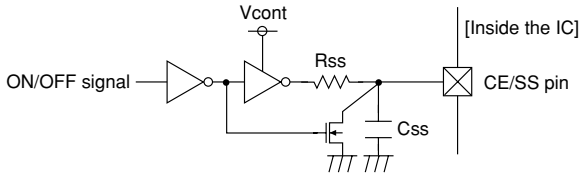
> Circuit example 1: N-ch open drain



> Circuit example 2: CMOS logic (low current dissipation)



> Circuit example 3: CMOS logic (low current dissipation), quick off

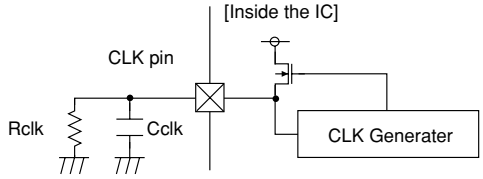


2. Oscillation Frequency

The oscillation frequency of the internal clock generator is approximated by the following equation according to the values of the capacitor and resistor attached to the CLK pin. To stablize the IC's operation, set the oscillation frequency within a range of 100kHz to 600kHz. Select a value for Cclk within a range of 150pF to 220pF and fix the frequency based on the value for Rclk.

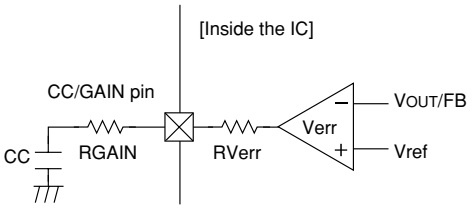
f = 1/(-Cclk × Rclk × ln0.26)

Example: When Cclk = 220 pF and Rclk = 10 kΩ, f = 1/(-220e^{-12} × 10e^{3} × ln(0.26)) = 337.43 kHz.



3. Gain and Frequency Characteristics of the Verr Amplifier

The gain at output and frequency characteristics of the Verr amplifier are adjusted by the values of the capacitor and resistor attached to the CC/GAIN pin. It is generally recommended to attach a CC of 220 to 1,000 pF without RGAIN. The greater the CC value, the more stable the phase and the slower the transient response. When using the IC with RGAIN connected, it should be noted that if the RGAIN resistance value is too high, abnormal oscillation may occur during transient response time. The size of RGAIN should be carefully evaluated before connection.

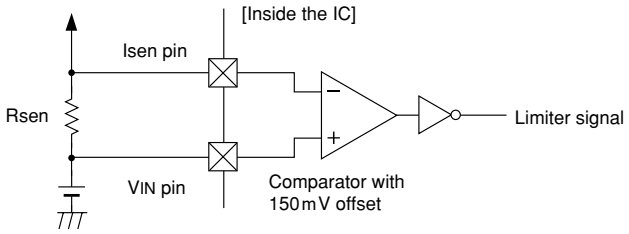


4. Current Limit

The current limit value is approximated by the following equation according to resistor RSEN inserted between the VIN and Isen pins. Double function, current FB input and current limiting, is assigned to the Isen pin. The current limiting value is approximated by the following equation according to the value for RSEN.

Ilpeak_limit = 0.15/Rsen

Example: When RSEN = 100 mΩ, Ilpeak_limit = 0.15/0.1 = 1.5 A



The inside error ampliphier sends feedback signal when the voltage occurs at RSEN resisitors because of the flow of coil current in order to phase compensate. The more the RSEN value becomes larger, the more the error signal becomes bigger, and it could lead to an intermittent oscillation. Please be careful if there is a problem with the application. When the regular operation, the voltage which occurs between RSEN resistors because of coil peak should be set lower than the current limit voltage of 90mV (min.). For more details, please refer the notes on the external components.

5. FB Voltage and Cfb

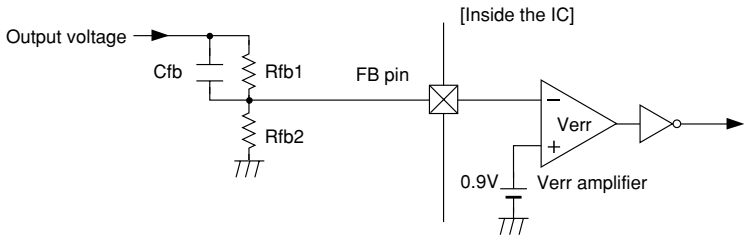
With regard to the XC9101D series, the output voltage is set by attaching externally divided resistors. The output voltage is determined by the equation shown below according to the values of Rfb1 and Rfb2. In general, the sum of Rfb1 and Rfb2 should be 1 MEG Ω or less.

V_{OUT} = 0.9 × (Rfb1 + Rfb2)/Rfb2

The value of Cfb (phase compensation capacitor) is approximated by the following equation according to the values of Rfb1 and fzfb. The value of fzfb should be 10 kHz, as a general rule.

Cfb = 1/(2 × π × Rfb1 × fzfb)

Example: When Rfb1 = 455 kΩ and Rfb2 = 100 kΩ : V_{OUT} = 0.9 × (455 k + 100 k)/100 k = 4.995 V
: Cfb = 1/(2 × π × 455 k × 10 k) = 34.98 pF



■Directions for use

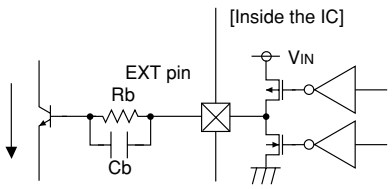
●Application Notes

1. The XC9101 series are designed for use with an output ceramic capacitor. If, however, the potential difference between input and output is too large, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output side. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.

2. The EXT pin of the XC9101 series is designed to minimize the through current that occurs in the internal circuitry. However, the gate drive of external PMOS has a low impedance for the sake of speed. Therefore, if the input voltage is high and the bypass capacitor is attached away from the IC, the charge/discharge current to the external PMOS may lead to unstable operations due to switching operation of the EXT pin.

   As a solution to this problem, place the bypass capacitor as close to the IC as possible, so that voltage variations at the V_{IN} and V_{SS} pins caused by switching are minimized. If this is not effective, insert a resistor of several to several tens of ohms between the EXT pin and PMOS gate. Remember that the insertion of a resistor slows down the switching speed and may result in reduced efficiency.

3. A PNP transistor can be used in place of PMOS. If using a PNP transistor, insert a resistor (Rb) and capacitor (Cb) between the EXT pin and the base of the PNP transistor in order to limit the base current without slowing the switching speed. Adjust Rb in a range of 500 Ω to 1 kΩ according to the load and hFE of the transistor. Use a ceramic capacitor for Cb, complying with Cb ≤ 1/(2 × π × Rb × Fosc × 0.7), as a rule.



4. Although the C_CLK connection capacitance range is from 150 ~ 220pF, the most suitable value for maximum stability is around 180pF.

●Recommended Pattern Layout

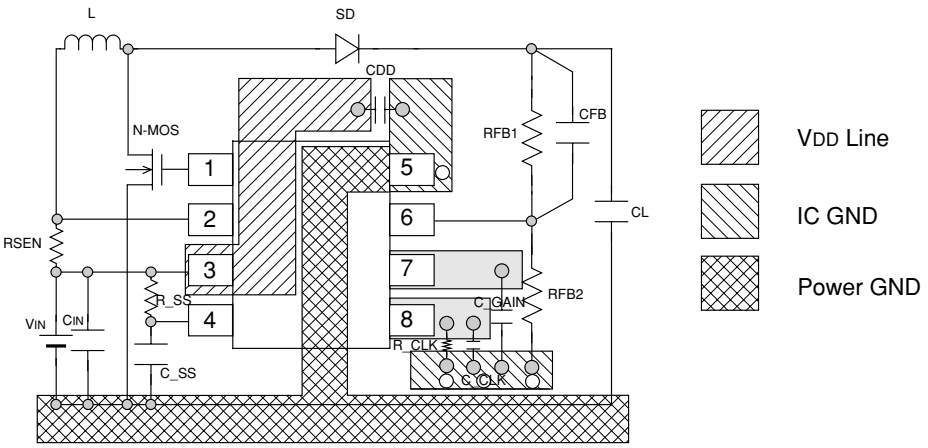
① In order to stablize V_{DD}'s voltage level, we recommend that a by-pass capacitor (C_{DD}) be connected as close as possible to the V_{IN} & V_{SS} pins.

② In order to stablize the GND voltage level which can fluctuate as a result of switching, we suggest that C_CLK's, R_CLK's & C_GAIN's GND be separated from Power GND and connected as close as possible to the V_{SS} pin (by-pass capacitor, C_{DD}). Please use a multi layer board and check the wiring carefully.

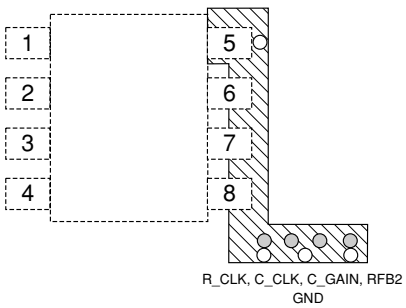
Pattern Layout Examples

XC9101D Series

2 Layer Evaluation Board

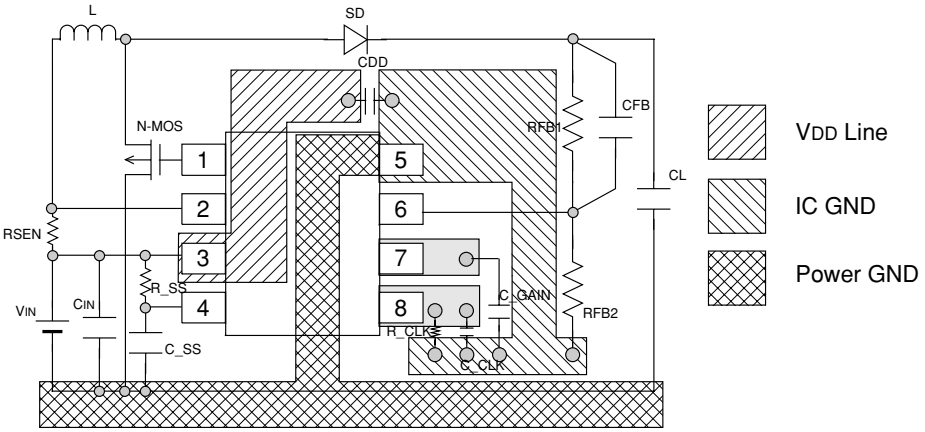


○ Through Hole



○ Through Hole

1 Layer Evaluation Board



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●Notes

Ensure that the absolute maximum ratings of the external components and the XC9101 DC/DC IC itself are not exceeded.

We recommend that sufficient counter measures are put in place to eliminate the heat that may be generated by the external N-MOSFET as a result of switching losses.

Try to use a N-MOSFET with as small a gate capacitance as possible in order to avoid overly large output spike voltages that may occur (such spikes occur in proportion to gate capacitance).

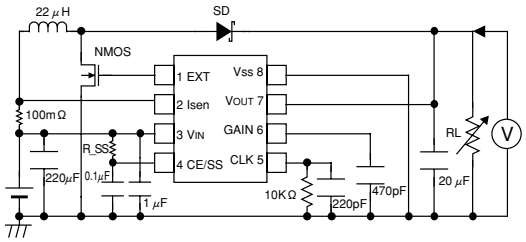
The performance of the XC9101 DC/DC converter is greatly influenced by not only its own characteristics, but also by those of the external components it is used with. We recommend that you refer to the specifications of each component to be used and take sufficient care when selecting components.

Wire external components as close to the IC as possible and use thick, short connecting wires to reduce wiring impedance. In particular, minimize the distance between the by-pass capacitor and the IC.

Make sure that the GND wiring is as strong as possible as variations in ground potential caused by ground current at the time of switching may result in unstable operation of the IC. Specifically, strengthen the ground wiring in the proximity of the V_{SS} pin.

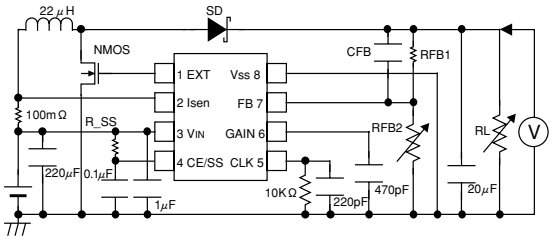
■Test Circuits

・Fig. ① (VOUT Type)



XC9101C33A R_SS：104kΩ C-SS：0.1μF
XC9101C50A R_SS：138kΩ C-SS：0.1μF

・Fig. ① (FB Type)



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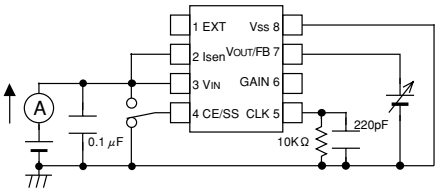
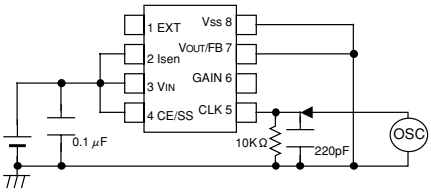
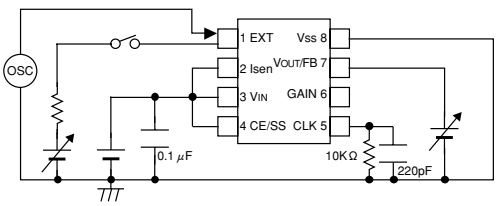
・Fig. ②



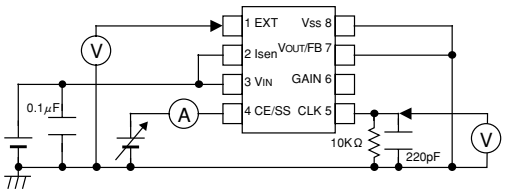
・Fig. ③



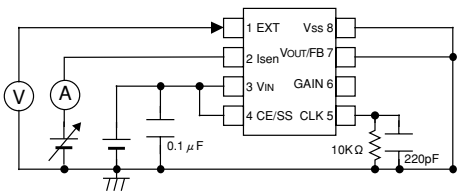
・Fig. ④



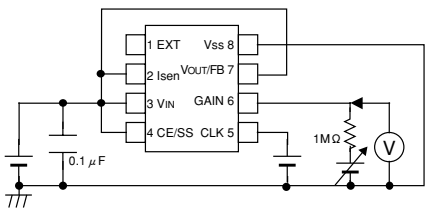
・Fig. ⑤



・Fig. ⑥



・Fig. ⑦



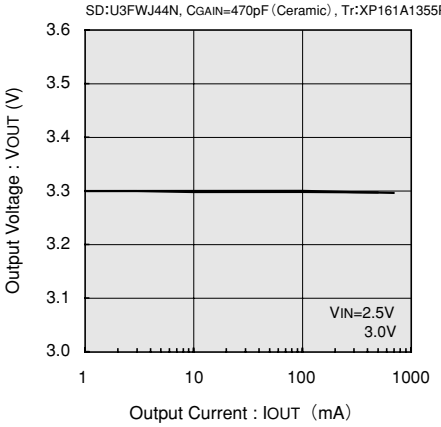
■Typical Performance Characteristics

XC9101D09AKR

(1) OUTPUT VOLTAGE vs. OUTPUT CURRENT

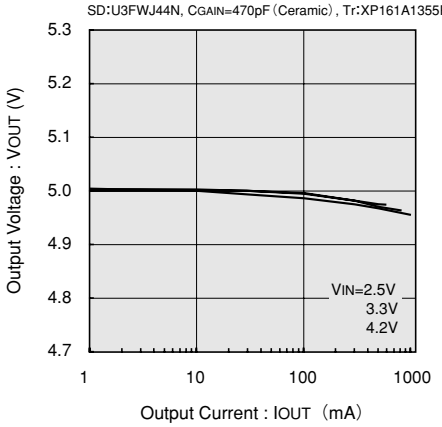
VOUT = 3.3V, FOSC : 180kHz

L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1355PR



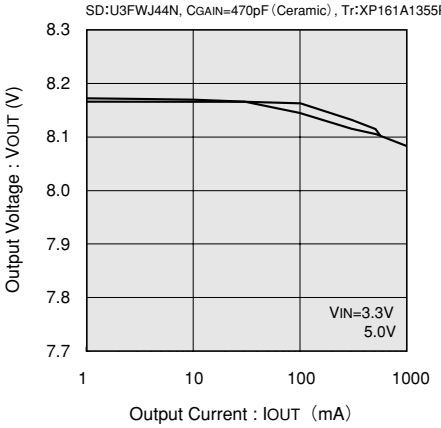
VOUT = 5.0V, FOSC : 180kHz

L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1355PR



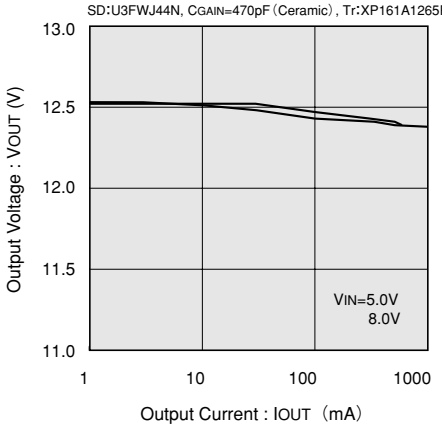
VOUT = 8.0V, FOSC : 330kHz

L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1355PR



VOUT = 12.0V, FOSC : 330kHz

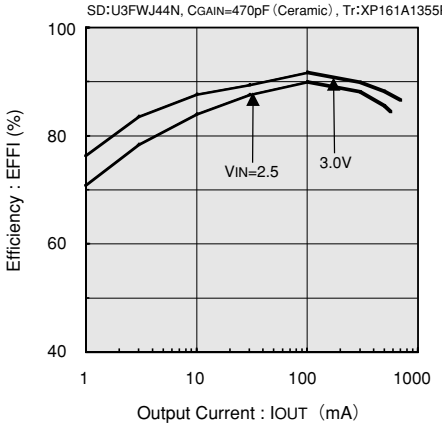
L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1265PR



(2) EFFICIENCY vs. OUTPUT CURRENT

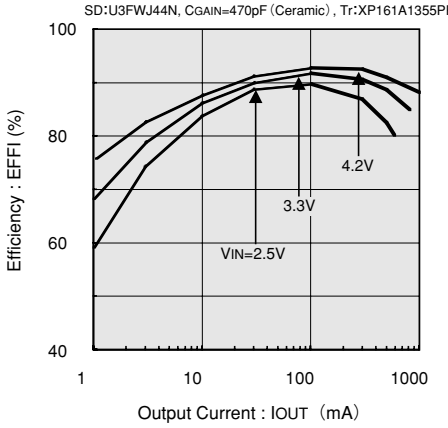
VOUT = 3.3V, FOSC : 180kHz

L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1355PR



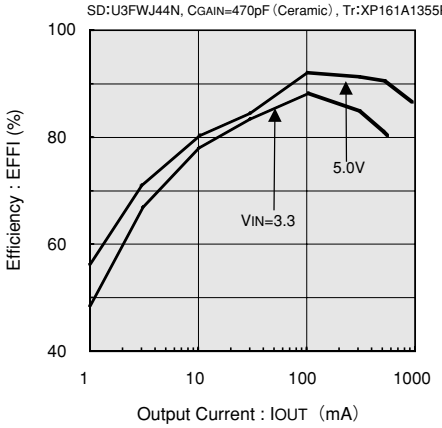
VOUT = 5.0V, FOSC : 180kHz

L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1355PR



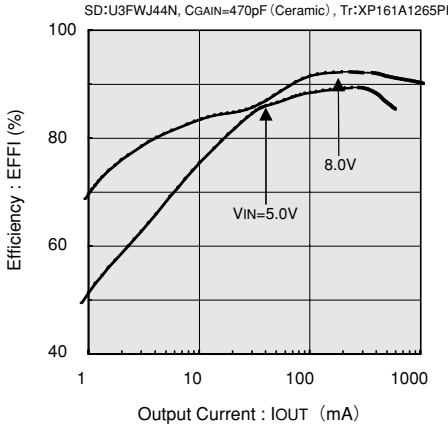
VOUT = 8.0V, FOSC : 180kHz

L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1355PR



VOUT = 12.0V, FOSC : 180kHz

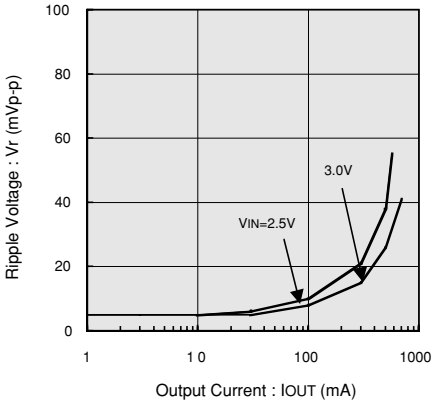
L=22μH, CIN=220μF (Electrolytic) +10μF (Ceramic)
CL=40μF (Ceramic), RSEN=50mΩ, CDD=1μF (Ceramic)
SD:U3FWJ44N, CGAIN=470pF (Ceramic), Tr:XP161A1265PR



(3) RIPPLE VOLTAGE vs. OUTPUT CURRENT

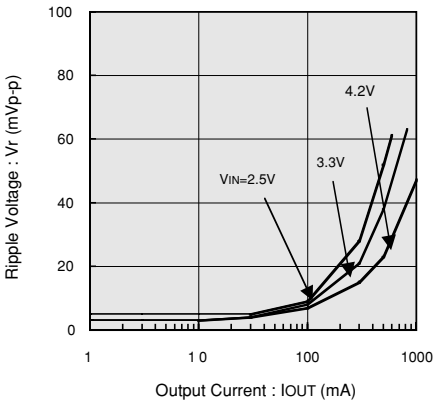
VOUT = 3.3V, FOSC : 180kHz

L=22μH,CIN=220μF(Electrolytic)+10μF(Ceramic)
CL=40μF(Ceramic),RSEN=50mΩ,CDD=1μF(Ceramic)
SD:U3FWJ44N,CGAIN=470pF(Ceramic),Tr:XP161A1355PR



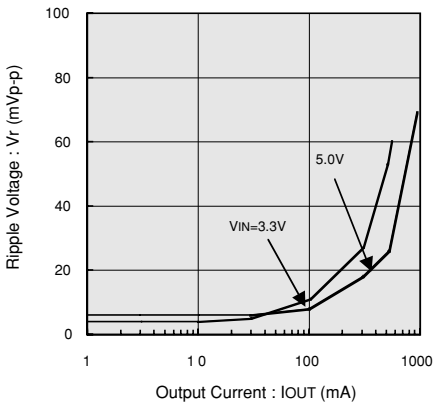
VOUT = 5.0V, FOSC : 180kHz

L=22μH,CIN=220μF(Electrolytic)+10μF(Ceramic)
CL=40μF(Ceramic),RSEN=50mΩ,CDD=1μF(Ceramic)
SD:U3FWJ44N,CGAIN=470pF(Ceramic),Tr:XP161A1355PR



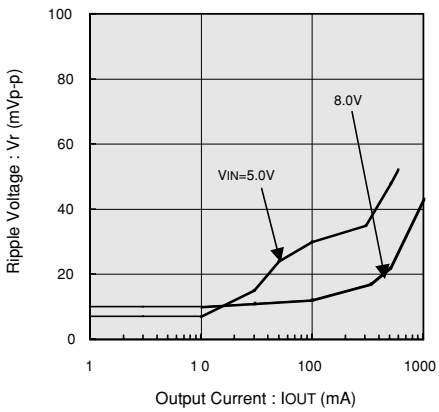
VOUT = 8.0V, FOSC : 330kHz

L=22μH,CIN=220μF(Electrolytic)+10μF(Ceramic)
CL=40μF(Ceramic),RSEN=50mΩ,CDD=1μF(Ceramic)
SD:U3FWJ44N,CGAIN=470pF(Ceramic),Tr:XP161A1355PR



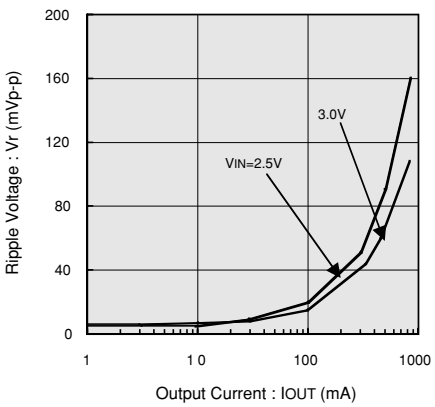
VOUT = 12.0V, FOSC : 330kHz

L=22μH,CIN=220μF(Electrolytic)+10μF(Ceramic)
CL=40μF(Ceramic),RSEN=50mΩ,CDD=1μF(Ceramic)
SD:U3FWJ44N,CGAIN=470pF(Ceramic),Tr:XP161A1265PR



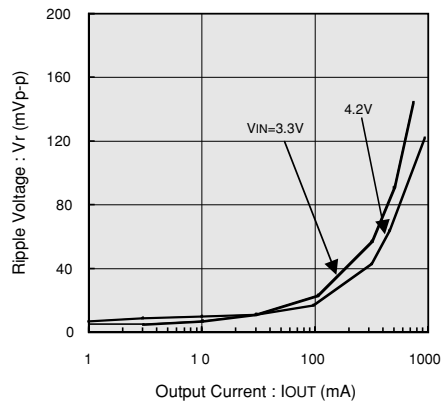
VOUT = 3.3V, FOSC : 180kHz

L=22μH,CL=94μF(Tantalum),CIN=94μF(Tantalum)
RSEN=50mΩ,CDD=1μF(Ceramic)
SD:U3FWJ44N,CGAIN=470pF(Ceramic),Tr:XP161A1355PR



VOUT = 5.0V, FOSC : 180kHz

L=22μH,CL=94μF(Tantalum),CIN=94μF(Tantalum)
RSEN=50mΩ,CDD=1μF(Ceramic)
SD:U3FWJ44N,CGAIN=470pF(Ceramic),Tr:XP161A1355PR



Note : If the difference between the input and output voltage is large or small, switching ON / OFF time will be shortened. As such, the external components used and their values (inductance value of the coil, resistor connected to CLK, capacitor etc.) may have a critical influence on the actual operation of the IC.