Supervisory Circuits with Watchdog and Manual Reset in 5-Lead SOT-23

Data Sheet **ADM6316/ADM6317/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322**

FEATURES

- 26 reset threshold options
  - 2.5 V to 5 V in 100 mV increments
- 4 reset timeout options
  - 1 ms, 20 ms, 140 ms, and 1120 ms (minimum)
- 4 watchdog timeout options
  - 6.3 ms, 102 ms, 1600 ms, and 25.6 sec (typical)
- Manual reset input
- Reset output stages
  - Push-pull active low
  - Open-drain active low
  - Push-pull active high
- Low power consumption: 5 µA
- Guaranteed reset output valid to V_{CC} = 1 V
- Power supply glitch immunity
- Specified over industrial temperature range
- 5-lead SOT-23 package

APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

FUNCTIONAL BLOCK DIAGRAMS

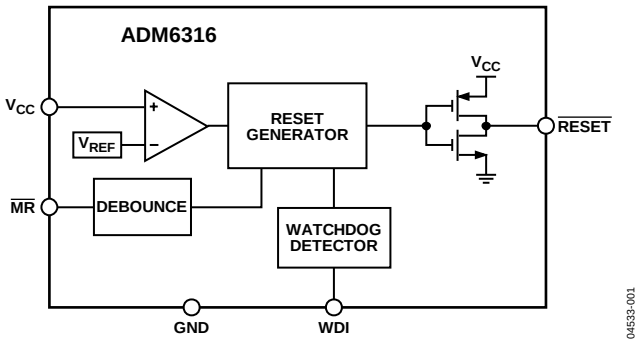

Figure 1.

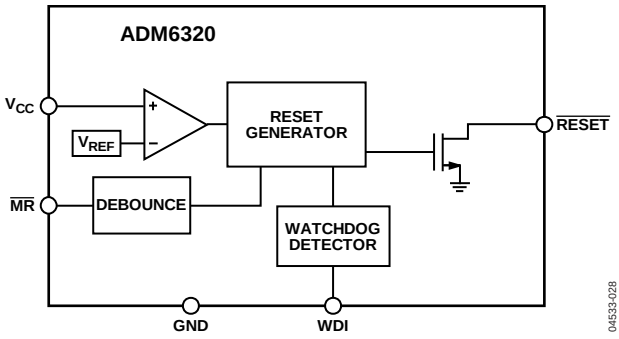

Figure 2.

GENERAL DESCRIPTION

The ADM6316/ADM6317/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 are supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. As well as providing power-on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period. A reset signal can also be asserted by an external push button through a manual reset input. The seven parts feature different combinations of watchdog input, manual reset input, and output stage configuration, as shown in Table 1.

Each part is available in a choice of 26 reset threshold options ranging from 2.5 V to 5 V in 100 mV increments. There are also four reset timeout options of 1 ms, 20 ms, 140 ms, and 1120 ms (minimum) and four watchdog timeout options of 6.3 ms, 102 ms, 1600 ms, and 25.6 sec (typical).

The ADM6316/ADM6317/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 are available in 5-lead SOT-23 packages and typically consume only 3 µA, making them suitable for use in low power portable applications.

Table 1. Selection Table

Part No.	Watchdog	Manual Reset	Output Stage	
			$\overline{\text{RESET}}$	RESET
ADM6316	Yes	Yes	Push-pull	No
ADM6317	Yes	Yes	No	Push-pull
ADM6318	Yes	No	Push-pull	Push-pull
ADM6319	No	Yes	Push-pull	Push-pull
ADM6320	Yes	Yes	Open-drain	No
ADM6321	Yes	No	Open-drain	Push-pull
ADM6322	No	Yes	Open-drain	Push-pull

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/13—Rev. E to Rev. F

Changes to Table 8 ... 12
Changes to Ordering Guide ... 13

10/10—Rev. D to Rev. E

Changes to Table 8 ... 12
Updated Outline Dimensions ... 13

8/08—Rev. C to Rev. D

Change to Figure 18 ... 9

4/07—Rev. B to Rev. C

Added Figure 2 ... 1
Changes to Figure 23 ... 13
Changes to Ordering Guide ... 13

1/07—Rev. A to Rev. B

Changes to Functional Block Diagram ... 1
Changes to Figure 18 ... 10

5/06—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Functional Block Diagram ... 1
Changes to Table 8 ... 12
Changes to Figure 22 ... 13
Changes to Ordering Guide ... 13

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	
Supply Current		10	20	µA	V_{CC} = 5.5 V
		5	12	µA	V_{CC} = 3.6 V
RESET THRESHOLD VOLTAGE	V_{TH} – 1.5%	V_{TH}	V_{TH} + 1.5%	V	T_A = 25°C
	V_{TH} – 2.5%	V_{TH}	V_{TH} + 2.5%	V	T_A = −40°C to +85°C
RESET THRESHOLD TEMPERATURE COEFFICIENT		40		ppm/°C	
RESET THRESHOLD HYSTERESIS		3		mV	
RESET TIMEOUT PERIOD					
ADM63xxA	1	1.4	2	ms	
ADM63xxB	20	28	40	ms	
ADM63xxC	140	200	280	ms	
ADM63xxD	1120	1600	2240	ms	
V_{CC} TO RESET DELAY		40		µs	V_{CC} falling at 1 mV/µs
PUSH-PULL OUTPUT (ADM6316, ADM6317, ADM6318, ADM6319, ADM6321, ADM6322)					
$\overline{\text{RESET}}$ Output Voltage			0.3	V	$V_{CC} \geq 1.0$ V, I_{SINK} = 50 µA
			0.3	V	$V_{CC} \geq 1.2$ V, I_{SINK} = 100 µA
			0.3	V	$V_{CC} \geq 2.7$ V, I_{SINK} = 1.2 mA
			0.4	V	$V_{CC} \geq 4.5$ V, I_{SINK} = 3.2 mA
	0.8 × V_{CC}			V	$V_{CC} \geq 2.7$ V, I_{SOURCE} = 500 µA
	V_{CC} – 1.5			V	$V_{CC} \geq 4.5$ V, I_{SOURCE} = 800 µA
$\overline{\text{RESET}}$ Rise Time		5	25	ns	From 10% to 90% V_{CC}, C_L = 5 pF, V_{CC} = 3.3 V
RESET Output Voltage			0.3	V	$V_{CC} \geq 2.7$ V, I_{SINK} = 1.2 mA
			0.4	V	$V_{CC} \geq 4.5$ V, I_{SINK} = 3.2 mA
	0.8 × V_{CC}			V	$V_{CC} \geq 1.8$ V, I_{SOURCE} = 150 µA
	0.8 × V_{CC}			V	$V_{CC} \geq 2.7$ V, I_{SOURCE} = 500 µA
	V_{CC} – 1.5			V	$V_{CC} \geq 4.5$ V, I_{SOURCE} = 800 µA
OPEN-DRAIN OUTPUT (ADM6320, ADM6321, ADM6322)					
$\overline{\text{RESET}}$ Output Voltage			0.3	V	$V_{CC} \geq 1.0$ V, I_{SINK} = 50 µA
			0.3	V	$V_{CC} \geq 1.2$ V, I_{SINK} = 100 µA
			0.3	V	$V_{CC} \geq 2.7$ V, I_{SINK} = 1.2 mA
			0.4	V	$V_{CC} \geq 4.5$ V, I_{SINK} = 3.2 mA
Open-Drain Reset Output Leakage Current			1	µA	
WATCHDOG INPUT (ADM6316, ADM6317, ADM6318, ADM6320, ADM6321)					
Watchdog Timeout Period					
ADM63xxxW	4.3	6.3	9.3	ms	
ADM63xxxX	71	102	153	ms	
ADM63xxxY	1.12	1.6	2.4	sec	
ADM63xxxZ	17.9	25.6	38.4	sec	
WDI Pulse Width	50			ns	$V_{IL} = 0.3 \times V_{CC}$, $V_{IH} = 0.7 \times V_{CC}$
WDI Input Threshold	0.3 × V_{CC}		0.7 × V_{CC}	V	
WDI Input Current		120	160	µA	$V_{WDI} = V_{CC}$, time average
	−20	−15		µA	V_{WDI} = 0, time average

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MANUAL RESET INPUT (ADM6316, ADM6317, ADM6319, ADM6320, ADM6322)					
$\overline{MR}$ Input Threshold	0.8		2.0	V	$V_{TH} > 4.0$ V
	$0.3 \times V_{CC}$		$0.7 \times V_{CC}$	V	$V_{TH} < 4.0$ V
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		100		ns	
$\overline{MR}$ Pull-Up Resistance	35	52	75	kΩ	
$\overline{MR}$ to Reset Delay		230		ns	$V_{CC} = 5$ V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
$\overline{RESET}$ (ADM6320, ADM6321, ADM6322)	−0.3 V to +6 V
All Other Pins	−0.3 V to (V_{CC} + 0.3 V)
Output Current (RESET, $\overline{RESET}$)	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
θ_{JA} Thermal Impedance, SOT-23	270°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

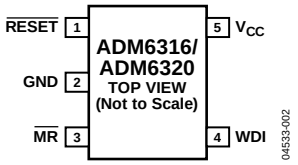

Figure 3. ADM6316/ADM6320 Pin Configuration

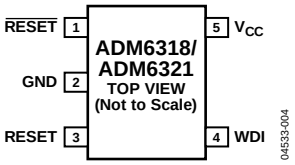

Figure 5. ADM6318/ADM6321 Pin Configuration

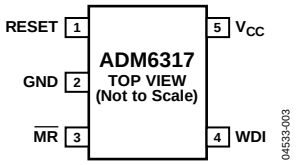

Figure 4. ADM6317 Pin Configuration

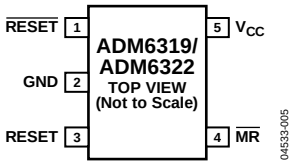

Figure 6. ADM6319/ADM6322 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$ (ADM6316/ADM6318/ADM6319/ ADM6320/ADM6321/ADM6322)	Active-Low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}. Push-Pull Output Stage for the ADM6316/ADM6318/ADM6319. Open-Drain Output Stage for the ADM6320/ADM6321/ADM6322.
	RESET (ADM6317)	Active-High Push-Pull Reset Output.
2	GND (all models)	Ground.
3	$\overline{\text{MR}}$ (ADM6316/ADM6317/ADM6320)	Manual Reset Input. This is an active-low input that when forced low for at least 1 µs, generates a reset. It features a 52 kΩ internal pull-up.
	RESET (ADM6318/ADM6319/ADM6321/ADM6322)	Active-High Push-Pull Reset Output.
4	WDI (ADM6316/ADM6317/ADM6318/ ADM6320/ADM6321)	Watchdog Input. Generates a reset if the logic level on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated. Leave this pin floating to disable the watchdog timer.
	$\overline{\text{MR}}$ (ADM6319/ADM6322)	Manual Reset Input.
5	V_{CC} (all models)	Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

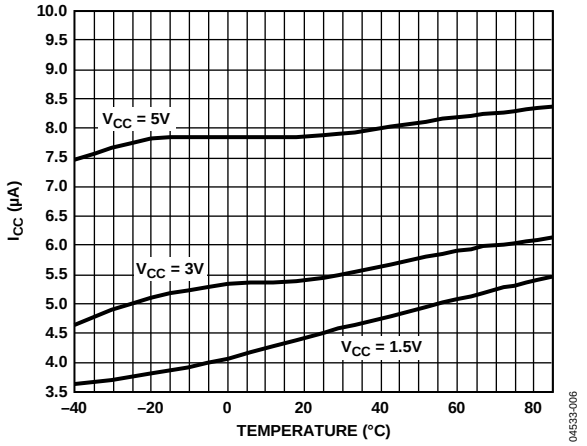

Figure 7. Supply Current vs. Temperature (ADM6316/ADM6317/ADM6318/ADM6320/ADM6321)

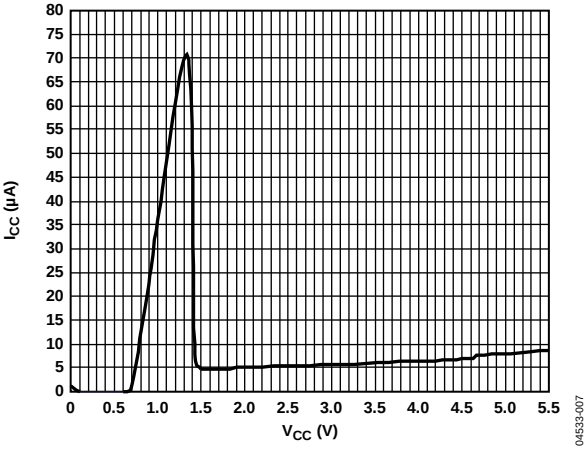

Figure 8. Supply Current vs. Supply Voltage

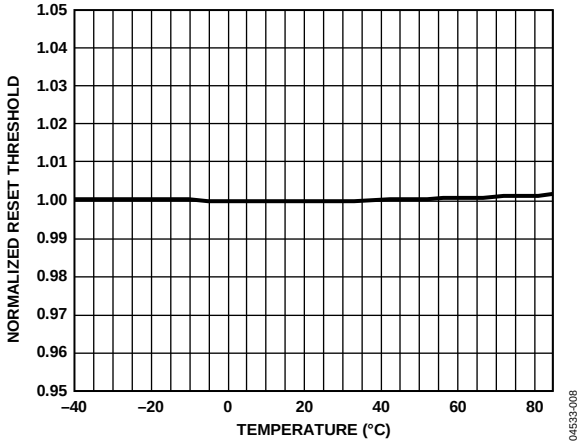

Figure 9. Normalized Reset Threshold vs. Temperature

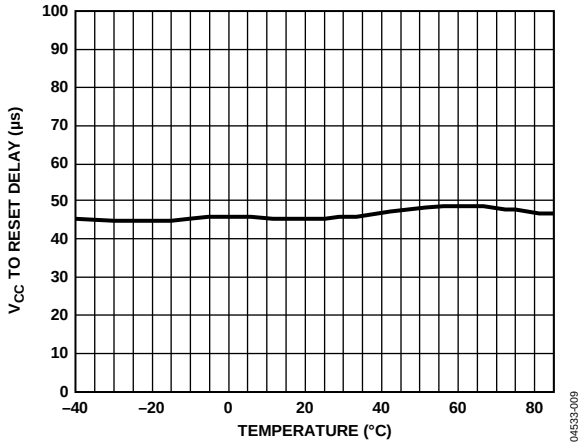

Figure 10. V_{CC} Falling to Reset Propagation Delay vs. Temperature

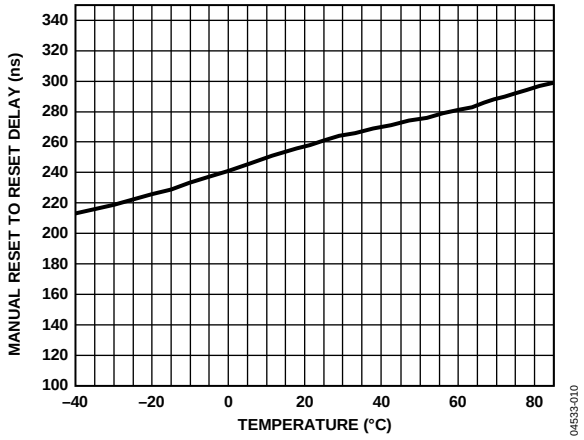

Figure 11. Manual Reset to Reset Propagation Delay vs. Temperature (ADM6316/ADM6317/ADM6319/ADM6320/ADM6322)

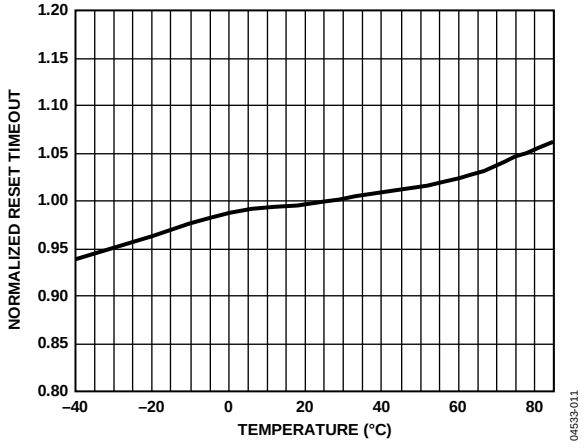

Figure 12. Normalized Reset Timeout Period vs. Temperature

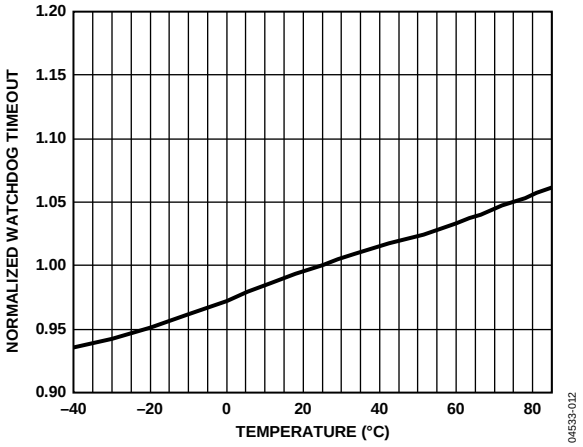

Figure 13. Normalized Watchdog Timeout Period vs. Temperature (ADM6316/ADM6317/ADM6318/ADM6320/ADM6321)

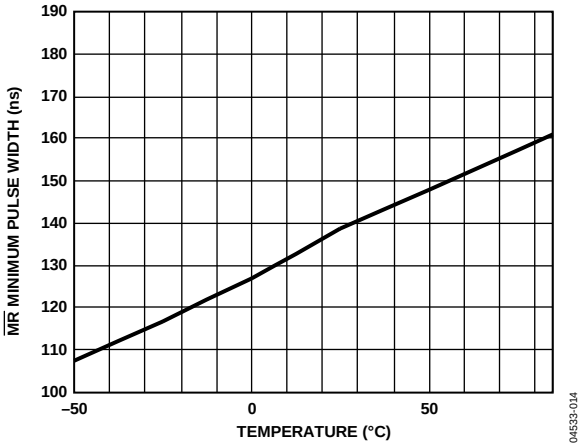

Figure 15. Manual Reset Minimum Pulse Width vs. Temperature (ADM6316/ADM6317/ADM6319/ADM6320/ADM6322)

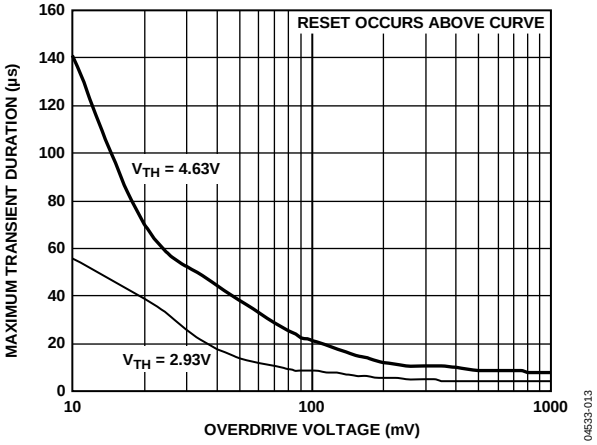

Figure 14. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

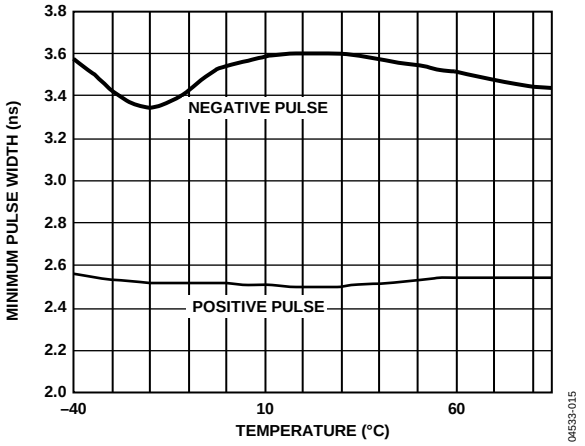

Figure 16. Watchdog Input Minimum Pulse Width vs. Temperature (ADM6316/ADM6317/ADM6318/ADM6320/ADM6321)

CIRCUIT DESCRIPTION

The ADM6316/ADM6317/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 provide microprocessor supply voltage supervision by controlling the microprocessor's reset input. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer (ADM6316/ADM6317/ADM6318/ADM6320/ADM6321). If the user detects a problem with the system's operation, a manual reset input is available (ADM6316/ADM6317/ADM6319/ADM6320/ADM6322) to reset the microprocessor, for example, by means of an external push button.

RESET OUTPUT

The ADM6316 features an active-low push-pull reset output, while the ADM6317/ADM6321/ADM6322 have active-high push-pull reset outputs. The ADM6318/ADM6319 feature dual active-low and active-high push-pull reset outputs. For active-low and active-high outputs, the reset signal is guaranteed to be logic low and logic high, respectively, for V_{CC} down to 1 V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low to high, or after the watchdog timer times out. Figure 17 illustrates the behavior of the reset outputs.

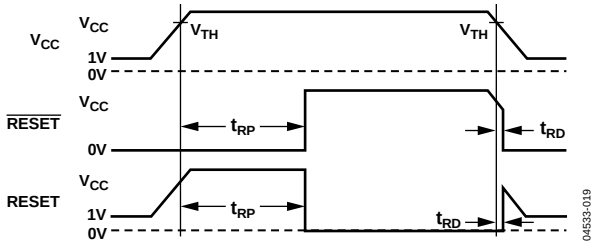

Figure 17. Reset Timing Diagram

OPEN-DRAIN $\overline{\text{RESET}}$ OUTPUT

The ADM6320/ADM6321/ADM6322 have an active-low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail no higher than 6 V. The resistor should comply with the microprocessor's logic low and logic high voltage level requirements while supplying input current and leakage paths on the $\overline{\text{RESET}}$ line. A 10 kΩ resistor is adequate in most situations.

MANUAL RESET INPUT

The ADM6316/ADM6317/ADM6319/ADM6320/ADM6322 feature a manual reset input ($\overline{MR}$), which when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 kΩ, internal pull-up so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative-going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The ADM6316/ADM6317/ADM6318/ADM6320/ADM6321 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

As well as logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{CC} or due to $\overline{MR}$ being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deassserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

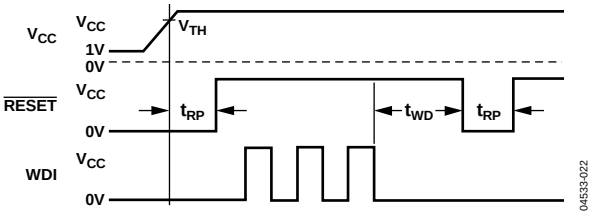

Figure 18. Watchdog Timing Diagram

APPLICATIONS INFORMATION

WATCHDOG INPUT CURRENT

To minimize watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 160 µA. Pulsing WDI low-to-high-to-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

NEGATIVE-GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM6316/ADM6317/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 14 plots V_{CC} transient duration vs. the transient magnitude. The curves show combinations of transient magnitude and duration for which a reset is not generated for 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any larger in magnitude or duration, a reset is generated. An optional 0.1 µF bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC} = 0 V

Both active-low and active-high reset outputs are guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active-low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For the active-high case, a resistor connected between RESET and V_{CC} pulls the output high when it is unable to source current. A large resistance, such as 100 kΩ, should be used so that it does not overload the reset output when V_{CC} is above 1 V.

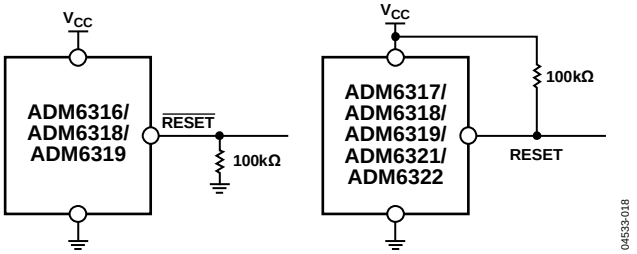

Figure 19. Ensuring Reset Valid to V_{CC} = 0 V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessor's watchdog strobe code, quickly switching WDI low to high and then high to low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-to-high-to-low WDI pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset (see Figure 20).

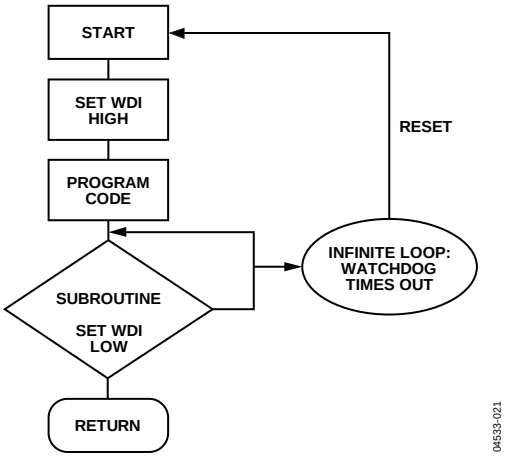

Figure 20. Watchdog Flow Diagram

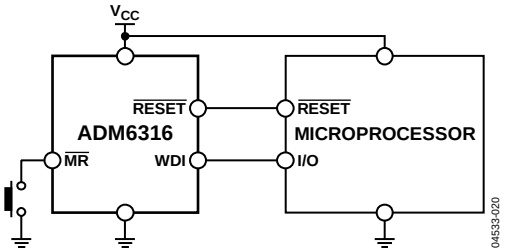

Figure 21. Typical Application Circuit

OPTIONS

Table 5. Reset Voltage Threshold Options

	T_A = +25°C			T_A = −40°C to +85°C		
Part No.	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
ADM63xxx50	4.925	5.000	5.075	4.875	5.125	V
ADM63xxx49	4.827	4.900	4.974	4.778	5.023	V
ADM63xxx48	4.728	4.800	4.872	4.680	4.920	V
ADM63xxx47	4.630	4.700	4.771	4.583	4.818	V
ADM63xxx46	4.561	4.630	4.699	4.514	4.746	V
ADM63xxx45	4.433	4.500	4.568	4.388	4.613	V
ADM63xxx44	4.314	4.390	4.446	4.270	4.490	V
ADM63xxx43	4.236	4.300	4.365	4.193	4.408	V
ADM63xxx42	4.137	4.200	4.263	4.095	4.305	V
ADM63xxx41	4.039	4.100	4.162	3.998	4.203	V
ADM63xxx40	3.940	4.00	4.060	3.900	4.100	V
ADM63xxx39	3.842	3.900	3.959	3.803	3.998	V
ADM63xxx38	3.743	3.800	3.857	3.705	3.895	V
ADM63xxx37	3.645	3.700	3.756	3.608	3.793	V
ADM63xxx36	3.546	3.600	3.654	3.510	3.690	V
ADM63xxx35	3.448	3.500	3.553	3.413	3.588	V
ADM63xxx34	3.349	3.400	3.451	3.315	3.485	V
ADM63xxx33	3.251	3.300	3.350	3.218	3.383	V
ADM63xxx32	3.152	3.200	3.248	3.120	3.280	V
ADM63xxx31	3.034	3.080	3.126	3.003	3.157	V
ADM63xxx30	2.955	3.000	3.045	2.925	3.075	V
ADM63xxx29	2.886	2.930	2.974	2.857	3.000	V
ADM63xxx28	2.758	2.800	2.842	2.730	2.870	V
ADM63xxx27	2.660	2.700	2.741	2.633	2.768	V
ADM63xxx26	2.591	2.630	2.669	2.564	2.696	V
ADM63xxx25	2.463	2.500	2.538	2.438	2.563	V

Table 6. Reset Timeout Options

Suffix	**Min**	**Typ**	**Max**	**Unit**
A	1	1.6	2	ms
B	20	30	40	ms
C	140	200	280	ms
D	1.12	1.60	2.24	sec

Table 7. Watchdog Timer Options

Suffix	**Min**	**Typ**	**Max**	**Unit**
W	4.3	6.3	9.3	ms
X	71	102	153	ms
Y	1.12	1.6	2.24	sec
Z	17.9	25.6	38.4	sec

Table 8. Standard Models

Model	Reset Threshold (V)	Minimum Reset Timeout (ms)	Typical Watchdog Timeout (sec)
ADM6316CW25-ARJZ-R7	2.5	140	0.0063
ADM6316DZ26-ARJ-RL7	2.63	1120	25.6
ADM6316DZ26-ARJZ-R7	2.63	1120	25.6
ADM6316AY27-ARJZ-R7	2.7	1	1.6
ADM6316AY29-ARJZ-R7	2.93	1	1.6
ADM6316AZ29ARJZ-R7	2.93	1	25.6
ADM6316CY29-ARJ-RL7	2.93	140	1.6
ADM6316CY29-ARJZ-R7	2.93	140	1.6
ADM6316BX30-ARJZ-R7	3	20	0.102
ADM6316DZ31-ARJ-RL7	3.08	1120	25.6
ADM6316DZ31-ARJZ-R7	3.08	1120	25.6
ADM6316BX46-ARJZ-R7	4.63	20	0.102
ADM6316CY26ARJZ-R7	2.63	140	1.6
ADM6316CY46-ARJ-RL7	4.63	140	1.6
ADM6316CY46-ARJZ-R7	4.63	140	1.6
ADM6318CZ28-ARJ-RL7	2.8	140	25.6
ADM6318CZ28-ARJZ-R7	2.8	140	25.6
ADM6318CY29-ARJZ-R7	2.93	140	1.6
ADM6318CY45-ARJZ-R7	4.5	140	1.6
ADM6318CY46-ARJ-RL7	4.63	140	1.6
ADM6318CY46-ARJZ-R7	4.63	140	1.6
ADM6318BX49-ARJZ-R7	4.9	20	0.102
ADM6319C29-ARJ-RL7	2.93	140	N/A
ADM6319C29-ARJZ-RL7	2.93	140	N/A
ADM6319B25ARJZ-R7	2.5	20	n/A
ADM6319B31-ARJZ-RL7	3.08	20	N/A
ADM6319C46-ARJ-RL7	4.63	140	N/A
ADM6319C46-ARJZ-RL7	4.63	140	N/A
ADM6320CZ27-ARJZ-R7	2.7	140	25.6
ADM6320CX29-ARJZ-R7	2.93	140	0.102
ADM6320CY29-ARJ-RL7	2.93	140	1.6
ADM6320CY29-ARJZ-R7	2.93	140	1.6
ADM6320CZ29-ARJ-RL7	2.93	140	25.6
ADM6320CZ29-ARJZ-R7	2.93	140	25.6
ADM6320BX33-ARJZ-R7	3.3	140	0.102
ADM6320CW33-ARJZ-R7	3.3	20	0.0063
ADM6320BX45-ARJZ-R7	4.5	20	0.102
ADM6320CY46-ARJ-RL7	4.63	140	1.6
ADM6320CY46-ARJZ-R7	4.63	140	1.6
ADM6321BZ25-ARJZ-R7	2.5	20	25.6
ADM6321AY30ARJZ-R7	3	1	1.6
ADM6321AY31ARJZ-R7	3.08	1	1.6
ADM6321AY43-ARJZ-R7	4.3	1	1.6
ADM6321CY46-ARJ-RL7	4.63	140	1.6
ADM6321CY46-ARJZ-R7	4.63	140	1.6
ADM6322C29ARJZ-RL7	2.93	140	N/A
ADM6322C46-ARJ-RL7	4.63	140	N/A
ADM6322C46-ARJZ-RL7	4.63	140	N/A

OUTLINE DIMENSIONS

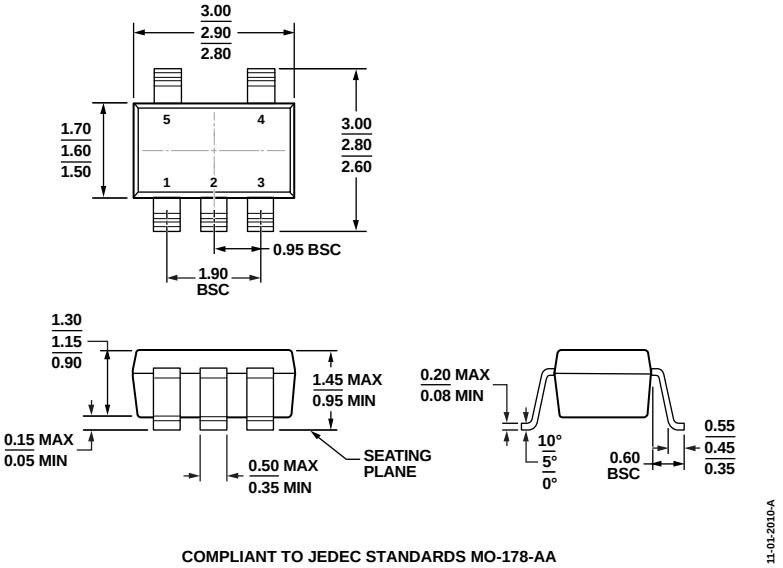

Figure 22. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

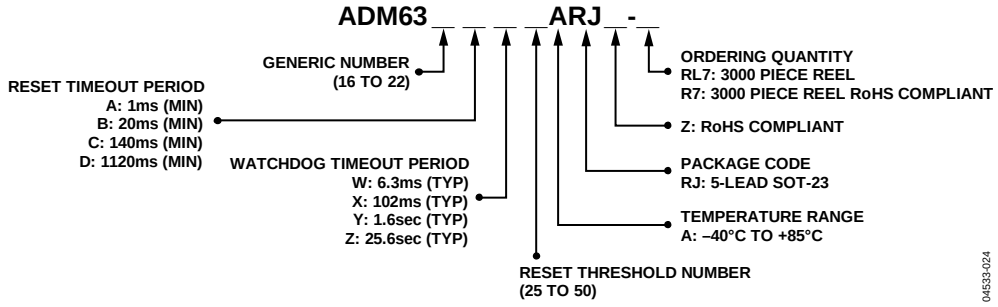

Figure 23. Ordering Code Structure (Modified Diagram)

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Ordering Quantity[4]	Package Description	Package Option	Branding
ADM6316xxxARJ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N00
ADM6316xxxARJZ-R7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	M7Q
ADM6317xxxARJZ-R7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	M9N
ADM6318xxxARJ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N02
ADM6318xxxARJZ-R7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	M4Q
ADM6319xxARJ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N03
ADM6319xxARJZ-R7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N0S
ADM6320xxxARJ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N04
ADM6320xxxARJZ-R7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N0T
ADM6321xxxARJ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N05
ADM6321xxxARJZ-R7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	M8L
ADM6322xxARJ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	N06
ADM6322xxARJZ-RL7	−40°C to +85°C	3,000	5-Lead SOT-23	RJ-5	M8J

[1] Complete the ordering code by inserting reset threshold, reset timeout, and watchdog timeout (ADM6316/ADM6317/ADM6318/ADM6320/ADM6321) suffixes from Table 5 to Table 7. No watchdog timeout is available for ADM6319/ADM6322.
[2] Contact sales for the availability of nonstandard models. See Table 8 for a list of standard models.
[3] Z = RoHS Compliant Part.
[4] A minimum of 12,000 (four reels) must be ordered.

NOTES

NOTES

NOTES

D04533-0-5/13(F)