Actel POWER MATTERS

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v1.2

IGLOOe Low-Power Flash FPGAs
with Flash*Freeze Technology

FlashLock

Features and Benefits

Low Power
- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- Low-Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Flash*Freeze Pin Allows Easy Entry to / Exit from Ultra-Low-Power Flash*Freeze Mode

High Capacity
- 600 k to 3 Million System Gates
- 108 to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Pro (Professional) I/O
- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—Up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II
- I/O Registers on Input, Output, and Enable Paths
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay
- Schmitt Trigger Option on Single-Ended Inputs
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO®e Family

Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks, Each with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

Embedded Memory
- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)

ARM Processor Support in IGLOOe FPGAs
- M1 IGLOOe Devices—Cortex™-M1 Soft Processor Available with or without Debug

IGLOOe Product Family

IGLOOe Devices	AGLE600	AGLE3000
ARM-Enabled IGLOOe Devices		M1AGLE3000
System Gates	600 k	3 M
VersaTiles (D-flip-flops)	13,824	75,264
Quiescent Current (typical) in Flash*Freeze Mode (µW)	49	137
RAM kbits (1,024 bits)	108	504
4,608-Bit Blocks	24	112
FlashROM Bits	1 k	1 k
Secure (AES) ISP	Yes	Yes
CCCs with Integrated PLLs	6	6
VersaNet Globals[1]	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
Package Pins FBGA	FG256, FG484	FG484, FG896

Notes:
1. *Refer to the Cortex-M1 Handbook for more information.*
2. *Six chip (main) and twelve quadrant global networks are available.*
3. *For devices supporting lower densities, refer to the IGLOO Low-Power Flash FPGAs with Flash*Freeze Technology handbook.*

I/Os Per Package[1]

IGLOOe Devices	AGLE600		AGLE3000	
ARM-Enabled IGLOOe Devices			M1AGLE3000	
	I/O Types			
Package	Single-Ended I/O[1]	Differential I/O Pairs	Single-Ended I/O[1]	Differential I/O Pairs
FG256	165	79	–	–
FG484	270	135	341	168
FG896	–	–	620	310

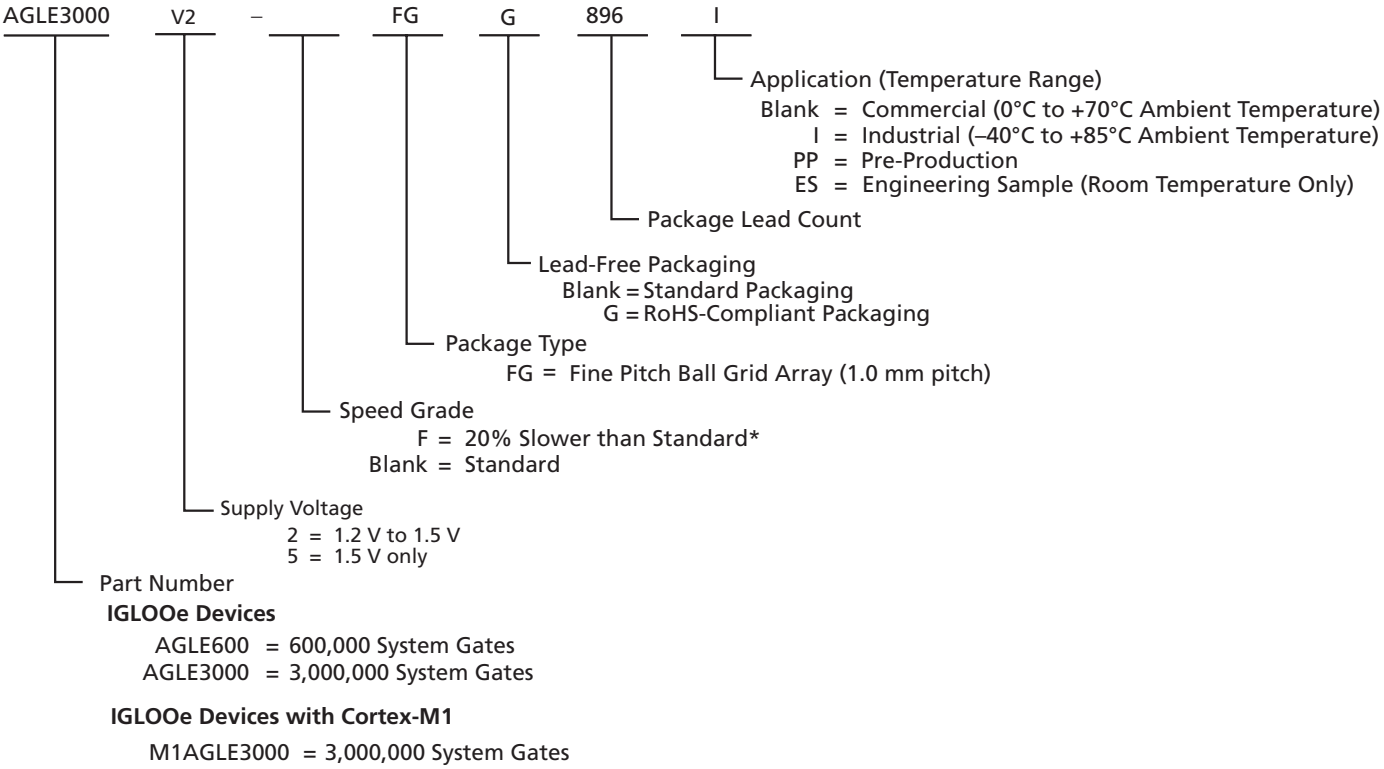
Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the IGLOOe Low-Power Flash FPGAs with Flash*Freeze Technology handbook to ensure compliance with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *For AGLE3000 devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
4. *FG256 and FG484 are footprint-compatible packages.*
5. *When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (V_{REF}) per minibank (group of I/Os). When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
6. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
7. *"G" indicates RoHS-compliant packages. Refer to "IGLOOe Ordering Information" on page III for the location of the "G" in the part number.*

IGLOOe FPGAs Package Sizes Dimensions

Package	FG256	FG484	FG896
Length × Width (mm × mm)	17 × 17	23 × 23	31 × 31
Nominal Area (mm^2)	289	529	961
Pitch (mm)	1	1	1
Height (mm)	1.6	2.23	2.23

IGLOOe Ordering Information



Notes:

1. *Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.*
2. *The DC and switching characteristics for the –F speed grade targets are based only on simulation. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*

Temperature Grade Offerings

Package	AGLE600	AGLE3000
		M1AGLPE3000
FG256	C, I	–
FG484	C, I	C, I
FG896	–	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature.
I = Industrial temperature range: –40°C to 85°C ambient temperature.

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.
C [2]	✓	✓
I [3]	–	✓

Notes:

1. *The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*
2. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
3. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

References made to IGLOOe devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Actel representative for device availability: http://www.actel.com/contact/default.aspx.

1 – IGLOOe Device Family Overview

General Description

The IGLOOe family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOOe devices enables entering and exiting an ultra-low-power mode while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low-power consumption while the IGLOOe device is completely functional in the system. This allows the IGLOOe device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOOe devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). IGLOOe is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOOe devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on 6 integrated phase-locked loops (PLLs). IGLOOe devices have up to 3 million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

M1 IGLOOe devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 IGLOOe device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Actel for use in M1 IGLOOe FPGAs.

The ARM-enabled devices have Actel ordering numbers that begin with M1AGLE and do not support AES decryption.

Flash*Freeze Technology

The IGLOOe device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low-power Flash*Freeze mode. IGLOOe devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOOe V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOOe device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOOe devices the best fit for portable electronics.

Flash Advantages

Low Power

Flash-based IGLOOe devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOOe devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOOe devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOOe device the lowest total system power offered by any FPGA.

Security

The nonvolatile, flash-based IGLOOe devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOOe devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOOe devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOOe devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOOe devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOOe devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOOe device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOOe family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOOe family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOOe device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOOe FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based IGLOOe devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOOe devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOOe device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOOe devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOOe devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOOe family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOOe family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOOe flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOOe FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOOe family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOOe family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOOe architecture provides granularity comparable to standard-cell ASICs. The IGLOOe device consists of five distinct and programmable architectural features (Figure 1-1 on page 4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOOe core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface.

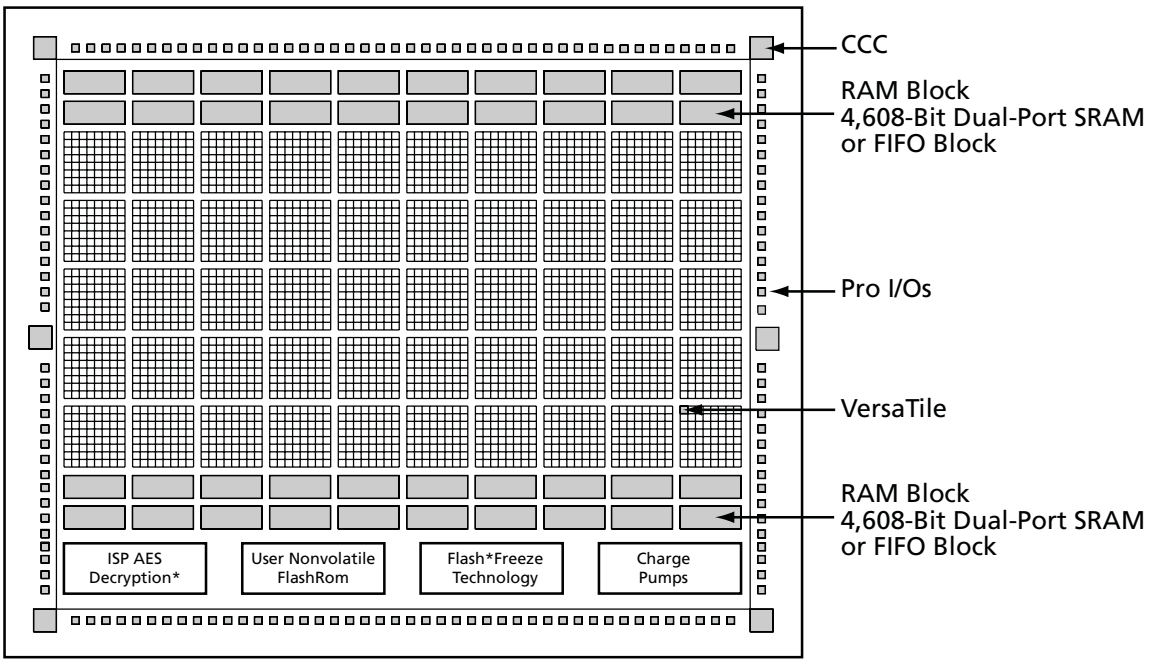


Figure 1-1 • **IGLOOe Device Architecture Overview**

*Flash*Freeze Technology*

The IGLOOe device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the

inherent low power static and dynamic capabilities of the IGLOOe device. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode.

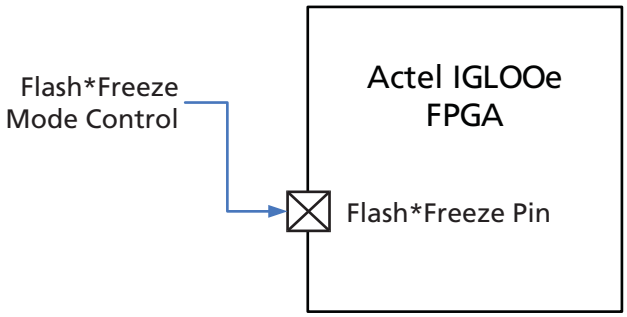


Figure 1-2 • **IGLOOe Flash*Freeze Mode**

VersaTiles

The IGLOOe core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The IGLOOe VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-3 for VersaTile configurations.

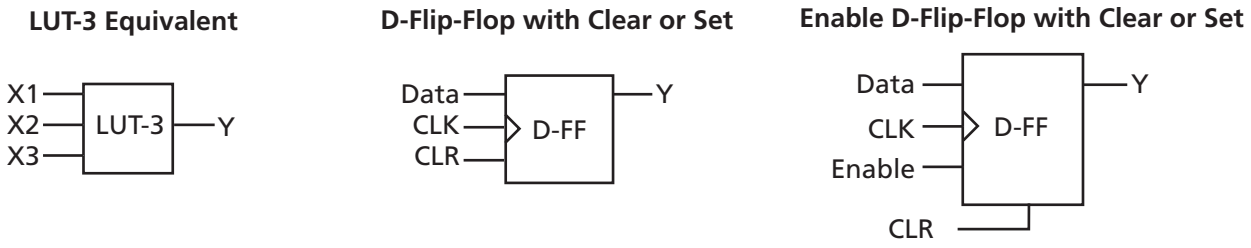


Figure 1-3 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel IGLOOe devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOOe IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOOe development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOOe devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOOe devices provide designers with very flexible clock conditioning capabilities. Each member of the IGLOOe family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

IGLOOe devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Pro I/Os with Advanced I/O Standards

The IGLOOe family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V). IGLOOe FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)

Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

IGLOOe banks support M-LVDS with 20 multi-drop points.

Part Number and Revision Date

Part Number 51700096-001-3
Revised October 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (June 2008)	The Quiescent Current values in the "IGLOOe Product Family" table were updated.	I
v1.0 (April 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
51700096-001-1 (March 2008)	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
51700096-001-0 (January 2008)	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 µW)" was removed from "Low-Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" sections.	I I, 1-7
Advance v0.4 (December 2007)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0.	N/A
Advance v0.3 (September 2007)	Table 1 • IGLOOe Product Family was updated to change the maximum number of user I/Os for AGLE3000.	i
	Table 2 • IGLOOe FPGAs Package Sizes Dimensions is new. Package dimensions were removed from the "I/Os Per Package1" table. The number of I/Os was updated for FG896.	ii
	A note regarding marking information was added to "IGLOOe Ordering Information".	iii
Advance v0.2 (July 2007)	Cortex-M1 device information was added to Cortex-M1 device information was added to Table 1 • IGLOOe Product Family, the "I/Os Per Package1" table, "IGLOOe Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
Advance v0.1	The words "ambient temperature" were added to the temperature range in the "IGLOOe Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

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Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status document may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

2 – IGLOOe DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI} and VMV [3]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*
3. *VMV pins must be connected to the corresponding V_{CCI} pins. See Pin Descriptions for further information.*

Table 2-2 • Recommended Operating Conditions [4]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient Temperature		0 to +70 [6]	–40 to +85 [7]	°C
T_J	Junction Temperature [8]		0 to + 85	–40 to +100	
V_{CC}	1.5 V DC core supply voltage[1]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage[2]		1.14 to 1.575	1.14 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP} [5]	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[3]	0 to 3.45	0 to 3.45	V
V_{CCPLL} [9]	Analog power supply (PLL)	1.5 V DC core supply voltage[1]	1.4 to 1.6	1.4 to 1.6	V
		1.2 V–1.5 V wide range core voltage[2]	1.14 to 1.575	1.14 to 1.575	V
V_{CCI} and VMV [10]	1.2 V DC supply voltage[2]		1.14 to 1.26	1.14 to 1.26	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *For IGLOOe V5 devices*
2. *For IGLOOe V2 devices only, operating at $V_{CCI} \geq V_{CC}$*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-20 on page 2-20. V_{CCI} should be at the same voltage within a given I/O bank.*
4. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
5. *V_{PUMP} can be left floating during operation (not programming mode).*
6. *Maximum T_J = 85 °C.*
7. *Maximum T_J = 100 °C.*
8. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.*
9. *V_{CCPLL} pins should be tied to V_{CC} pins. See Pin Descriptions for further information.*
10. *VMV pins must be connected to the corresponding V_{CCI} pins. See Pin Descriptions for further information.*

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits [1]**

V_{CCI}	Average V_{CCI}–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *The device meets overshoot/undershoot specification requirements for PCI inputs with V_{CCI} = 3.45 V at 85°C maximum, whereas the average toggling of inputs at one-sixth of PCI frequency is considered.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. $V_{CCI} > V_{CC} – 0.75$ V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until V_{CC} and V_{CCPLX} exceed brownout activation levels. The V_{CC} activation level is specified as 1.1 V worst-case (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the *Power-Up/-Down Behavior of Low-Power Flash Devices* chapter of the handbook for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

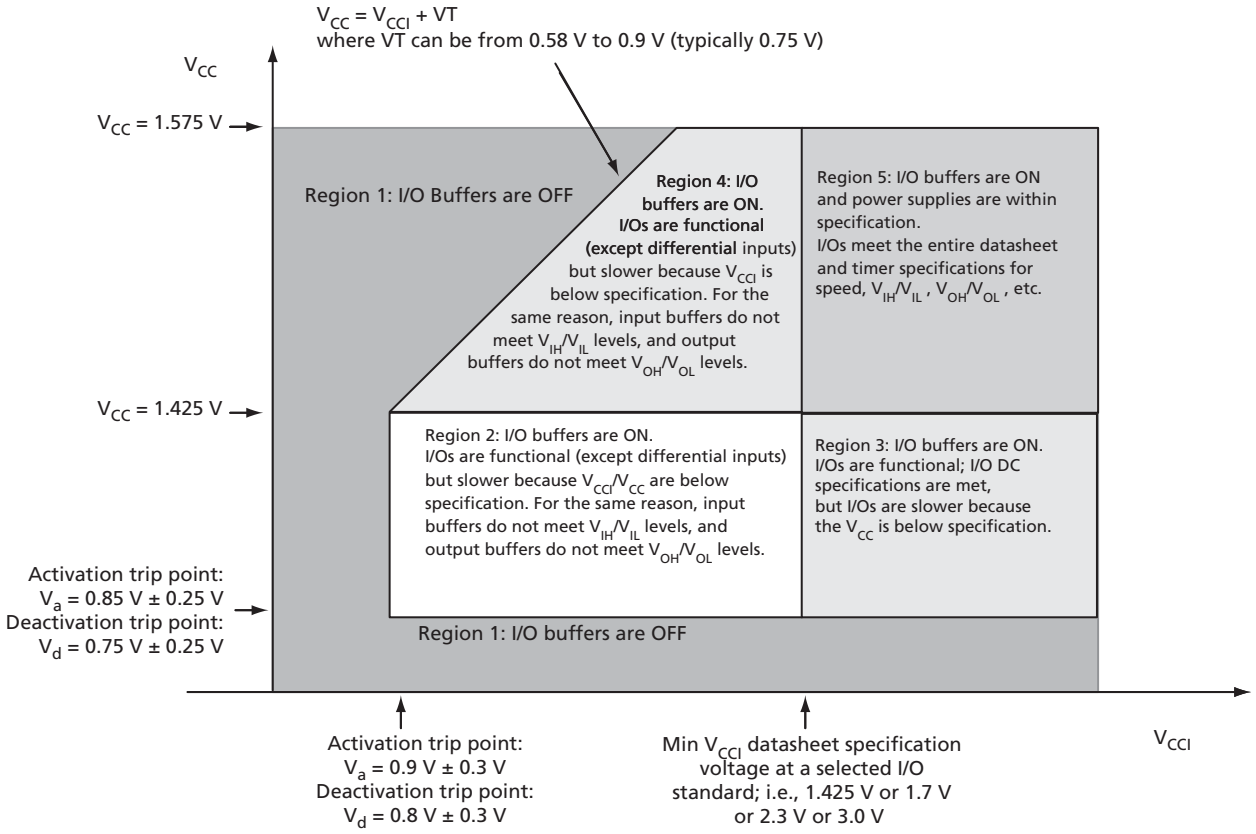


Figure 2-1 • **V5 – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

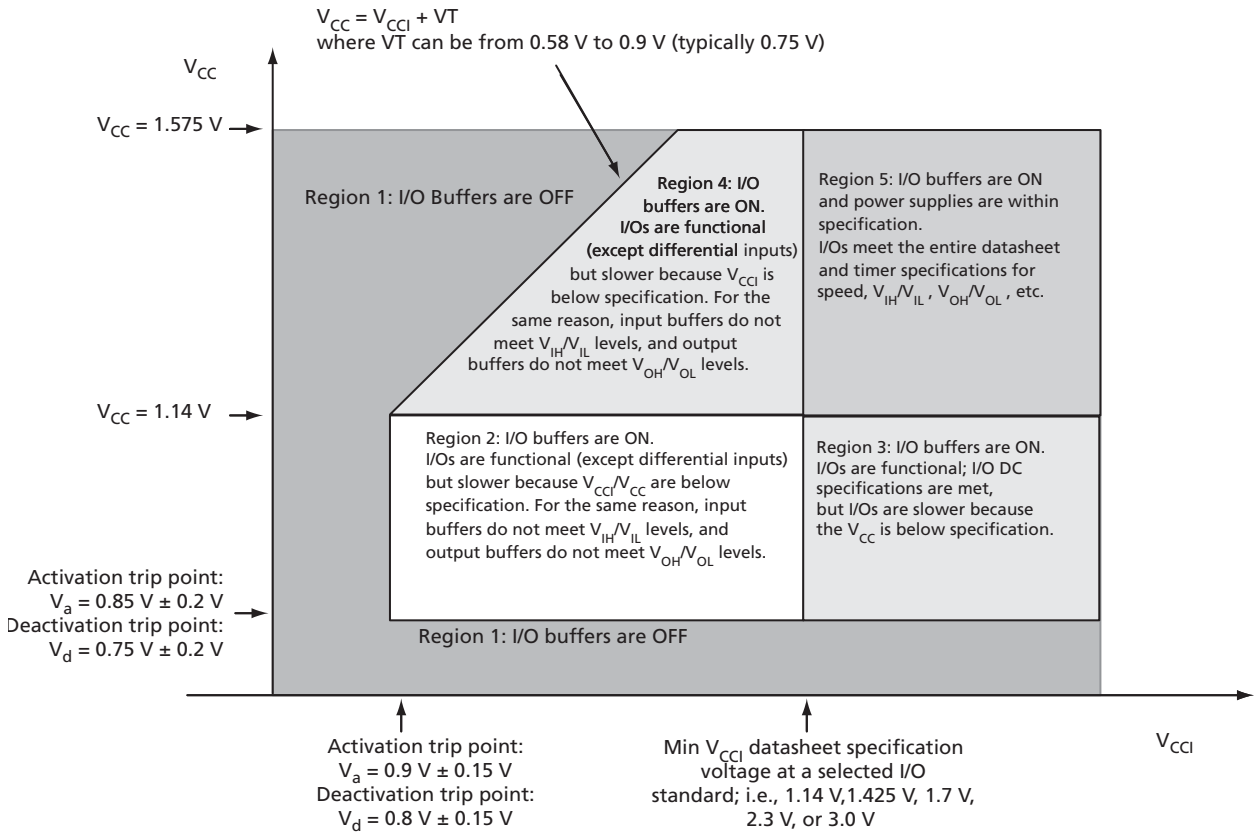


Figure 2-2 • **V2 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 2-1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2-2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{13.6\text{°C/W}} = 2.206\ \text{W}$$

EQ 2-2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C,V_{CC} = 1.425 V) For IGLOOe V2 or V5 devices, 1.5 V DC Core Supply Voltage**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.425	0.95	0.96	0.98	1.00	1.01	1.02
1.5	0.88	0.89	0.91	0.93	0.93	0.94
1.575	0.82	0.84	0.85	0.87	0.88	0.89

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, V_{CC} = 1.14 V) For IGLOOe V2, 1.2 V DC Core Supply Voltage**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.14	0.97	0.98	0.99	1.00	1.01	1.01
1.2	0.84	0.85	0.86	0.87	0.88	0.88
1.26	0.76	0.77	0.78	0.79	0.79	0.80

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (V_{CC}, V_{CCI}, and V_{JTAG}), operating temperature, system clock frequency, and power modes usage. Actel recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Quiescent Supply Current (I_{DD}), IGLOOe Flash*Freeze Mode***

	Core Voltage	AGLE600	AGLE3000	Units
Typical (25°C)	1.2 V	34	95	µA
	1.5 V	72	310	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-9 • **Quiescent Supply Current (I_{DD}), IGLOOe Sleep Mode (V_{CC} = 0 V)***

	Core Voltage	AGLE600	AGLE3000	Units
V_{CCI}/V_{JTAG} = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
V_{CCI}/V_{JTAG} = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
V_{CCI}/V_{JTAG} = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
V_{CCI}/V_{JTAG} = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
V_{CCI}/V_{JTAG}= 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-10 • **Quiescent Supply Current (I_{DD}), IGLOOe Shutdown Mode (V_{CC}, V_{CCI} = 0 V)***

	Core Voltage	AGLE600	AGLE3000	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-11 • Quiescent Supply Current, No IGLOOe Flash*Freeze Mode*

	Core Voltage	AGLE600	AGLE3000	Units
I_{CCA} Current[2]				
Typical (25°C)	1.2 V	28	89	µA
	1.5 V	82	320	µA
I_{CCI} or I_{JTAG} Current[3, 4]				
V_{CCI}/V_{JTAG} = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
V_{CCI}/V_{JTAG} = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
V_{CCI}/V_{JTAG} = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
V_{CCI}/V_{JTAG} = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
V_{CCI}/V_{JTAG}= 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

Notes:

1. *To calculate total device I_{DD}, multiply the number of banks used in I_{CCI} and add I_{CCA} contribution.*
2. *Includes V_{CC}, V_{CCPLL}, and V_{PUMP} currents.*
3. *Per V_{CCI} or V_{JTAG} bank*
4. *Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Power per I/O Pin

Table 2-12 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	V_{CCI} (V)	Static Power P_{DC6} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS [3]	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger [3]	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.07
2.5 V GTL	2.5	2.13	3.62
3.3 V GTL+	3.3	2.81	2.97
2.5 V GTL+	2.5	2.57	2.55
HSTL (I)	1.5	0.17	0.85
HSTL (II)	1.5	0.17	0.85
SSTL2 (I)	2.5	1.38	3.30
SSTL2 (II)	2.5	1.38	3.30
SSTL3 (I)	3.3	3.21	8.08
SSTL3 (II)	3.3	3.21	8.08
Differential			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.71	1.62

Notes:

1. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
2. *P_{AC9} is the total dynamic power measured on V_{CCI}.*
3. *Applicable for IGLOOe V2 devices only.*

Table 2-13 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS [4]	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*
4. *Applicable for IGLOOe V2 devices only.*

Power Consumption of Various Internal Resources

Table 2-14 • Different Components Contributing to the Dynamic Power Consumption in IGLOOe Devices For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)	
		AGLE600	AGLE3000
P_{AC1}	Clock contribution of a Global Rib	19.7	12.77
P_{AC2}	Clock contribution of a Global Spine	4.16	1.85
P_{AC3}	Clock contribution of a VersaTile row	0.88	
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.11	
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.057	
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.207	
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.207	
P_{AC8}	Average contribution of a routing net	0.7	
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-9.	
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-13 on page 2-10.	
P_{AC11}	Average contribution of a RAM block during a read operation	25.00	
P_{AC12}	Average contribution of a RAM block during a write operation	30.00	
P_{AC13}	Dynamic contribution for PLL	2.70	

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power calculator or SmartPower in Actel Libero® Integrated Design Environment (IDE) software.*

Table 2-15 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Definition	Device Specific Static Power (mW)	
		AGLE600	AGLE3000
P_{DC1}	Array static power in Active mode	See Table 2-11 on page 2-8.	
P_{DC2}	Array static power in Static (Idle) mode	See Table 2-10 on page 2-7.	
P_{DC3}	Array static power in Flash*Freeze mode	See Table 2-8 on page 2-7.	
P_{DC4}	Static PLL contribution	1.84	
P_{DC5}	Bank quiescent power (V_{CCI}-dependent)	See Table 2-11 on page 2-8.	
P_{DC6}	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-9.	
P_{DC7}	I/O output pin static power (standard-dependent)	See Table 2-13 on page 2-10.	

Table 2-16 • Different Components Contributing to the Dynamic Power Consumption in IGLOOe Devices For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)	
		AGLE600	AGLE3000
P_{AC1}	Clock contribution of a Global Rib	12.61	8.17
P_{AC2}	Clock contribution of a Global Spine	2.66	1.18
P_{AC3}	Clock contribution of a VersaTile row	0.56	
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.071	
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.045	
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.186	
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.109	
P_{AC8}	Average contribution of a routing net	0.449	
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-8 on page 2-7.	
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-9 on page 2-7 and Table 2-10 on page 2-7.	
P_{AC11}	Average contribution of a RAM block during a read operation	25.00	
P_{AC12}	Average contribution of a RAM block during a write operation	30.00	
P_{AC13}	Dynamic PLL contribution	2.10	

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power calculator or SmartPower in Actel Libero IDE software.*

Table 2-17 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Definition	Device Specific Static Power (mW)	
		AGLE600	AGLE3000
P_{DC1}	Array static power in Active mode	See Table 2-11 on page 2-8.	
P_{DC2}	Array static power in Static (Idle) mode	See Table 2-10 on page 2-7.	
P_{DC3}	Array static power in Flash*Freeze mode	See Table 2-8 on page 2-7.	
P_{DC4}	Static PLL contribution	0.90	
P_{DC5}	Bank quiescent power (V_{CCI}-dependent)	See Table 2-11 on page 2-8.	
P_{DC6}	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-9.	
P_{DC7}	I/O output pin static power (standard-dependent)	See Table 2-13 on page 2-10.	

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-18 on page 2-15.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-19 on page 2-15.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-19 on page 2-15. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = (P_{DC1}$ or P_{DC2} or $P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 2-18 on page 2-15.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 2-18 on page 2-15.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-18 on page 2-15.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-18 on page 2-15.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-18 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-18 on page 2-15.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-18 on page 2-15.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-19 on page 2-15.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-19 on page 2-15.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-19 on page 2-15.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-18 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-19 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

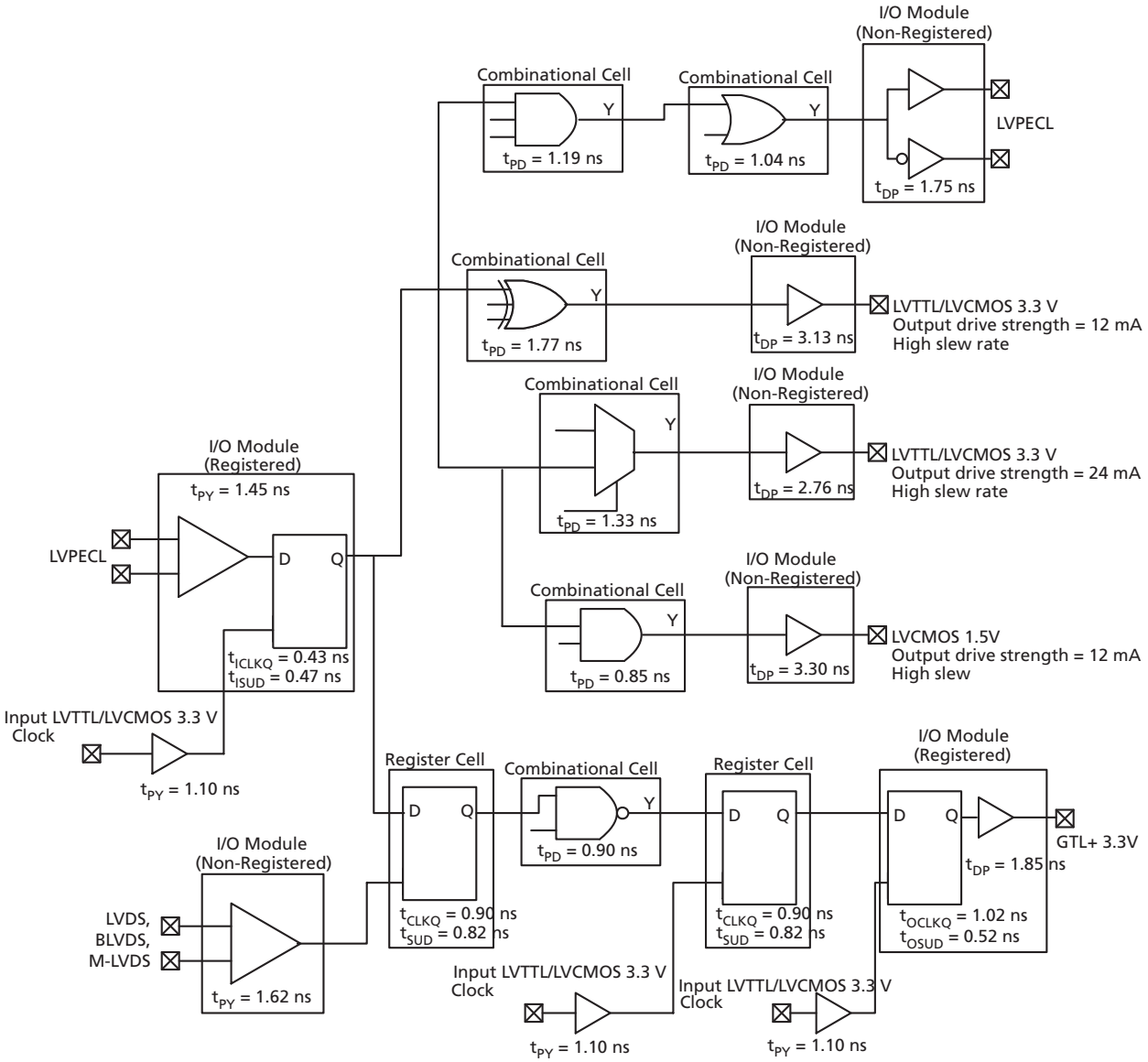


Figure 2-3 • **Timing Model**
Operating Conditions: Std. Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case V_{CC} = 1.425 V, Applicable to 1.5 V DC Core Voltage, V2 and V5 devices

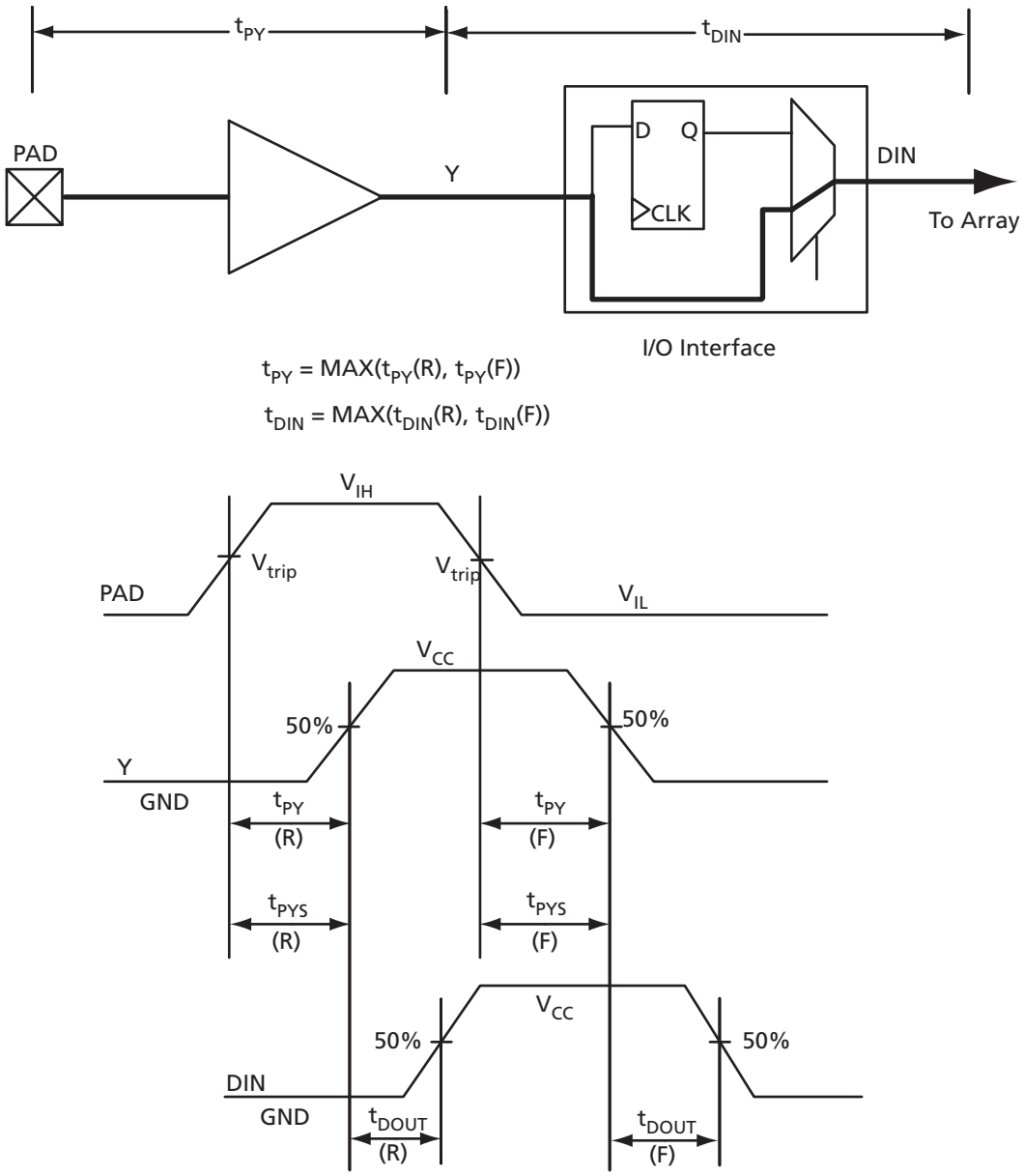


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

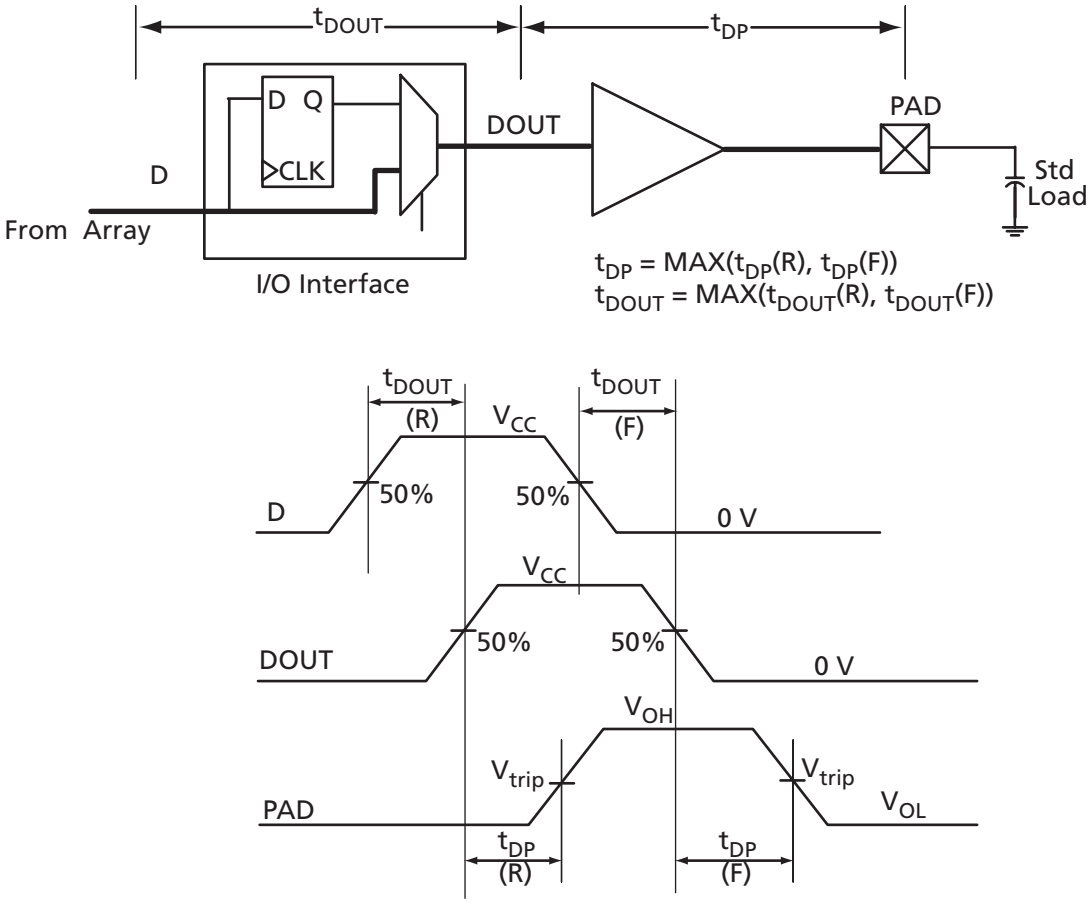


Figure 2-5 • **Output Buffer Model and Delays (example)**

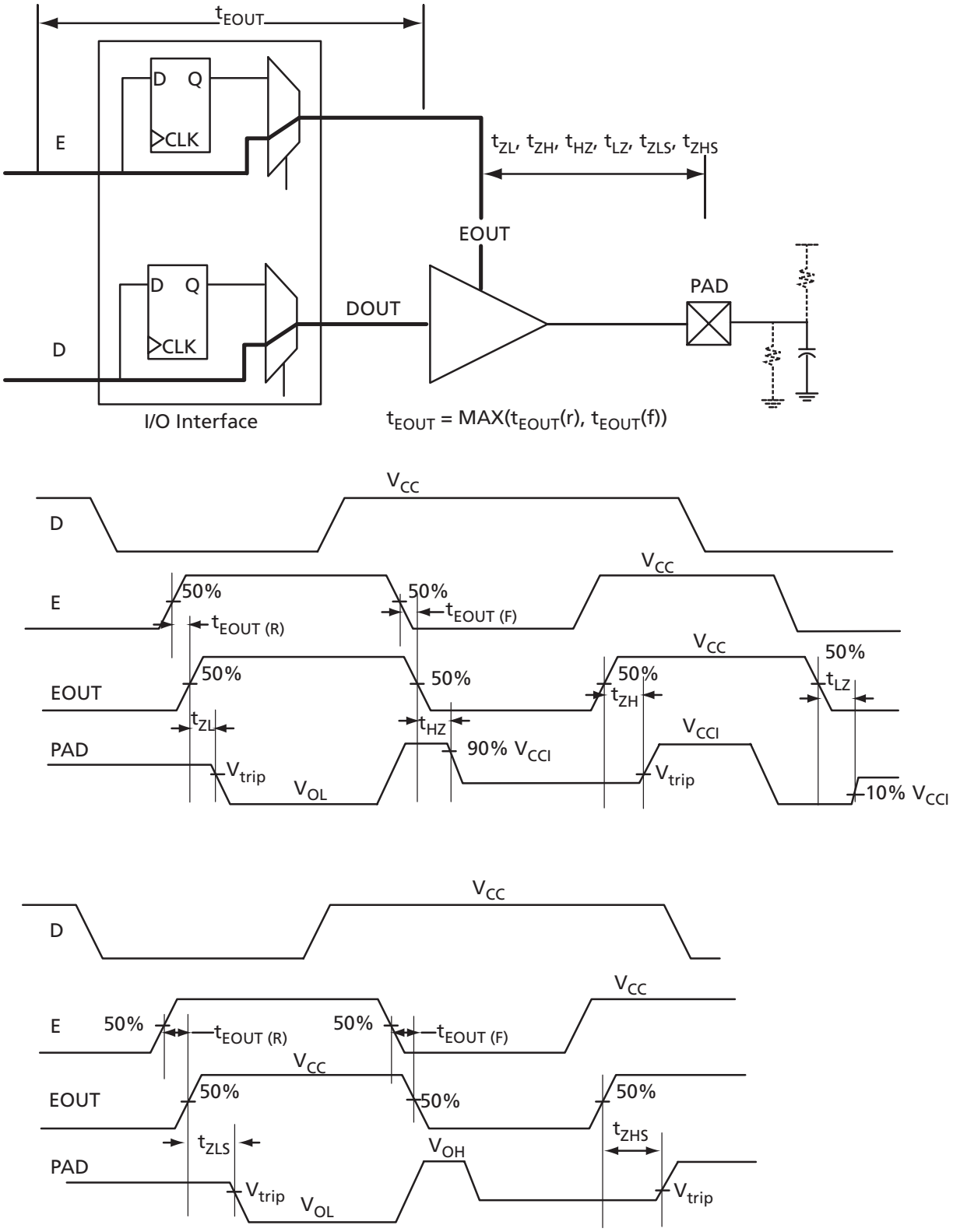


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-20 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1]	I_{OH}[1]
			Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65*V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65*V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
1.2 V LVCMOS[4]	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
2.5 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	2.7	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	2.7	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575	0.4	V_{CCI} – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575	0.4	V_{CCI} – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	2.7	0.54	V_{CCI} – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	2.7	0.35	V_{CCI} – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output Slew Rates can be extracted from IBIS Models, located at http://www.actel.com/download/ibis/default.aspx.*
4. *Applicable to V2 Devices ONLY, operating in the 1.2 V core range.*

Table 2-21 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standards	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[3]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *Applicable to V2 Devices ONLY, operating in the 1.2 V core range.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • Summary of AC Measuring Points

Standard	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_REF})	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
1.2 V LVCMOS	–	–	0.6 V
3.3 V PCI	–	–	0.285*V_{CCI} (RR)
	–	–	0.615*V_{CCI} (FF))
3.3 V PCI-X	–	–	0.285*V_{CCI} (RR)
	–	–	0.615*V_{CCI} (FF)
3.3 V GTL	0.8 V	1.2 V	V_{REF}
2.5 V GTL	0.8 V	1.2 V	V_{REF}
3.3 V GTL+	1.0 V	1.5 V	V_{REF}
2.5 V GTL+	1.0 V	1.5 V	V_{REF}
HSTL (I)	0.75 V	0.75 V	V_{REF}
HSTL (II)	0.75 V	0.75 V	V_{REF}
SSTL2 (I)	1.25 V	1.25 V	V_{REF}
SSTL2 (II)	1.25 V	1.25 V	V_{REF}
SSTL3 (I)	1.5 V	1.485 V	V_{REF}
SSTL3 (II)	1.5 V	1.485 V	V_{REF}
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-23 • I/O AC Parameter Definitions

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5	–	0.98	2.18	0.19	1.10	1.37	0.67	2.22	1.72	2.78	3.17	5.85	5.35	ns
2.5 V LVCMOS	12 mA	High	5	–	0.98	2.21	0.19	1.34	1.45	0.67	2.25	1.89	2.86	3.06	5.88	5.52	ns
1.8 V LVCMOS	12 mA	High	5	–	0.98	2.44	0.19	1.30	1.63	0.67	2.48	2.07	3.15	3.67	6.11	5.70	ns
1.5 V LVCMOS	12 mA	High	5	–	0.98	2.77	0.19	1.50	1.82	0.67	2.82	2.35	3.33	3.78	6.45	5.98	ns
3.3 V PCI	Per PCI spec	High	10	25 2	0.98	2.44	0.19	0.98	1.45	0.67	2.49	1.84	2.79	3.17	6.12	5.47	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 2	0.98	2.44	0.19	0.94	1.37	0.67	2.49	1.84	2.79	3.17	6.12	5.47	ns
3.3 V GTL	25 mA	High	10	25	0.98	1.83	0.19	2.41	–	0.67	1.84	1.83	0.00	0.00	5.47	5.46	ns
2.5 V GTL	25 mA	High	10	25	0.98	1.90	0.19	2.04	–	0.67	1.94	1.87	0.00	0.00	5.57	5.50	ns
3.3 V GTL+	35 mA	High	10	25	0.98	1.85	0.19	1.35	–	0.67	1.88	1.81	0.00	0.00	5.51	5.44	ns
2.5 V GTL+	33 mA	High	10	25	0.98	1.97	0.19	1.29	–	0.67	2.00	1.84	0.00	0.00	5.63	5.47	ns
HSTL (I)	8 mA	High	20	50	0.98	2.74	0.19	1.77	–	0.67	2.79	2.73	0.00	0.00	6.42	6.36	ns
HSTL (II)	15 mA	High	20	25	0.98	2.62	0.19	1.77	–	0.67	2.66	2.40	0.00	0.00	6.29	6.03	ns
SSTL2 (I)	15 mA	High	30	50	0.98	1.91	0.19	1.15	–	0.67	1.94	1.72	0.00	0.00	5.57	5.35	ns
SSTL2 (II)	18 mA	High	30	25	0.98	1.94	0.19	1.15	–	0.67	1.97	1.66	0.00	0.00	5.60	5.29	ns
SSTL3 (I)	14 mA	High	30	50	0.98	2.05	0.19	1.09	–	0.67	2.09	1.71	0.00	0.00	5.72	5.34	ns
SSTL3 (II)	21 mA	High	30	25	0.98	1.86	0.19	1.09	–	0.67	1.89	1.58	0.00	0.00	5.52	5.21	ns
LVDS/B-LVDS/ M-LVDS	24 mA	High	–	–	0.98	1.77	0.19	1.62	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.98	1.75	0.19	1.45	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-42 for connectivity. This resistor is not required during normal operation.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5	–	1.55	2.46	0.26	1.31	1.57	1.10	2.51	2.04	3.27	3.96	8.32	7.85	ns
2.5 V LVCMOS	12 mA	High	5	–	1.55	2.50	0.26	1.55	1.76	1.10	2.54	2.22	3.34	3.83	8.35	8.03	ns
1.8 V LVCMOS	12 mA	High	5	–	1.55	2.74	0.26	1.53	1.95	1.10	2.79	2.41	3.66	4.54	8.60	8.21	ns
1.5 V LVCMOS	12 mA	High	5	–	1.55	3.09	0.26	1.72	2.15	1.10	3.15	2.70	3.85	4.66	8.96	8.51	ns
1.2 V LVCMOS	2mA	High	5	–	1.55	4.07	0.26	2.06	2.96	1.10	3.90	3.43	3.80	4.02	9.49	9.03	ns
3.3 V PCI	Per PCI spec	High	10	25 2	1.55	2.74	0.26	1.19	1.63	1.10	2.80	2.16	3.28	3.96	8.60	7.97	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 2	1.55	2.74	0.26	1.21	1.57	1.10	2.80	2.16	3.28	3.96	8.60	7.97	ns
3.3 V GTL	25 mA	High	10	25	1.55	2.09	0.26	2.75	–	1.10	2.10	2.09	–	–	7.91	7.89	ns
2.5 V GTL	25 mA	High	10	25	1.55	2.16	0.26	2.35	–	1.10	2.20	2.13	–	–	8.01	7.94	ns
3.3 V GTL+	35 mA	High	10	25	1.55	2.11	0.26	1.61	–	1.10	2.15	2.07	–	–	7.95	7.88	ns
2.5 V GTL+	33 mA	High	10	25	1.55	2.23	0.26	1.55	–	1.10	2.28	2.11	–	–	8.08	7.91	ns
HSTL (I)	8 mA	High	20	50	1.55	3.10	0.26	1.94	–	1.10	3.12	3.10	–	–	8.93	8.91	ns
HSTL (II)	15 mA	High	20	25	1.55	2.93	0.26	1.94	–	1.10	2.98	2.75	–	–	8.79	8.55	ns
SSTL2 (I)	15 mA	High	30	50	1.55	2.17	0.26	1.39	–	1.10	2.21	2.04	–	–	8.02	7.84	ns
SSTL2 (II)	18 mA	High	30	25	1.55	2.20	0.26	1.39	–	1.10	2.24	1.97	–	–	8.05	7.78	ns
SSTL3 (I)	14 mA	High	30	50	1.55	2.32	0.26	1.32	–	1.10	2.37	2.02	–	–	8.17	7.83	ns
SSTL3 (II)	21 mA	High	30	25	1.55	2.12	0.26	1.32	–	1.10	2.16	1.89	–	–	7.97	7.70	ns
LVDS/B-LVDS/ M-LVDS	24 mA	High	–	–	1.55	2.19	0.26	1.88	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	1.55	2.16	0.26	1.70	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-42 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-26 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-27 • **I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 2-27 • I/O Output Buffer Maximum Resistances[1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 2-28 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
V_{CCI}	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k
1.2 V	TBD	TBD	TBD	TBD

Notes:

1. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{WEAK\ PULL\text{-}DOWN\text{-}MIN}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{WEAK\ PULL\text{-}UP\text{-}MIN}$

Table 2-29 • **I/O Short Currents I_{OSH}/I_{OSL}**

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X Specification	Per PCI Curves	
3.3 V GTL	25 mA	268	181
2.5 V GTL	25 mA	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

* T_J = 100°C

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-30 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 2-31 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-32 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

* *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 2-33 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

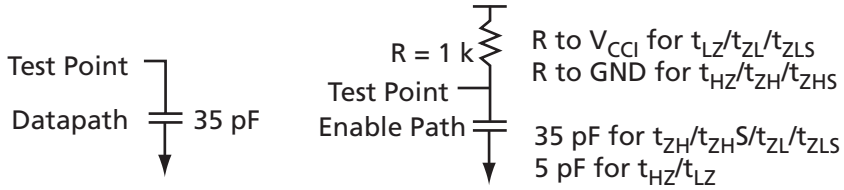


Figure 2-7 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-35 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	5.04	0.19	1.10	1.37	0.67	5.13	4.10	2.33	2.22	8.76	7.73	ns
8 mA	Std.	0.98	4.16	0.19	1.10	1.37	0.67	4.23	3.54	2.60	2.72	7.86	7.17	ns
12 mA	Std.	0.98	3.53	0.19	1.10	1.37	0.67	3.60	3.12	2.78	3.03	7.23	6.75	ns
16 mA	Std.	0.98	3.36	0.19	1.10	1.37	0.67	3.42	3.03	2.82	3.12	7.05	6.66	ns
24 mA	Std.	0.98	3.26	0.19	1.10	1.37	0.67	3.32	3.04	2.87	3.45	6.95	6.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-36 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	2.93	0.19	1.10	1.37	0.67	2.99	2.33	0.00	2.34	6.62	5.96	ns
8 mA	Std.	0.98	2.45	0.19	1.10	1.37	0.67	2.50	1.92	2.60	2.84	6.13	5.55	ns
12 mA	Std.	0.98	2.18	0.19	1.10	1.37	0.67	2.22	1.72	2.78	3.17	5.85	5.35	ns
16 mA	Std.	0.98	2.13	0.19	1.10	1.37	0.67	2.17	1.69	2.83	3.26	5.80	5.32	ns
24 mA	Std.	0.98	2.15	0.19	1.10	1.37	0.67	2.19	1.64	2.88	3.58	5.82	5.27	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.53	0.26	1.31	1.57	1.10	5.63	4.53	2.78	2.85	11.44	10.34	ns
8 mA	Std.	1.55	4.58	0.26	1.31	1.57	1.10	4.67	3.95	3.07	3.44	10.48	9.76	ns
12 mA	Std.	1.55	3.92	0.26	1.31	1.57	1.10	3.99	3.51	3.27	3.80	9.80	9.32	ns
16 mA	Std.	1.55	3.73	0.26	1.31	1.57	1.10	3.79	3.41	3.31	3.90	9.60	9.22	ns
24 mA	Std.	1.55	3.62	0.26	1.31	1.57	1.10	3.69	3.42	3.36	4.28	9.50	9.23	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.27	0.26	1.31	1.57	1.10	3.33	2.67	2.78	2.99	9.14	8.48	ns
8 mA	Std.	1.55	2.75	0.26	1.31	1.57	1.10	2.81	2.24	3.07	3.58	8.61	8.05	ns
12 mA	Std.	1.55	2.46	0.26	1.31	1.57	1.10	2.51	2.04	3.27	3.96	8.32	7.85	ns
16 mA	Std.	1.55	2.41	0.26	1.31	1.57	1.10	2.46	2.00	3.32	4.06	8.27	7.81	ns
24 mA	Std.	1.55	2.43	0.26	1.31	1.57	1.10	2.48	1.95	3.37	4.44	8.29	7.76	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Table 2-39 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

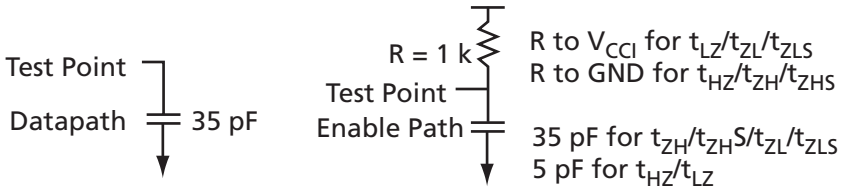


Figure 2-8 • AC Loading

Table 2-40 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	5

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-41 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	5.70	0.19	1.34	1.45	0.67	5.81	4.87	2.34	2.01	9.44	8.50	ns
8 mA	Std.	0.98	4.71	0.19	1.34	1.45	0.67	4.79	4.17	2.65	2.60	8.42	7.80	ns
12 mA	Std.	0.98	4.00	0.19	1.34	1.45	0.67	4.07	3.67	2.86	2.99	7.70	7.30	ns
16 mA	Std.	0.98	3.78	0.19	1.34	1.45	0.67	3.85	3.56	2.90	3.09	7.48	7.19	ns
24 mA	Std.	0.98	3.69	0.19	1.34	1.45	0.67	3.75	3.57	2.96	3.46	7.38	7.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-42 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	3.02	0.19	1.34	1.45	0.67	3.08	2.74	2.34	2.08	6.71	6.37	ns
8 mA	Std.	0.98	2.51	0.19	1.34	1.45	0.67	2.56	2.17	2.65	2.69	6.19	5.80	ns
12 mA	Std.	0.98	2.21	0.19	1.34	1.45	0.67	2.25	1.89	2.86	3.06	5.88	5.52	ns
16 mA	Std.	0.98	2.16	0.19	1.34	1.45	0.67	2.20	1.84	2.90	3.17	5.83	5.47	ns
24 mA	Std.	0.98	2.17	0.19	1.34	1.45	0.67	2.21	1.77	2.96	3.57	5.84	5.40	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-43 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	6.24	0.26	1.55	1.76	1.10	6.36	5.34	2.80	2.61	12.17	11.15	ns
8 mA	Std.	1.55	5.17	0.26	1.55	1.76	1.10	5.27	4.61	3.12	3.30	11.08	10.42	ns
12 mA	Std.	1.55	4.41	0.26	1.55	1.76	1.10	4.49	4.08	3.34	3.75	10.30	9.89	ns
16 mA	Std.	1.55	4.18	0.26	1.55	1.76	1.10	4.26	3.96	3.39	3.87	10.06	9.77	ns
24 mA	Std.	1.55	4.08	0.26	1.55	1.76	1.10	4.15	3.98	3.45	4.30	9.96	9.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-44 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.36	0.26	1.55	1.76	1.10	3.43	3.11	2.80	2.70	9.23	8.92	ns
8 mA	Std.	1.55	2.82	0.26	1.55	1.76	1.10	2.87	2.51	3.12	3.40	8.68	8.32	ns
12 mA	Std.	1.55	2.50	0.26	1.55	1.76	1.10	2.54	2.22	3.34	3.83	8.35	8.03	ns
16 mA	Std.	1.55	2.44	0.26	1.55	1.76	1.10	2.49	2.16	3.39	3.95	8.29	7.97	ns
24 mA	Std.	1.55	2.45	0.26	1.55	1.76	1.10	2.50	2.09	3.45	4.42	8.31	7.90	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-45 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	16	16	91	74	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

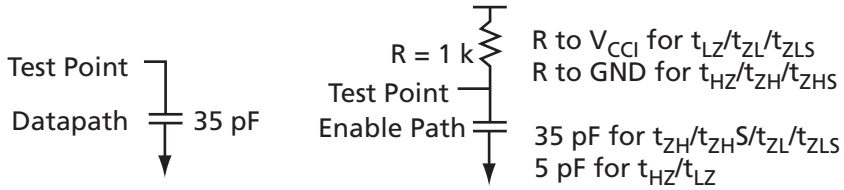


Figure 2-9 • AC Loading

Table 2-46 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	5

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-47 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	7.53	0.19	1.30	1.63	0.67	7.67	6.34	2.40	1.21	11.30	9.97	ns
4 mA	Std.	0.98	6.24	0.19	1.30	1.63	0.67	6.36	5.38	2.77	2.48	9.99	9.01	ns
6 mA	Std.	0.98	5.33	0.19	1.30	1.63	0.67	5.43	4.73	3.01	2.96	9.06	8.36	ns
8 mA	Std.	0.98	5.02	0.19	1.30	1.63	0.67	5.11	4.60	3.07	3.09	8.74	8.23	ns
12 mA	Std.	0.98	4.93	0.19	1.30	1.63	0.67	5.02	4.61	3.15	3.57	8.65	8.24	ns
16 mA	Std.	0.98	4.93	0.19	1.30	1.63	0.67	5.02	4.61	3.15	3.57	8.65	8.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-48 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	3.53	0.19	1.30	1.63	0.67	3.59	3.47	2.39	1.23	7.22	7.10	ns
4 mA	Std.	0.98	2.90	0.19	1.30	1.63	0.67	2.96	2.65	2.76	2.56	6.59	6.28	ns
6 mA	Std.	0.98	2.52	0.19	1.30	1.63	0.67	2.57	2.24	3.01	3.03	6.20	5.87	ns
8 mA	Std.	0.98	2.45	0.19	1.30	1.63	0.67	2.49	2.17	3.07	3.17	6.12	5.80	ns
12 mA	Std.	0.98	2.44	0.19	1.30	1.63	0.67	2.48	2.07	3.15	3.67	6.11	5.70	ns
16 mA	Std.	0.98	2.44	0.19	1.30	1.63	0.67	2.48	2.07	3.15	3.67	6.11	5.70	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-49 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.20	0.26	1.53	1.95	1.10	8.35	6.89	2.86	1.68	14.16	12.69	ns
4 mA	Std.	1.55	6.82	0.26	1.53	1.95	1.10	6.95	5.88	3.25	3.16	12.75	11.69	ns
6 mA	Std.	1.55	5.84	0.26	1.53	1.95	1.10	5.95	5.20	3.51	3.71	11.75	11.00	ns
8 mA	Std.	1.55	5.51	0.26	1.53	1.95	1.10	5.61	5.06	3.58	3.87	11.42	10.87	ns
12 mA	Std.	1.55	5.41	0.26	1.53	1.95	1.10	5.51	5.07	3.66	4.42	11.32	10.88	ns
16 mA	Std.	1.55	5.41	0.26	1.53	1.95	1.10	5.51	5.07	3.66	4.42	11.32	10.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-50 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.91	0.26	1.53	1.95	1.10	3.98	3.88	2.85	1.70	9.79	9.68	ns
4 mA	Std.	1.55	3.24	0.26	1.53	1.95	1.10	3.30	3.01	3.24	3.25	9.11	8.82	ns
6 mA	Std.	1.55	2.83	0.26	1.53	1.95	1.10	2.88	2.58	3.51	3.80	8.69	8.39	ns
8 mA	Std.	1.55	2.75	0.26	1.53	1.95	1.10	2.80	2.51	3.57	3.95	8.61	8.31	ns
12 mA	Std.	1.55	2.74	0.26	1.53	1.95	1.10	2.79	2.41	3.66	4.54	8.60	8.21	ns
16 mA	Std.	1.55	2.74	0.26	1.53	1.95	1.10	2.79	2.41	3.66	4.54	8.60	8.21	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-51 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	25	33	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	32	39	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	66	55	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	66	55	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

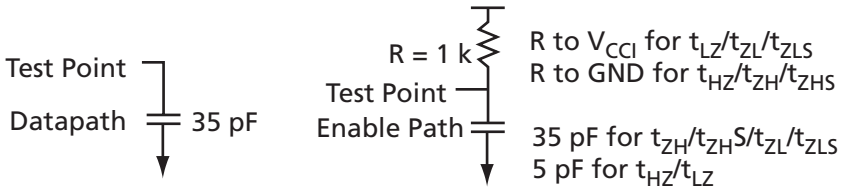


Figure 2-10 • AC Loading

Table 2-52 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	5

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-53 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	7.82	0.19	1.50	1.82	0.67	7.97	6.49	2.89	2.41	11.60	10.12	ns
4 mA	Std.	0.98	6.72	0.19	1.50	1.82	0.67	6.84	5.71	3.17	2.96	10.47	9.34	ns
6 mA	Std.	0.98	6.32	0.19	1.50	1.82	0.67	6.44	5.56	3.24	3.11	10.07	9.19	ns
8 mA	Std.	0.98	6.24	0.19	1.50	1.82	0.67	6.36	5.56	3.33	3.66	9.99	9.19	ns
12 mA	Std.	0.98	6.24	0.19	1.50	1.82	0.67	6.36	5.56	3.33	3.66	9.99	9.19	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-54 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	3.34	0.19	1.50	1.82	0.67	3.41	3.07	2.88	2.50	7.04	6.70	ns
4 mA	Std.	0.98	2.88	0.19	1.50	1.82	0.67	2.94	2.57	3.17	3.05	6.57	6.20	ns
6 mA	Std.	0.98	3.90	0.19	1.50	1.82	0.67	3.97	3.79	3.17	3.20	7.60	7.42	ns
8 mA	Std.	0.98	2.77	0.19	1.50	1.82	0.67	2.82	2.35	3.33	3.78	6.45	5.98	ns
12 mA	Std.	0.98	2.77	0.19	1.50	1.82	0.67	2.82	2.35	3.33	3.78	6.45	5.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-55 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.51	0.26	1.72	2.15	1.10	8.67	7.05	3.38	3.07	14.48	12.86	ns
4 mA	Std.	1.55	7.33	0.26	1.72	2.15	1.10	7.47	6.22	3.69	3.71	13.27	12.03	ns
6 mA	Std.	1.55	6.90	0.26	1.72	2.15	1.10	7.03	6.07	3.75	3.88	12.84	11.88	ns
8 mA	Std.	1.55	6.82	0.26	1.72	2.15	1.10	6.95	6.07	3.86	4.52	12.75	11.88	ns
12 mA	Std.	1.55	6.82	0.26	1.72	2.15	1.10	6.95	6.07	3.86	4.52	12.75	11.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-56 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.71	0.26	1.72	2.15	1.10	3.78	3.46	3.37	3.18	9.59	9.26	ns
4 mA	Std.	1.55	3.22	0.26	1.72	2.15	1.10	3.28	2.92	3.68	3.81	9.09	8.73	ns
6 mA	Std.	1.55	4.30	0.26	1.72	2.15	1.10	4.38	4.21	3.69	4.00	10.19	10.02	ns
8 mA	Std.	1.55	3.09	0.26	1.72	2.15	1.10	3.15	2.70	3.85	4.66	8.96	8.51	ns
12 mA	Std.	1.55	3.09	0.26	1.72	2.15	1.10	3.15	2.70	3.85	4.66	8.96	8.51	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-57 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

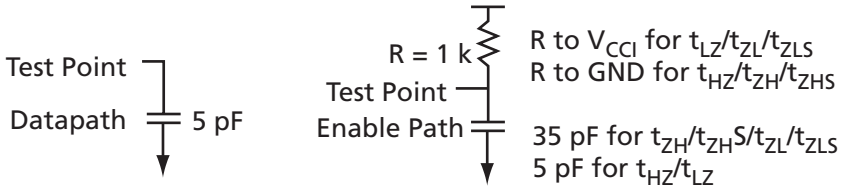


Figure 2-11 • AC Loading

Table 2-58 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-59 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	9.93	0.26	2.06	2.96	1.10	9.50	7.45	3.68	4.03	15.10	13.05	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-60 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.07	0.26	2.06	2.96	1.10	3.90	3.43	3.80	4.02	9.49	9.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-61 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 2-12.

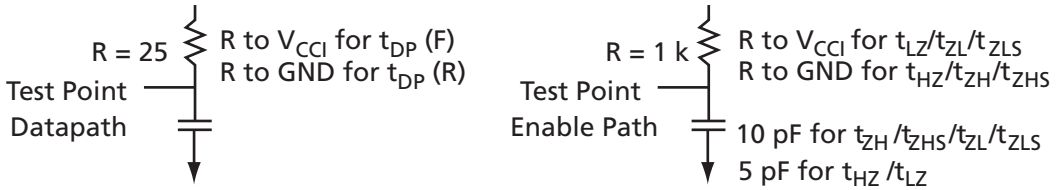


Figure 2-12 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-62.

Table 2-62 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	–	10

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-63 • 3.3 V PCI/PCI-X – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.44	0.19	0.98	1.45	0.67	2.49	1.84	2.79	3.17	6.12	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-64 • 3.3 V PCI/PCI-X – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.74	0.26	1.19	1.63	1.10	2.80	2.16	3.28	3.96	8.60	7.97	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-65 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

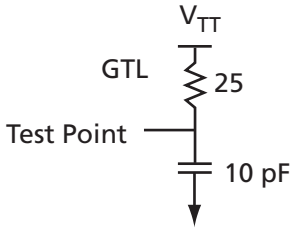


Figure 2-13 • AC Loading

Table 2-66 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-67 • 3.3 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.83	0.19	2.41	0.67	1.84	1.83			5.47	5.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-68 • 3.3 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.09	0.26	2.75	1.10	2.10	2.09			7.91	7.89	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-69 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

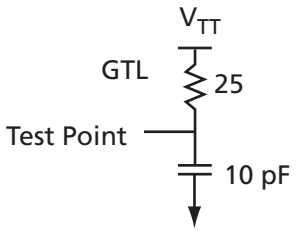


Figure 2-14 • AC Loading

Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-71 • 2.5 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.90	0.19	2.04	0.67	1.94	1.87			5.57	5.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-72 • 2.5 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.16	0.26	2.35	1.10	2.20	2.13			8.01	7.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V

Table 2-73 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
35 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

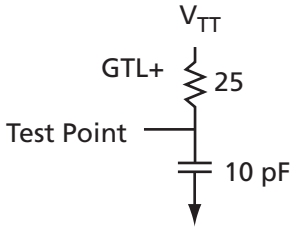


Figure 2-15 • AC Loading

Table 2-74 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-75 • 3.3 V GTL+ – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.85	0.19	1.35	0.67	1.88	1.81			5.51	5.44	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-76 • 3.3 V GTL+ – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.11	0.26	1.61	1.10	2.15	2.07			7.95	7.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-77 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
33 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	33	33	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

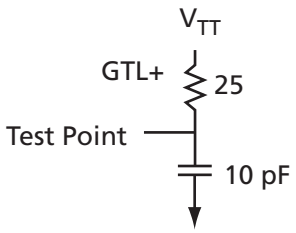


Figure 2-16 • AC Loading

Table 2-78 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-79 • 2.5 V GTL+ – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.97	0.19	1.29	0.67	2.00	1.84			5.63	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-80 • 2.5 V GTL+ – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.23	0.26	1.55	1.10	2.28	2.11			8.08	7.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-81 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	8	8	32	39	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

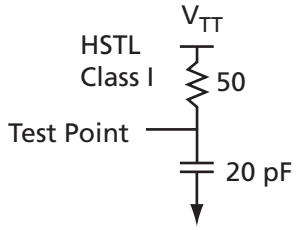


Figure 2-17 • AC Loading

Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

** Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-83 • HSTL Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.74	0.19	1.77	0.67	2.79	2.73			6.42	6.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-84 • HSTL Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	3.10	0.26	1.94	1.10	3.12	3.10			8.93	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-85 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
15 mA[3]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	15	15	66	55	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

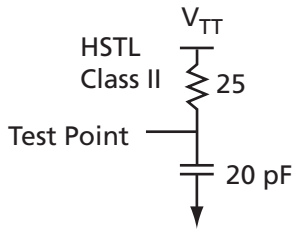


Figure 2-18 • AC Loading

Table 2-86 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-87 • HSTL Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.62	0.19	1.77	0.67	2.66	2.40			6.29	6.03	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-88 • HSTL Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.93	0.26	1.94	1.10	2.98	2.75			8.79	8.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
15 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} – 0.62	15	15	83	87	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

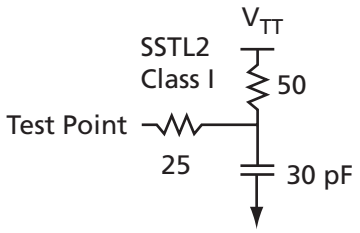


Figure 2-19 • AC Loading

Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-91 • SSTL 2 Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.91	0.19	1.15	0.67	1.94	1.72			5.57	5.35	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-92 • SSTL 2 Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.17	0.26	1.39	1.10	2.21	2.04			8.02	7.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-93 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
18 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

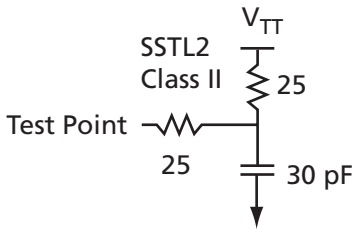


Figure 2-20 • AC Loading

Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-95 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.94	0.19	1.15	0.67	1.97	1.66			5.60	5.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-96 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.20	0.26	1.39	1.10	2.24	1.97			8.05	7.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-97 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
14 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14	54	51	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

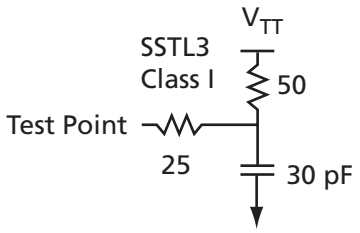


Figure 2-21 • AC Loading

Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-99 • SSTL 3 Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.05	0.19	1.09	0.67	2.09	1.71			5.72	5.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-100 • SSTL 3 Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.32	0.26	1.32	1.10	2.37	2.02			8.17	7.83	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-101 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
21 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} - 0.9	21	21	103	109	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

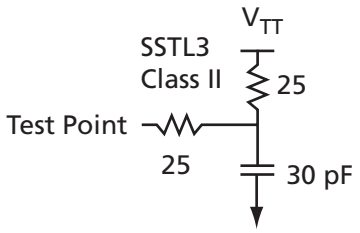


Figure 2-22 • AC Loading

Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-103 • SSTL 3 Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.86	0.19	1.09	0.67	1.89	1.58			5.52	5.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-104 • SSTL 3 Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.12	0.26	1.32	1.10	2.16	1.89			7.97	7.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-23. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOOe also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

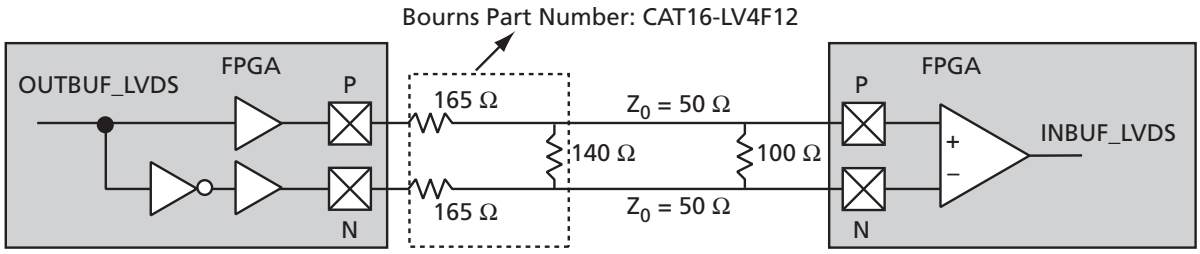


***Figure 2-23* • LVDS Circuit Diagram and Board-Level Implementation**

Table 2-105 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output LOW Voltage	0.9	1.075	1.25	V
V_{OH}	Output HIGH Voltage	1.25	1.425	1.6	V
I_{OL} [4]	Output Lower Current	0.65	0.91	1.16	mA
I_{OH} [4]	Output HIGH Current	0.65	0.91	1.16	mA
V_I	Input Voltage	0		2.925	V
I_{IH} [3]	Input HIGH Leakage Current			10	µA
I_{IL} [3]	Input LOW Leakage Current			10	µA
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common-Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common-Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350		mV

Notes:

1. *± 5%*
2. *Differential input voltage = ±350 mV*
3. *Currents are measured at 85°C junction temperature.*
4. *I_{OL}/I_{OH} is defined by V_{ODIFF}/(resistor network).*

Table 2-106 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-107 • LVDS – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.98	1.77	0.19	1.62	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-108 • LVDS – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.19	0.26	1.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-24. The input and output buffer delays are available in the LVDS section in Table 2-107 on page 2-64 and Table 2-108 on page 2-64.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

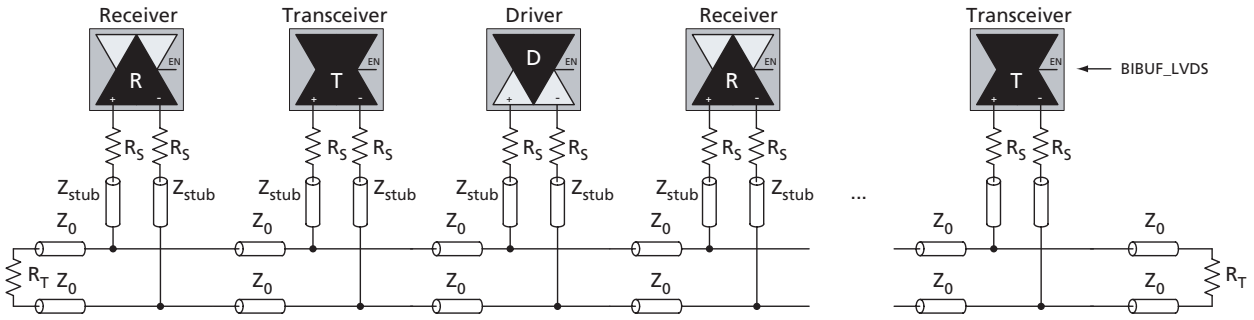


Figure 2-24 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-25. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

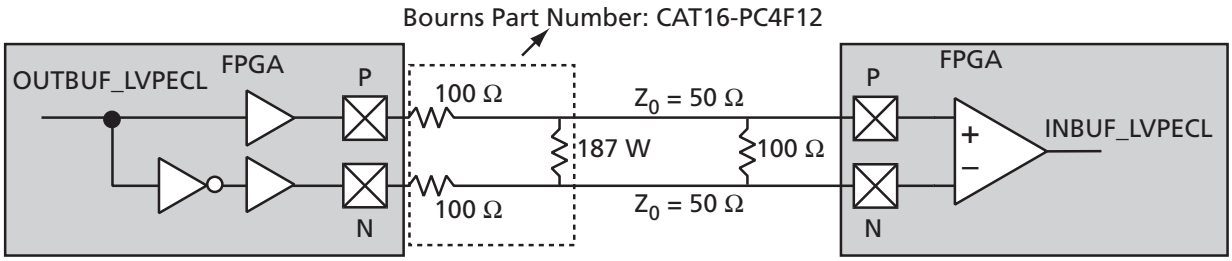


Figure 2-25 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-109 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-110 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

* *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-111 • LVPECL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.98	1.75	0.19	1.45	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-112 • LVPECL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.16	0.26	1.70	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

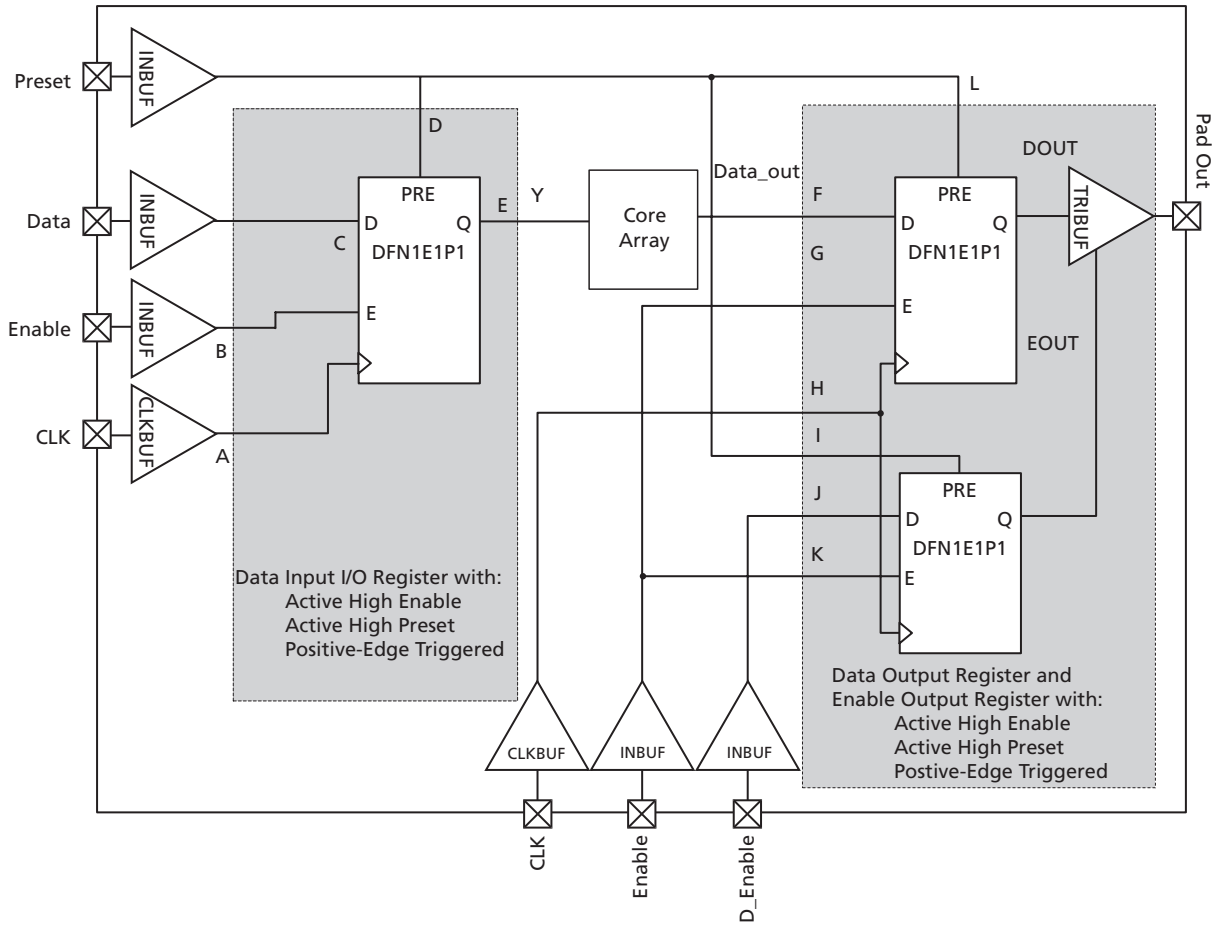


Figure 2-26 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-113 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

** See Figure 2-26 on page 2-67 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

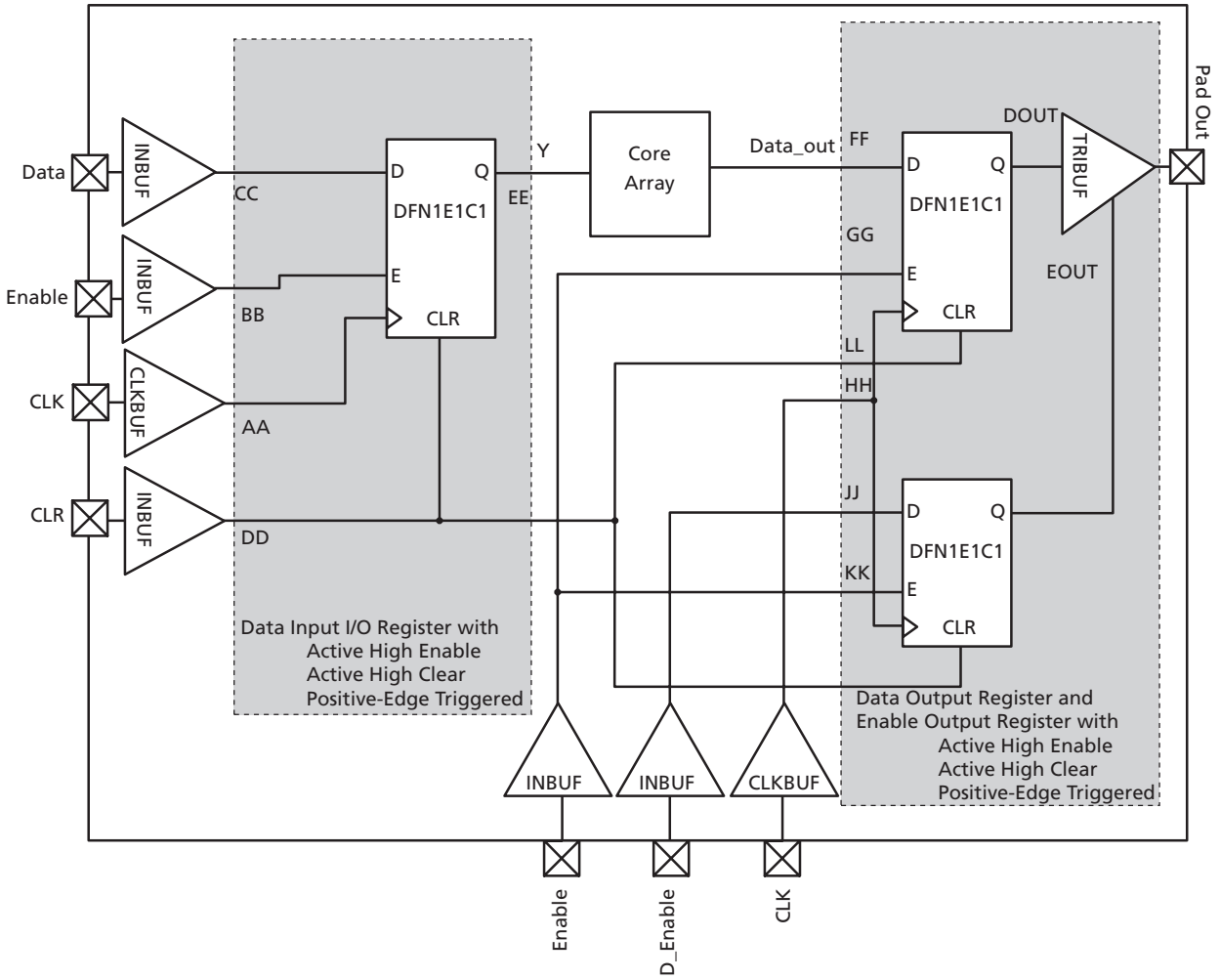


Figure 2-27 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-114 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-27 on page 2-69 for more information.*

Input Register

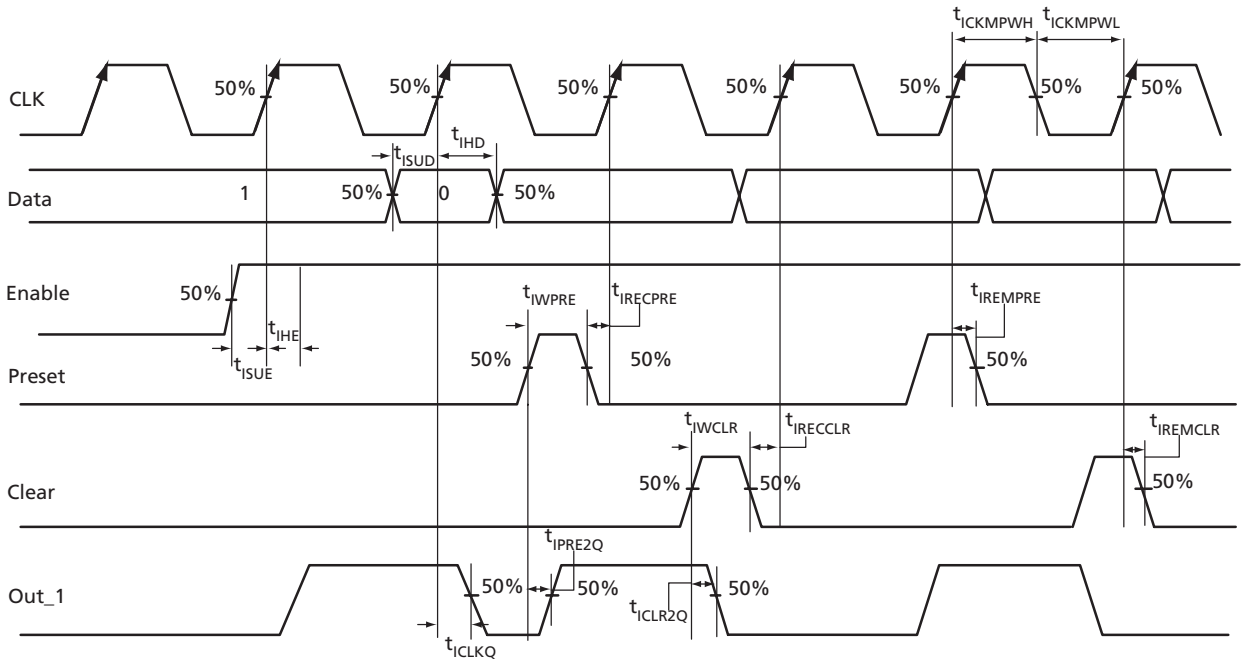


Figure 2-28 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-115 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-116 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.97	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	1.02	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Output Register

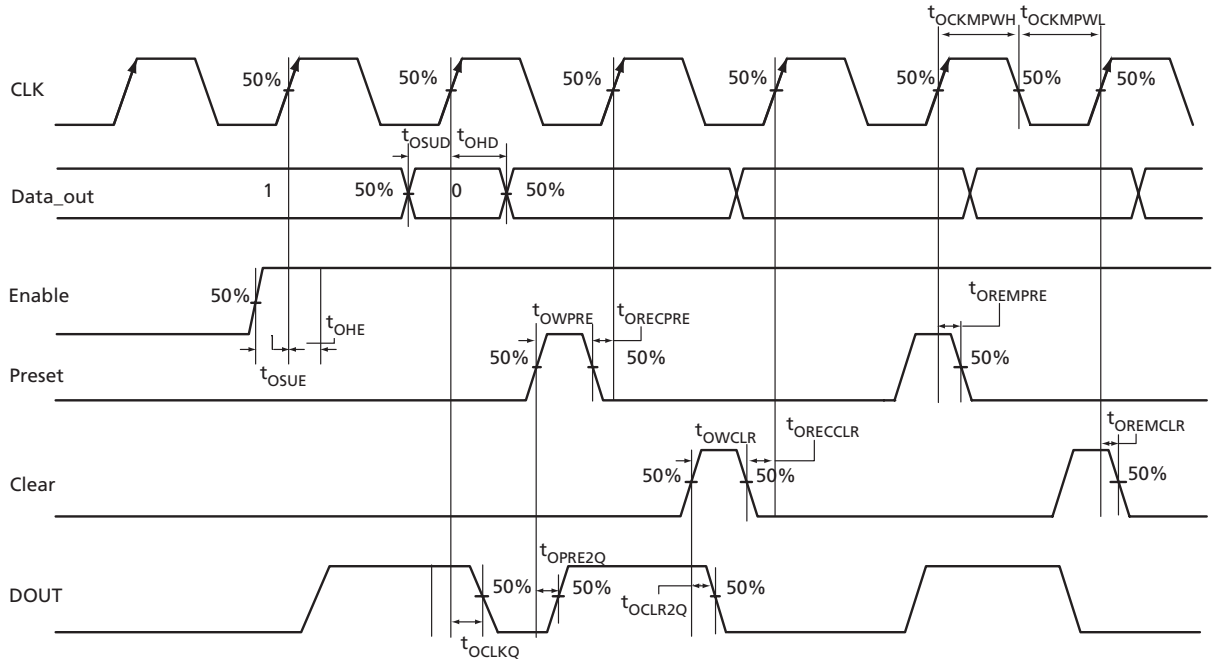


Figure 2-29 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-117 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-118 • Output Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	1.11	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Output Enable Register

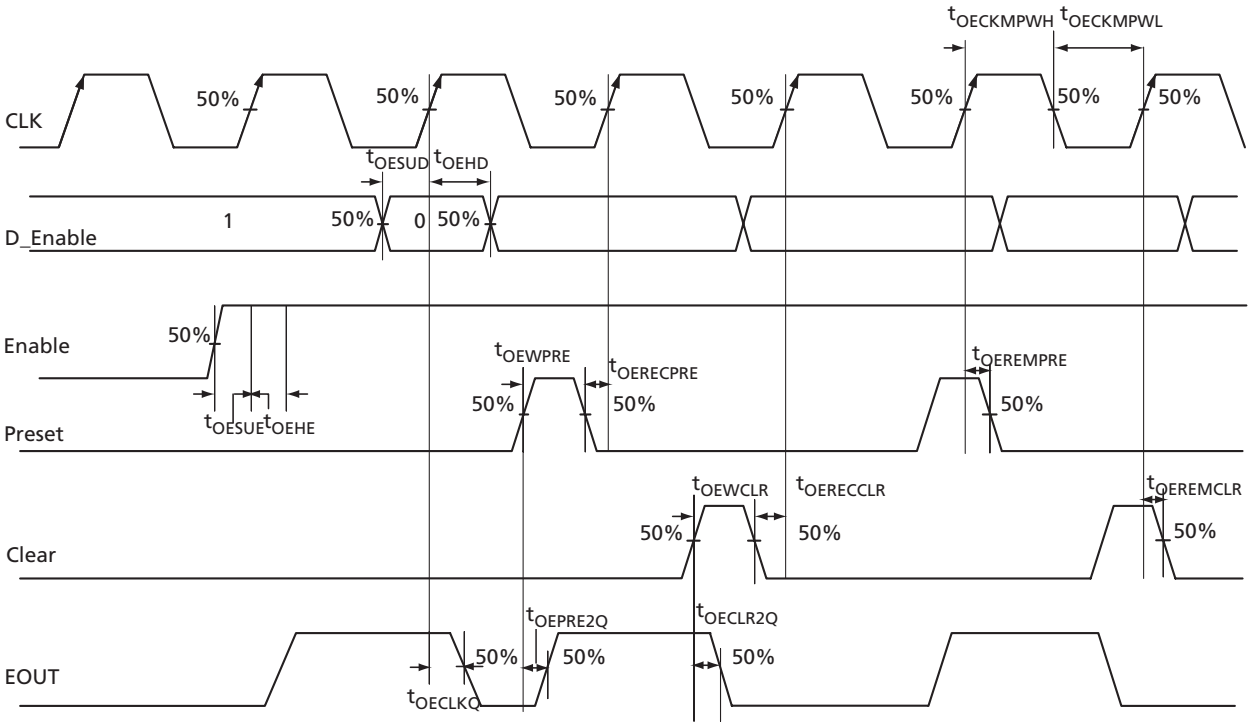


Figure 2-30 • **Output Enable Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-119 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.73	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-120 • Output Enable Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

DDR Module Specifications

Input DDR Module

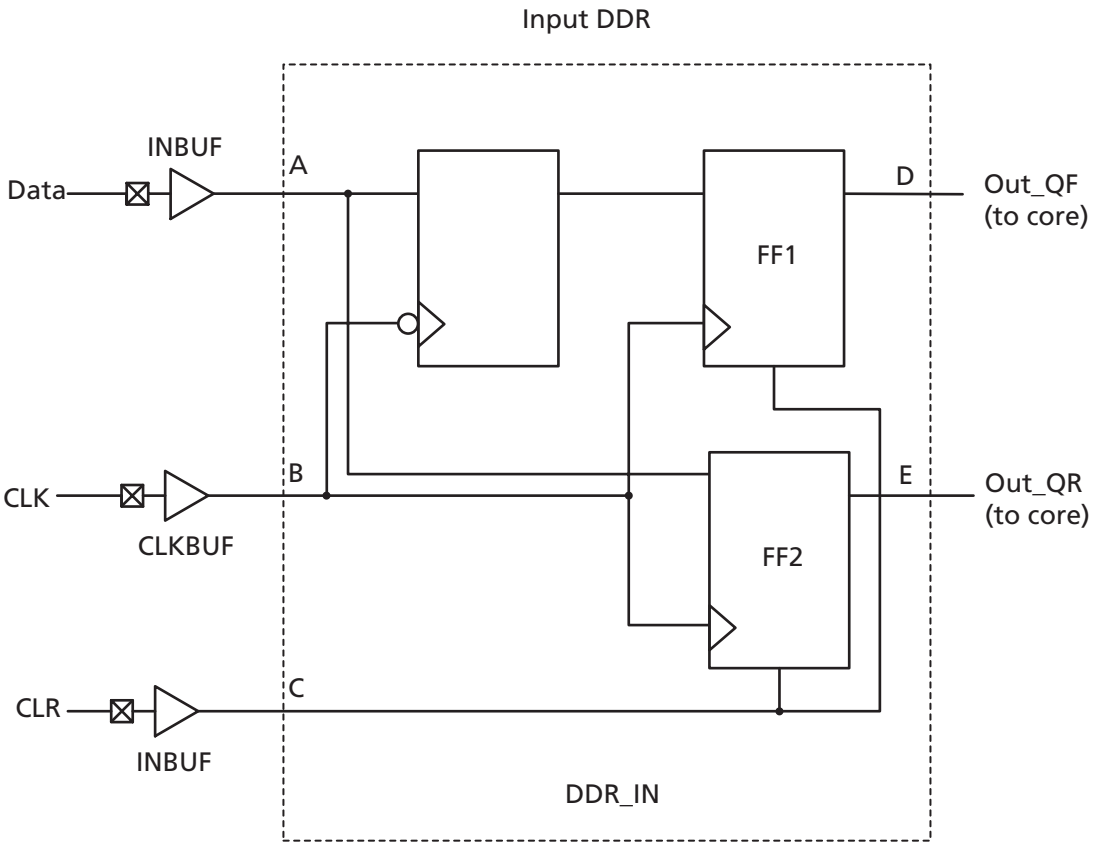


***Figure 2-31* • Input DDR Timing Model**

***Table 2-121* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

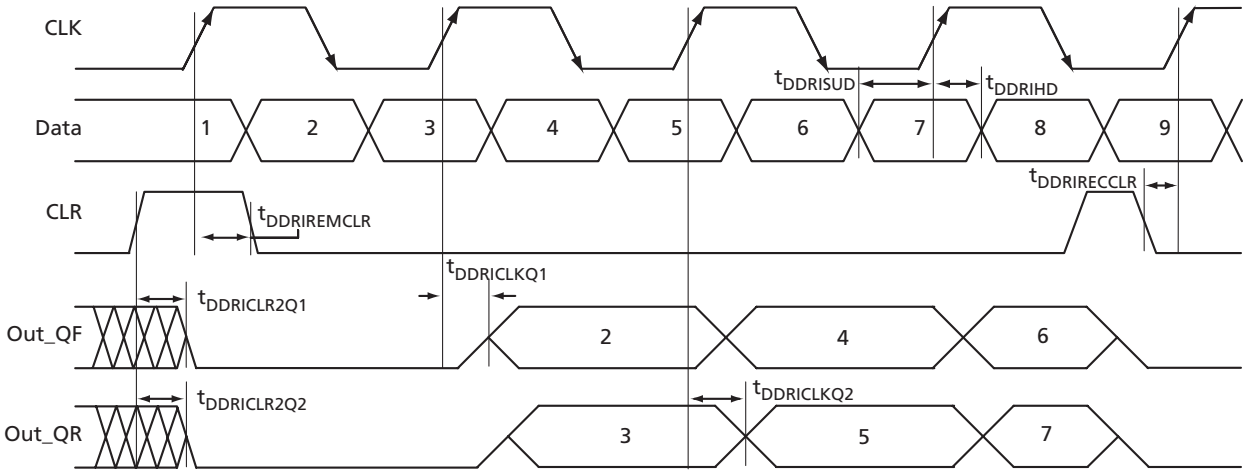


Figure 2-32 • **Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-122 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR		MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-123 • Input DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR		MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Output DDR Module

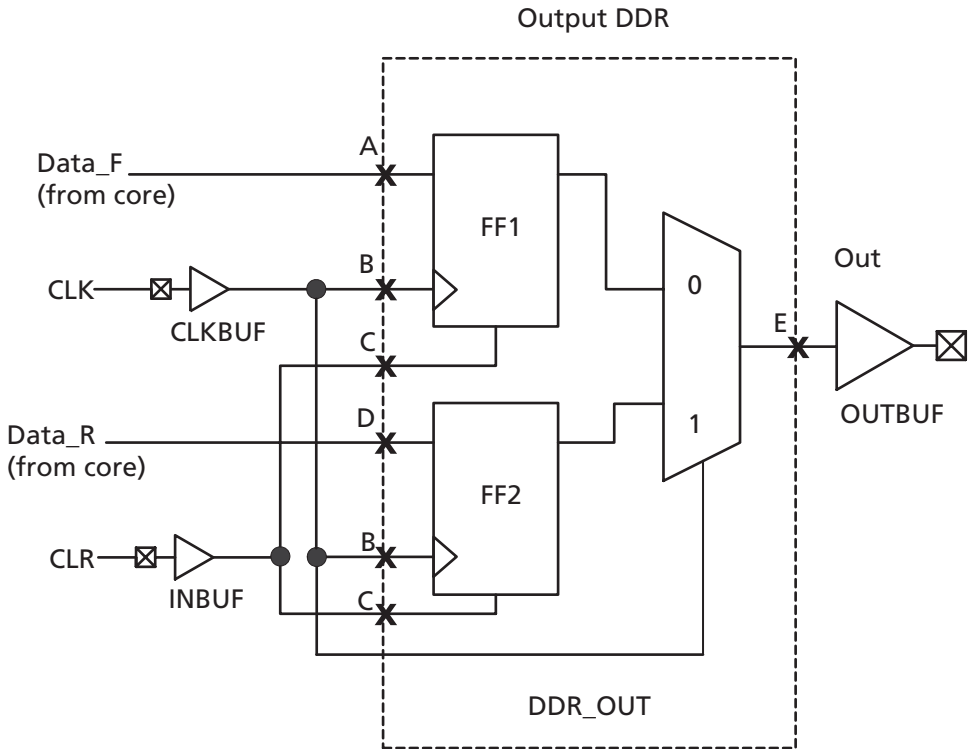


Figure 2-33 • **Output DDR Timing Model**

Table 2-124 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

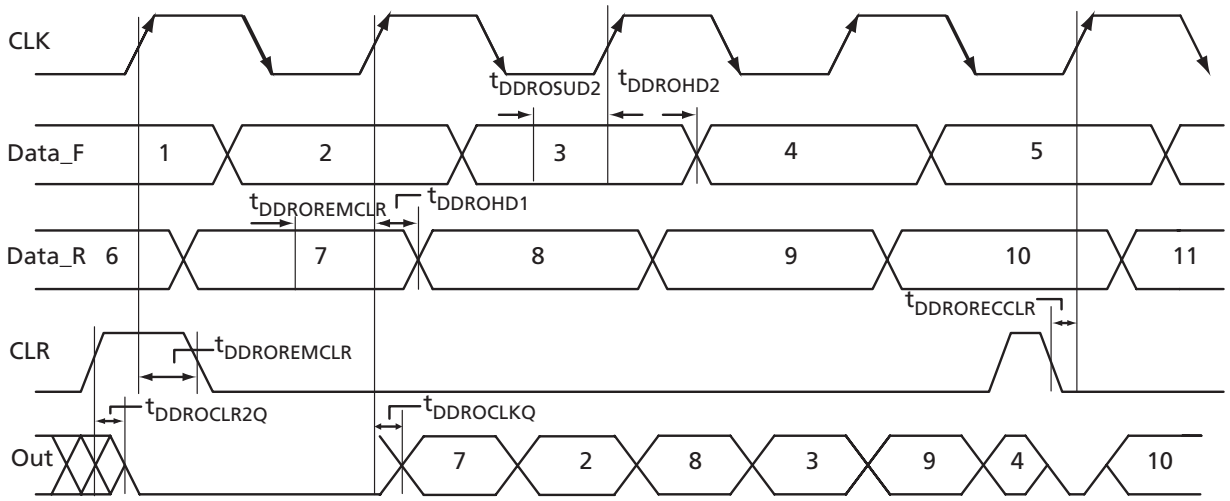


Figure 2-34 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-125 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR		MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-126 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR		MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOOe library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

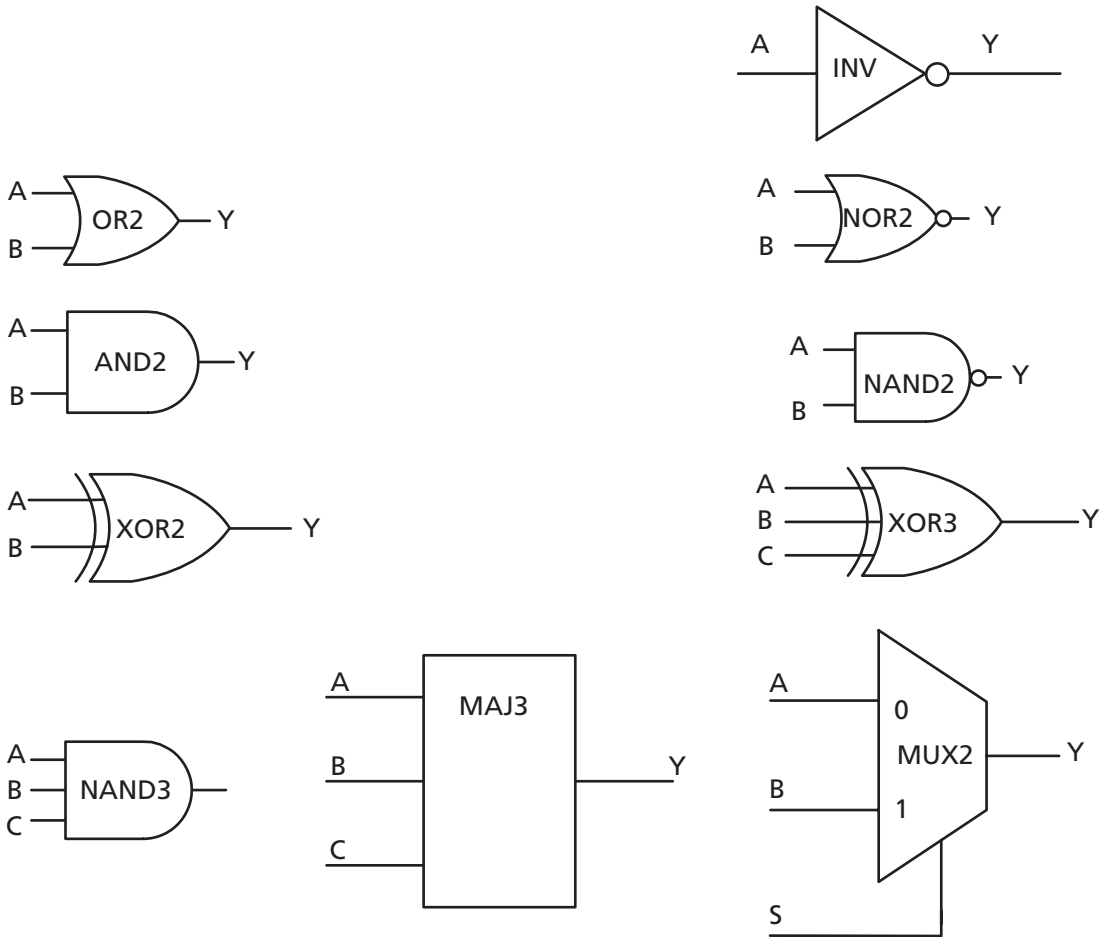


Figure 2-35 • **Sample of Combinatorial Cells**

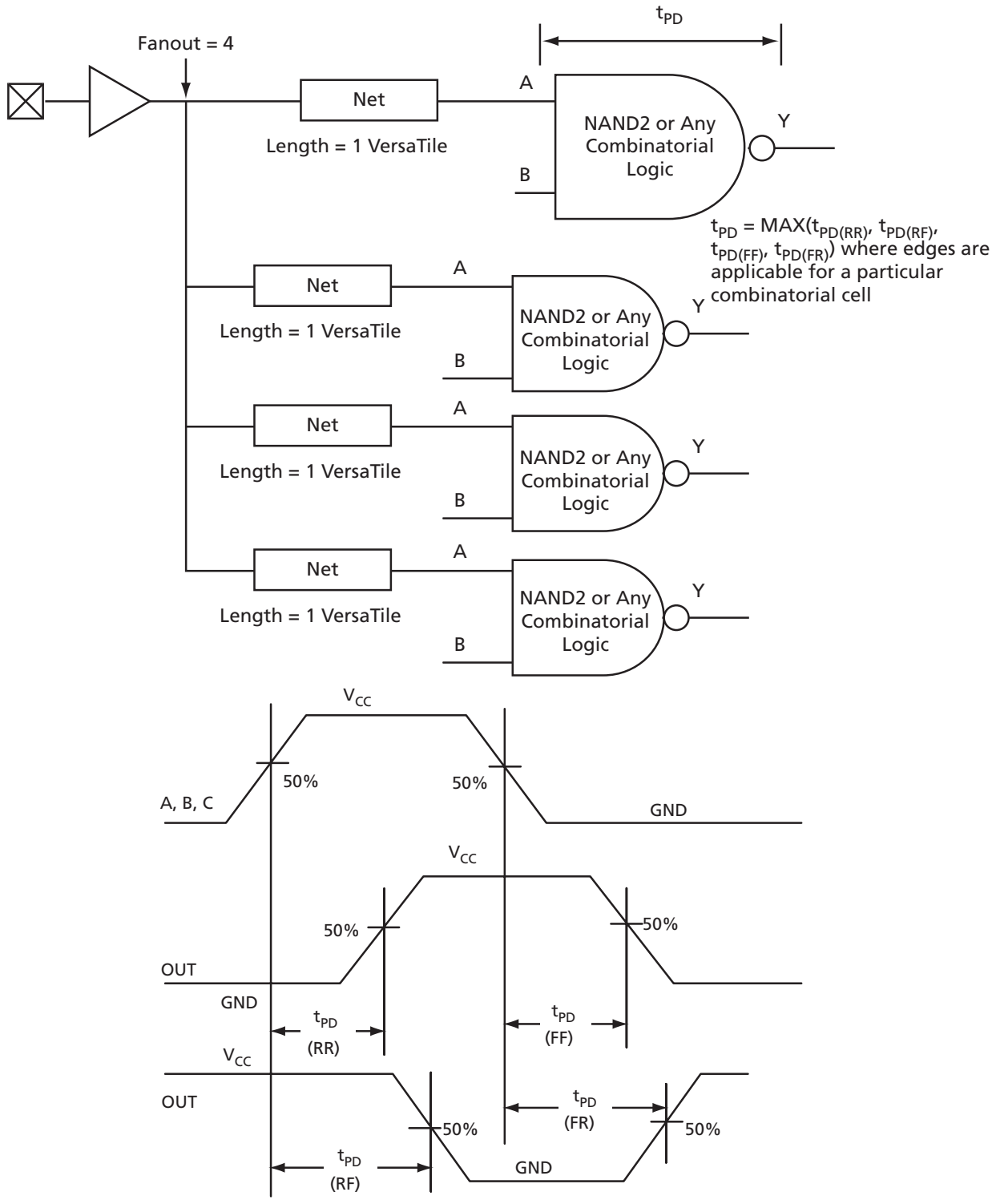


Figure 2-36 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-127 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y = !(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	Y = A ⊕ B	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	1.33	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-128 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.35	ns
AND2	Y = A · B	t_{PD}	1.42	ns
NAND2	Y = !(A · B)	t_{PD}	1.58	ns
OR2	Y = A + B	t_{PD}	2.10	ns
NOR2	Y = !(A + B)	t_{PD}	1.94	ns
XOR2	Y = A ⊕ B	t_{PD}	2.33	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	2.34	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.05	ns
MUX2	Y = A !S + B S	t_{PD}	2.64	ns
AND3	Y = A · B · C	t_{PD}	2.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The IGLOOe library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

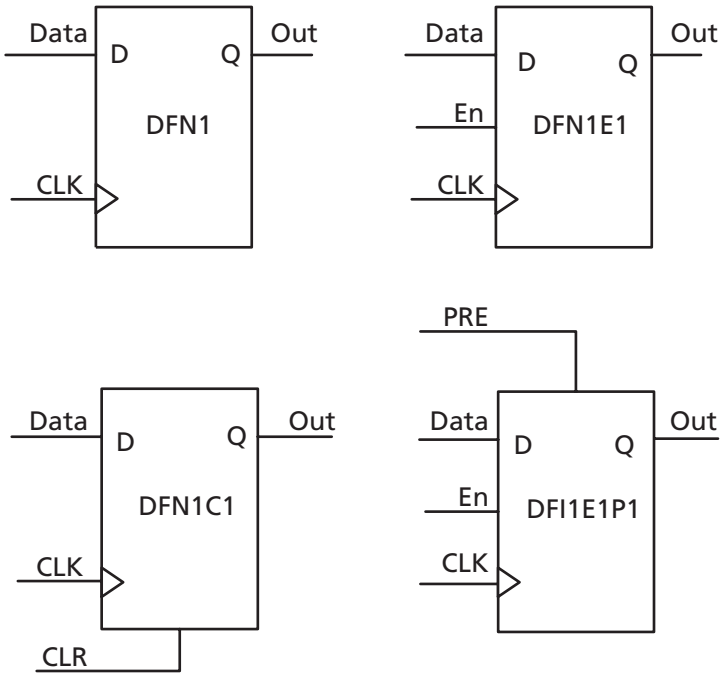


Figure 2-37 • **Sample of Sequential Cells**

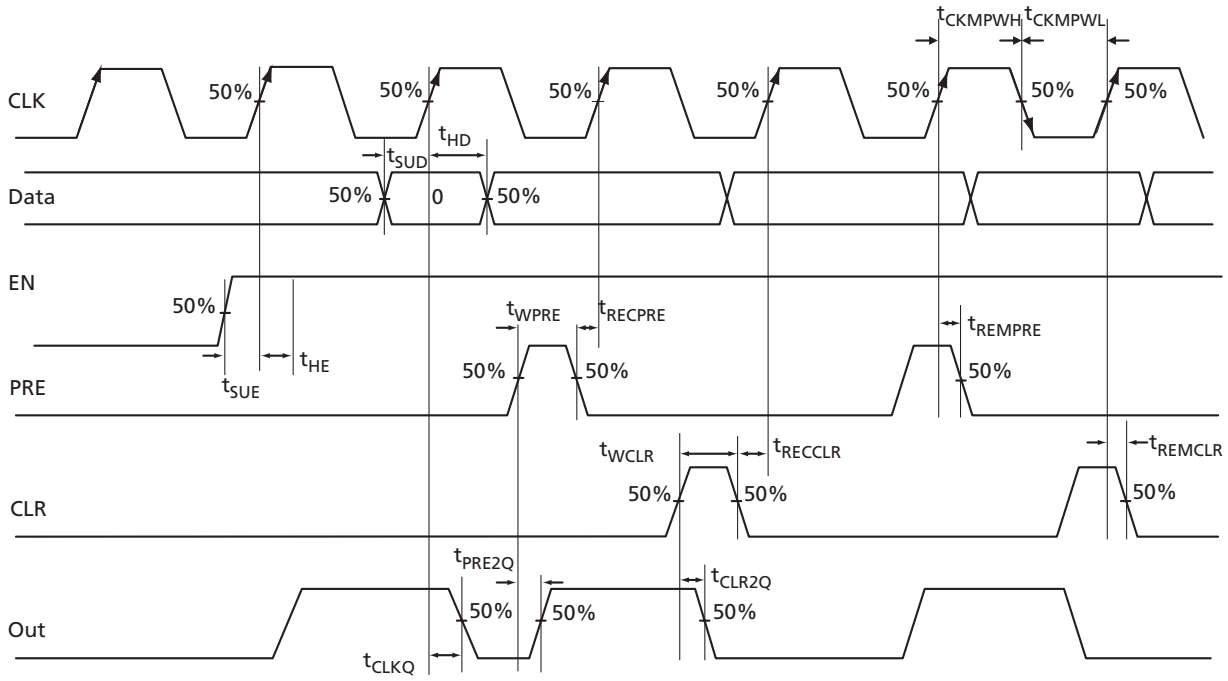


Figure 2-38 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-129 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-130 • Register Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Global Resource Characteristics

AGLE600 Clock Tree Topology

Clock delays are device-specific. Figure 2-39 is an example of a global tree used for clock routing. The global tree presented in Figure 2-39 is driven by a CCC located on the west side of the AGLE600 device. It is used to drive all D-flip-flops in the device.

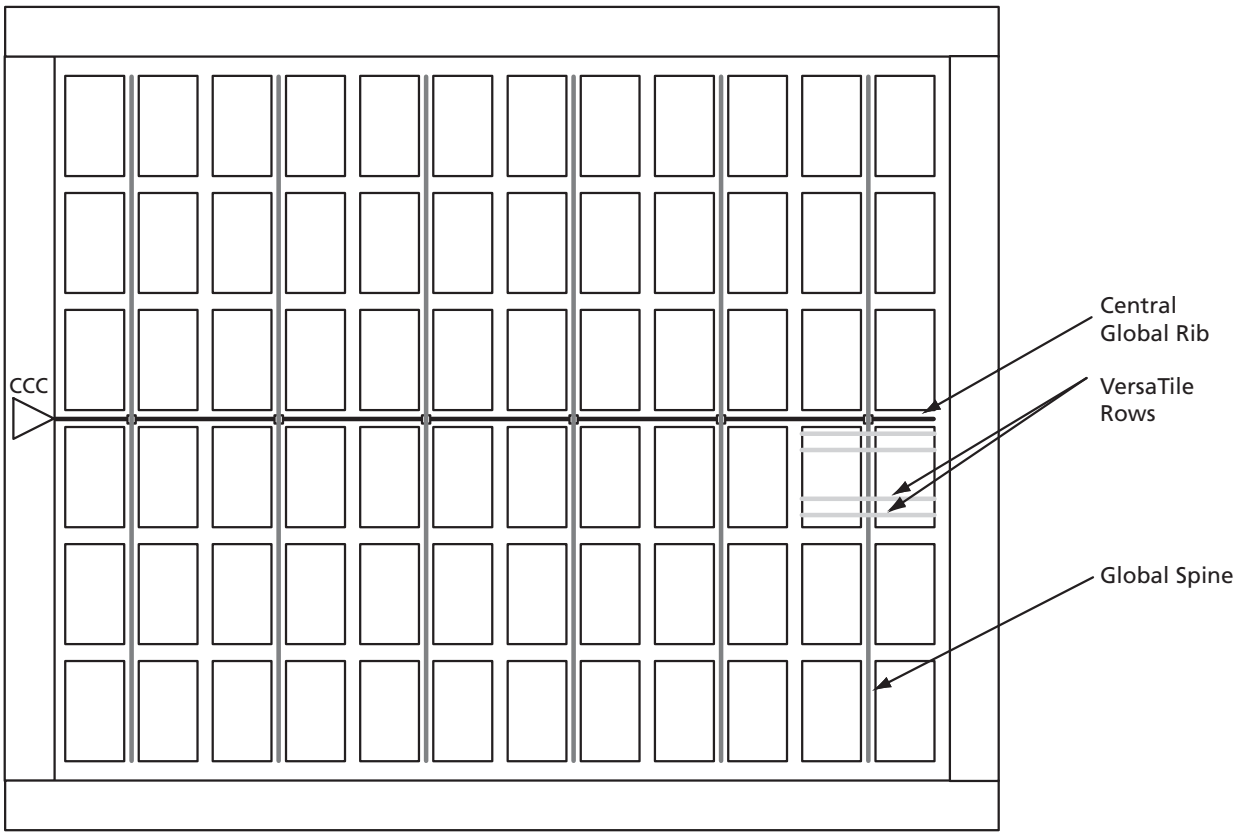


***Figure 2-39* • Example of Global Tree Use in an AGLE600 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-92. Table 2-131 and Table 2-133 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-131* • AGLE600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-132* • AGLE3000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.00	2.34	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.09	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-133 • AGLE600 Global Resource
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-134 • AGLE3000 Global Resource
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.83	3.27	ns
t_{RCKH}	Input HIGH Delay for Global Clock	3.00	3.61	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-135 • **IGLOOe CCC/PLL Specification**
For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Serial Clock (SCLK) for Dynamic PLL[3]			100	ps
Delay Increments in Programmable Delay Blocks[1, 2]		360		
Number of Programmable Values in Each Programmable Delay Block			32	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 250 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2, 4]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2, 4]	0.025		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns

Notes:

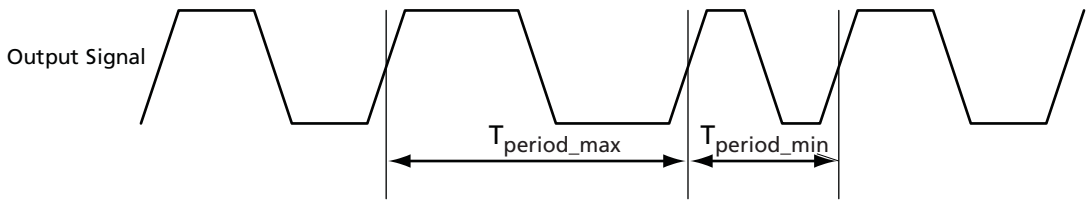
1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *Maximum value obtained for a Std. speed grade device in Worst Case Commercial Conditions.For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
4. *For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the Clock Conditioning Circuits in IGLOO and ProASIC3 Devices chapter of the handbook.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*

Table 2-136 • IGLOOe CCC/PLL Specification
For IGLOOe V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Serial Clock (SCLK) for Dynamic PLL[4]			60	ps
Delay Increments in Programmable Delay Blocks[1, 2]		580		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 160 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]		5.7		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-40 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

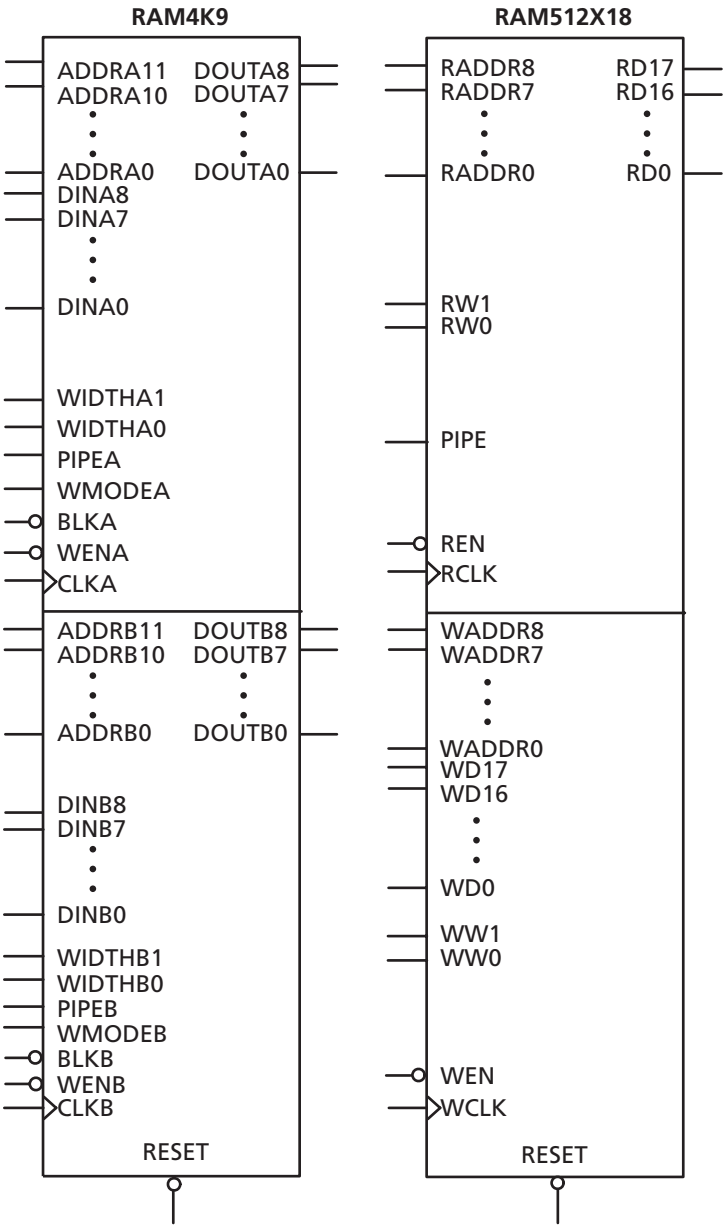


Figure 2-41 • **RAM Models**

Timing Waveforms

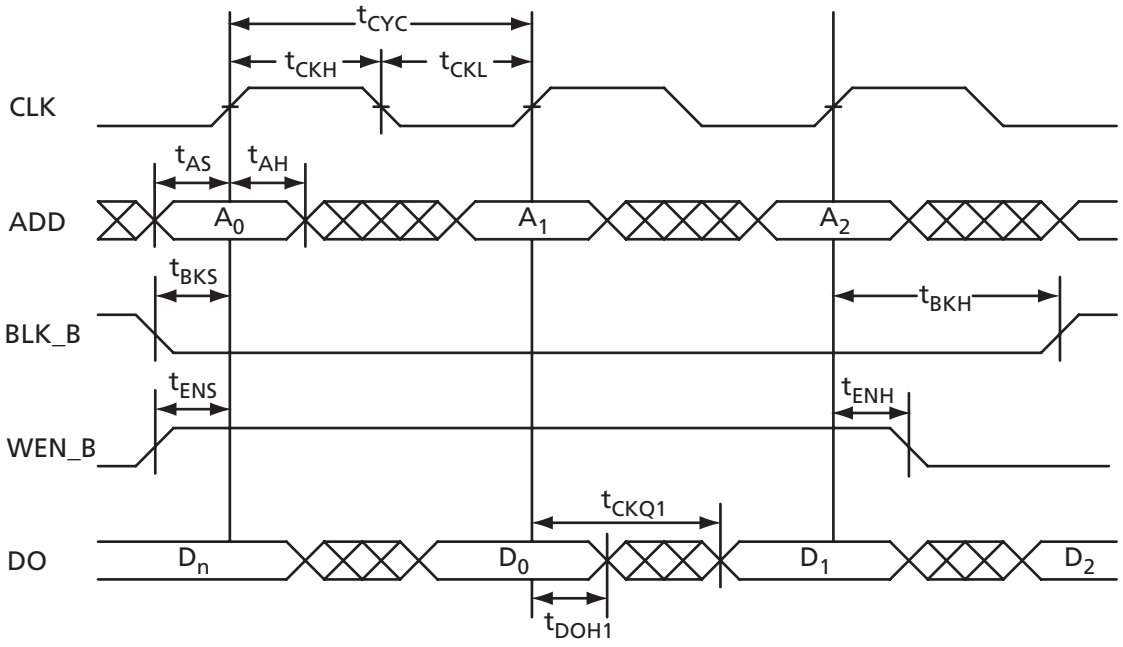


Figure 2-42 • **RAM Read for Pass-Through Output**

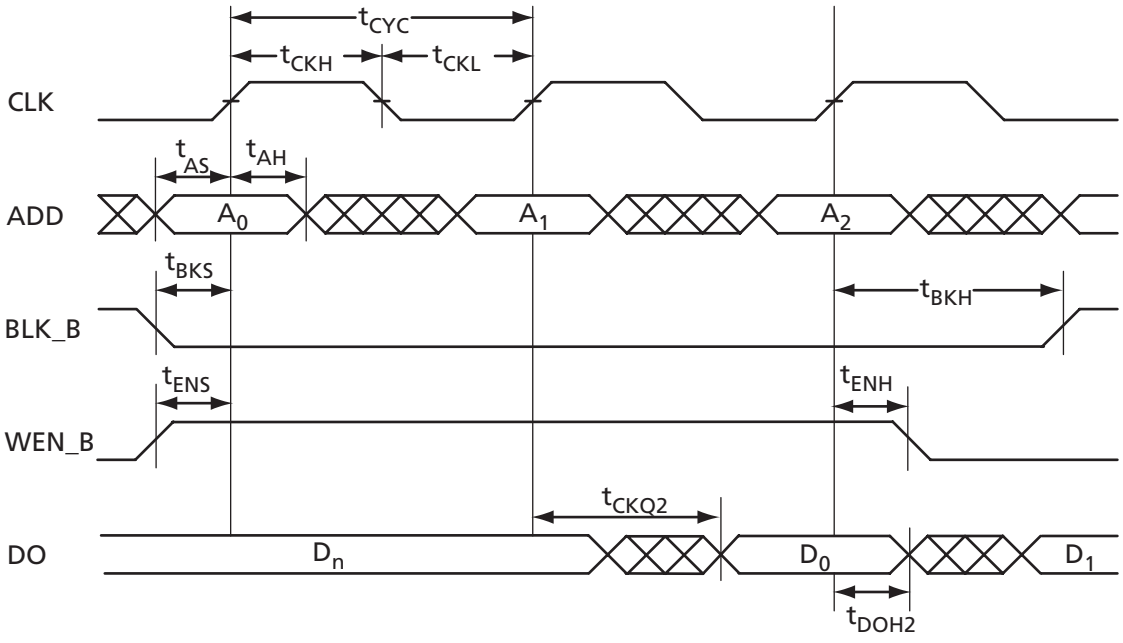


Figure 2-43 • **RAM Read for Pipelined Output**

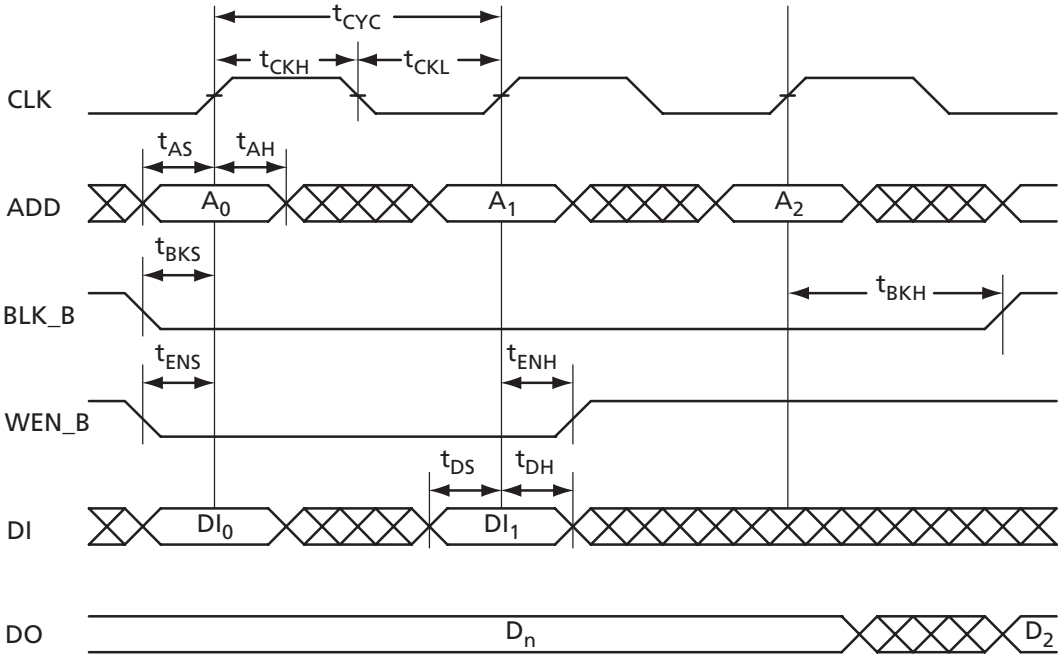


Figure 2-44 • **RAM Write, Output Retained (WMODE = 0)**

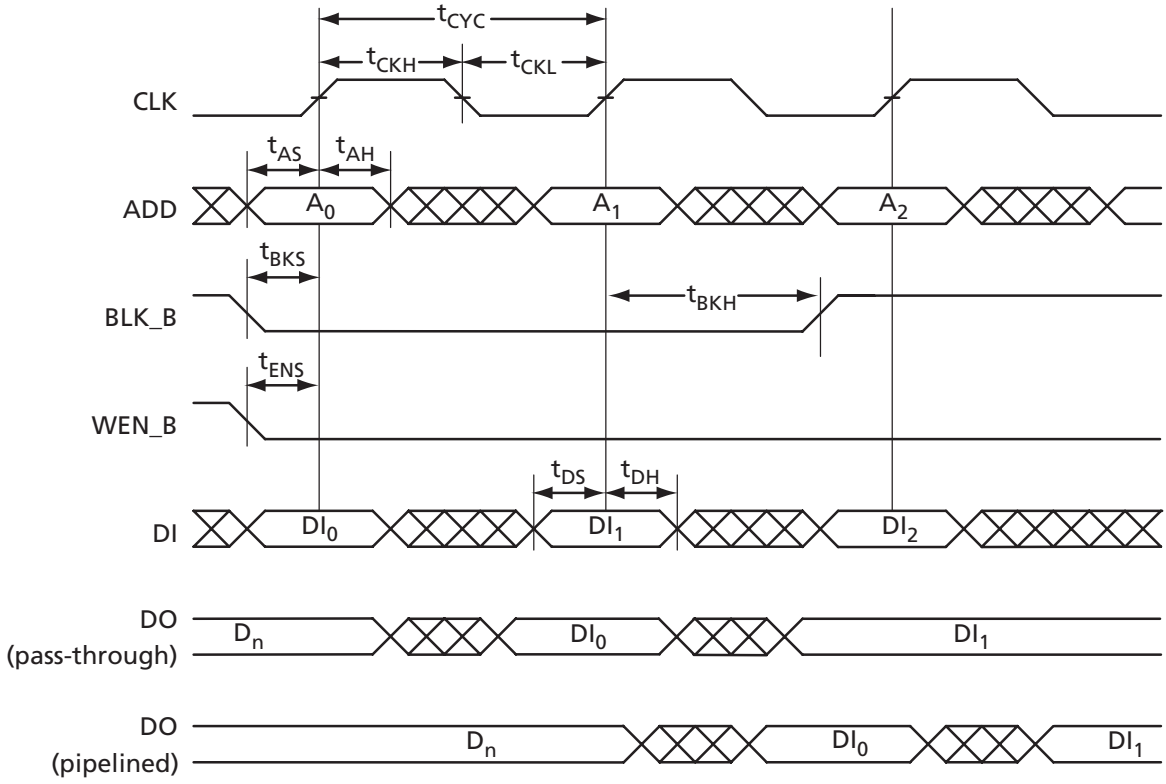


Figure 2-45 • **RAM Write, Output as Write Data (WMODE = 1)**

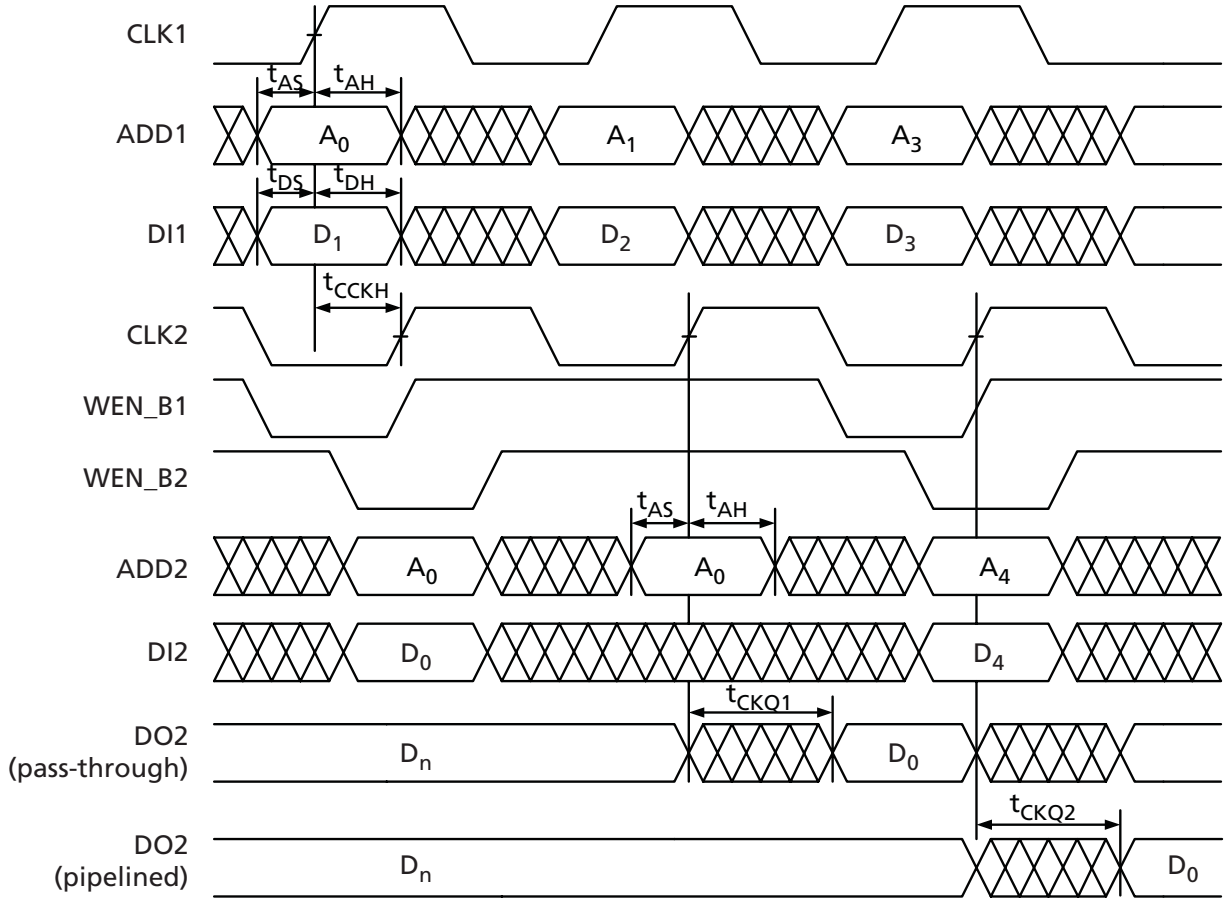


Figure 2-46 • **Write Access after Write onto Same Address**

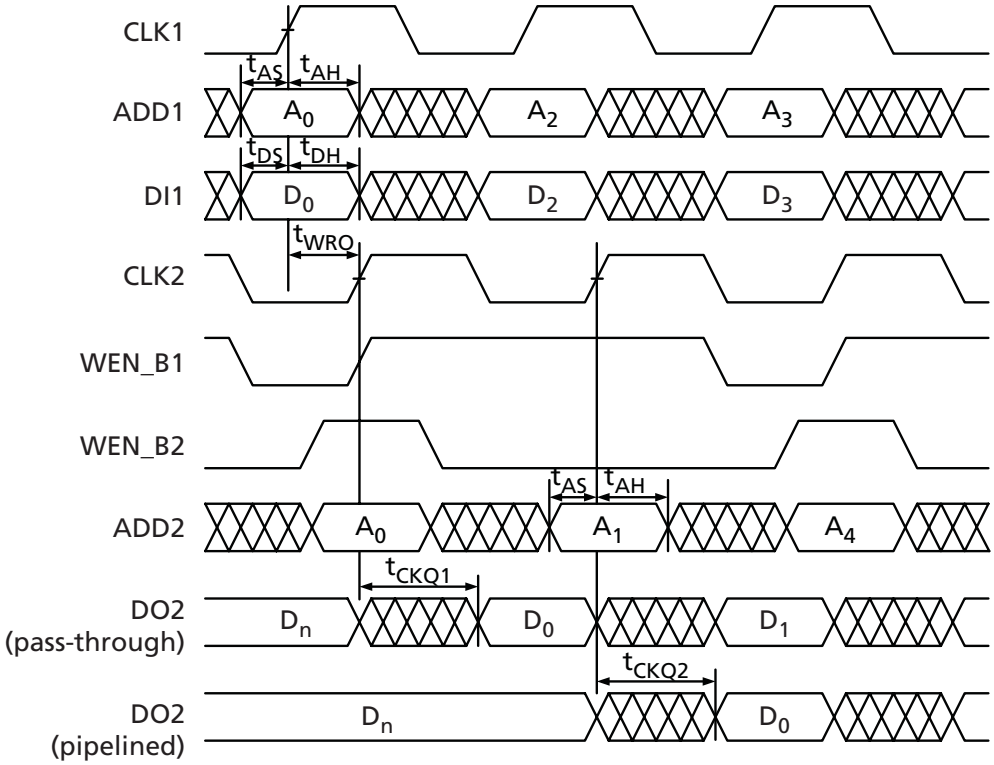


Figure 2-47 • **Read Access after Write onto Same Address**

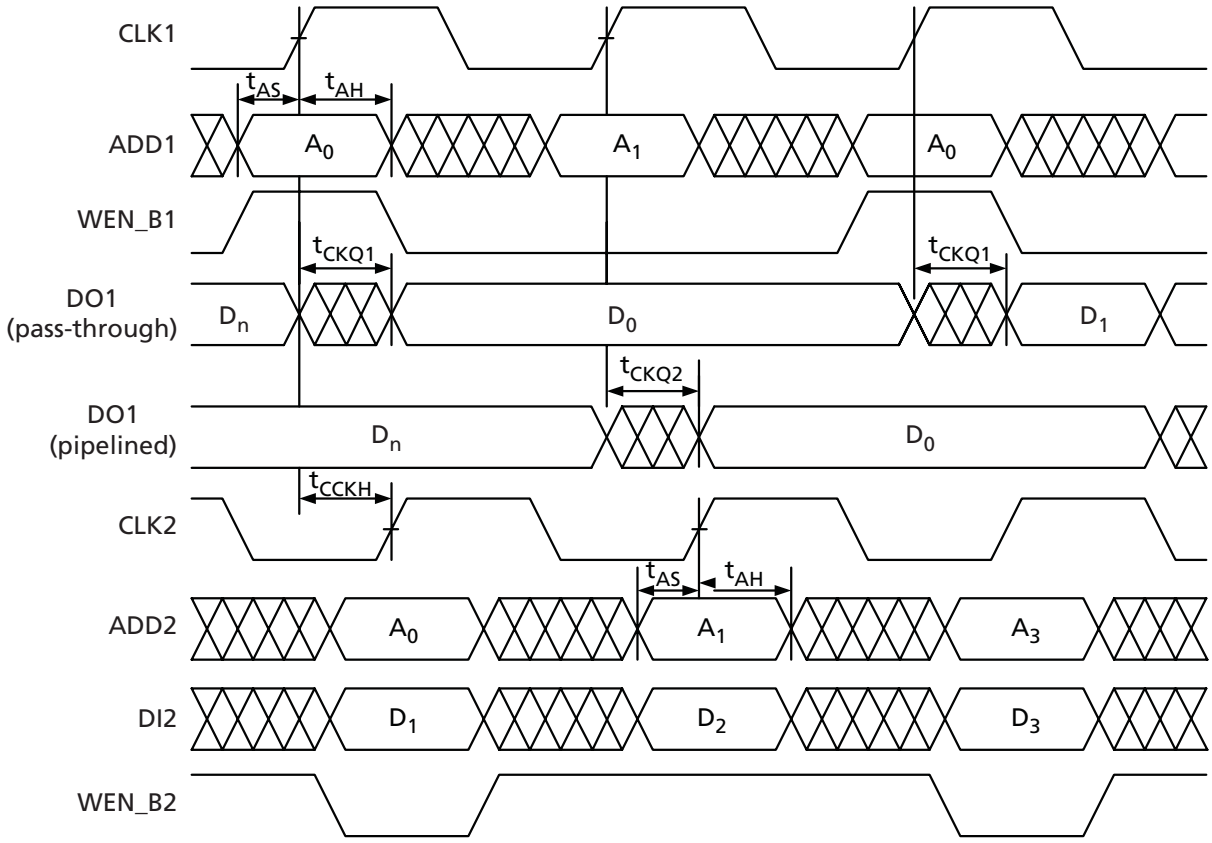


***Figure 2-48* • Write Access after Read onto Same Address**

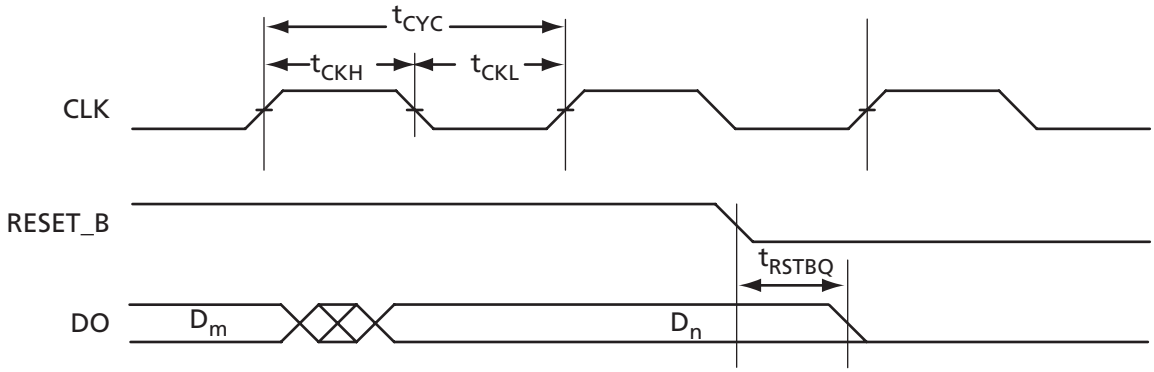


***Figure 2-49* • RAM Reset**

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-137 • RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	0.83	ns
t_{AH}	Address Hold Time	0.16	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.81	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.16	ns
t_{BKS}	BLK_B Setup Time	1.65	ns
t_{BKH}	BLK_B Hold Time	0.16	ns
t_{DS}	Input Data (DI) Setup Time	0.71	ns
t_{DH}	Input Data (DI) Hold Time	0.36	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	3.53	ns
	Clock HIGH to New Data Valid on DO (pass-through, WMODE = 1)	3.06	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.81	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	2.06	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-138 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	0.83	ns
t_{AH}	Address Hold Time	0.16	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.73	ns
t_{ENH}	REB_B, WEN_B Hold Time	0.08	ns
t_{DS}	Input Data (DI) Setup Time	0.71	ns
t_{DH}	Input Data (DI) Hold Time	0.36	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	4.21	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.71	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	2.06	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-139 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	1.53	ns
t_{AH}	Address Hold Time	0.29	ns
t_{ENS}	REN_B, WEN_B Setup Time	1.50	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.29	ns
t_{BKS}	BLK_B Setup Time	3.05	ns
t_{BKH}	BLK_B Hold Time	0.29	ns
t_{DS}	Input Data (DI) Setup Time	1.33	ns
t_{DH}	Input Data (DI) Hold Time	0.66	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	6.61	ns
	Clock HIGH to New Data Valid on DO (pass-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	3.38	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	3.86	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B Removal	1.12	ns
$t_{RECRSTB}$	RESET_B Recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-140 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	1.53	ns
t_{AH}	Address Hold Time	0.29	ns
t_{ENS}	REN_B, WEN_B Setup Time	1.36	ns
t_{ENH}	REB_B, WEN_B Hold Time	0.15	ns
t_{DS}	Input Data (DI) Setup Time	1.33	ns
t_{DH}	Input Data (DI) Hold Time	0.66	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	7.88	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	3.20	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	3.86	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B Removal	1.12	ns
$t_{RECRSTB}$	RESET_B Recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

FIFO

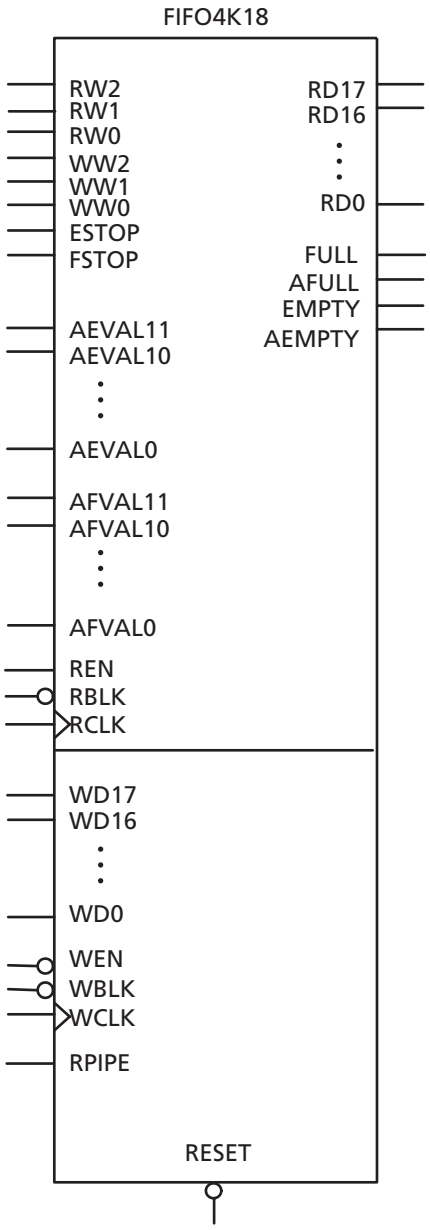


Figure 2-50 • **FIFO Model**

Timing Waveforms

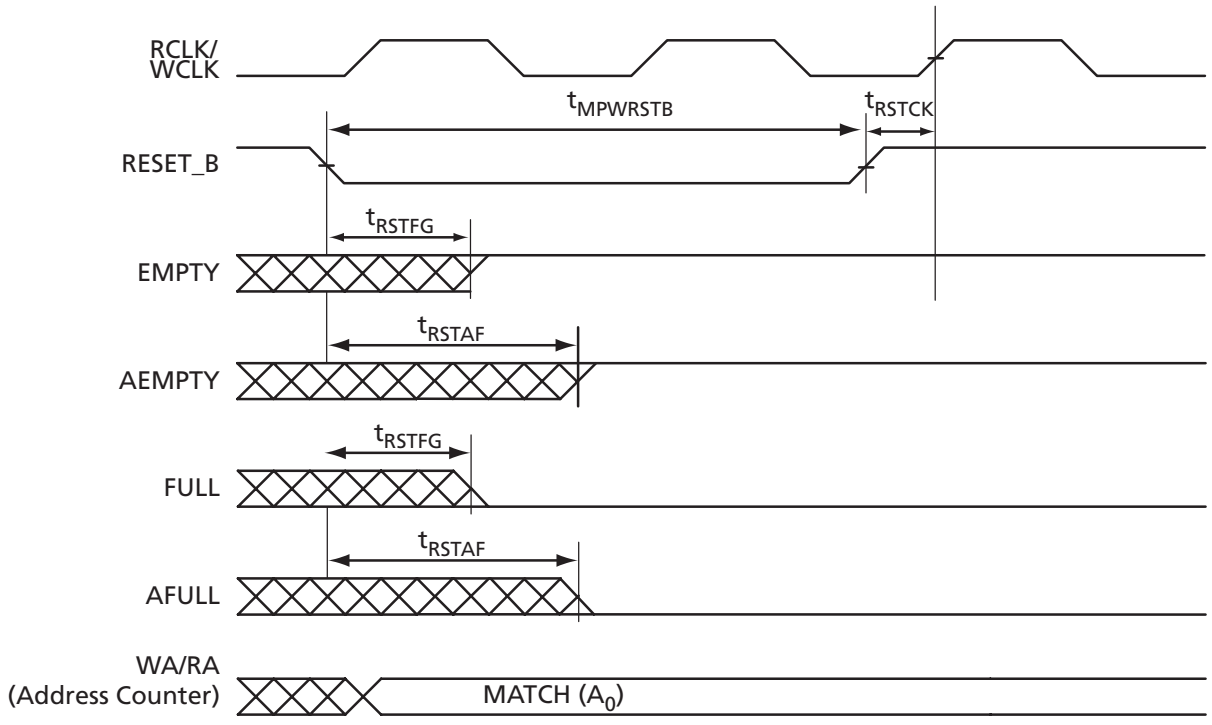


Figure 2-51 • **FIFO Reset**

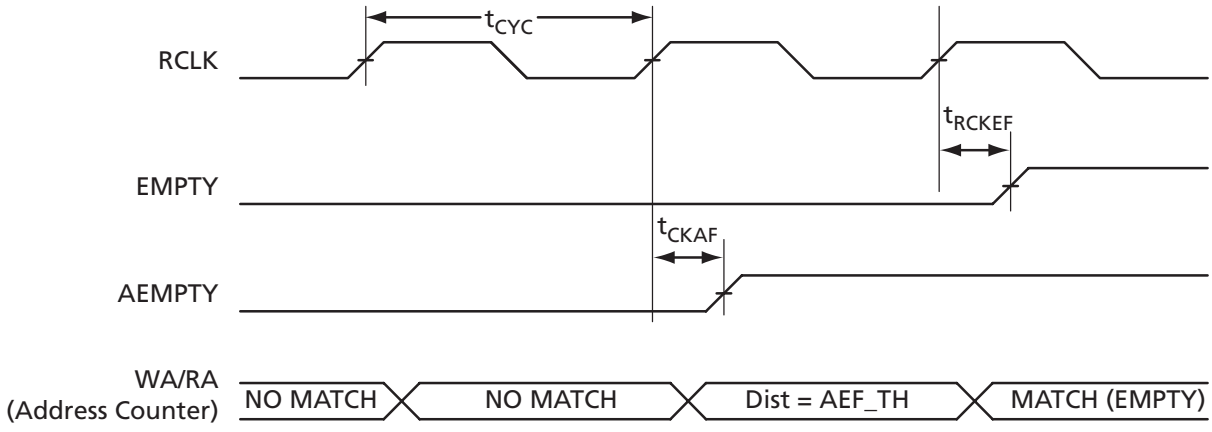


Figure 2-52 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

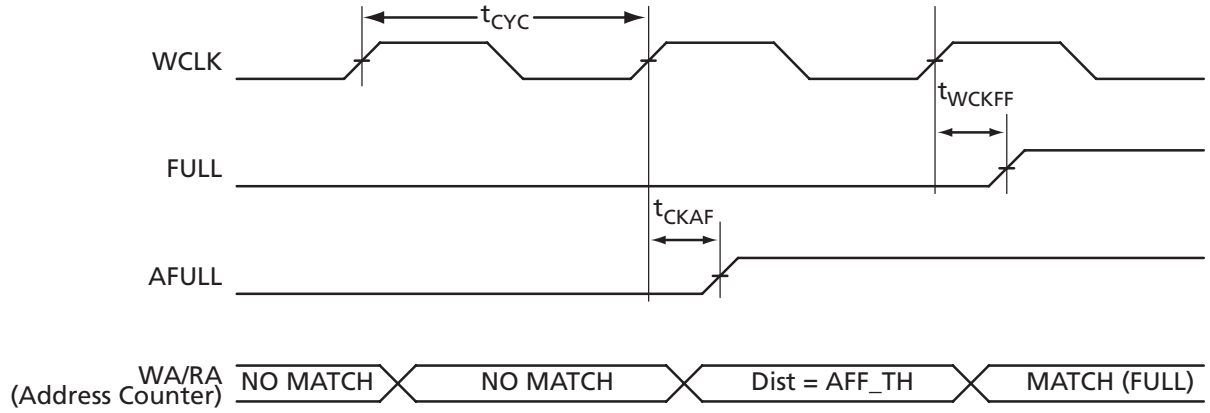


***Figure 2-53* • FIFO FULL Flag and AFULL Flag Assertion**

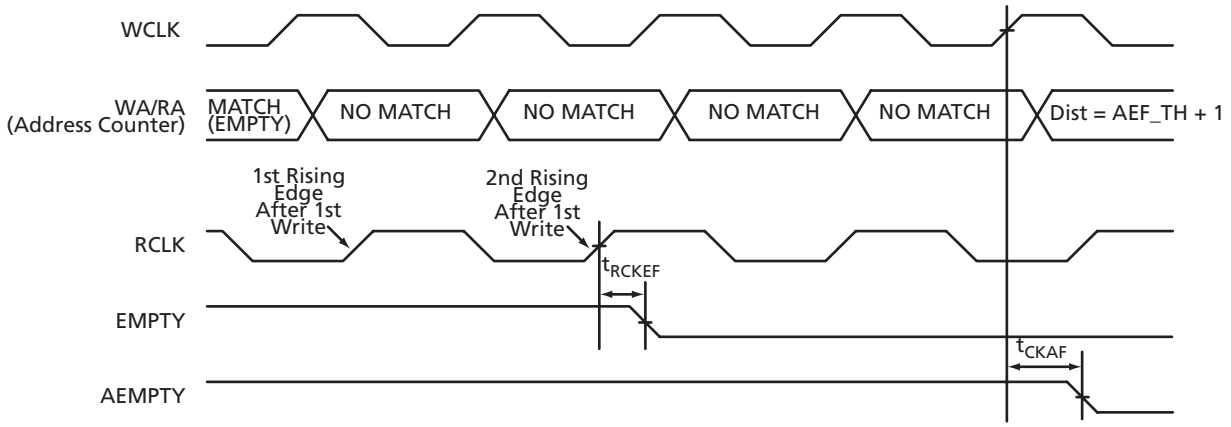


***Figure 2-54* • FIFO EMPTY Flag and AEMPTY Flag Deassertion**

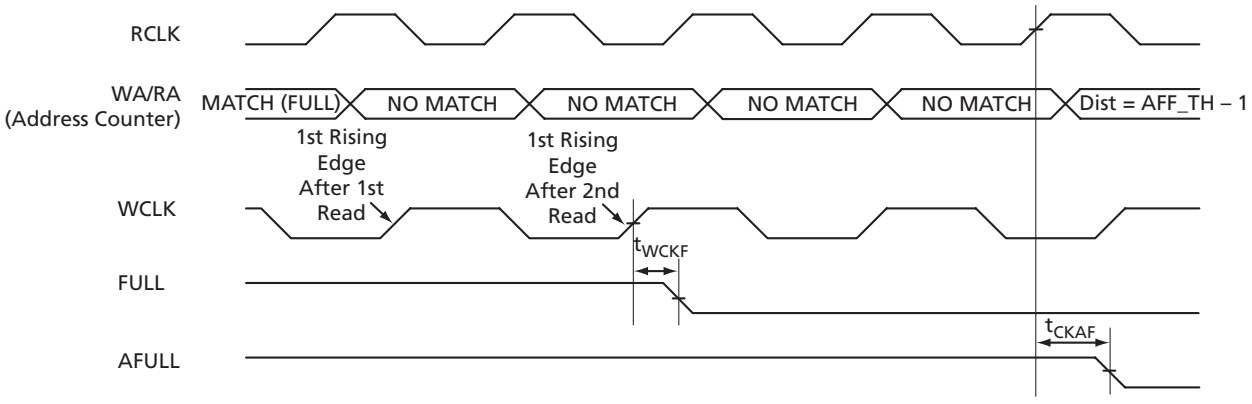


***Figure 2-55* • FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-141 • FIFO

Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.99	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.16	ns
t_{BKS}	BLK_B Setup Time	0.30	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.76	ns
t_{DH}	Input Data (DI) Hold Time	0.25	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (pass-through)	3.33	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.80	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	3.53	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	3.35	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	12.85	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	3.48	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	12.72	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	2.02	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	2.02	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-142 • FIFO
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	4.13	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.31	ns
t_{BKS}	BLK_B Setup Time	0.47	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.56	ns
t_{DH}	Input Data (DI) Hold Time	0.49	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (pass-through)	6.80	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	3.62	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	6.85	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (pass-through)	4.09	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	4.09	ns
$t_{REMRSTB}$	RESET_B Removal	1.23	ns
$t_{RECRSTB}$	RESET_B Recovery	6.58	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Embedded FlashROM Characteristics

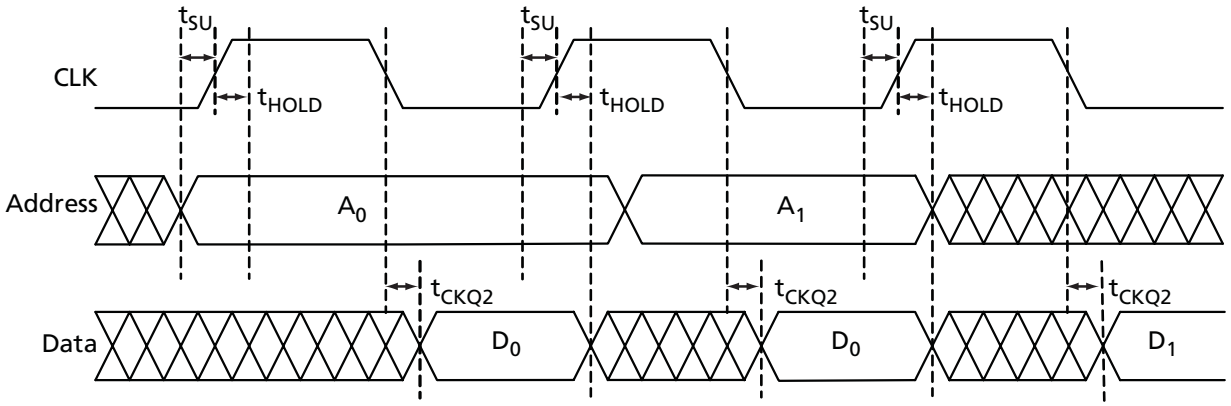


***Figure 2-56* • Timing Diagram**

Timing Characteristics

Applies to 1.5 V DC Core Voltage

***Table 2-143* • Embedded FlashROM Access Time**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.58	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock-to-Out	34.14	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

Applies to 1.2 V DC Core Voltage

***Table 2-144* • Embedded FlashROM Access Time**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock-to-Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-16 for more details.

Timing Characteristics

Applies to 1.2 V DC Core Voltage

***Table 2-145* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Applies to 1.5 V DC Core Voltage

***Table 2-146* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Part Number and Revision Date

Part Number 51700096-002-2
Revised July 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (Advance v0.3)	Page
Advance v0.2 (June 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	2-2
Advance v0.1 (January 2008)	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather then simulation values.	N/A
	Table 2-1 · Absolute Maximum Ratings was updated to add VMV to the V_{CCI} parameter row and remove the word "output" from the parameter description for V_{CCI}. Table note 3 was added.	2-1
	Table 2-2 · Recommended Operating Conditions [4] was updated to include the T_J parameter. Table note 9 is new.	2-2
	In Table 2-3 · Flash Programming Limits – Retention, Storage, and Operating Temperature1, the maximum operating junction temperature was changed from 110° to 100°.	2-2
	VMV was removed fromTable 2-4 · Overshoot and Undershoot Limits 1. The title of the table was revised to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Figure 2-2 · V2 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels is new.	2-5
	EQ 2-2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-8 · Quiescent Supply Current (I_{DD}), IGLOOe Flash*Freeze Mode*, Table 2-9 · Quiescent Supply Current (I_{DD}), IGLOOe Sleep Mode (VCC = 0 V)*, and Table 2-10 · Quiescent Supply Current (IDD), IGLOOe Shutdown Mode (VCC, VCCI = 0 V)* were updated to remove VMV and include P_{DC6} and P_{DC7}. V_{CCI} and V_{JTAG} were removed from the statement about I_{DD} in the table note for Table 2-9 · Quiescent Supply Current (I_{DD}), IGLOOe Sleep Mode (VCC = 0 V)*.	2-7
	Note 2 of Table 2-11 · Quiescent Supply Current, No IGLOOe Flash*Freeze Mode* was updated to include V_{CCPLL}. Note 4 was updated to include P_{DC6} and P_{DC7}.	2-8
	Table note 3 was added to Table 2-12 · Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and referenced for 1.2 V LVCMOS.	2-9

Previous Version	Changes in Current Version (Advance v0.3)	Page
Advance v0.1 (continued)	Table 2-13 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 was updated to change P_{DC3} to P_{DC7}. The table notes were updated to reflect that power was measured on V_{CCI}. Table note 4 is new.	2-10
	Table 2-15 · Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-17 · Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add P_{DC6} and P_{DC7}, and to change the definition for P_{DC5} to bank quiescent power.	2-11, 2-12
	A table subtitle was added for Table 2-17 · Different Components Contributing to the Static Power Consumption in IGLOO Devices	2-12
	The "Total Static Power Consumption—P_{STAT}" section was updated to revise the calculation of P_{STAT}, including P_{DC6} and P_{DC7}.	2-13
	Footnote 1 was updated to include information about P_{AC13}. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-16
	In Table 2-21 · Summary of Maximum and Minimum DC Input Levels, T_J was changed to T_A in notes 1 and 2.	2-21
	Table 2-31 · Schmitt Trigger Input Hysteresis was updated to included a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode).	2-28
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-41
Advance v0.4 (December 2007)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1.	N/A
Advance v0.3 (September 2007)	Table 2-4 • IGLOOe CCC/PLL Specification and Table 2-5 • IGLOOe CCC/PLL Specification were updated.	2-18, 2-19
	The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core.	2-60
	Figure 2-38 • Flash*Freeze Mode Type 1 – Timing Diagram was updated to modify the LSICC signal.	2-56
	Table 2-32 • Flash*Freeze Pin Location in IGLOOe Family Packages (device-independent) was updated for the FG896 package.	2-64
	Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal.	2-58
	Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section.	3-6
	Table 3-8 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode† was updated.	3-6
	Table 3-9 • Quiescent Supply Current (IDD), IGLOOe Sleep Mode (VCC = 0 V)† was updated.	3-6
	Table 3-11 • Quiescent Supply Current, No IGLOOe Flash*Freeze Mode1 was updated.	3-6

Previous Version	Changes in Current Version (Advance v0.3)	Page
Advance v0.3 (continued)	Table 3-99 • Minimum and Maximum DC Input and Output Levels was updated.	3-51
	Table 3-136 • JTAG 1532 and Table 3-135 • JTAG 1532 were updated.	3-95
Advance v0.1	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 6–8 were added.	3-2

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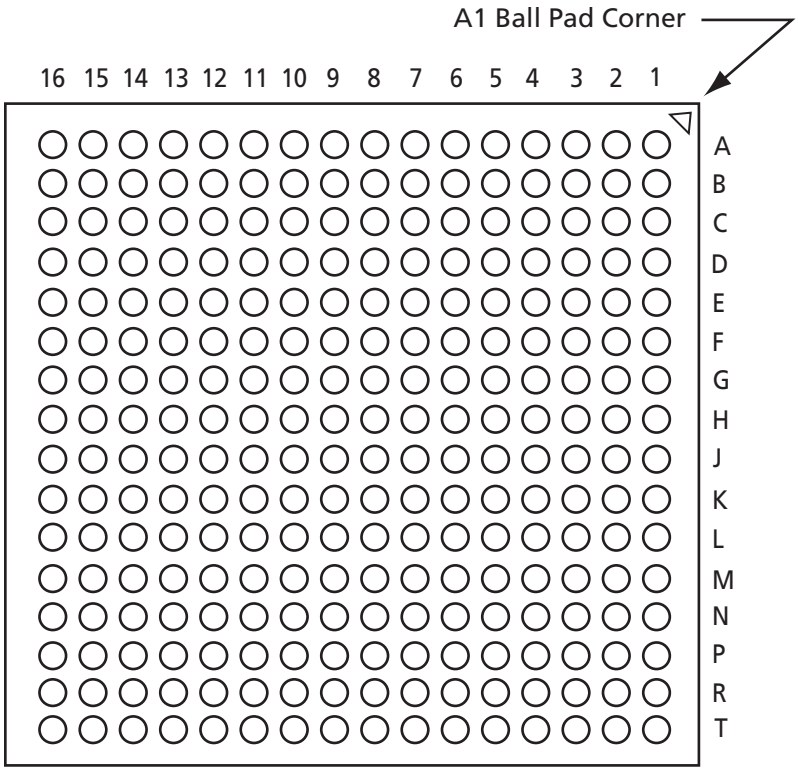
3 – Package Pin Assignments

256-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin FBGA	
Pin Number	AGLE600 Function
A1	GND
A2	GAA0/IO00NDB0V0
A3	GAA1/IO00PDB0V0
A4	GAB0/IO01NDB0V0
A5	IO05PDB0V0
A6	IO10PDB0V1
A7	IO12PDB0V2
A8	IO16NDB0V2
A9	IO23NDB1V0
A10	IO23PDB1V0
A11	IO28NDB1V1
A12	IO28PDB1V1
A13	GBB1/IO34PDB1V1
A14	GBA0/IO35NDB1V1
A15	GBA1/IO35PDB1V1
A16	GND
B1	GAB2/IO133PDB7V1
B2	GAA2/IO134PDB7V1
B3	GNDQ
B4	GAB1/IO01PDB0V0
B5	IO05NDB0V0
B6	IO10NDB0V1
B7	IO12NDB0V2
B8	IO16PDB0V2
B9	IO20NDB1V0
B10	IO24NDB1V0
B11	IO24PDB1V0
B12	GBC1/IO33PDB1V1
B13	GBB0/IO34NDB1V1
B14	GNDQ
B15	GBA2/IO36PDB2V0
B16	IO42NDB2V0
C1	IO133NDB7V1
C2	IO134NDB7V1
C3	VMV7

256-Pin FBGA	
Pin Number	AGLE600 Function
C4	V_{CCPLA}
C5	GAC0/IO02NDB0V0
C6	GAC1/IO02PDB0V0
C7	IO15NDB0V2
C8	IO15PDB0V2
C9	IO20PDB1V0
C10	IO25NDB1V0
C11	IO27PDB1V0
C12	GBC0/IO33NDB1V1
C13	V_{CCPLB}
C14	VMV2
C15	IO36NDB2V0
C16	IO42PDB2V0
D1	IO128PDB7V1
D2	IO129PDB7V1
D3	GAC2/IO132PDB7V1
D4	V_{COMPLA}
D5	GNDQ
D6	IO09NDB0V1
D7	IO09PDB0V1
D8	IO13PDB0V2
D9	IO21PDB1V0
D10	IO25PDB1V0
D11	IO27NDB1V0
D12	GNDQ
D13	V_{COMPLB}
D14	GBB2/IO37PDB2V0
D15	IO39PDB2V0
D16	IO39NDB2V0
E1	IO128NDB7V1
E2	IO129NDB7V1
E3	IO132NDB7V1
E4	IO130PDB7V1
E5	VMV0
E6	$V_{CCI}B0$
E7	$V_{CCI}B0$

256-Pin FBGA	
Pin Number	AGLE600 Function
E8	IO13NDB0V2
E9	IO21NDB1V0
E10	$V_{CCI}B1$
E11	$V_{CCI}B1$
E12	VMV1
E13	GBC2/IO38PDB2V0
E14	IO37NDB2V0
E15	IO41NDB2V0
E16	IO41PDB2V0
F1	IO124PDB7V0
F2	IO125PDB7V0
F3	IO126PDB7V0
F4	IO130NDB7V1
F5	$V_{CCI}B7$
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	$V_{CCI}B2$
F13	IO38NDB2V0
F14	IO40NDB2V0
F15	IO40PDB2V0
F16	IO45PSB2V1
G1	IO124NDB7V0
G2	IO125NDB7V0
G3	IO126NDB7V0
G4	GFC1/IO120PPB7V0
G5	$V_{CCI}B7$
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}

256-Pin FBGA	
Pin Number	AGLE600 Function
G12	V_{CCI}B2
G13	GCC1/IO50PPB2V1
G14	IO44NDB2V1
G15	IO44PDB2V1
G16	IO49NSB2V1
H1	GFB0/IO119NPB7V0
H2	GFA0/IO118NDB6V1
H3	GFB1/IO119PPB7V0
H4	V_{COMPLF}
H5	GFC0/IO120NPB7V0
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO50NPB2V1
H13	GCB1/IO51PPB2V1
H14	GCA0/IO52NPB3V0
H15	V_{COMPLC}
H16	GCB0/IO51NPB2V1
J1	GFA2/IO117PSB6V1
J2	GFA1/IO118PDB6V1
J3	V_{CCPLF}
J4	IO116NDB6V1
J5	GFB2/IO116PDB6V1
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO54PPB3V0
J13	GCA1/IO52PPB3V0
J14	GCC2/IO55PPB3V0
J15	V_{CCPLC}

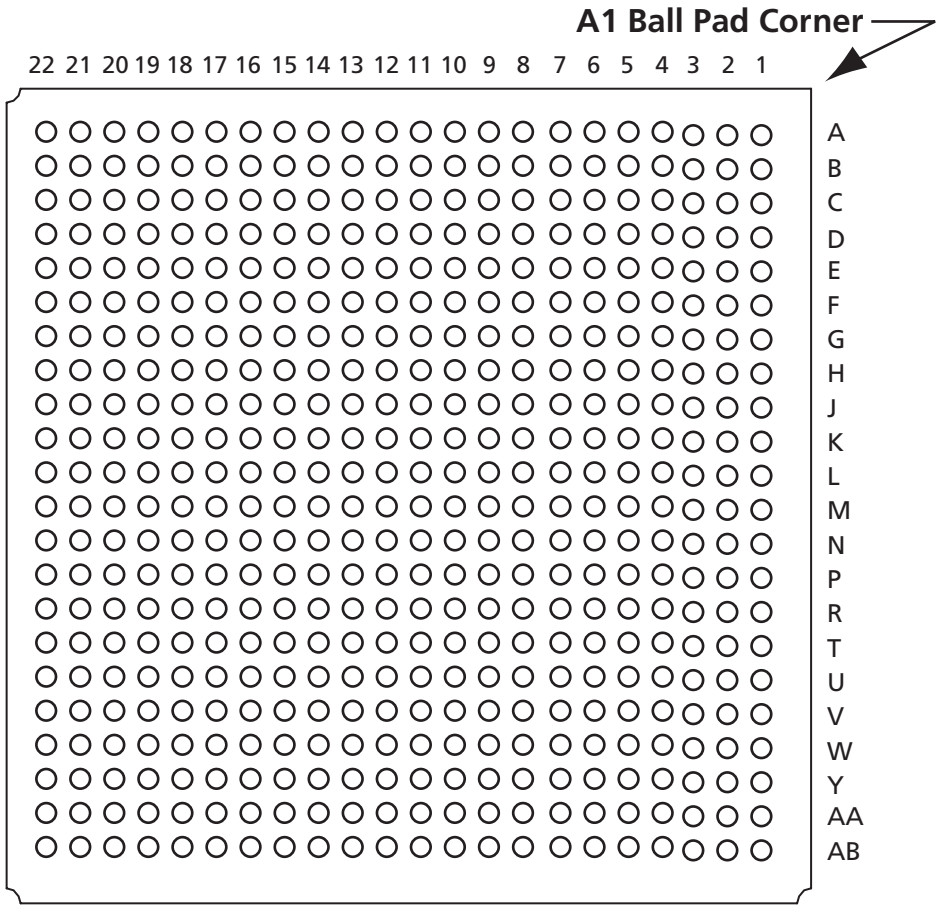
256-Pin FBGA	
Pin Number	AGLE600 Function
J16	GCA2/IO53PSB3V0
K1	GFC2/IO115PSB6V1
K2	IO113PPB6V1
K3	IO112PDB6V1
K4	IO112NDB6V1
K5	V_{CCI}B6
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B3
K13	IO54NPB3V0
K14	IO57NPB3V0
K15	IO55NPB3V0
K16	IO57PPB3V0
L1	IO113NPB6V1
L2	IO109PPB6V0
L3	IO108PDB6V0
L4	IO108NDB6V0
L5	V_{CCI}B6
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B3
L13	GDB0/IO66NPB3V1
L14	IO60NDB3V1
L15	IO60PDB3V1
L16	IO61PDB3V1
M1	IO109NPB6V0
M2	IO106NDB6V0
M3	IO106PDB6V0

256-Pin FBGA	
Pin Number	AGLE600 Function
M4	GEC0/IO104NPB6V0
M5	VMV5
M6	V_{CCI}B5
M7	V_{CCI}B5
M8	IO84NDB5V0
M9	IO84PDB5V0
M10	V_{CCI}B4
M11	V_{CCI}B4
M12	VMV3
M13	V_{CCPLD}
M14	GDB1/IO66PPB3V1
M15	GDC1/IO65PDB3V1
M16	IO61NDB3V1
N1	IO105PDB6V0
N2	IO105NDB6V0
N3	GEC1/IO104PPB6V0
N4	V_{COMPLE}
N5	GNDQ
N6	GEA2/IO101PPB5V2
N7	IO92NDB5V1
N8	IO90NDB5V1
N9	IO82NDB5V0
N10	IO74NDB4V1
N11	IO74PDB4V1
N12	GNDQ
N13	V_{COMPLD}
N14	V_{JTAG}
N15	GDC0/IO65NDB3V1
N16	GDA1/IO67PDB3V1
P1	GEB1/IO103PDB6V0
P2	GEB0/IO103NDB6V0
P3	VMV6
P4	V_{CCPLE}
P5	IO101NPB5V2
P6	IO95PPB5V1
P7	IO92PDB5V1

256-Pin FBGA	
Pin Number	**AGLE600 Function**
P8	IO90PDB5V1
P9	IO82PDB5V0
P10	IO76NDB4V1
P11	IO76PDB4V1
P12	VMV4
P13	TCK
P14	V_{PUMP}
P15	TRST
P16	GDA0/IO67NDB3V1
R1	GEA1/IO102PDB6V0
R2	GEA0/IO102NDB6V0
R3	GNDQ
R4	GEC2/IO99PDB5V2
R5	IO95NPB5V1
R6	IO91NDB5V1
R7	IO91PDB5V1
R8	IO83NDB5V0
R9	IO83PDB5V0
R10	IO77NDB4V1
R11	IO77PDB4V1
R12	IO69NDB4V0
R13	GDB2/IO69PDB4V0
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO100NDB5V2
T3	FF/GEB2/IO100PDB5V2
T4	IO99NDB5V2
T5	IO88NDB5V0
T6	IO88PDB5V0
T7	IO89NSB5V0
T8	IO80NSB4V1
T9	IO81NDB4V1

256-Pin FBGA	
Pin Number	**AGLE600 Function**
T10	IO81PDB4V1
T11	IO70NDB4V0
T12	GDC2/IO70PDB4V0
T13	IO68NDB4V0
T14	GDA2/IO68PDB4V0
T15	TMS
T16	GND

484-Pin FBGA



Note: This is the bottom view of the package.

Note

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484-Pin FBGA	
Pin Number	AGLE600 Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	V_{CCI}B1
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC

484-Pin FBGA	
Pin Number	AGLE600 Function
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B3
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	V_{CCI}B4
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B7
B3	NC
B4	IO03NDB0V0
B5	IO03PDB0V0
B6	IO07NDB0V1

484-Pin FBGA	
Pin Number	AGLE600 Function
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0
B14	NC
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	V_{CCI}B2
B22	GND
C1	V_{CCI}B7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	V_{CC}
C9	V_{CC}
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

484-Pin FBGA	
Pin Number	AGLE600 Function
C21	NC
C22	V_{CCI}B2
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO05PDB0V0
D9	IO10PDB0V1
D10	IO12PDB0V2
D11	IO16NDB0V2
D12	IO23NDB1V0
D13	IO23PDB1V0
D14	IO28NDB1V1
D15	IO28PDB1V1
D16	GBB1/IO34PDB1V1
D17	GBA0/IO35NDB1V1
D18	GBA1/IO35PDB1V1
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO133PDB7V1
E5	GAA2/IO134PDB7V1
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO05NDB0V0
E9	IO10NDB0V1
E10	IO12NDB0V2

484-Pin FBGA	
Pin Number	AGLE600 Function
E11	IO16PDB0V2
E12	IO20NDB1V0
E13	IO24NDB1V0
E14	IO24PDB1V0
E15	GBC1/IO33PDB1V1
E16	GBB0/IO34NDB1V1
E17	GNDQ
E18	GBA2/IO36PDB2V0
E19	IO42NDB2V0
E20	GND
E21	NC
E22	NC
F1	NC
F2	IO131NDB7V1
F3	IO131PDB7V1
F4	IO133NDB7V1
F5	IO134NDB7V1
F6	VMV7
F7	V_{CCPLA}
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO15NDB0V2
F11	IO15PDB0V2
F12	IO20PDB1V0
F13	IO25NDB1V0
F14	IO27PDB1V0
F15	GBC0/IO33NDB1V1
F16	V_{CCPLB}
F17	VMV2
F18	IO36NDB2V0
F19	IO42PDB2V0
F20	NC
F21	NC
F22	NC
G1	IO127NDB7V1
G2	IO127PDB7V1

484-Pin FBGA	
Pin Number	AGLE600 Function
G3	NC
G4	IO128PDB7V1
G5	IO129PDB7V1
G6	GAC2/IO132PDB7V1
G7	V_{COMPLA}
G8	GNDQ
G9	IO09NDB0V1
G10	IO09PDB0V1
G11	IO13PDB0V2
G12	IO21PDB1V0
G13	IO25PDB1V0
G14	IO27NDB1V0
G15	GNDQ
G16	V_{COMPLB}
G17	GBB2/IO37PDB2V0
G18	IO39PDB2V0
G19	IO39NDB2V0
G20	IO43PDB2V0
G21	IO43NDB2V0
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO128NDB7V1
H5	IO129NDB7V1
H6	IO132NDB7V1
H7	IO130PDB7V1
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO13NDB0V2
H12	IO21NDB1V0
H13	V_{CCI}B1
H14	V_{CCI}B1
H15	VMV1

484-Pin FBGA	
Pin Number	AGLE600 Function
H16	GBC2/IO38PDB2V0
H17	IO37NDB2V0
H18	IO41NDB2V0
H19	IO41PDB2V0
H20	V_{CC}
H21	NC
H22	NC
J1	IO123NDB7V0
J2	IO123PDB7V0
J3	NC
J4	IO124PDB7V0
J5	IO125PDB7V0
J6	IO126PDB7V0
J7	IO130NDB7V1
J8	V_{CCI}B7
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B2
J16	IO38NDB2V0
J17	IO40NDB2V0
J18	IO40PDB2V0
J19	IO45PPB2V1
J20	NC
J21	IO48PDB2V1
J22	IO46PDB2V1
K1	IO121NDB7V0
K2	IO121PDB7V0
K3	NC
K4	IO124NDB7V0
K5	IO125NDB7V0
K6	IO126NDB7V0
K7	GFC1/IO120PPB7V0

484-Pin FBGA	
Pin Number	AGLE600 Function
K8	V_{CCI}B7
K9	V_{CC}
K10	GND
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B2
K16	GCC1/IO50PPB2V1
K17	IO44NDB2V1
K18	IO44PDB2V1
K19	IO49NPB2V1
K20	IO45NPB2V1
K21	IO48NDB2V1
K22	IO46NDB2V1
L1	NC
L2	IO122PDB7V0
L3	IO122NDB7V0
L4	GFB0/IO119NPB7V0
L5	GFA0/IO118NDB6V1
L6	GFB1/IO119PPB7V0
L7	V_{COMPLF}
L8	GFC0/IO120NPB7V0
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO50NPB2V1
L16	GCB1/IO51PPB2V1
L17	GCA0/IO52NPB3V0
L18	V_{COMPLC}
L19	GCB0/IO51NPB2V1
L20	IO49PPB2V1

484-Pin FBGA	
Pin Number	AGLE600 Function
L21	IO47NDB2V1
L22	IO47PDB2V1
M1	NC
M2	IO114NPB6V1
M3	IO117NDB6V1
M4	GFA2/IO117PDB6V1
M5	GFA1/IO118PDB6V1
M6	V_{CCPLF}
M7	IO116NDB6V1
M8	GFB2/IO116PDB6V1
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO54PPB3V0
M16	GCA1/IO52PPB3V0
M17	GCC2/IO55PPB3V0
M18	V_{CCPLC}
M19	GCA2/IO53PDB3V0
M20	IO53NDB3V0
M21	IO56PDB3V0
M22	NC
N1	IO114PPB6V1
N2	IO111NDB6V1
N3	NC
N4	GFC2/IO115PPB6V1
N5	IO113PPB6V1
N6	IO112PDB6V1
N7	IO112NDB6V1
N8	V_{CCI}B6
N9	V_{CC}
N10	GND
N11	GND
N12	GND

484-Pin FBGA	
Pin Number	AGLE600 Function
N13	GND
N14	V_{CC}
N15	V_{CCI}B3
N16	IO54NPB3V0
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	V_{CCI}B6
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	V_{CC}
R4	IO109NPB6V0

484-Pin FBGA	
Pin Number	AGLE600 Function
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5
R9	V_{CCI}B5
R10	V_{CCI}B5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	V_{CCI}B4
R14	V_{CCI}B4
R15	VMV3
R16	V_{CCPLD}
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	V_{CC}
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO65NDB3V1

484-Pin FBGA	
Pin Number	AGLE600 Function
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1

484-Pin FBGA	
Pin Number	**AGLE600 Function**
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	FF/GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC

484-Pin FBGA	
Pin Number	**AGLE600 Function**
W22	NC
Y1	V_{CCI}B6
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1
Y7	IO94PDB5V1
Y8	V_{CC}
Y9	V_{CC}
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B3

484-Pin FBGA	
Pin Number	AGLE3000 Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO16NDB0V1
A7	IO16PDB0V1
A8	IO18PDB0V2
A9	IO24PDB0V2
A10	IO28NDB0V3
A11	IO28PDB0V3
A12	IO46PDB1V0
A13	IO54PDB1V1
A14	IO56NDB1V1
A15	IO56PDB1V1
A16	IO64NDB1V2
A17	IO64PDB1V2
A18	IO72NDB1V3
A19	IO74NDB1V4
A20	V_{CCI}B1
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B6
AA3	IO228PDB5V4
AA4	IO224PDB5V3
AA5	IO218NDB5V3
AA6	IO218PDB5V3
AA7	IO212NDB5V2
AA8	IO212PDB5V2
AA9	IO198PDB5V0
AA10	IO198NDB5V0
AA11	IO188PPB4V4
AA12	IO180NDB4V3
AA13	IO180PDB4V3
AA14	IO170NDB4V2

484-Pin FBGA	
Pin Number	AGLE3000 Function
AA15	IO170PDB4V2
AA16	IO166NDB4V1
AA17	IO166PDB4V1
AA18	IO160NDB4V0
AA19	IO160PDB4V0
AA20	IO158NPB4V0
AA21	V_{CCI}B3
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B5
AB4	IO216NDB5V2
AB5	IO216PDB5V2
AB6	IO210NDB5V2
AB7	IO210PDB5V2
AB8	IO208NDB5V1
AB9	IO208PDB5V1
AB10	IO197NDB5V0
AB11	IO197PDB5V0
AB12	IO174NDB4V2
AB13	IO174PDB4V2
AB14	IO172NDB4V2
AB15	IO172PDB4V2
AB16	IO168NDB4V1
AB17	IO168PDB4V1
AB18	IO162NDB4V1
AB19	IO162PDB4V1
AB20	V_{CCI}B4
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B7
B3	IO06PPB0V0
B4	IO08NDB0V0
B5	IO08PDB0V0
B6	IO14NDB0V1

484-Pin FBGA	
Pin Number	AGLE3000 Function
B7	IO14PDB0V1
B8	IO18NDB0V2
B9	IO24NDB0V2
B10	IO34PDB0V4
B11	IO40PDB0V4
B12	IO46NDB1V0
B13	IO54NDB1V1
B14	IO62NDB1V2
B15	IO62PDB1V2
B16	IO68NDB1V3
B17	IO68PDB1V3
B18	IO72PDB1V3
B19	IO74PDB1V4
B20	IO76NPB1V4
B21	V_{CCI}B2
B22	GND
C1	V_{CCI}B7
C2	IO303PDB7V3
C3	IO305PDB7V3
C4	IO06NPB0V0
C5	GND
C6	IO12NDB0V1
C7	IO12PDB0V1
C8	V_{CC}
C9	V_{CC}
C10	IO34NDB0V4
C11	IO40NDB0V4
C12	IO48NDB1V0
C13	IO48PDB1V0
C14	V_{CC}
C15	V_{CC}
C16	IO70NDB1V3
C17	IO70PDB1V3
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0

484-Pin FBGA	
Pin Number	AGLE3000 Function
C21	IO94PPB2V1
C22	V_{CCI}B2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0

484-Pin FBGA	
Pin Number	AGLE3000 Function
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	V_{CCPLA}
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	V_{CCPLB}
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2

484-Pin FBGA	
Pin Number	AGLE3000 Function
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	V_{COMPLA}
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	V_{COMPLB}
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	V_{CC}
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO36NDB0V4
H12	IO42NDB1V0
H13	V_{CCI}B1
H14	V_{CCI}B1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2

484-Pin FBGA	
Pin Number	AGLE3000 Function
H19	IO100PDB2V2
H20	V_{CC}
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	V_{CCI}B7
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	V_{CCI}B7
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	AGLE3000 Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B2
K16	GCC1/IO112PPB2V3
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	V_{COMPLF}
L8	GFC0/IO275NPB7V0
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3
L17	GCA0/IO114NPB3V0
L18	V_{COMPLC}
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2

484-Pin FBGA	
Pin Number	AGLE3000 Function
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	V_{CCPLF}
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO116PPB3V0
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	V_{CCPLC}
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3
N8	V_{CCI}B6
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B3
N16	IO116NPB3V0

484-Pin FBGA	
Pin Number	AGLE3000 Function
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	V_{CCI}B6
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	V_{CC}
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5

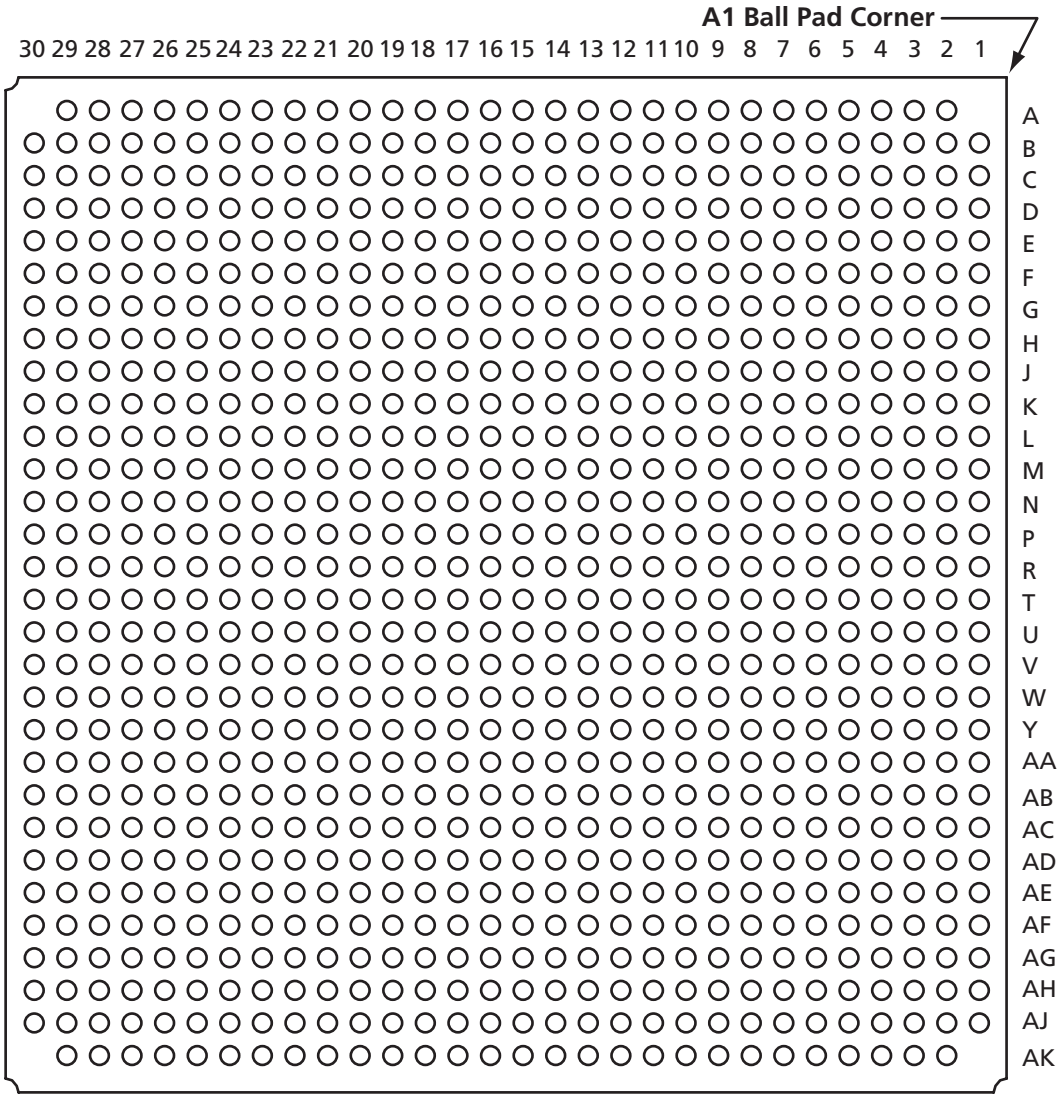
484-Pin FBGA	
Pin Number	AGLE3000 Function
R9	V_{CCI}B5
R10	V_{CCI}B5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	V_{CCI}B4
R14	V_{CCI}B4
R15	VMV3
R16	V_{CCPLD}
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	V_{CC}
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2

484-Pin FBGA	
Pin Number	AGLE3000 Function
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3

484-Pin FBGA	
Pin Number	**AGLE3000 Function**
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	V_{CCI}B6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND

484-Pin FBGA	
Pin Number	**AGLE3000 Function**
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	V_{CC}
Y9	V_{CC}
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	V_{CC}
Y15	V_{CC}
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	V_{CCI}B3

896-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

896-Pin FBGA	
Pin Number	AGLE3000 Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1

896-Pin FBGA	
Pin Number	AGLE3000 Function
AA8	IO245NDB6V1
AA9	GEB1/IO235PPB6V0
AA10	V_{CC}
AA11	IO226PPB5V4
AA12	V_{CCI}B5
AA13	V_{CCI}B5
AA14	V_{CCI}B5
AA15	V_{CCI}B5
AA16	V_{CCI}B4
AA17	V_{CCI}B4
AA18	V_{CCI}B4
AA19	V_{CCI}B4
AA20	IO174PDB4V2
AA21	V_{CC}
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	V_{CCI}B6
AB8	V_{CCPLE}
AB9	V_{CC}
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1

896-Pin FBGA	
Pin Number	AGLE3000 Function
AB13	IO206PDB5V1
AB14	IO198NDB5V0
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	V_{CC}
AB23	V_{CCPLD}
AB24	V_{CCI}B3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	V_{COMPLE}
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4

896-Pin FBGA	
Pin Number	AGLE3000 Function
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	V_{COMPLD}
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	V_{CCI}B6
AD6	GNDQ
AD6	GNDQ
AD7	V_{CC}
AD8	VMV5
AD9	V_{CCI}B5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1

896-Pin FBGA	
Pin Number	AGLE3000 Function
AD22	V_{CCI}B4
AD23	TCK
AD24	V_{CC}
AD25	TRST
AD26	V_{CCI}B3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	V_{CC}
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND

896-Pin FBGA	
Pin Number	AGLE3000 Function
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	V_{CC}
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	V_{CCI}B6
AF4	IO220NPB5V3
AF5	V_{CC}
AF6	IO228NDB5V4
AF7	V_{CCI}B5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	V_{CCI}B4
AF25	IO154NPB4V0
AF26	V_{CC}
AF27	TDO
AF28	V_{CCI}B3
AF29	GNDQ

896-Pin FBGA	
Pin Number	AGLE3000 Function
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	V_{CC}
AG3	IO232NPB5V4
AG4	GND
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	V_{JTAG}
AG29	V_{CC}
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	V_{CC}

896-Pin FBGA	
Pin Number	AGLE3000 Function
AH4	FF/GEB2/IO232PPB5V4
AH5	V_{CCI}B5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	V_{CCI}B4
AH27	TDI
AH28	V_{CC}
AH29	V_{PUMP}
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	V_{CC}
AJ5	IO217NPB5V2
AJ6	V_{CC}
AJ7	IO215NPB5V2

896-Pin FBGA	
Pin Number	AGLE3000 Function
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	V_{CC}
AJ26	IO156NPB4V0
AJ27	V_{CC}
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4

896-Pin FBGA	
Pin Number	AGLE3000 Function
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	V_{CC}
B5	IO14PPB0V1
B6	V_{CC}
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2

896-Pin FBGA	
Pin Number	AGLE3000 Function
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	V_{CC}
B26	GBC0/IO79NPB1V4
B27	V_{CC}
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	V_{CC}
C4	GAA0/IO00NPB0V0
C5	V_{CCI}B0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4

896-Pin FBGA	
Pin Number	AGLE3000 Function
C25	IO75PDB1V4
C26	V_{CCI}B1
C27	IO64PPB1V2
C28	V_{CC}
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	V_{CC}
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	V_{CC}

896-Pin FBGA	
Pin Number	AGLE3000 Function
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	V_{CCI}B7
E4	IO305PPB7V3
E5	V_{CC}
E6	GAC0/IO02NDB0V0
E7	V_{CCI}B0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	V_{CCI}B1
E25	IO74PDB1V4
E26	V_{CC}
E27	GBB1/IO80PPB1V4
E28	V_{CCI}B2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	V_{CC}
F3	IO306PDB7V4
F4	IO297PDB7V2

896-Pin FBGA	
Pin Number	AGLE3000 Function
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	V_{CC}
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	V_{CCI}B7
G6	GNDQ
G6	GNDQ

896-Pin FBGA	
Pin Number	AGLE3000 Function
G7	V_{CC}
G8	VMV0
G9	V_{CCI}B0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	V_{CCI}B1
G23	VMV1
G24	V_{CC}
G25	GNDQ
G25	GNDQ
G26	V_{CCI}B2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	V_{COMPLA}
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0

896-Pin FBGA	
Pin Number	AGLE3000 Function
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	V_{COMPLB}
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3
J5	IO295NDB7V2
J6	IO299NDB7V3
J7	$V_{CCI}B7$
J8	V_{CCPLA}
J9	V_{CC}
J10	IO04NPB0V0
J11	IO18NDB0V2
J12	IO20NDB0V2
J13	IO20PDB0V2
J14	IO32NDB0V3
J15	IO32PDB0V3

896-Pin FBGA	
Pin Number	AGLE3000 Function
J16	IO42PDB1V0
J17	IO44NDB1V0
J18	IO44PDB1V0
J19	IO54NDB1V1
J20	IO54PDB1V1
J21	IO76NPB1V4
J22	V_{CC}
J23	V_{CCPLB}
J24	$V_{CCI}B2$
J25	IO90PDB2V1
J26	IO90NDB2V1
J27	GBB2/IO83PDB2V0
J28	IO83NDB2V0
J29	IO91PDB2V1
J30	IO91NDB2V1
K1	IO288NDB7V1
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	V_{CC}
K11	IO04PPB0V0
K12	$V_{CCI}B0$
K13	$V_{CCI}B0$
K14	$V_{CCI}B0$
K15	$V_{CCI}B0$
K16	$V_{CCI}B1$
K17	$V_{CCI}B1$
K18	$V_{CCI}B1$
K19	$V_{CCI}B1$
K20	IO76PPB1V4

896-Pin FBGA	
Pin Number	AGLE3000 Function
K21	V_{CC}
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	V_{CC}
L12	V_{CC}
L13	V_{CC}
L14	V_{CC}
L15	V_{CC}
L16	V_{CC}
L17	V_{CC}
L18	V_{CC}
L19	V_{CC}
L20	V_{CC}
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0

896-Pin FBGA	
Pin Number	AGLE3000 Function
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	V_{CCI}B7
M11	V_{CC}
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	V_{CC}
M21	V_{CCI}B2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0

896-Pin FBGA	
Pin Number	AGLE3000 Function
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	V_{CCI}B7
N11	V_{CC}
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	V_{CC}
N21	V_{CCI}B2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0

896-Pin FBGA	
Pin Number	AGLE3000 Function
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	V_{CCI}B7
P11	V_{CC}
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	V_{CC}
P21	V_{CCI}B2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	V_{COMPLF}
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	V_{CCI}B7

896-Pin FBGA	
Pin Number	AGLE3000 Function
R11	V_{CC}
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	V_{CC}
R21	$V_{CCI}B2$
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	V_{COMPLC}
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4
T2	V_{CCPLF}
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	$V_{CCI}B6$
T11	V_{CC}
T12	GND
T13	GND
T14	GND
T15	GND

896-Pin FBGA	
Pin Number	AGLE3000 Function
T16	GND
T17	GND
T18	GND
T19	GND
T20	V_{CC}
T21	$V_{CCI}B3$
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	V_{CCPLC}
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	$V_{CCI}B6$
U11	V_{CC}
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	V_{CC}

896-Pin FBGA	
Pin Number	AGLE3000 Function
U21	$V_{CCI}B3$
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	$V_{CCI}B6$
V11	V_{CC}
V12	GND
V13	GND
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	V_{CC}
V21	$V_{CCI}B3$
V22	IO120NDB3V0
V23	IO128NDB3V1
V24	IO132PDB3V2
V25	IO130PPB3V2

896-Pin FBGA	
Pin Number	AGLE3000 Function
V26	IO126NDB3V1
V27	IO129NDB3V1
V28	IO127NDB3V1
V29	IO125NDB3V1
V30	IO123PDB3V1
W1	IO266NDB6V4
W2	IO262NDB6V3
W3	IO260NDB6V3
W4	IO252NDB6V2
W5	IO251NDB6V2
W6	IO251PDB6V2
W7	IO255NDB6V2
W8	IO249PPB6V1
W9	IO253PDB6V2
W10	V_{CCI}B6
W11	V_{CC}
W12	GND
W13	GND
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND
W20	V_{CC}
W21	V_{CCI}B3
W22	IO134PDB3V2
W23	IO138PDB3V3
W24	IO132NDB3V2
W25	IO136NPB3V2
W26	IO130NPB3V2
W27	IO141PDB3V3
W28	IO135PDB3V2
W29	IO131PDB3V2
W30	IO123NDB3V1

896-Pin FBGA	
Pin Number	AGLE3000 Function
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	V_{CC}
Y12	V_{CC}
Y13	V_{CC}
Y14	V_{CC}
Y15	V_{CC}
Y16	V_{CC}
Y17	V_{CC}
Y18	V_{CC}
Y19	V_{CC}
Y20	V_{CC}
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2

Part Number and Revision Date

Part Number 51700096-003-1
Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.1)	Page
v1.0 (January 2008)	The naming conventions changed for the following pins in the "484-Pin FBGA" for the A3GLE600: **Pin Number** — **New Function Name** J19 — IO45PPB2V1 K20 — IO45NPB2V1 M2 — IO114NPB6V1 N1 — IO114PPB6V1 N4 — GFC2/IO115PPB6V1 P3 — IO115NPB6V1	3-6
Advance v0.4 (December 2007)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is v1.0.	N/A
Advance v0.3 (September 2007)	The "484-Pin FBGA" table for AGLE3000 is new.	4-11
	The "896-Pin FBGA" package and table for AGLE3000 is new.	4-16

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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51700096-005-5/10.08